DATA BOOK

President's Message

Dear Customer:

Total customer satisfaction is Xicor's number one goal. Xicor provides an extensive product offering to satisfy your needs in field-programmable nonvolatile microperipherals and support memory chips such as SerialFlash Memory, E^2PROMs, NOVRAMs, E^2POTs, and others. These CMOS products are available in a wide variety of speeds, voltages, package types, and a variety of interface configurations. The majority of the products are offered with extended temperature ranges, and many comply with all of the requirements of MIL-STD-883 Revision C for Class B products.

Xicor has shipped to its customers more than 300 million units. New, innovative products continuously join them as a result of our extensive research and development activities. Xicor's worldwide sales, marketing and applications organizations are dedicated to supporting your requirements. We appreciate your business and look forward to supplying your present and future requirements.

R. Cl C

Raphael Klein
President
July, 1995

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Xicor offers the best applications support in the industry to our customers.

1. **Field Applications Engineers in each sales office**
2. **Factory Applications Support HOTLINE at (408) 432-8888**
3. **On line Applications Bulletin Board (800) 258-8864 —14.4K baud**
4. **Interfacing Software available on the Applications Bulletin Board**
5. **Latest Datasheets and Application Notes available by FaxBack (408) 954-1627 or (408) 954-1711**
6. **World Wide Web design resource at http://www.xicor.com**
7. **Xicor's E-mail address: info@smtpgate.xicor.com**

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( ) = Country Code

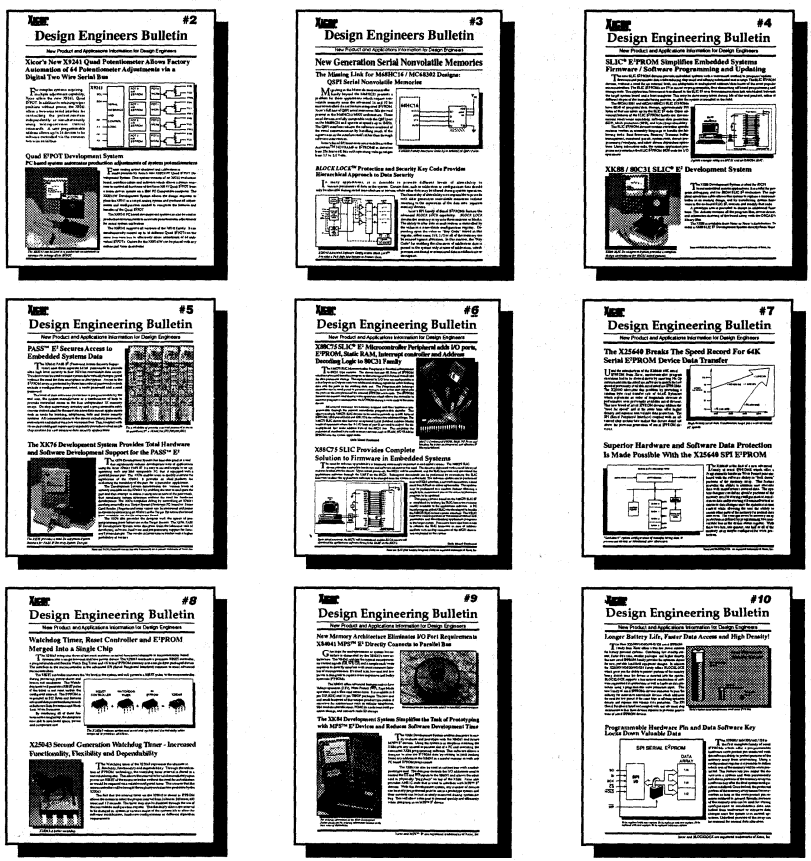
Let our Applications Team help turn your ideas into reality!

NEW—Design News!

Specifications for **thirty new products** are included in this new data book.

Xicor issues Design Engineering Bulletins as new products are introduced. These Bulletins supply information on the latest new products including data sheets, application notes, and software. This data book contains all information previously published in Design Engineering Bulletins #2 through #10.

Please contact the local Xicor sales office for information on new products and future Design Engineering Bulletins, or use the BRC located at the back of this book, or see us on the WWW.



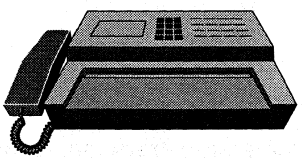
NOTE: Call your local Xicor sales office to receive Bulletins issued after the publication of this data book. All Bulletins shown above are included in this data book.

NEW—Xicor's FaxBack Service!

This year Xicor introduced an automated FaxBack response system, available twenty-four hours-a-day, seven days-a-week.

Up-to-date index provides Xicor's latest product offerings. Xicor FaxBack provides a selection index for product information. To receive this index, simply call (408) 954-1627 and request fax selection number, "2000."

Once you've received this index you can scan under the "part number" column to locate the particular data sheet of interest. By using the corresponding "FaxBack number" you can select the product data sheet you wish to receive. Within minutes your request will be delivered.



A touch-tone telephone and a fax machine/fax modem are all you need to instantly retrieve information about Xicor products. In addition, Xicor's FaxBack is also accessible from the Application Bulletin Board (BBS).

FREE—Applications Software!

Xicor offers an Applications Bulletin Board which contains applications information, product information, and interface software routines for a variety of Xicor products.

The BBS may be accessed at (800) 258-8864 or (408) 943-0655. Information is partitioned into the following file libraries based upon the topic or product. These libraries are currently available.

INTEL	Interface Routines for Intel Microcontrollers
MOTOROLA	Interface Routines for Motorola Microcontrollers
ZILOG	Interface Routines for Zilog Microcontrollers
NEC	Interface Routines for NEC Microcontrollers
PRGRMR	Latest Xicor Programmer Software
SLIC	The SLIC (Self Loading Integrated Code) Support Files
EEPOT	Interface Routines for Xicor's E^2POTs
SECURE	Interface Routines for PASS (Password Access Security Supervisor)
MPS	Interface Routines for Xicor MPS Devices
LapKit/51	Xicor PC Keyboard Controller and Power Management Chipset

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- For FaxBack numbers, see the following Alphanumeric Index.

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SECTION 2—SERIAL PRODUCTS

NOVRAMS

E^2PROMS

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Application Note Index (Cont.)

Precautions for the Handling of MOS Devices

Xicor products are designed with effective input protection to prevent damage to the devices under most conditions. However, any MOS circuit can be catastrophically damaged by excessive electrostatic discharge or transient voltages. The following procedures are recommended to avoid accidental circuit damage.

1. Testing MOS Circuits:

1. All units should be handled directly from the conductive or antistatic plastic tube in which they were shipped if possible. This action minimizes touching of individual leads.
2. If units are to be tested without using the tube carrier, the following precautions should be taken:
   a. Table surfaces which potentially will come in contact with the devices either directly or indirectly (such as through shipping tubes) must be metal or of another conductive material and should be electrically connected to the test equipment and to the test operator (a grounding bracelet is recommended).
   b. The units should be transported in bundled antistatic tubes or metal trays, both of which will assume a common potential when placed on a conductive table top.
   c. Do not band tubes together with adhesive tape or rubber bands without first wrapping them in a conductive layer.

II. Test Equipment (Including Environmental Equipment):

1. All equipment must be properly returned to the same reference potential (ground) as the devices, the operator, and the container for the devices.
2. Devices to be tested should be protected from high voltage surges developed by:
   a. Turning electrical equipment on or off.
   b. Relay switching.
   c. Transients from voltage sources (AC line or power supplies).

III. Assembling MOS Devices Onto PC Boards:

1. The MOS circuits should be mounted on the PC board last.
2. Similar precautions should be taken as in Item 1 above, at the assembly work station.
3. Soldering irons or solder baths should be at the same reference (ground) potential as the devices.
4. Plastic materials which are not antistatic treated should be kept away from devices as they develop and maintain high levels of static charge.

IV. Device Handling:

1. Handling of devices should be kept to a minimum. If handling is required, avoid touching the leads directly.

V. General:

1. The handler should take every precaution that the device will see the same reference potential when moved.
2. Anyone handling individual devices should develop a habit of first touching the container in which the units are stored before touching the units.
3. Before placing the units into a PC board, the handler should touch the PC board first.
4. Personnel should not wear clothing which will build up static charge. They should wear smocks and clothing made of 100% cotton rather than wool or synthetic fibers.
5. Be careful of electrostatic build up through the movement of air over plastic material. This is especially true of acid sinks.
6. Personnel or operators should always wear grounded wrist straps when working with MOS devices.
7. A 1MΩ resistance ground strap is recommended and will protect people up to 5000V AC RMS or DC by limiting current to 5mA.
8. Antistatic ionized air equipment is very effective and useful in preventing electrostatic damage.
9. Low humidity maximizes potential static problems. Maintaining humidity levels above 45% is one of the most effective ways to guard against static handling problems.

PRODUCT SELECTION GUIDES

SERIALFLASH MEMORY

DEVICE	BIT DENSITY	ORG.	CLOCK RATE	PACKAGE (N0.PINS) P(8)	S(8)	V(14)	V(20)	TEMP. RANGE COM	IND	MIL	SUPPLY VOLTAGE 1.8V - 3.6V	FEATURES
X25F008	8K	X8	1MHZ	◆	◆	◆		◆	◆		◆	SPI INTERFACE, BLOCKLOCK
X25F016	16K	X8	1MHZ	◆	◆	◆		◆	◆		◆	SPI INTERFACE, BLOCKLOCK
X25F032	32K	X8	1MHZ	◆	◆	◆		◆	◆		◆	SPI INTERFACE, BLOCKLOCK
X25F064	64K	X8	1MHZ	◆	◆		◆	◆	◆		◆	SPI INTERFACE, BLOCKLOCK
X24F008	8K	X8	100KHZ	◆	◆	◆		◆	◆		◆	2-WIRE INTERFACE, BLOCKLOCK
X24F016	16K	X8	100KHZ	◆	◆	◆		◆	◆		◆	2-WIRE INTERFACE, BLOCKLOCK
X24F032	32K	X8	100KHZ	◆	◆	◆		◆	◆		◆	2-WIRE INTERFACE, BLOCKLOCK
X24F064	64K	X8	100KHZ	◆	◆		◆	◆	◆		◆	2-WIRE INTERFACE, BLOCKLOCK

PRODUCT SELECTION GUIDES

SERIAL E²PROMS

DEVICE	BIT DENSITY	ORG.	CLOCK RATE	PACKAGE				NO. PINS		TEMP. RANGE			SUPPLY VOLTAGE			FEATURES
				D	P	S	V	8	14	COM	IND	MIL	5	3	2.7	
X24001	128	X8	1MHZ		◆	◆	◆	◆		◆	◆	◆	◆	◆	◆	TWO WIRE INTERFACE 12V ONLY PROGRAMMING
X24012	1K	X8	100KHZ		◆	◆		◆		◆	◆	◆	◆	◆	◆	TWO WIRE INTERFACE, SLAVE ADDRESS PIN 7 = NO CONNECT
X24022	2K	X8	100KHZ		◆	◆		◆		◆	◆	◆	◆	◆	◆	TWO WIRE INTERFACE, SLAVE ADDRESS PIN 7 = NO CONNECT
X24042	4K	X8	100KHZ		◆	◆		◆		◆	◆	◆	◆	◆	◆	TWO WIRE INTERFACE, SLAVE ADDRESS PIN 7 = NO CONNECT
X24164	16K	X8	100KHZ		◆	◆		◆		◆	◆	◆	◆	◆	◆	TWO WIRE INTERFACE, SLAVE ADDRESS WITH DEVICE ADDRESSING
X24645	64K	X8	100KHZ		◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	TWO WIRE INTERFACE BLOCK PROTECTION
X24C00	128	X8	1MHZ		◆	◆	◆	◆		◆	◆	◆	◆	◆	◆	TWO WIRE INTERFACE
X24C01	1K	X8	100KHZ		◆	◆	◆	◆		◆	◆	◆	◆	◆	◆	TWO WIRE INTERFACE
X24C01A	1K	X8	100KHZ		◆	◆		◆		◆	◆	◆	◆	◆	◆	TWO WIRE INTERFACE, SLAVE ADDRESS
X24C02	2K	X8	100KHZ		◆	◆		◆	◆	◆	◆	◆	◆	◆	◆	TWO WIRE INTERFACE, SLAVE ADDRESS
X24C04	4K	X8	100KHZ	◆	◆	◆		◆	◆	◆	◆	◆	◆	◆	◆	TWO WIRE INTERFACE, SLAVE ADDRESS
X24C08	8K	X8	100KHZ		◆	◆		◆	◆	◆	◆	◆	◆	◆	◆	TWO WIRE INTERFACE, SLAVE ADDRESS
X24C16	16K	X8	100KHZ	◆	◆	◆		◆	◆	◆	◆	◆	◆	◆	◆	TWO WIRE INTERFACE, SLAVE ADDRESS
X25020	2K	X8	1MHZ		◆	◆	◆	◆		◆	◆	◆	◆	◆	◆	SPI, SSI INTERFACE BLOCK LOCK
X25021	2K	X8	1MHZ		◆	◆	◆	◆		◆	◆	◆	◆	◆	◆	SPI, SSI INTERFACE BLOCK LOCK
X25040	4K	X8	1MHZ		◆	◆	◆	◆		◆	◆	◆	◆	◆	◆	SPI, SSI INTERFACE BLOCK LOCK
X25041	4K	X8	1MHZ		◆	◆	◆	◆		◆	◆	◆	◆	◆	◆	SPI, SSI INTERFACE BLOCK LOCK
X25043	4K	X8	1MHZ		◆	◆	◆	◆		◆	◆	◆	◆	◆	◆	WATCHDOG TIMER WITH E²PROM
X25080	8K	X8	2MHZ		◆	◆	◆	◆		◆	◆	◆	◆	◆	◆	SPI, SSI INTERFACE BLOCK LOCK
X25160	16K	X8	2MHZ		◆	◆	◆	◆		◆	◆	◆	◆	◆	◆	SPI, SSI INTERFACE BLOCK LOCK
X25320	32K	X8	2MHZ		◆	◆	◆	◆		◆	◆	◆	◆		◆	SPI, SSI INTERFACE BLOCK LOCK
X25640	64K	X8	1MHZ		◆	◆		◆	◆	◆	◆	◆	◆			SPI, SSI INTERFACE BLOCK LOCK
X25642	64K	X8	2MHZ		◆	◆	◆	◆		◆	◆	◆	◆		◆	SPI, SSI INTERFACE BLOCK LOCK
X25128	128K	X8	2MHZ		◆	◆		◆	16	◆	◆	◆	◆		◆	SPI, SSI INTERFACE BLOCK LOCK
X25C02	2K	X8	1MHZ		◆	◆		◆		◆	◆	◆	◆			SPI, SSI INTERFACE

SERIAL NOVRAMS

DEVICE	BIT DENSITY	ORG.	CLOCK RATE	PACKAGE			NO. PINS	TEMP. RANGE			SUPPLY VOLTAGE			FEATURES
				D	P	S		COM	IND	MIL	5	3	2.7	
X24C44	256	X16	1MHZ		◆	◆	8	◆	◆	◆	◆			NONVOLATILE STATIC RAM
X24C45	256	X16	1MHZ		◆	◆	8	◆	◆	◆	◆			NONVOLATILE STATIC RAM WITH AUTOSTORE®
X25401	256	X16	1MHZ		◆	◆	8	◆	◆	◆	◆			SPI INTERFACE NONVOLATILE STATIC RAM WITH AUTOSTORE®

PRODUCT SELECTION GUIDES

PARALLEL NOVRAMS

PART #	BIT DENSITY	ORG.	FASTEST ACCESS TIME (NS)	PACKAGE OPTIONS, NO. OF PINS D	P	J	E	S	T	K	FEATURE & COMMENTS
X20C04	4K	X8	150	28	28	32	32				CMOS NONVOLATILE STATIC RAM
X20C05	4K	X8	35	28	28	32	32				HIGH SPEED CMOS NONVOLATILE STATIC RAM WITH AUTOSTORE®
X20C16	16K	X8	35	28	28	32	32	28	32		HIGH SPEED CMOS NONVOLATILE STATIC RAM WITH AUTOSTORE®
X20C17	16K	X8	35	24	24						HIGH SPEED CMOS NOVRAM, 24 PIN JEDEC SRAM PINOUT
X22C10	256	X4	120	18	18			16			CMOS NIBBLE WIDE NONVOLATILE STATIC RAM
X22C12	1K	X4	150	18	18			20			CMOS NIBBLE WIDE NONVOLATILE STATIC RAM
XM20C64	64K	X8	55	28	66						HIGH SPEED NOVRAM; FULL MILITARY

All of the preceding products are available across commercial, industrial, and military temperature ranges.

BUS ORIENTED MICROCONTROLLER PERIPHERALS

DEVICE	BIT DENSITY	ORG	ACCESS TIME (NS)	PACKAGE D	J	L	P	S	NO. PINS	TEMP. RANGE COM	IND	MIL	SUPPLY VOLTAGE	FEATURES
X68C64	64K	X8	120	◆			◆	◆	24	◆	◆	◆	5V	DUAL PLANE, CONCURRENT READ & WRITE MOTOROLA 68XX INTERFACE.
X68C64 SLIC	64K	X8	120	◆			◆	◆	24	◆	◆	◆	5V	DUAL PLANE, CONCURRENT READ & WRITE MOTOROLA 68XX INTERFACE WITH SELF LOADING INTEGRATED CODE.
X68C75 SLIC	64K	X8	120	◆	◆	◆	◆		48, 44	◆	◆	◆	5V	DUAL PLANE/CONCURRENT READ & WRITE WITH TWO PORT EXPANSION WITH SELF LOADING INTEGRATED CODE.
X86C64	64K	X8	120	◆			◆	◆	24	◆	◆	◆	5V	DUAL PLANE, CONCURRENT READ & WRITE ZILOG 86XX INTERFACE.
X88C64	64K	X8	120	◆			◆	◆	24	◆	◆	◆	5V	DUAL PLANE, CONCURRENT READ & WRITE INTEL 88XX INTERFACE.
X88C64 SLIC	64K	X8	120	◆			◆	◆	24	◆	◆	◆	5V	DUAL PLANE, CONCURRENT READ & WRITE INTEL 88XX INTERFACE WITH SELF LOADING INTEGRATED CODE.
X88C75 SLIC	64K	X8	120	◆	◆	◆	◆		48, 44	◆	◆	◆	5V	DUAL PLANE/CONCURRENT READ & WRITE WITH TWO PORT EXPANSION WITH SELF LOADING INTEGRATED CODE.

PRODUCT SELECTION GUIDES

CMOS DIGITALLY CONTROLLED POTENTIOMETERS, E²POTS

DEVICE	RESISTANCE (OHMS)	CLOCK SPEED	D	P	S	V	NO. PINS	TEMP. RANGE COM	IND	MIL	SUPPLY-VOLTAGE	FEATURES
X9221U	50K,50K	100KHZ		◆	◆		20	◆	◆		5V	DUAL, 2-WIRE INTERFACE
X9221W	10K,10K	100KHZ		◆	◆		20	◆	◆		5V	DUAL, 2-WIRE INTERFACE
X9221Y	2K,2K	100KHZ		◆	◆		20	◆	◆		5V	DUAL, 2-WIRE INTERFACE
X9241M	2K,10K,10K, 50K	100KHZ	◆	◆	◆		20	◆	◆	◆	5V	QUAD, DIRECT POSITION READ AND WRITE 2-WIRE INTERFACE
X9241U	50K,50K,50K, 50K	100KHZ	◆	◆	◆		20	◆	◆	◆	5V	QUAD, DIRECT POSITION READ AND WRITE 2-WIRE INTERFACE
X9241W	10K,10K,10K, 10K	100KHZ	◆	◆	◆		20	◆	◆	◆	5V	QUAD, DIRECT POSITION READ AND WRITE 2-WIRE INTERFACE
X9241Y	2K,2K,2K,2K	100KHZ	◆	◆	◆		20	◆	◆	◆	5V	QUAD, DIRECT POSITION READ AND WRITE 2-WIRE INTERFACE
X9312T	100K	250KHZ	◆	◆	◆		8	◆	◆	◆	5V	100 STEP, 0V TO 15V
X9312U	50K	250KHZ	◆	◆	◆		8	◆	◆	◆	5V	100 STEP, 0V TO 15V
X9312W	10K	250KHZ	◆	◆	◆		8	◆	◆	◆	5V	100 STEP, 0V TO 15V
X9312Z	1K	250KHZ	◆	◆	◆		8	◆	◆	◆	5V	100 STEP, 0V TO 15V
X9313T	100K	250KHZ		◆	◆	◆	8	◆	◆	◆	3V, 5V	32 STEP, –5V TO +5V
X9313U	50K	250KHZ		◆	◆	◆	8	◆	◆	◆	3V, 5V	32 STEP, –5V TO +5V
X9313W	10K	250KHZ		◆	◆	◆	8	◆	◆	◆	3V, 5V	32 STEP, –5V TO +5V
X9313Z	1K	250KHZ		◆	◆	◆	8	◆	◆	◆	3V, 5V	32 STEP, –5V TO +5V
X9314W	10K	250KHZ		◆	◆	◆	8	◆	◆	◆	3V, 5V	32 STEP, –5V TO +5V, LOG TAPER
X9511W	10K	250KHZ		◆	◆		8	◆	◆	◆	5V	32 STEP, PUSHPOT
X9511Z	1K	250KHZ		◆	◆		8	◆	◆	◆	5V	32 STEP, PUSHPOT
X9514W	10K	250KHZ		◆	◆		8	◆	◆	◆	5V	32 STEP, LOG TAPER, PUSHPOT
X9C102	1K	250KHZ	◆	◆	◆		8	◆	◆	◆	SV	100 STEP, –5V TO +5V
X9C103	10K	250KHZ	◆	◆	◆		8	◆	◆	◆	5V	100 STEP, –5V TO +5V
X9C104	100K	250KHZ	◆	◆	◆		8	◆	◆	◆	5V	100 STEP, –5V TO +5V
X9C503	50K	250KHZ	◆	◆	◆		8	◆	◆	◆	5V	100 STEP, –5V TO +5V

PASSWORD PROTECTED SECURITY SUPERVISOR

DEVICE	BIT DESITY	ORG.	CLOCK RATE	PACKAGE D	P	A	NO. PINS	TEMP. RANGE COM	IND	MIL	SUPPLY VOLTAGE 5	3	2.7	FEATURES
X76F041	4K	X8	1MHZ		◆	◆	8	◆	◆	◆	◆	◆		(3) 64 BIT PASSWORDS (READ, WRITE, CONFIGURATION)

MICRO PORT SAVER™ E²PROM

DEVICE	BIT DENSITY	ORG.	ACCESS TIME (NS)	PACKAGE D	P	S	NO. PINS	TEMP. RANGE COM	IND	MIL	SUPPLY VOLTAGE 5	3	2.7	FEATURES
X84041	4K	X8	45		◆	◆	8	◆	◆	◆	◆	◆	◆	PARALLEL BUS INTERFACE ($\overline{CE}$, $\overline{WE}$, $\overline{OE}$, I/O), 3.3 MBPS DATA TRANSFER RATE

PRODUCT SELECTION GUIDES

PARALLEL E²PROMS

PART #	BIT DENSITY	ORG.	FASTEST ACCESS TIME (NS)	PACKAGE OPTIONS, NO. OF PINS D	P	J	E	S	F	K	T	FEATURES & COMMENTS
X2804C	4K	X8	250	24	24							5V, ELECTRICALLY BYTE ALTERABLE E²PROM
X2816C	16K	X8	90	24	24	32	32	24				5V, ELECTRICALLY BYTE ALTERABLE E²PROM
X2864B	64K	X8	150	28	28	32	32					5V, BYTE ALTERABLE E²PROM
X28C64	64K	X8	150	28	28	32	32	28	28	28	32	5V, BYTE ALTERABLE CMOS E²PROM
X28HC64	64K	X8	55	28	28	32	32	28	28	28	32	5V, HIGH SPEED, BYTE ALTERABLE CMOS E²PROM
X28C256	256K	X8	150	28	28	32	32	28	28	28	32	5V, HIGH SPEED, BYTE ALTERABLE CMOS E²PROM
X28HC256	256K	X8	70	28	28	32	32	28	28	28	32	5V, HIGH SPEED, BYTE ALTERABLE CMOS E²PROM
X28VC256	256K	X8	45	28	28	32	32	28	28	28	32	5V, VERY HIGH SPEED, BYTE ALTERABLE, CMOS E²PROM
X28C512	512K	X8	90	32	32	32	32		32	36	40	5V, BYTE ALTERABLE CMOS E²PROM
X28C513	512K	X8	90			32	32					256K TO 512K PLCC AND LCC UPGRADE PATH
X28C010	1M	X8	120	32	32	32	32	32	32	36	40	5V, BYTE ALTERABLE, CMOS E²PROM
X28HT512	512K	X8	200	32					32	36		5V, HIGH TEMPERATURE (170°C) OPERATION
X28HT010	1M	X8	200	32					32			5V, HIGH TEMPERATURE (170°) OPERATION
X28LC512	512K	X8	150	32	32	32					40	3.3V, BYTE ALTERABLE CMOS EEPROM
X28LC513	512K	X8	150			32						3.3V, BYTE ALTERABLE CMOS EEPROM
XM28C010	1M	X8	70	32	66							5V, HIGH SPEED BYTE ALTERABLE CMOS E²PROM
XM28C020	2M	X8	150	32	66							5V, HIGH SPEED BYTE ALTERABLE CMOS E²PROM
XM28C040	4M	X8	150	32	66							5V, HIGH SPEED BYTE ALTERABLE CMOS E²PROM

MIL-STD-883 PRODUCT SELECTION GUIDE

XICOR PART NUMBER	ORGANIZATION	FASTEST SPEEDS*	CERDIP	PLCC/ LCC	FLAT PACK	PGA	SMD #
NOVRAMS							
X20C04	512 X 8	200NS	28	32			
X20C05	512 X 8	45NS	28	32			
X20C16	2K X 8	45NS	28	32			
X22C10	64 X 4	120NS	18				
X22C12	256 X 4	120NS	18				
SERIAL NOVRAMS							
X24C44	16 X 16	1MHZ	8				
X24C45	16 X 16	1MHZ	8				
SERIAL E^2PROMS							
X24C04	512 X 8	100KHZ	8				
X24C16	2K X 8	100KHZ	8				
E^2POTENTIOMETERS							
X9241	2KΩ, 10KΩ, 50KΩ, COMBO		20				
X9C102	1KΩ		8				
X9C103	10KΩ		8				
X9C104	100KΩ		8				
X9C503	50KΩ		8				
5 VOLT, BYTE ALTERABLE E^2PROMS							
X28C64	8K X 8	150NS	28	32	28	28	5962-87514
X28HC64	8K X 8	70NS	28	32	28	28	
X28C256	32K X 8	200NS	28	32	28	28	5962-88525
X28HC256	32K X 8	70NS	28	32	28	28	5962-88634
X28VC256	32K X 8	55NS	38	32	28	28	5962-88634
X28C512	64K X 8	120NS	32	32	32	36	5962-90869
X28C513	64K X 8	120NS		32			5962-90869
X28C010	128K X 8	120NS	32	32	32	36	5962-38267
MICROCONTROLLER PERIPHERAL MEMORY							
X68C64	8K X 8	120NS	24	32			
X68C64 SLIC	8K X 8	120NS	24	32			
X86C64	8K X 8	120NS	24	32			
X88C64	8K X 8	120NS	24	32			
X88C64 SLIC	8K X 8	120NS	24	32			

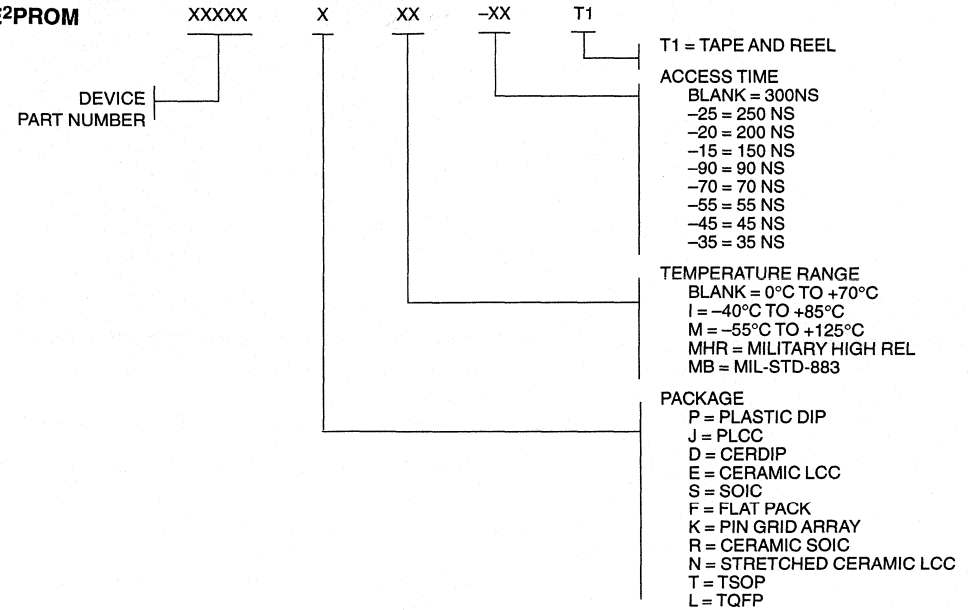
*Speeds for parallel access devices minimum t_{AA} in ns; for serial devices speed is maximum clock rate in Hz.

STANDARD MEMORY MODULES

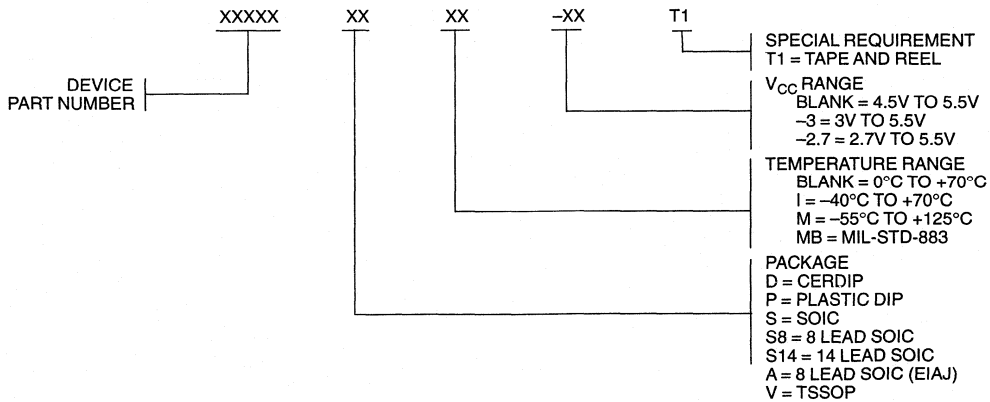
XICOR P/N	CONFIG	PIN #	PKG	SUBSTRATE	TEMP. RANGES			BASE COMPONENT	QTY PER
					C/I	M	HR		
XM20C64	8K X 8	28	DIP	CERAMIC	X	X	X	X20C16E	4
XM20C64P	8K X 8	66	PGA	CERAMIC PUMA	X	X	X	X20C16E	4
XM28C010	128K X 8	32	DIP	CERAMIC	X	X	X	X28VC256E	4
XM28C010P	32K X 32	66	PGA	CERAMIC PUMA	X	X	X	X28VC256E	4
XM28C020	256 X 8	32	DIP	CERAMIC	X	X	X	X28C513E	4
XM28C020P	64K X 32	66	PGA	CERAMIC PUMA	X	X	X	X28C513E	4
XM28C040	512K X 8	32	DIP	CERAMIC	X	X	X	X28C010N	4
XM28C040P	128K X 32	66	PGA	CERAMIC PUMA	X	X	X	X28C010E	4

ORDERING INFORMATION

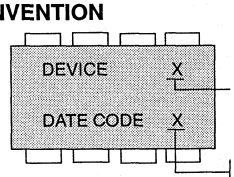
PARALLEL E²PROM



SERIAL E²PROMS



SERIAL E² MARK CONVENTION



BLANK = 8 LEAD SOIC
P = PLASTIC
S = SOIC
D = CERDIP

LETTER CODE VCC	TEMP. RANGE COM	IND	MIL
4.5V TO 5.5V	BLANK	I	M
3.0V TO 5.5V	D	E	–
2.7V TO 5.5V	F	G	–

NOTES

NOVRAM is Xicor's nonvolatile static RAM device family.
E²POT™ is a trademark of Xicor, Inc.

3807-2.3 12/4/95 T12/C0/D0 NS

256 Bit X22C10 64 x 4

Nonvolatile Static RAM

FEATURES

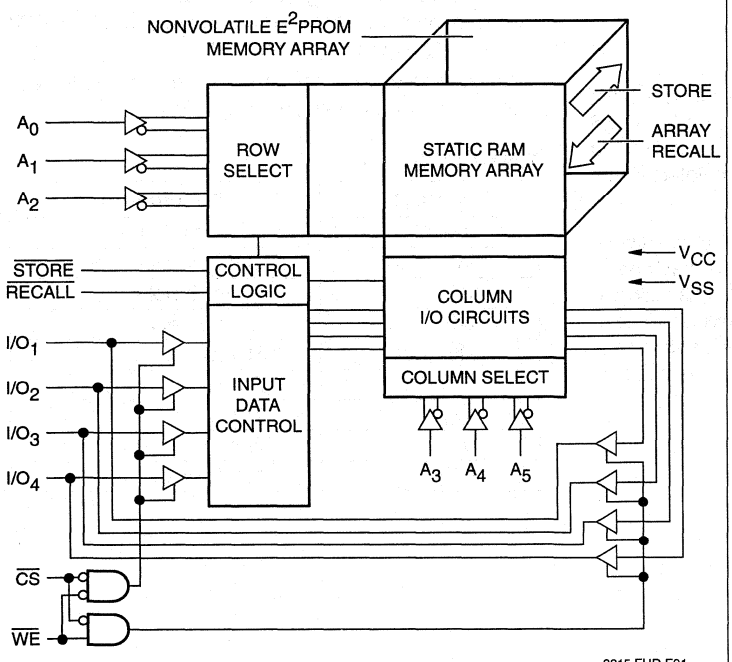
- **High Performance CMOS**
  - **—120ns RAM Access Time**
- **High Reliability**
  - **—Store Cycles: 1,000,000**
  - **—Data Retention: 100 Years**
- **Low Power Consumption**
  - **—Active: 40mA Max.**
  - **—Standby: 100μA Max.**
- **Infinite Array Recall, RAM Read and Write Cycles**
- **Nonvolatile Store Inhibit: V_{CC} = 3.5V Typical**
- **Fully TTL and CMOS Compatible**
- **JEDEC Standard 18-Pin 300-mil DIP**
- **100% Compatible with X2210**
  - **—With Timing Enhancements**

DESCRIPTION

The X22C10 is a 64 x 4 CMOS NOVRAM featuring a high-speed static RAM overlaid bit-for-bit with a nonvolatile E^2PROM. The NOVRAM design allows data to be easily transferred from RAM to E^2PROM (STORE) and from E^2PROM to RAM (RECALL). The STORE operation is completed within 5ms or less and the RECALL is completed within 1μs.

Xicor NOVRAMs are designed for unlimited write operations to the RAM, either RECALLs from E^2PROM or writes from the host. The X22C10 will reliably endure 1,000,000 STORE cycles. Inherent data retention is greater than 100 years.

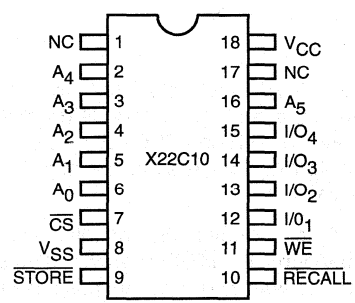
FUNCTIONAL DIAGRAM



3815 FHD F01

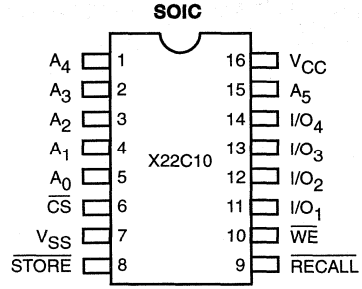
PIN CONFIGURATION

PLASTIC DIP
CERDIP



3815 FHD F02

SOIC



3815 FHD F08.1

3815-2.3 5/25/95 T26/C4/D0 TD

PIN DESCRIPTIONS AND DEVICE OPERATION

Addresses (A_0–A_5)

The address inputs select a 4-bit memory location during a read or write operation.

Chip Select ($\overline{CS}$)

The Chip Select input must be LOW to enable read or write operations with the RAM array. $\overline{CS}$ HIGH will place the I/O pins in the high impedance state.

Write Enable ($\overline{WE}$)

The Write Enable input controls the I/O buffers, determining whether a RAM read or write operation is enabled. When $\overline{CS}$ is LOW and $\overline{WE}$ is HIGH, the I/O pins will output data from the selected RAM address locations. When both $\overline{CS}$ and $\overline{WE}$ are LOW, data presented at the I/O pins will be written to the selected address location.

Data In/Data Out (I/O_1–I/O_4)

Data is written to or read from the X22C10 through the I/O pins. The I/O pins are placed in the high impedance state when either $\overline{CS}$ is HIGH or during either a store or recall operation.

$\overline{STORE}$

The $\overline{STORE}$ input, when LOW, will initiate the transfer of the entire contents of the RAM array to the E^2PROM array. The $\overline{WE}$ and $\overline{RECALL}$ inputs are inhibited during the store cycle. The store operation is completed in 5ms or less.

A store operation has priority over RAM read/write operations. If $\overline{STORE}$ is asserted during a read operation, the read will be discontinued. If $\overline{STORE}$ is asserted during a RAM write operation, the write will be immediately terminated and the store performed. The data at the RAM address that was being written will be unknown in both the RAM and E^2PROM arrays.

$\overline{RECALL}$

The $\overline{RECALL}$ input, when LOW, will initiate the transfer of the entire contents of the E^2PROM array to the RAM array. The transfer of data will be completed in 1µs or less.

An array recall has priority over RAM read/write operations and will terminate both operations when $\overline{RECALL}$ is asserted. $\overline{RECALL}$ LOW will also inhibit the $\overline{STORE}$ input.

Automatic Recall

Upon power-up the X22C10 will automatically recall data from the E^2PROM array into the RAM array.

Write Protection

The X22C10 has three write protect features that are employed to protect the contents of the nonvolatile memory.

- V_{CC} Sense—All functions are inhibited when V_{CC} is <3.5V typical.
- Write Inhibit—Holding either $\overline{STORE}$ HIGH or $\overline{RECALL}$ LOW during power-up or power-down will prevent an inadvertent store operation and E^2PROM data integrity will be maintained.
- Noise Protection—A $\overline{STORE}$ pulse of typically less than 20ns will not initiate a store cycle.

PIN NAMES

Symbol	Description
A_0–A_5	Address Inputs
I/O_1–I/O_4	Data Inputs/Outputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{RECALL}$	Recall
$\overline{STORE}$	Store
V_{CC}	+5V
V_{SS}	Ground
NC	No Connect

3815 PGM T01

ABSOLUTE MAXIMUM RATINGS

Temperature under Bias ..... –65°C to +135°C
Storage Temperature ..... –65°C to +150°C
Voltage on any Pin with
Respect to V_{SS} ..... –1V to +7V
D.C. Output Current 5mA
Lead Temperature
(Soldering, 10 seconds) ..... 300°C

COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	+70°C
Industrial	–40°C	+85°C
Military	–55°C	+125°C

3815 PGM T12.1

Supply Voltage	Limits
X22C10	5V ±10%

3815 PGM T13

D.C. OPERATING CHARACTERISTICS (Over the recommended operating conditions, unless otherwise specified.)

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
I_{CC}	V_{CC} Supply Current, RAM Read/Write		40	mA	$\overline{CS}$ = V_{IL}, I/Os = Open, All Others = V_{IH}, Addresses = 0.4V/2.4V Levels @ f = 8MHz
I_{SB1}	V_{CC} Standby Current (TTL Inputs)		2	mA	Store or Recall Functions Not Active, I/Os = Open, All Other Inputs = V_{IH}
I_{SB2}	V_{CC} Standby Current (CMOS Inputs)		100	µA	Store or Recall functions Not Active, I/Os = Open, All Other Inputs = V_{CC} –0.3V
I_{LI}	Input Leakage Current		10	µA	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output Leakage Current		10	µA	V_{OUT} = V_{SS} to V_{CC}
V_{IL}(2)	Input LOW Voltage	–1	0.8	V	
V_{IH}(2)	Input HIGH Voltage	2	V_{CC} + 1	V	
V_{OL}	Output LOW Voltage		0.4	V	I_{OL} = 4.2mA
V_{OH}	Output HIGH Voltage	2.4		V	I_{OH} = –2mA

3815 PGM T02.3

CAPACITANCE T_A = +25°C, f = 1MHz, V_{CC} = 5V

Symbol	Parameter	Max.	Units	Test Conditions
$C_{I/O}$(1)	Input/Output Capacitance	8	pF	$V_{I/O}$ = 0V
C_{IN}(1)	Input Capacitance	6	pF	V_{IN} = 0V

3815 PGM T03

Notes: (1) This parameter is periodically sampled and not 100% tested.
(2) V_{IL} min. and V_{IH} max. are for reference only and are not tested.

MODE SELECTION

$\overline{CE}$	$\overline{WE}$	$\overline{RECALL}$	$\overline{STORE}$	I/O	Mode
H	X	H	H	Output High Z	Not Selected(3)
L	H	H	H	Output Data	Read RAM
L	L	H	H	Input Data HIGH	Write "1" RAM
L	L	H	H	Input Data LOW	Write "0" RAM
X	H	L	H	Output High Z	Array Recall
H	X	L	H	Output High Z	Array Recall
X	H	H	L	Output High Z	Nonvolatile Store(4)
H	X	H	L	Output High Z	Nonvolatile Store(4)

3815 PGM T05.1

ENDURANCE AND DATA RETENTION

Parameter	Min.	Units
Endurance	100,000	Data Changes Per Bit
Store Cycles	1,000,000	Store Cycles
Data Retention	100	Years

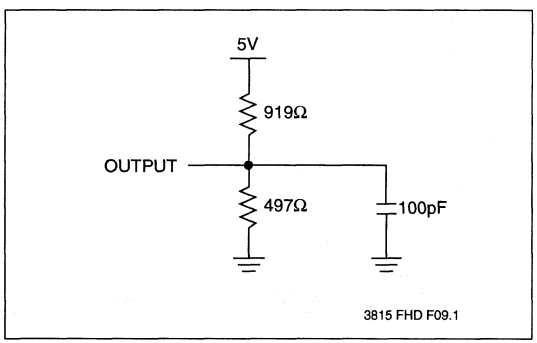
3815 PGM T06

POWER-UP TIMING

Symbol	Parameter	Max.	Units
t_{PUR}(5)	Power-up to Read Operation	100	µs
t_{PUW}(5)	Power-up to Write or Store Operation	5	ms

3815 PGM T07

EQUIVALENT A.C. LOAD CIRCUIT



3815 FHD F09.1

A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3V
Input Rise and Fall Times	10ns
Input and Output Timing Levels	1.5V

3815 PGM T04.1

Notes: (3) Chip is deselected but may be automatically completing a store cycle.
(4) $\overline{STORE}$ = LOW is required only to initiate the store cycle, after which the store cycle will be automatically completed (e.g. $\overline{STORE}$ = X).
(5) t_{PUR} and t_{PUW} are the delays required from the time V_{CC} is stable until the specified operation can be initiated. These parameters are periodically sampled and not 100% tested.

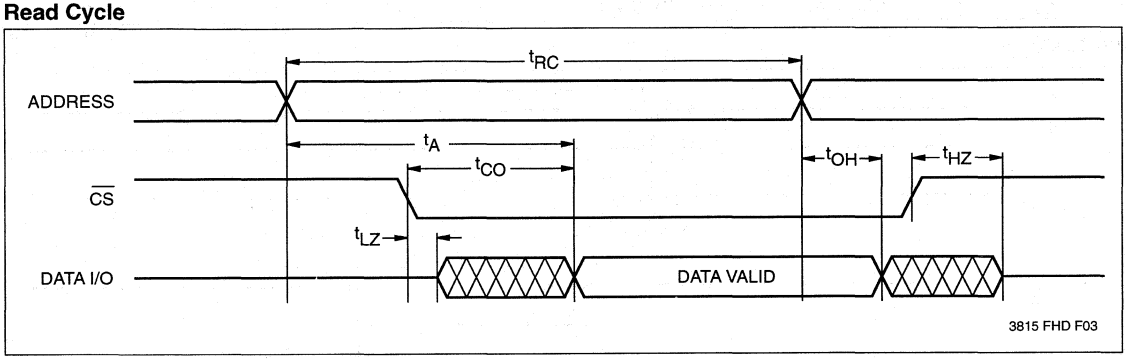
A.C. CHARACTERISTICS (Over the recommended operating conditions, unless otherwise specified.

Read Cycle Limits

Symbol	Parameter	Min.	Max.	Units
t_{RC}	Read Cycle Time	120		ns
t_{AA}	Access Time		120	ns
t_{CO}	Chip Select to Output Valid		120	ns
t_{OH}	Output Hold from Address Change	0		ns
t_{LZ}(6)	Chip Select to Output in Low Z	0		ns
t_{HZ}(6)	Chip Deselect to Output in High Z		50	ns

3815 PGM T08

Read Cycle



3815 FHD F03

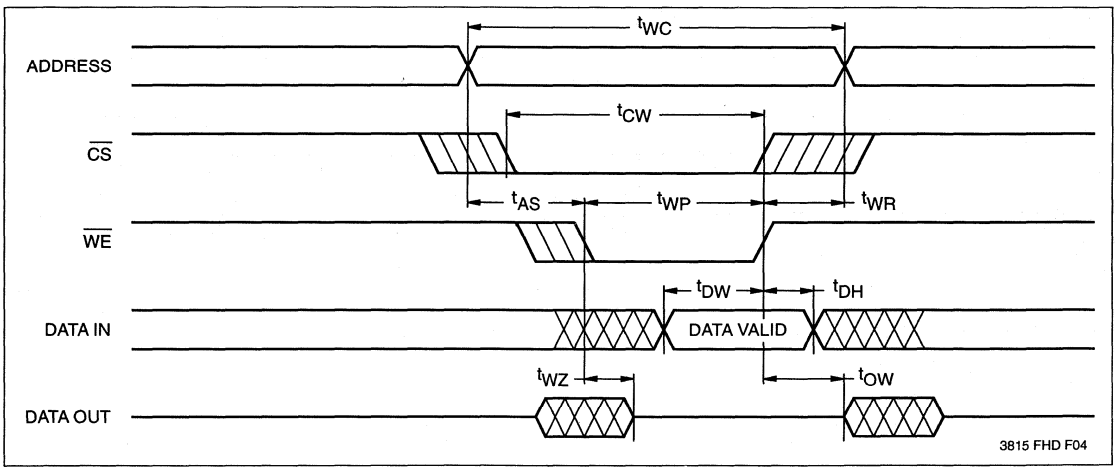
Note: (6) t_{LZ} min. and t_{HZ} min. are periodically sampled and not 100% tested.

Write Cycle Limits

Symbol	Parameter	Min.	Max.	Units
t_{WC}	Write Cycle Time	120		ns
t_{CW}	Chip Select to End of Write	90		ns
t_{AS}	Address Setup Time	0		ns
t_{WP}	Write Pulse Width	90		ns
t_{WR}	Write Recovery Time	0		ns
t_{DW}	Data Valid to End of Write	40		ns
t_{DH}	Data Hold Time	0		ns
t_{WZ}	Write Enable to Output in High Z		50	ns
t_{OW}	Output Active from End of Write	0		ns

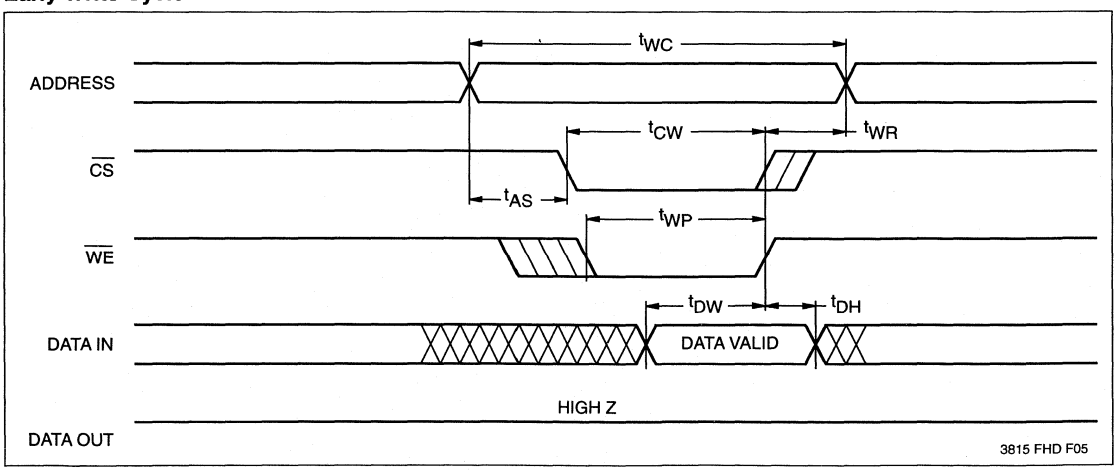
3815 PGM T09

Write Cycle



3815 FHD F04

Early Write Cycle



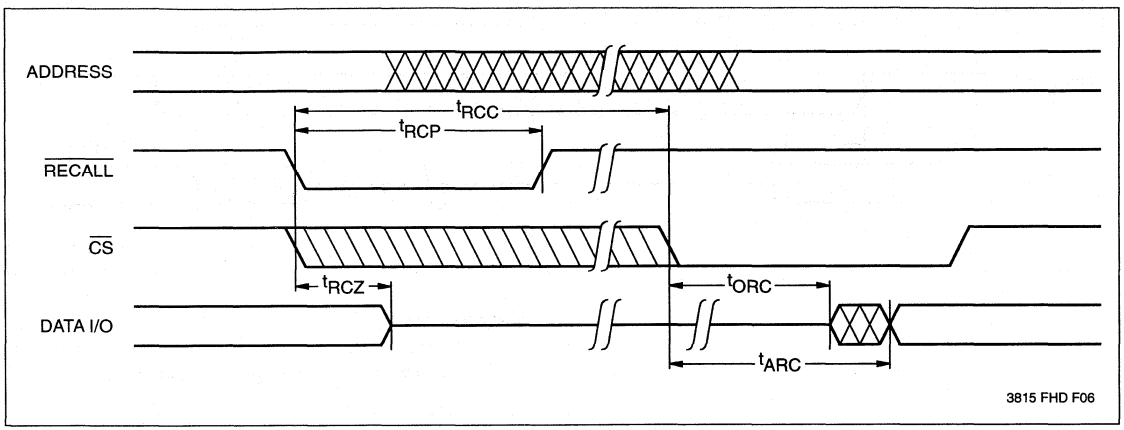
3815 FHD F05

Recall Cycle Limits

Symbol	Parameter	Min.	Max.	Units
t_{RCC}	Array Recall Time		1	µs
t_{RCP}(7)	Recall Pulse Width	90		ns
t_{RCZ}	Recall to Output in High Z		50	ns
t_{ORC}	Output Active from End of Recall	0		ns
t_{ARC}	Recalled Data Access Time from End of Recall		150	ns

3815 PGM T10

Recall Cycle



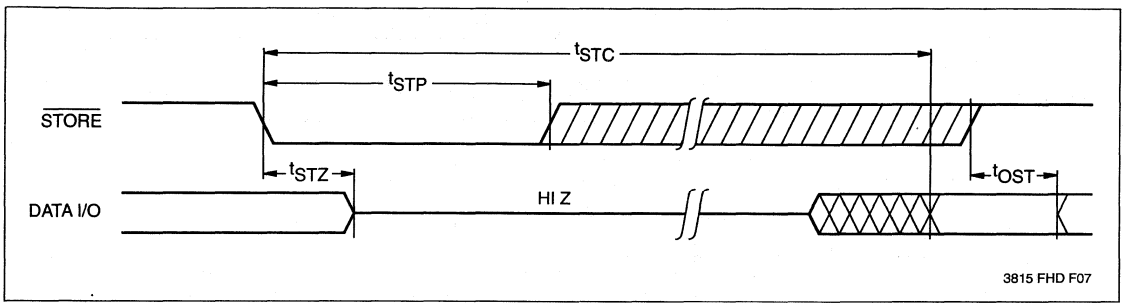
Note: (7) RECALL rise time must be less than 1µs.

Store Cycle Limits

Symbol	Parameter	Min.	Max.	Units
t_{STC}	Internal Store Time		5	ms
t_{STP}	Store Pulse Width	90		ns
t_{STZ}	Store to Output in High Z		50	ns
t_{OST}	Output Active from End of Store	0		ns

3815 PGM T11

Store Cycle Limits

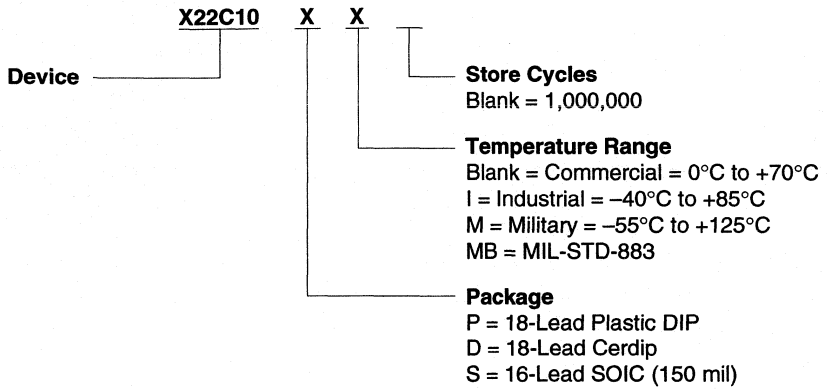


3815 FHD F07

SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

ORDERING INFORMATION



NOTES

1K Bit X22C12 256 x 4

Nonvolatile Static RAM

FEATURES

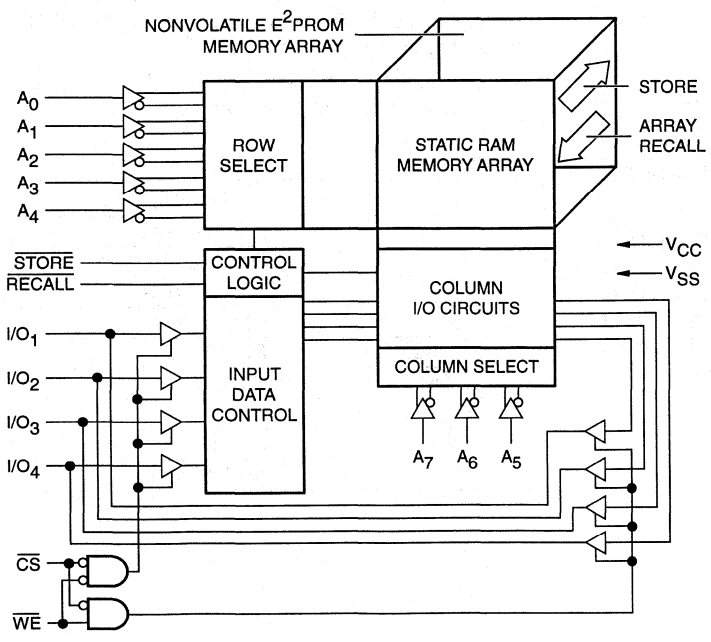
- **High Performance CMOS**
  - **—150ns RAM Access Time**
- **High Reliability**
  - **—Store Cycles: 1,000,000**
  - **—Data Retention: 100 Years**
- **Low Power Consumption**
  - **—Active: 40mA Max.**
  - **—Standby: 100µA Max.**
- **Infinite Array Recall, RAM Read and Write Cycles**
- **Nonvolatile Store Inhibit: V_{CC} = 3.5V Typical**
- **Fully TTL and CMOS Compatible**
- **JEDEC Standard 18-Pin 300-mil DIP**
- **100% Compatible with X2212**
  - **—With Timing Enhancements**

DESCRIPTION

The X22C12 is a 256 x 4 CMOS NOVRAM featuring a high-speed static RAM overlaid bit-for-bit with a nonvolatile E^2PROM. The NOVRAM design allows data to be easily transferred from RAM to E^2PROM (STORE) and from E^2PROM to RAM (RECALL). The STORE operation is completed within 5ms or less and the RECALL is completed within 1µs.

Xicor NOVRAMs are designed for unlimited write operations to the RAM, either RECALLs from E^2PROM or writes from the host. The X22C12 will reliably endure 1,000,000 STORE cycles. Inherent data retention is greater than 100 years.

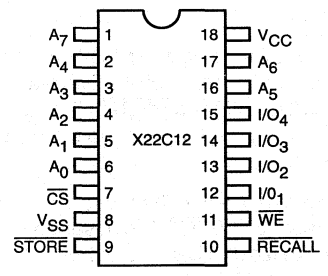
FUNCTIONAL DIAGRAM



3817 FHD F01

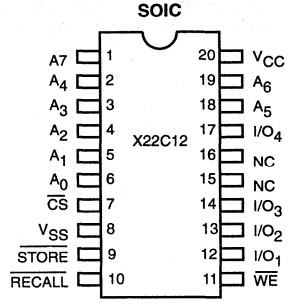
PIN CONFIGURATION

PLASTIC DIP
CERDIP



3817 FHD F02

SOIC



3815 FHD F10.1

PIN DESCRIPTIONS AND DEVICE OPERATION

Addresses (A_0–A_7)

The address inputs select a 4-bit memory location during a read or write operation.

Chip Select ($\overline{CS}$)

The Chip Select input must be LOW to enable read or write operations with the RAM array. $\overline{CS}$ HIGH will place the I/O pins in the high impedance state.

Write Enable ($\overline{WE}$)

The Write Enable input controls the I/O buffers, determining whether a RAM read or write operation is enabled. When $\overline{CS}$ is LOW and $\overline{WE}$ is HIGH, the I/O pins will output data from the selected RAM address locations. When both $\overline{CS}$ and $\overline{WE}$ are LOW, data presented at the I/O pins will be written to the selected address location.

Data In/Data Out (I/O_1–I/O_4)

Data is written to or read from the X22C12 through the I/O pins. The I/O pins are placed in the high impedance state when either $\overline{CS}$ is HIGH or during either a store or recall operation.

$\overline{STORE}$

The $\overline{STORE}$ input, when LOW, will initiate the transfer of the entire contents of the RAM array to the E^2PROM array. The $\overline{WE}$ and $\overline{RECALL}$ inputs are inhibited during the store cycle. The store operation is completed in 5ms or less.

A store operation has priority over RAM read/write operations. If $\overline{STORE}$ is asserted during a read operation, the read will be discontinued. If $\overline{STORE}$ is asserted during a RAM write operation, the write will be immediately terminated and the store performed. The data at the RAM address that was being written will be unknown in both the RAM and E^2PROM arrays.

$\overline{RECALL}$

The $\overline{RECALL}$ input, when LOW, will initiate the transfer of the entire contents of the E^2PROM array to the RAM array. The transfer of data will be completed in 1µs or less.

An array recall has priority over RAM read/write operations and will terminate both operations when $\overline{RECALL}$ is asserted. $\overline{RECALL}$ LOW will also inhibit the $\overline{STORE}$ input.

Automatic Recall

Upon power-up the X22C12 will automatically recall data from the E^2PROM array into the RAM array.

Write Protection

The X22C12 has three write protect features that are employed to protect the contents of the nonvolatile memory.

- V_{CC} Sense—All functions are inhibited when V_{CC} is <3.5V typical.
- Write Inhibit—Holding either $\overline{STORE}$ HIGH or $\overline{RECALL}$ LOW during power-up or power-down will prevent an inadvertent store operation and E^2PROM data integrity will be maintained.
- Noise Protection—A $\overline{STORE}$ pulse of typically less than 20ns will not initiate a store cycle.

PIN NAMES

Symbol	Description
A_0–A_7	Address Inputs
I/O_1–I/O_4	Data Inputs/Outputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{RECALL}$	Recall
$\overline{STORE}$	Store
V_{CC}	+5V
V_{SS}	Ground
NC	No Connect

3817 PGM T01

ABSOLUTE MAXIMUM RATINGS

Temperature under Bias ..... –65°C to +135°C
Storage Temperature ..... –65°C to +150°C
Voltage on any Pin with
Respect to V_{SS} ..... –1V to +7V
D.C. Output Current 5mA
Lead Temperature
(Soldering, 10 seconds) ..... 300°C

COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	+70°C
Industrial	–40°C	+85°C
Military	–55°C	+125°C

3817 PGM T12.1

Supply Voltage	Limits
X22C12	5V ±10%

3817 PGM T13

D.C. OPERATING CHARACTERISTICS (Over the recommended operating conditions, unless otherwise specified.)

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
I_{CC}	V_{CC} Supply Current, RAM Read/Write		40	mA	$\overline{CS}$ = V_{IL}, I/Os = Open, All Others = V_{IH}, Addresses = 0.4V/2.4V Levels @ f = 8MHz
I_{SB1}	V_{CC} Standby Current (TTL Inputs)		2	mA	Store or Recall Functions Not Active, I/Os = Open, All Other Inputs = V_{IH}
I_{SB2}	V_{CC} Standby Current (CMOS Inputs)		100	µA	Store or Recall functions Not Active, I/Os = Open, All Other Inputs = V_{CC} –0.3V
I_{LI}	Input Leakage Current		10	µA	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output Leakage Current		10	µA	V_{OUT} = V_{SS} to V_{CC}
V_{IL}(2)	Input LOW Voltage	–1	0.8	V	
V_{IH}(2)	Input HIGH Voltage	2	V_{CC} + 1	V	
V_{OL}	Output LOW Voltage		0.4	V	I_{OL} = 4.2mA
V_{OH}	Output HIGH Voltage	2.4		V	I_{OH} = –2mA

3817 PGM T02.3

CAPACITANCE T_A = +25°C, f = 1MHz, V_{CC} = 5V

Symbol	Parameter	Max.	Units	Test Conditions
$C_{I/O}$(1)	Input/Output Capacitance	8	pF	$V_{I/O}$ = 0V
C_{IN}(1)	Input Capacitance	6	pF	V_{IN} = 0V

3815 PGM T03.1

Notes: (1) This parameter is periodically sampled and not 100% tested.
(2) V_{IL} min. and V_{IH} max. are for reference only and are not tested.

MODE SELECTION

$\overline{CE}$	$\overline{WE}$	$\overline{RECALL}$	$\overline{STORE}$	I/O	Mode
H	X	H	H	Output High Z	Not Selected(3)
L	H	H	H	Output Data	Read RAM
L	L	H	H	Input Data High	Write "1" RAM
L	L	H	H	Input Data Low	Write "0" RAM
X	H	L	H	Output High Z	Array Recall
H	X	L	H	Output High Z	Array Recall
X	H	H	L	Output High Z	Nonvolatile Store(4)
H	X	H	L	Output High Z	Nonvolatile Store(4)

3817 PGM T05.1

ENDURANCE AND DATA RETENTION

Parameter	Min.	Units
Endurance	100,000	Data Changes Per Bit
Store Cycles	1,000,000	Store Cycles
Data Retention	100	Years

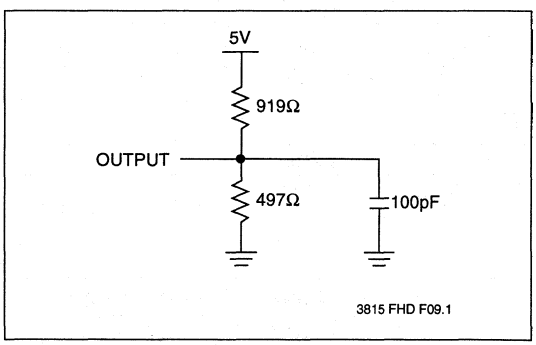
3817 PGM T06

POWER-UP TIMING

Symbol	Parameter	Max.	Units
t_{PUR}(5)	Power-up to Read Operation	100	µs
t_{PUW}(5)	Power-up to Write or Store Operation	5	ms

3817 PGM T07

EQUIVALENT A.C. LOAD CIRCUIT



3815 FHD F09.1

A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3V
Input Rise and Fall Times	10ns
Input and Output Timing Levels	1.5V

3817 PGM T04.1

Notes: (3) Chip is deselected but may be automatically completing a store cycle.
(4) $\overline{STORE}$ = LOW is required only to initiate the store cycle, after which the store cycle will be automatically completed (e.g. $\overline{STORE}$ = X).
(5) t_{PUR} and t_{PUW} are the delays required from the time V_{CC} is stable until the specified operation can be initiated. These parameters are periodically sampled and not 100% tested.

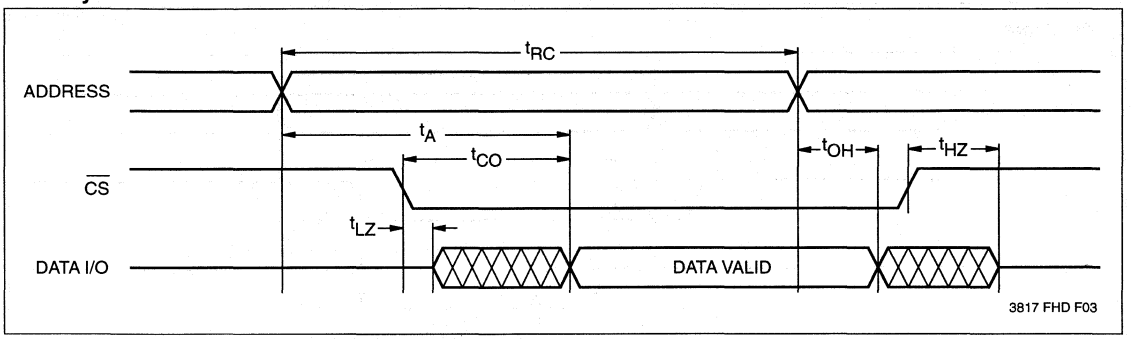
A.C. CHARACTERISTICS (Over the recommended operating conditions, unless otherwise specified.)

Read Cycle Limits

Symbol	Parameter	Min.	Max.	Units
t_{RC}	Read Cycle Time	150		ns
t_{AA}	Access Time		150	ns
t_{CO}	Chip Select to Output Valid		150	ns
t_{OH}	Output Hold from Address Change	0		ns
t_{LZ}(6)	Chip Select to Output in Low Z	0		ns
t_{HZ}(6)	Chip Deselect to Output in High Z		50	ns

3817 PGM T08

Read Cycle



3817 FHD F03

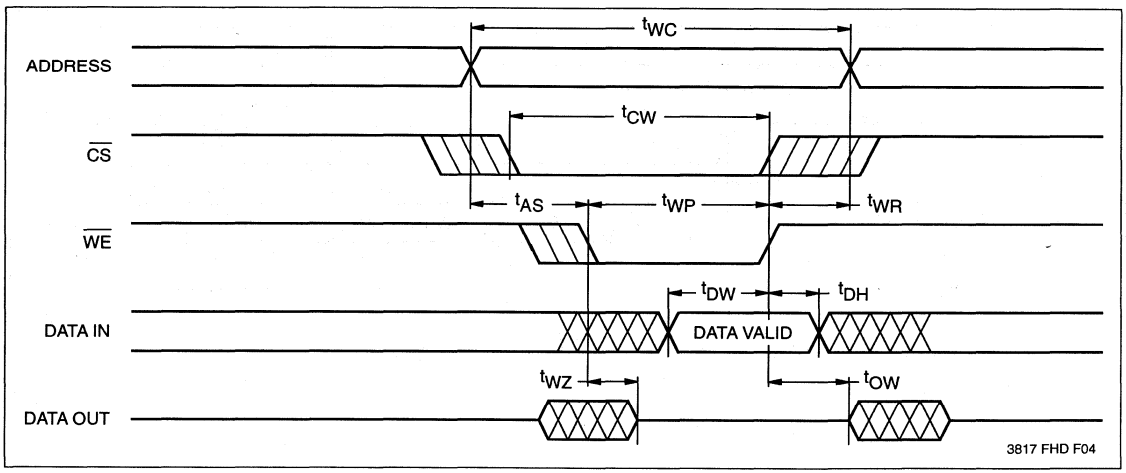
Note: (6) t_{LZ} min. and t_{HZ} min. are periodically sampled and not 100% tested.

Write Cycle Limits

Symbol	Parameter	Min.	Max.	Units
t_{WC}	Write Cycle Time	150		ns
t_{CW}	Chip Select to End of Write	90		ns
t_{AS}	Address Setup Time	0		ns
t_{WP}	Write Pulse Width	90		ns
t_{WR}	Write Recovery Time	0		ns
t_{DW}	Data Valid to End of Write	40		ns
t_{DH}	Data Hold Time	0		ns
t_{WZ}	Write Enable to Output in High Z		50	ns
t_{OW}	Output Active from End of Write	0		ns

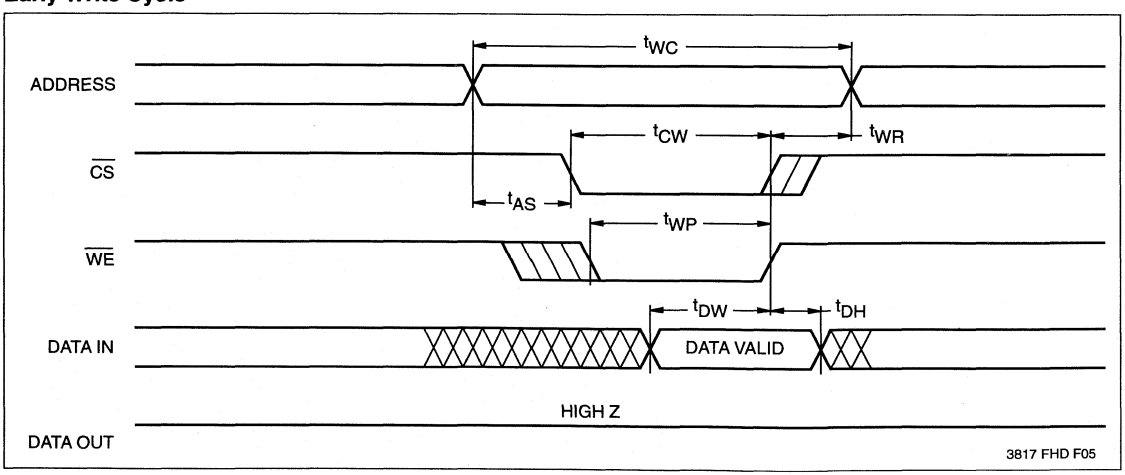
3817 PGM T09.1

Write Cycle



3817 FHD F04

Early Write Cycle



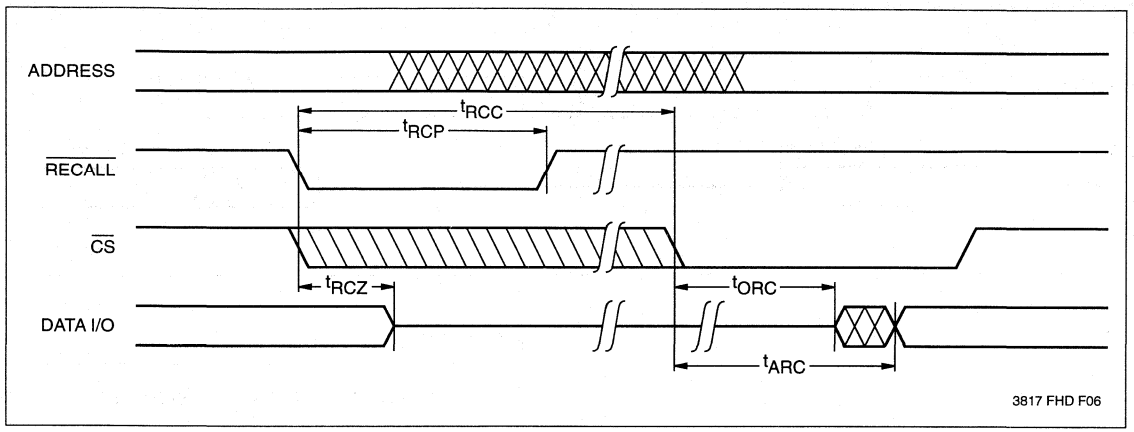
3817 FHD F05

Recall Cycle Limits

Symbol	Parameter	Min.	Max.	Units
t_{RCC}	Array Recall Time		1	µs
t_{RCP}(7)	Recall Pulse Width	90		ns
t_{RCZ}	Recall to Output in High Z		50	ns
t_{ORC}	Output Active from End of Recall	0		ns
t_{ARC}	Recalled Data Access Time from End of Recall		120	ns

3817 PGM T10

Recall Cycle



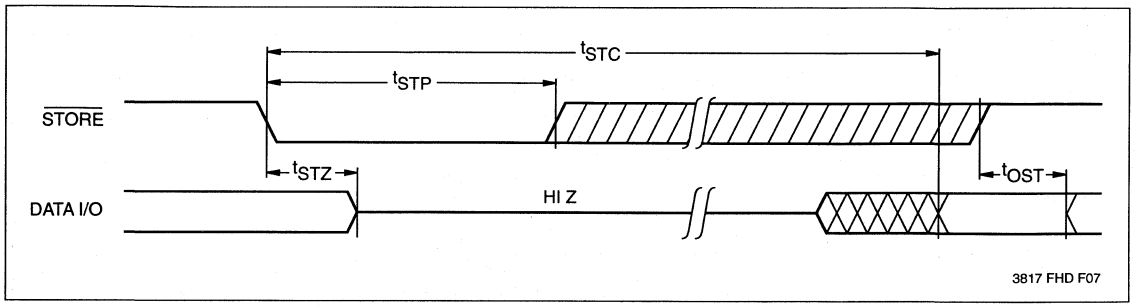
Note: (7) $\overline{\text{RECALL}}$ rise time must be less than 1µs.

Store Cycle Limits

Symbol	Parameter	Min.	Max.	Units
t_{STC}	Internal Store Time		5	ms
t_{STP}	Store Pulse Width	90		ns
t_{STZ}	Store to Output in High Z		50	ns
t_{OST}	Output Active from End of Store	0		ns

3817 PGM T11

Store Cycle Limits

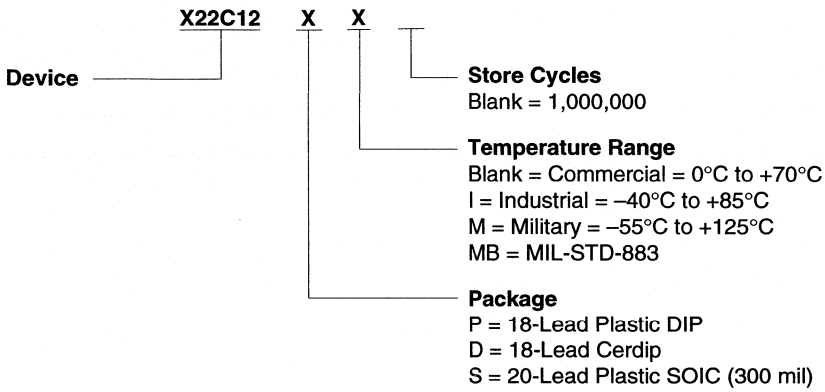


3817 FHD F07

SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

ORDERING INFORMATION



NOTES

Nonvolatile Static RAM

FEATURES

- **High Reliability**
  - **—Endurance: 1,000,000 Nonvolatile Store Operations**
  - **—Retention: 100 Years Minimum**
- **Power-on Recall**
  - **—E^2PROM Data Automatically Recalled Into SRAM Upon Power-up**
- **Lock Out Inadvertent Store Operations**
- **Low Power CMOS**
  - **—Standby: 250µA**
- **Infinite E^2PROM Array Recall, and RAM Read and Write Cycles**
- **Compatible with X2004**

DESCRIPTION

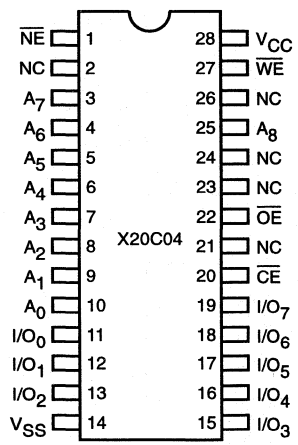
The Xicor X20C04 is a 512 x 8 NOVRAM featuring a static RAM overlaid bit-for-bit with a nonvolatile electrically erasable PROM (E^2PROM). The X20C04 is fabricated with advanced CMOS floating gate technology to achieve low power and wide power-supply margin. The X20C04 features the JEDEC approved pinout for byte-wide memories, compatible with industry standard RAMs, ROMs, EPROMs, and E^2PROMs.

The NOVRAM design allows data to be easily transferred from RAM to E^2PROM (store) and E^2PROM to RAM (recall). The store operation is completed in 5ms or less and the recall operation is completed in 5µs or less.

Xicor NOVRAMS are designed for unlimited write operations to RAM, either from the host or recalls from E^2PROM, and a minimum 1,000,000 store operations to the E^2PROM. Data retention is specified to be greater than 100 years.

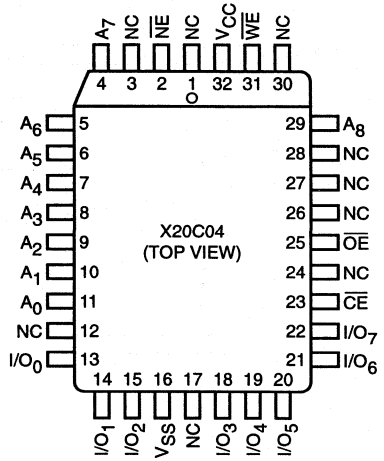
PIN CONFIGURATION

PLASTIC
CERDIP



3825 FHD F02

LCC
PLCC



3825 FHD F03

PIN DESCRIPTIONS

Addresses (A_0–A_8)

The Address inputs select an 8-bit memory location during a read or write operation.

Chip Enable ($\overline{CE}$)

The Chip Enable input must be LOW to enable all read/write operations. When $\overline{CE}$ is HIGH, power consumption is reduced.

Output Enable ($\overline{OE}$)

The Output Enable input controls the data output buffers and is used to initiate read and recall operations. Output Enable LOW disables a store operation regardless of the state of $\overline{CE}$, $\overline{WE}$, or $\overline{NE}$.

Data In/Data Out (I/O_0–I/O_7)

Data is written to or read from the X20C04 through the I/O pins. The I/O pins are placed in the high impedance state when either $\overline{CE}$ or $\overline{OE}$ is HIGH or when $\overline{NE}$ is LOW.

Write Enable ($\overline{WE}$)

The Write Enable input controls the writing of data to both the static RAM and stores to the E^2PROM.

Nonvolatile Enable ($\overline{NE}$)

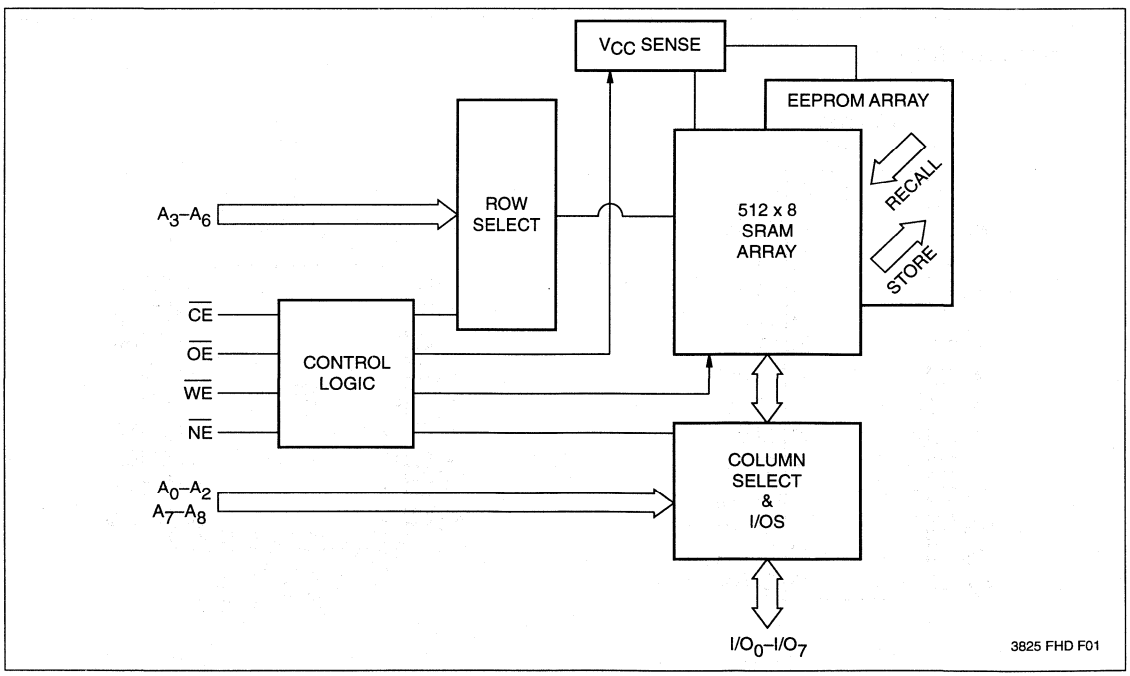
The Nonvolatile Enable input controls all accesses to the E^2PROM array (store and recall functions).

PIN NAMES

Symbol	Description
A_0–A_8	Address Inputs
I/O_0–I/O_7	Data Input/Output
$\overline{WE}$	Write Enable
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{NE}$	Nonvolatile Enable
V_{CC}	+5V
V_{SS}	Ground
NC	No Connect

3825 PGM T01

FUNCTIONAL DIAGRAM



3825 FHD F01

DEVICE OPERATION

The $\overline{CE}$, $\overline{OE}$, $\overline{WE}$ and $\overline{NE}$ inputs control the X20C04 operation. The X20C04 byte-wide NOVRAM uses a 2-line control architecture to eliminate bus contention in a system environment. The I/O bus will be in a high impedance state when either $\overline{OE}$ or $\overline{CE}$ is HIGH, or when $\overline{NE}$ is LOW.

RAM Operations

RAM read and write operations are performed as they would be with any static RAM. A read operation requires $\overline{CE}$ and $\overline{OE}$ to be LOW with $\overline{WE}$ and $\overline{NE}$ HIGH. A write operation requires $\overline{CE}$ and $\overline{WE}$ to be LOW with $\overline{NE}$ HIGH. There is no limit to the number of read or write operations performed to the RAM portion of the X20C04.

Nonvolatile Operations

With $\overline{NE}$ LOW, recall operation is performed in the same manner as RAM read operation. A recall operation causes the entire contents of the E^2PROM to be written into the RAM array. The time required for the operation to complete is 5µs or less. A store operation causes the entire contents of the RAM array to be stored in the nonvolatile E^2PROM. The time for the operation to complete is 5ms or less.

Power-Up Recall

Upon power-up (V_{CC}), the X20C04 performs an automatic array recall. When V_{CC} minimum is reached, the recall is initiated, regardless of the state of $\overline{CE}$, $\overline{OE}$, $\overline{WE}$ and $\overline{NE}$.

Write Protection

The X20C04 has five write protect features that are employed to protect the contents of both the nonvolatile memory and the RAM.

- V_{CC} Sense—All functions are inhibited when V_{CC} is ≤ 3.5V.
- A RAM write is required before a Store Cycle is initiated.
- Write Inhibit—Holding either $\overline{OE}$ LOW, $\overline{WE}$ HIGH, $\overline{CE}$ HIGH, or $\overline{NE}$ HIGH during power-up and power-down will prevent an inadvertent store operation.
- Noise Protection—A combined $\overline{WE}$, $\overline{NE}$, $\overline{OE}$ and $\overline{CE}$ pulse of less than 20ns will not initiate a Store Cycle.
- Noise Protection—A combined $\overline{WE}$, $\overline{NE}$, $\overline{OE}$ and $\overline{CE}$ pulse of less than 20ns will not initiate a recall cycle.

SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

ABSOLUTE MAXIMUM RATINGS*

Temperature under Bias ..... –65°C to +135°C
Storage Temperature ..... –65°C to +150°C
Voltage on any Pin with
Respect to V_{SS} ..... –1V to +7V
D.C. Output Current 10mA
Lead Temperature (Soldering, 10 seconds) ..... 300°C

***COMMENT**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	+70°C
Industrial	–40°C	+85°C
Military	–55°C	+125°C

3825 PGM T02.1

Supply Voltage	Limits
X20C04	5V ±10%

3825 PGM T03

D.C. OPERATING CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits			Test Conditions
		Min.	Max.	Units	
I_{CC1}	V_{CC} Current (Active)		100	mA	$\overline{NE} = \overline{WE} = V_{IH}$, $\overline{CE} = \overline{OE} = V_{IL}$ Address Inputs = 0.4V/2.4V levels @ f = 5MHz. All I/Os = Open
I_{CC2}	V_{CC} Current During Store		10	mA	All Inputs = V_{IH} All I/Os = Open
I_{SB1}	V_{CC} Standby Current (TTL Input)		10	mA	$\overline{CE} = V_{IH}$ All Other Inputs = V_{IH}, All I/Os = Open
I_{SB2}	V_{CC} Standby Current (CMOS Input)		250	µA	All Inputs = V_{CC} – 0.3V All I/Os = Open
I_{LI}	Input Leakage Current		10	µA	$V_{IN} = V_{SS}$ to V_{CC}
I_{LO}	Output Leakage Current		10	µA	$V_{OUT} = V_{SS}$ to V_{CC}, $\overline{CE} = V_{IH}$
V_{IL}(1)	Input LOW Voltage	–1	0.8	V	
V_{IH}(1)	Input HIGH Voltage	2	V_{CC} + 0.5	V	
V_{OL}	Output LOW Voltage		0.4	V	I_{OL} = 2.1mA
V_{OH}	Output HIGH Voltage	2.4		V	I_{OH} = –400µA

3825 PGM T04.3

POWER-UP TIMING

Symbol	Parameter	Max.	Units
t_{PUR}(2)	Power-Up to RAM Operation	100	µs
t_{PUW}(2)	Power-Up to Nonvolatile Operation	5	ms

3825 PGM T05

CAPACITANCE T_A = +25°C, F = 1MHz, V_{CC} = 5V.

Symbol	Test	Max.	Units	Conditions
$C_{I/O}$(2)	Input/Output Capacitance	10	pF	$V_{I/O}$ = 0V
C_{IN}(2)	Input Capacitance	6	pF	V_{IN} = 0V

3825 PGM T06.1

Notes: (1) V_{IL} min. and V_{IH} max. are for reference only and are not tested.
(2) This parameter is periodically sampled and not 100% tested.

ENDURANCE AND DATA RETENTION

Parameter	Min.	Units
Endurance	100,000	Data Changes Per Bit
Store Cycles	1,000,000	Store Cycles
Data Retention	100	Years

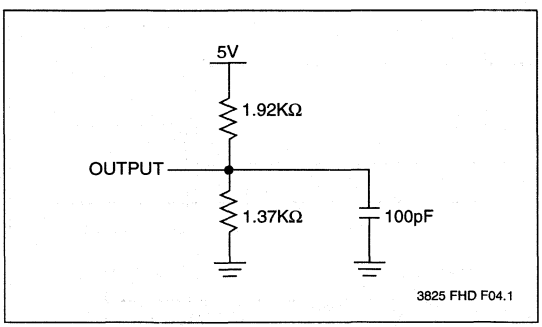
3825 PGM T07.1

MODE SELECTION

$\overline{CE}$	$\overline{WE}$	$\overline{NE}$	$\overline{OE}$	Mode	I/O	Power
H	X	X	X	Not Selected	Output High Z	Standby
L	H	H	L	Read RAM	Output Data	Active
L	L	H	X	Write "1" RAM	Input Data High	Active
L	L	H	X	Write "0" RAM	Input Data Low	Active
L	H	L	L	Array Recall	Output High Z	Active
L	L	L	H	Nonvolatile Storing	Output High Z	Active
L	H	H	H	Output Disabled	Output High Z	Active
L	L	L	L	Not Allowed	Output High Z	Active
L	H	L	H	No Operation	Output High Z	Active

3825 PGM T09.1

EQUIVALENT A.C. LOAD CIRCUIT



3825 FHD F04.1

A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3V
Input Rise and Fall Times	10ns
Input and Output Timing Levels	1.5V

3825 PGM T08.2

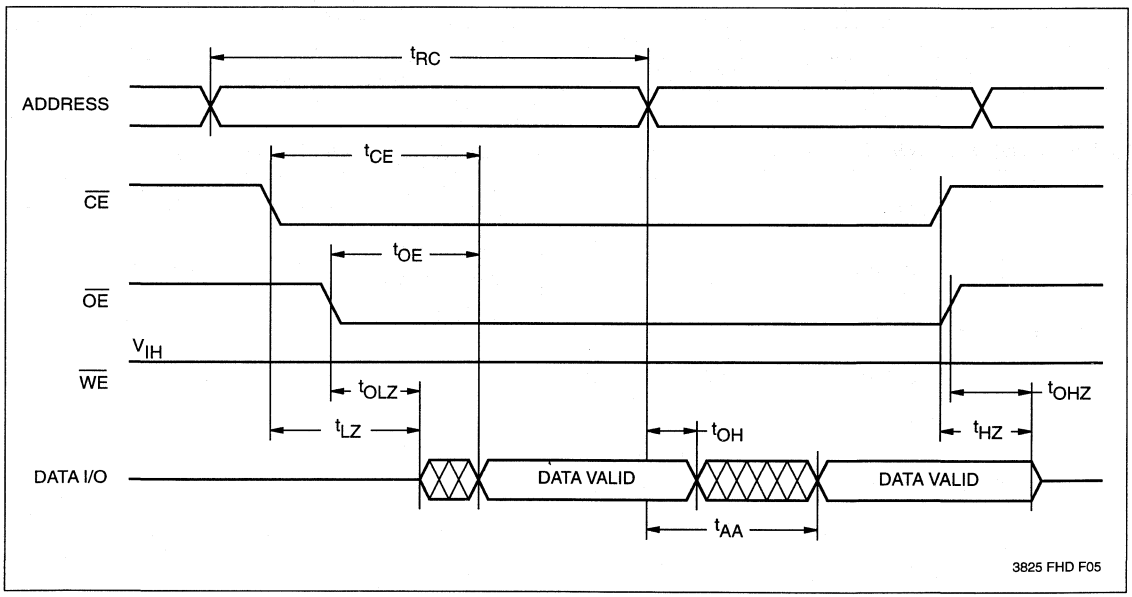
A.C. CHARACTERISTICS (Over the recommended operating conditions unless otherwise specified)

Read Cycle Limits

Symbol	Parameter	X20C04-15		X20C04-20		X20C04-25		X20C04		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	150		200		250		300		ns
t_{CE}	Chip Enable Access Time		150		200		250		300	ns
t_{AA}	Address Access Time		150		200		250		300	ns
t_{OE}	Output Enable Access Time		50		70		100		150	ns
t_{LZ}(3)	Chip Enable to Output in Low Z	0		0		0		0		ns
t_{OLZ}(3)	Output Enable to Output in Low Z	0		0		0		0		ns
t_{HZ}(3)	Chip Disable to Output in High Z		80		100		100		100	ns
t_{OHZ}(3)	Output Disable to Output in High Z		80		100		100		100	ns
t_{OH}	Output Hold From Address Change	0		0		0		0		ns

3825 PGM T10

Read Cycle



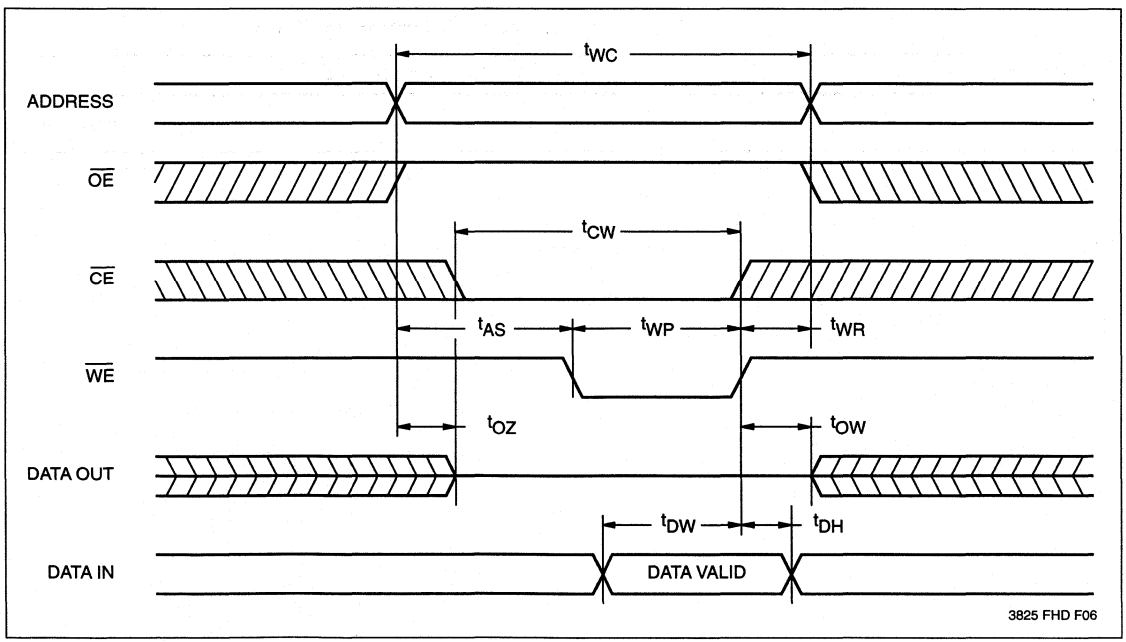
Note: (3) t_{LZ} min., t_{HZ}, t_{OLZ} min., and t_{OHZ} are periodically sampled and not 100% tested. t_{HZ} max. and t_{OHZ} max. are measured, with C_L = 5pF from the point when $\overline{CE}$ or $\overline{OE}$ return HIGH (whichever occurs first) to the time when the outptus are no longer driven.

Write Cycle Limits

Symbol	Parameter	X20C04-15		X20C04-20		X20C04-25		X20C04		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{WC}	Write Cycle Time	150		200		250		300		ns
t_{CW}	Chip Enable to End of Write Input	150		200		250		300		ns
t_{AS}	Address Setup Time	0		0		0		0		ns
t_{WP}	Write Pulse Width	100		120		150		200		ns
t_{WR}	Write Recovery Time	0		0		0		0		ns
t_{DW}	Data Setup to End of Write	100		120		150		200		ns
t_{DH}	Data Hold Time	0		0		0		0		ns
t_{WZ}(4)	Write Enable to Output in High Z		80		100		100		100	ns
t_{OW}(4)	Output Active from End of Write	5		5		5		5		ns
t_{OZ}(4)	Output Enable to Output in High Z		80		100		100		100	ns

3825 PGM T11

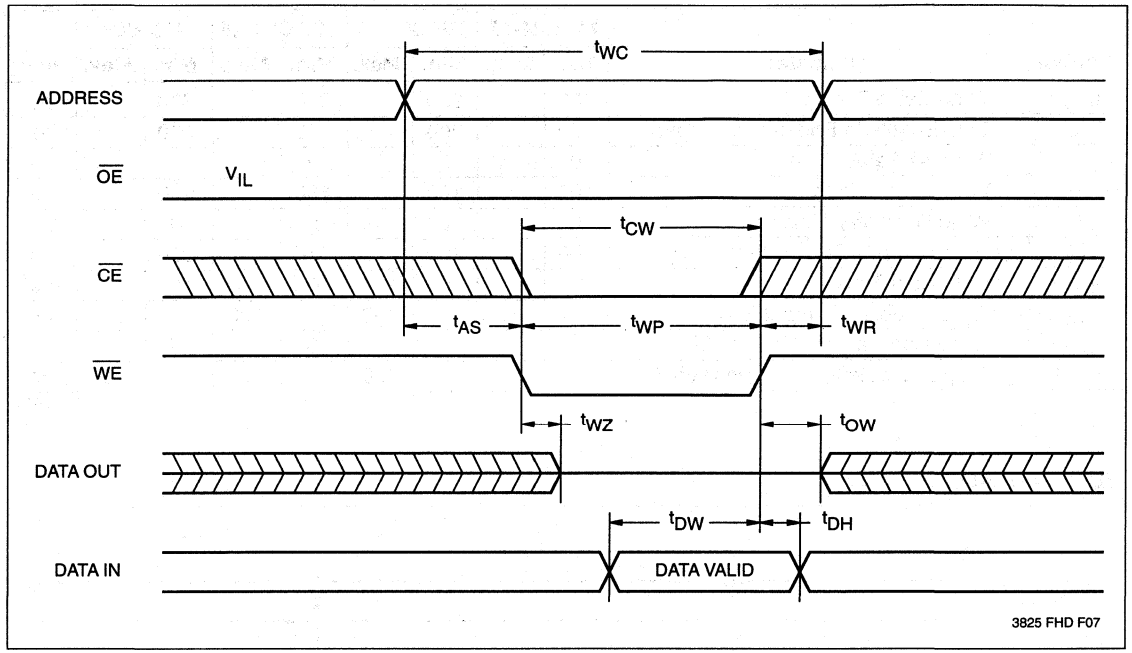
$\overline{WE}$ Controlled Write Cycle



3825 FHD F06

Note: (4) t_{WZ}, t_{OW}, and t_{OZ} are periodically sampled and not 100% tested.

$\overline{CE}$ Controlled Write Cycle

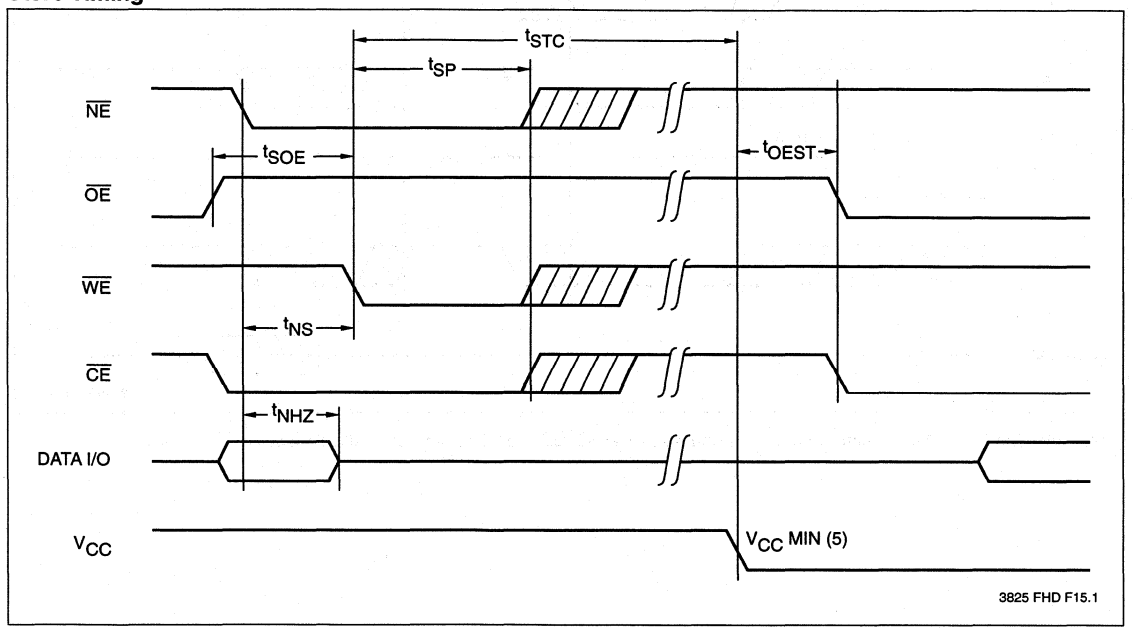


STORE CYCLE LIMITS

Symbol	Parameter	X20C04-15		X20C04-20		X20C04-25		X20C04		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{STC}	Store Cycle Time		5		5		5		5	ms
t_{SP}	Store Pulse Width	100		120		150		200		ns
t_{NHZ}	Nonvolatile Enable to Output in High Z		80		100		100		100	ns
t_{OEST}	Output Enable From End of Store	10		10		10		10		ns
t_{SOE}	$\overline{OE}$ Disable to Store Function	20		20		20		20		ns
t_{NS}	$\overline{NE}$ Setup Time from $\overline{WE}$	0		0		0		0		ns

3825 PGM T09

Store Timing



3825 FHD F15.1

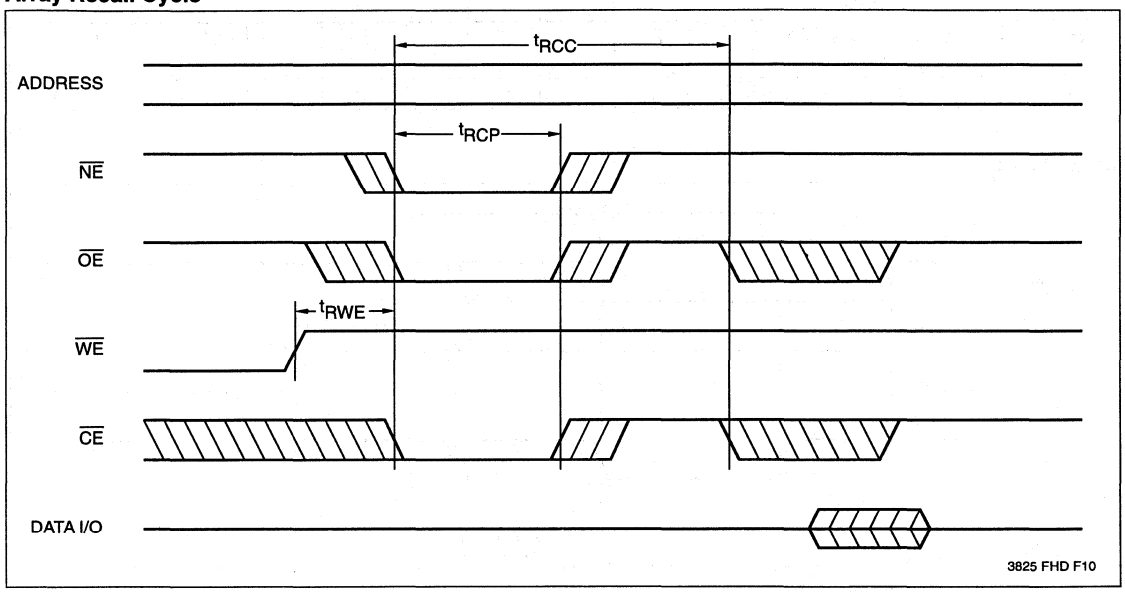
Note: (5) X20C04 V_{CC} min. = 4.5V
The Store Pulse Width (t_{SP}) is a minimum time that $\overline{NE}$, $\overline{WE}$ and $\overline{CE}$ must be LOW simultaneously.

ARRAY RECALL CYCLE LIMITS

Symbol	Parameter	X20C04-15		X20C04-20		X20C04-25		X20C04		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{RCC}	Array Recall Cycle Time		5		5		5		5	µs
t_{RCP}(6)	Recall Pulse Width to InitiateRecall	0.1	1	0.12	1	0.15	1	0.2	1	µs
t_{RWE}	$\overline{WE}$ Setup Time to $\overline{NE}$	0		0		0		0		ns

3825 PGM T13.1

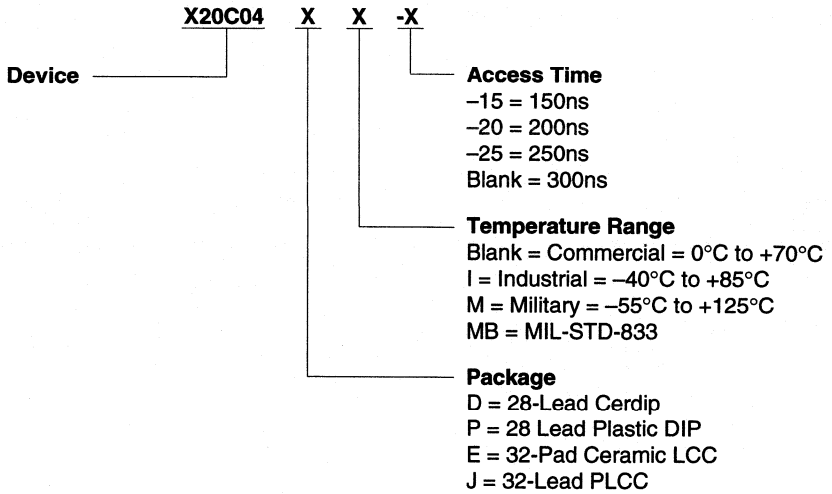
Array Recall Cycle



3825 FHD F10

Note: (6) The Recall Pulse Width (t_{RCP}) is a minimum time that $\overline{NE}$, $\overline{OE}$ and $\overline{CE}$ must be LOW simultaneously.

ORDERING INFORMATION



NOTES

APPLICATION NOTE
AVAILABLE
AN56

4K X20C05 512 x 8

High Speed AUTOSTORE™ NOVRAM

1

FEATURES

- Fast Access Time: 35ns, 45ns, 55ns
- High Reliability
  - —Endurance: 1,000,000 Nonvolatile Store Operations
  - —Retention: 100 Years Minimum
- Power-on Recall
  - —E^2PROM Data Automatically Recalled Into SRAM Upon Power-up
- AUTOSTORE™ NOVRAM
  - —User Enabled Option
  - —Automatically Stores SRAM Data Into the E^2PROM Array When V_{CC} Low Threshold is Detected
  - —Open Drain AUTOSTORE Status Output Pin
- Software Data Protection
  - —Locks Out Inadvertent Store Operations
- Low Power CMOS
  - —Standby: 250µA
- Infinite E^2PROM Array Recall, and RAM Read and Write Cycles
- Upward compatible with X20C16 (16K)

DESCRIPTION

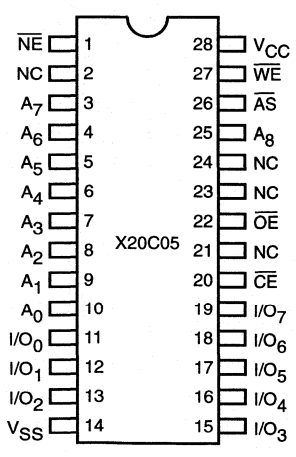
The Xicor X20C05 is a 512 x 8 NOVRAM featuring a high-speed static RAM overlaid bit-for-bit with a non-volatile electrically erasable PROM (E^2PROM). The X20C05 is fabricated with advanced CMOS floating gate technology to achieve high speed with low power and wide power-supply margin. The X20C05 features the JEDEC approved pinout for byte-wide memories, compatible with industry standard RAMs, ROMs, EPROMs, and E^2PROMs.

The NOVRAM design allows data to be easily transferred from RAM to E^2PROM (store) and E^2PROM to RAM (recall). The store operation is completed in 5ms or less and the recall operation is completed in 5µs or less.

Xicor NOVRAMs are designed for unlimited write operations to RAM, either from the host or recalls from E^2PROM, and a minimum 1,000,000 store operations to the E^2PROM. Data retention is specified to be greater than 100 years.

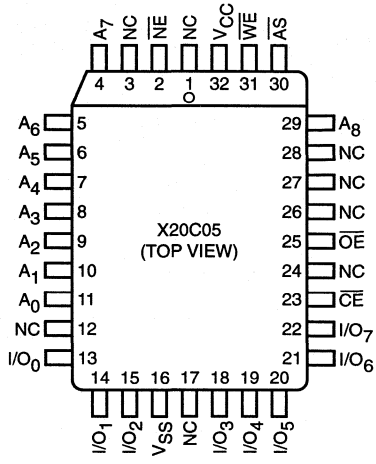
PIN CONFIGURATION

PLASTIC
CERDIP



3827 FHD F02

LCC
PLCC



3827 FHD F03

AUTOSTORE™ NOVRAM is a trademark of Xicor, Inc.

PIN DESCRIPTIONS

Addresses (A_0–A_8)

The Address inputs select an 8-bit memory location during a read or write operation.

Chip Enable ($\overline{CE}$)

The Chip Enable input must be LOW to enable all read/write operations. When $\overline{CE}$ is HIGH, power consumption is reduced.

Output Enable ($\overline{OE}$)

The Output Enable input controls the data output buffers and is used to initiate read and recall operations. Output Enable LOW disables a store operation regardless of the state of $\overline{CE}$, $\overline{WE}$, or $\overline{NE}$.

Data In/Data Out (I/O_0–I/O_7)

Data is written to or read from the X20C05 through the I/O pins. The I/O pins are placed in the high impedance state when either $\overline{CE}$ or $\overline{OE}$ is HIGH or when $\overline{NE}$ is LOW.

Write Enable ($\overline{WE}$)

The Write Enable input controls the writing of data to the RAM.

Nonvolatile Enable ($\overline{NE}$)

The Nonvolatile Enable input controls the recall function to the E²PROM array.

AUTOSTORE Output ($\overline{AS}$)

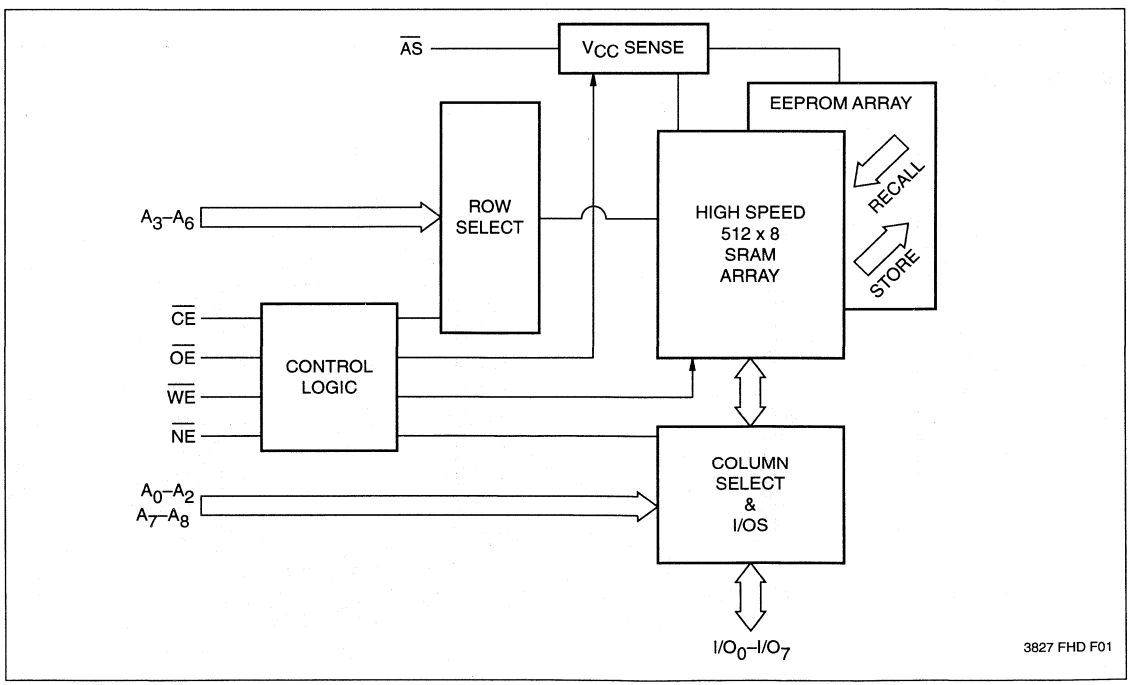
$\overline{AS}$ is an open drain output which, when asserted indicates V_{CC} has fallen below the AUTOSTORE threshold (V_{ASTH}). $\overline{AS}$ may be wire-ORed with multiple open drain outputs and used as an interrupt input to a microcontroller.

PIN NAMES

Symbol	Description
A_0–A_8	Address Inputs
I/O_0–I/O_7	Data Input/Output
$\overline{WE}$	Write Enable
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{NE}$	Nonvolatile Enable
$\overline{AS}$	AUTOSTORE Output
V_{CC}	+5V
V_{SS}	Ground
NC	No Connect

3827 PGM T01

FUNCTIONAL DIAGRAM



3827 FHD F01

DEVICE OPERATION

The $\overline{CE}$, $\overline{OE}$, $\overline{WE}$ and $\overline{NE}$ inputs control the X20C05 operation. The X20C05 byte-wide NOVRAM uses a 2-line control architecture to eliminate bus contention in a system environment. The I/O bus will be in a high impedance state when either $\overline{OE}$ or $\overline{CE}$ is HIGH, or when $\overline{NE}$ is LOW.

RAM Operations

RAM read and write operations are performed as they would be with any static RAM. A read operation requires $\overline{CE}$ and $\overline{OE}$ to be LOW with $\overline{WE}$ and $\overline{NE}$ HIGH. A write operation requires $\overline{CE}$ and $\overline{WE}$ to be LOW with $\overline{NE}$ HIGH. There is no limit to the number of read or write operations performed to the RAM portion of the X20C05.

MEMORY TRANSFER OPERATIONS

There are two memory transfer operations: a recall operation whereby the data stored in the E^2PROM array is transferred to the RAM array; and a store operation which causes the entire contents of the RAM array to be stored in the E^2PROM array.

Recall operations are performed automatically upon power-up and under host system control when $\overline{NE}$, $\overline{OE}$ and $\overline{CE}$ are LOW and $\overline{WE}$ is HIGH. The recall operation takes a maximum of 5µs.

There are two methods of initiating a store operation. The first is the software store command. This command takes the place of the hardware store employed on the X20C04. This command is issued by entering into the special command mode: $\overline{NE}$, $\overline{CE}$, and $\overline{WE}$ strobe LOW while at the same time a specific address and data combination is sent to the device. This is a three step operation: the first address/data combination is 155[H]/AA[H]; the second combination is 0AA[H]/55[H]; and the final command combination is 155[H]/33[H]. This sequence of pseudo write operations will immediately initiate a store operation. Refer to the software command timing diagrams for details on set and hold times for the various signals.

The second method of storing data is through the AUTOSTORE command. When enabled, data is automatically stored from the RAM into the E^2PROM array whenever V_{CC} falls below the preset AUTOSTORE threshold. This feature is enabled by performing the first two steps for the software store with the command combination being 155[H]/CC[H].

The AUTOSTORE feature is disabled by issuing the three step command sequence with the command combination being 155[H]/CD[H]. The AUTOSTORE feature will also be reset if V_{CC} falls below the power-up reset threshold (approximately 3.5V) and is then raised back into the operating range.

DATA PROTECTION

The X20C05 supports two methods of protecting the nonvolatile data.

—If after power-up the AUTOSTORE feature is not enabled, no AUTOSTORE can occur.

—If after power-up no RAM write operations have occurred no store operation can be initiated. The software store and AUTOSTORE commands will be ignored.

SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
———	Must be steady	Will be steady
⟋⟋⟋	May change from LOW to HIGH	Will change from LOW to HIGH
⟍⟍⟍	May change from HIGH to LOW	Will change from HIGH to LOW
⟋⟍⟋⟍	Don't Care: Changes Allowed	Changing: State Not Known
⟋⟍ ⟍⟋	N/A	Center Line is High Impedance

ABSOLUTE MAXIMUM RATINGS*

Temperature under Bias ..... –65°C to +135°C
Storage Temperature ..... –65°C to +150°C
Voltage on any Pin with
Respect to V_{SS} ..... –1V to +7V
D.C. Output Current 10mA
Lead Temperature (Soldering, 10 seconds) ..... 300°C

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	+70°C
Industrial	–40°C	+85°C
Military	–55°C	+125°C

3827 PGM T02.1

Supply Voltage	Limits
X20C05	5V ±10%

3827 PGM T03.1

D.C. OPERATING CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits			Test Conditions
		Min.	Max.	Units	
I_{CC1}	V_{CC} Current (Active)		100	mA	$\overline{NE} = \overline{WE} = V_{IH}$, $\overline{CE} = \overline{OE} = V_{IL}$ Address Inputs = 0.4V/2.4V Levels @ f = 20MHz. All I/Os = Open
I_{CC2}	V_{CC} Current During Store		5	mA	All Inputs = V_{IH}
I_{CC3}	V_{CC} Current During AUTOSTORE		2.5	mA	All I/Os = Open
I_{SB1}	V_{CC} Standby Current (TTL Input)		10	mA	$\overline{CE} = V_{IH}$ All Other Inputs = V_{IH}, All I/Os = Open
I_{SB2}	V_{CC} Standby Current (CMOS Input)		250	µA	All Inputs = V_{CC} – 0.3V All I/Os = Open
I_{LI}	Input Leakage Current		10	µA	$V_{IN} = V_{SS}$ to V_{CC}
I_{LO}	Output Leakage Current		10	µA	$V_{OUT} = V_{SS}$ to V_{CC}, $\overline{CE} = V_{IH}$
V_{IL}(1)	Input LOW Voltage	–1	0.8	V	
V_{IH}(1)	Input HIGH Voltage	2	V_{CC} + 0.5	V	
V_{OL}	Output LOW Voltage		0.4	V	I_{OL} = 4mA
V_{OLAS}	AUTOSTORE Output		0.4	V	I_{OLAS} = 1mA
V_{OH}	Output HIGH Voltage	2.4		V	I_{OH} = –4mA

3827 PGM T04.3

POWER-UP TIMING

Symbol	Parameter	Max.	Units
t_{PUR}(2)	Power-Up to RAM Operation	100	µs
t_{PUW}(2)	Power-Up to Nonvolatile Operation	5	ms

3827 PGM T05

CAPACITANCE T_A = +25°C, f = 1MHz, V_{CC} = 5V.

Symbol	Test	Max.	Units	Conditions
$C_{I/O}$(2)	Input/Output Capacitance	10	pF	$V_{I/O}$ = 0V
C_{IN}(2)	Input Capacitance	6	pF	V_{IN} = 0V

3827 PGM T06.2

Notes: (1) V_{IL} min. and V_{IH} max. are for reference only and are not tested.
(2) This parameter is periodically sampled and not 100% tested.

ENDURANCE AND DATA RETENTION

Parameter	Min.	Units
Endurance	100,000	Data Changes Per Bit
Store Cycles	1,000,000	Store Cycles
Data Retention	100	Years

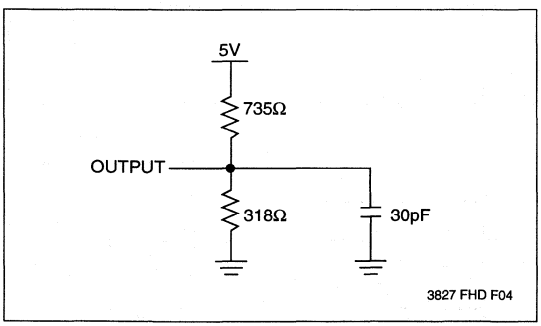
3827 PGM T07.1

MODE SELECTION

$\overline{CE}$	$\overline{WE}$	$\overline{NE}$	$\overline{OE}$	Mode	I/O	Power
H	X	X	X	Not Selected	Output High Z	Standby
L	H	H	L	Read RAM	Output Data	Active
L	L	H	X	Write "1" RAM	Input Data High	Active
L	L	H	X	Write "0" RAM	Input Data Low	Active
L	H	L	L	Array Recall	Output High Z	Active
L	L	L	H	Software Command	Input Data	Active
L	H	H	H	Output Disabled	Output High Z	Active
L	L	L	L	Not Allowed	Output High Z	Active
L	H	L	H	No Operation	Output High Z	Active

3827 PGM T09

EQUIVALENT A.C. LOAD CIRCUIT



3827 FHD F04

A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3V
Input Rise and Fall Times	5ns
Input and Output Timing Levels	1.5V

3827 PGM T08.2

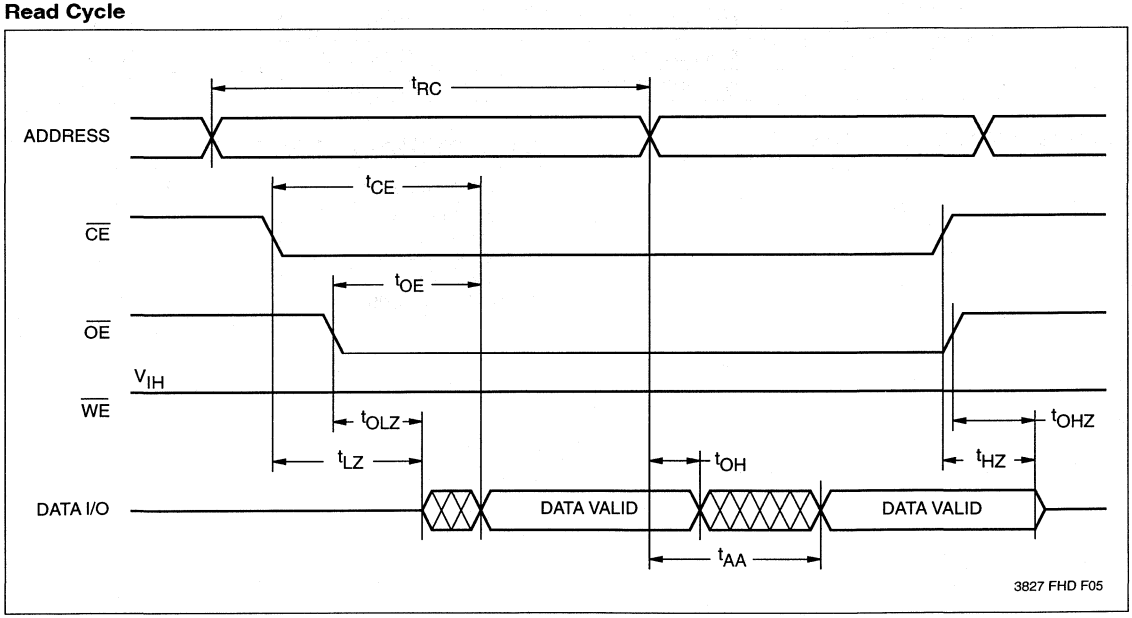
A.C. CHARACTERISTICS (Over the recommended operating conditions unless otherwise specified)

Read Cycle Limits

Symbol	Parameter	X20C05-35		X20C05-45		X20C05-55		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	35		45		55		ns
t_{CE}	Chip Enable Access Time		35		45		55	ns
t_{AA}	Address Access Time		35		45		55	ns
t_{OE}	Output Enable Access Time		20		25		30	ns
t_{LZ}(3)	Chip Enable to Output in Low Z	0		0		0		ns
t_{OLZ}(3)	Output Enable to Output in Low Z	0		0		0		ns
t_{HZ}(3)	Chip Disable to Output in High Z		15		20		25	ns
t_{OHZ}(3)	Output Disable to Output in High Z		15		20		25	ns
t_{OH}	Output Hold From Address Change	0		0		0		ns

3827 PGM T10

Read Cycle



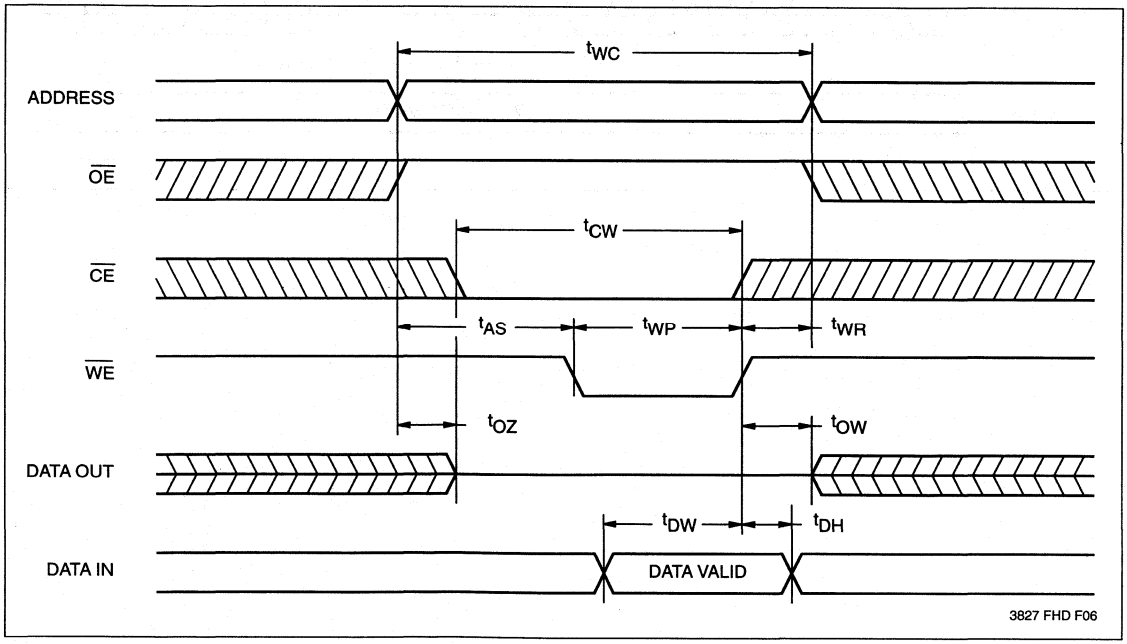
Note: (3) t_{LZ} min., t_{HZ}, t_{OLZ} min., and t_{OHZ} are periodically sampled and not 100% tested. t_{HZ} and t_{OHZ} are measured, with C_L = 5pF, from the point when $\overline{CE}$ or $\overline{OE}$ return HIGH (whichever occurs first) to the time when the outptus are no longer driven.

Write Cycle Limits

Symbol	Parameter	X20C05-25		X20C05-35		X20C05-45		X20C05-55		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{WC}	Write Cycle Time	25		35		45		55		ns
t_{CW}	Chip Enable to End of Write Input	25		30		35		40		ns
t_{AS}	Address Setup Time	0		0		0		0		ns
t_{WP}	Write Pulse Width	30		30		35		40		ns
t_{WR}	Write Recovery Time	0		0		0		0		ns
t_{DW}	Data Setup to End of Write	15		15		20		25		ns
t_{DH}	Data Hold Time	0		0		3		3		ns
t_{WZ}(4)	Write Enable to Output in High Z				15		20		25	ns
t_{OW}(4)	Output Active from End of Write	5		5		5		5		ns
t_{OZ}(4)	Output Enable to Output in High Z				15		20		25	ns

3827 PGM T11

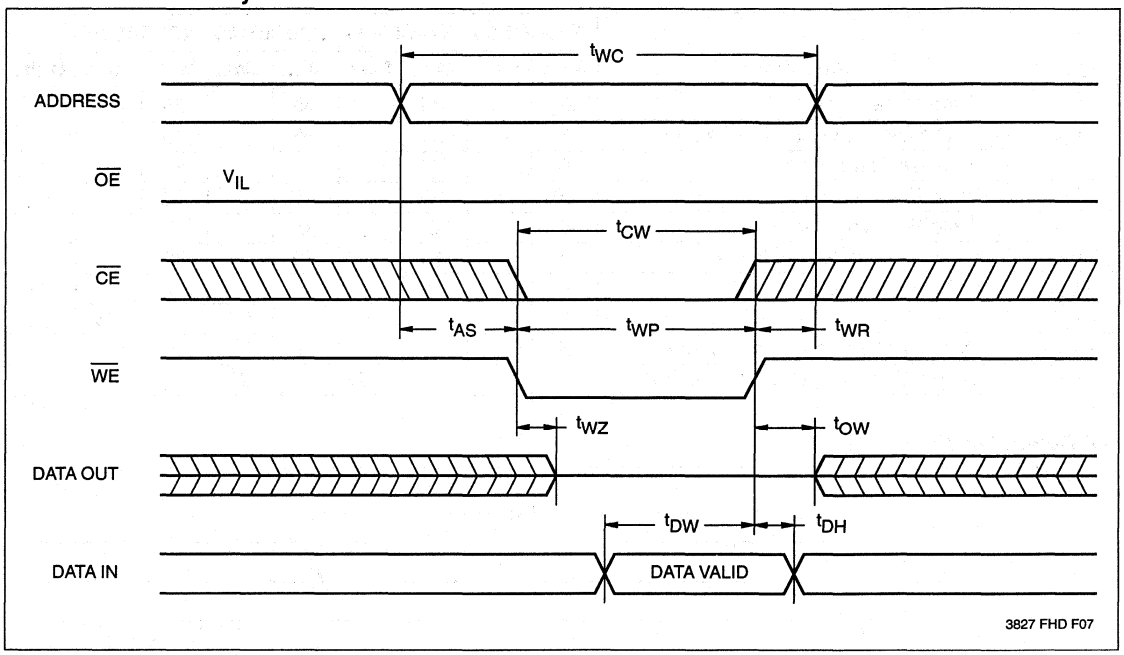
$\overline{WE}$ Controlled Write Cycle



3827 FHD F06

Note: (4) t_{WZ}, t_{OW} and t_{OZ} are periodically sampled and not 100% tested.

$\overline{CE}$ Controlled Write Cycle

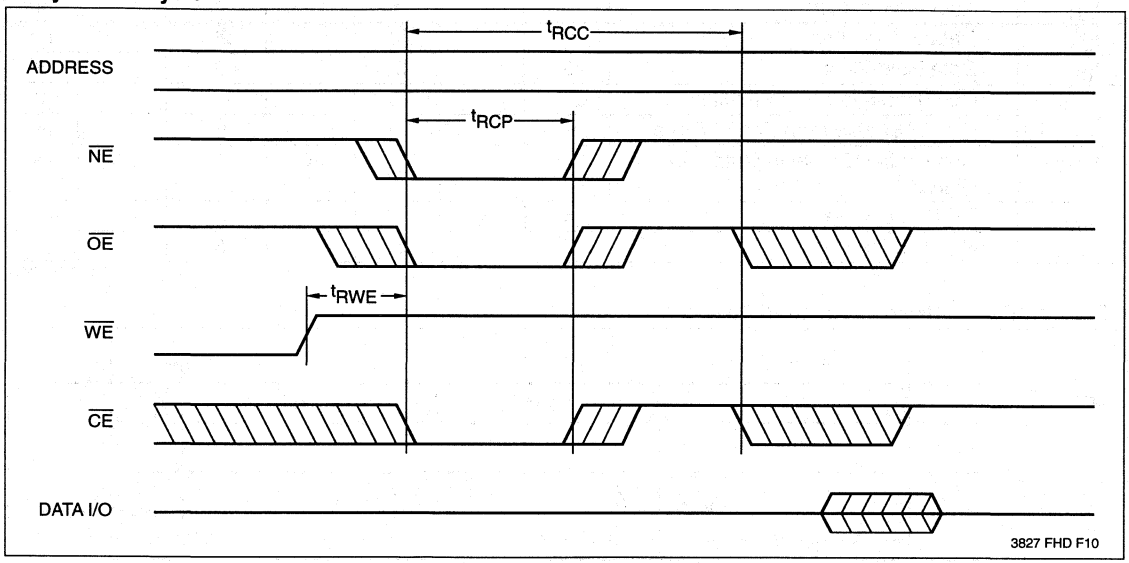


Array Recall Cycle Limits

Symbol	Parameter	X20C05-35		X20C05-45		X20C05-55		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{RCC}	Array Recall Cycle Time		5		5		5	µs
t_{RCP}(5)	Recall Pulse Width to Initiate Recall	30		40		50		ns
t_{RWE}	$\overline{WE}$ Setup Time to $\overline{NE}$	0		0		0		ns

3827 PGM T13.1

Array Recall Cycle



3827 FHD F10

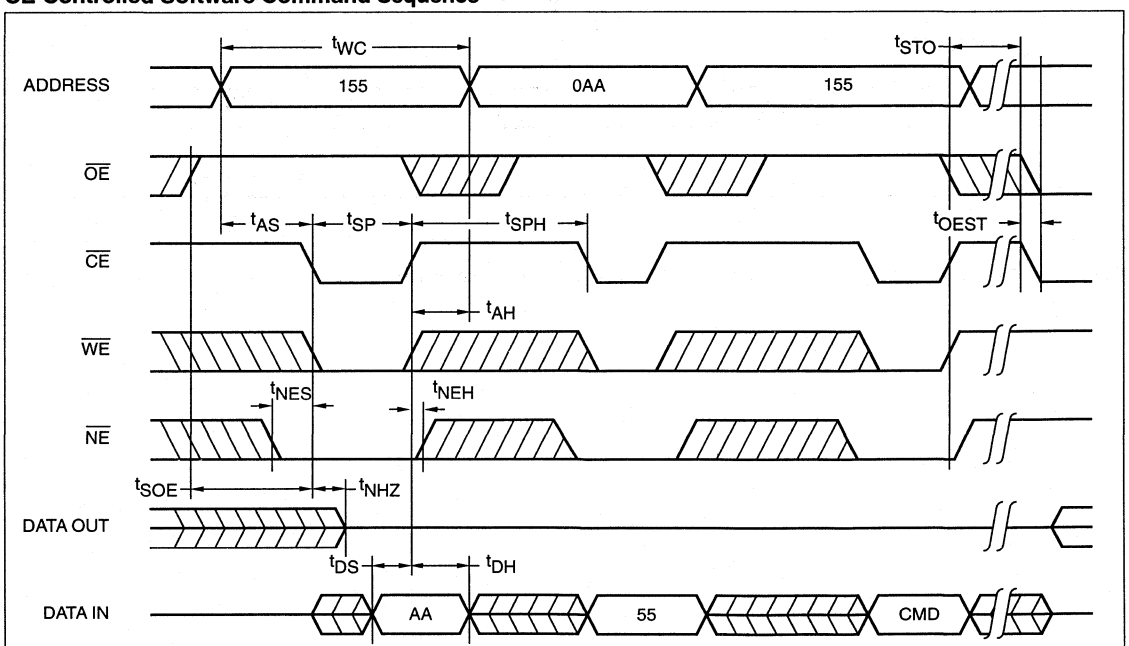
Note: (5) The Recall Pulse Width (t_{RCP}) is a minimum time that $\overline{NE}$, $\overline{OE}$ and $\overline{CE}$ must be LOW simultaneously.

Software Command Timing Limits

Symbol	Parameter	X20C05-35		X20C05-45		X20C05-55		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{STO}	Store Cycle Time		5		5		5	ms
t_{SP}(6)	Store Pulse Width	30		40		50		ns
t_{SPH}	Store Pulse Hold Time	35		45		55		ns
t_{WC}	Write Cycle Time	35		45		55		ns
t_{AS}	Address Setup Time	0		0		0		ns
t_{AH}	Address Hold time	0		0		0		ns
t_{DS}	Data Setup Time	15		20		25		ns
t_{DH}	Data Hold Time	0		3		3		ns
t_{SOE}(7)	$\overline{OE}$ Disable to Store Function	20		20		20		ns
t_{OEST}(7)	Output Enable from End of Store	10		10		10		ns
t_{NHZ}(7)	Nonvolatile Enable to Output in High Z		15		20		25	ns
t_{NES}	$\overline{NE}$ Setup Time	5		5		5		ns
t_{NEH}	$\overline{NE}$ Hold Time	5		5		5		ns

3827 PGM T12.1

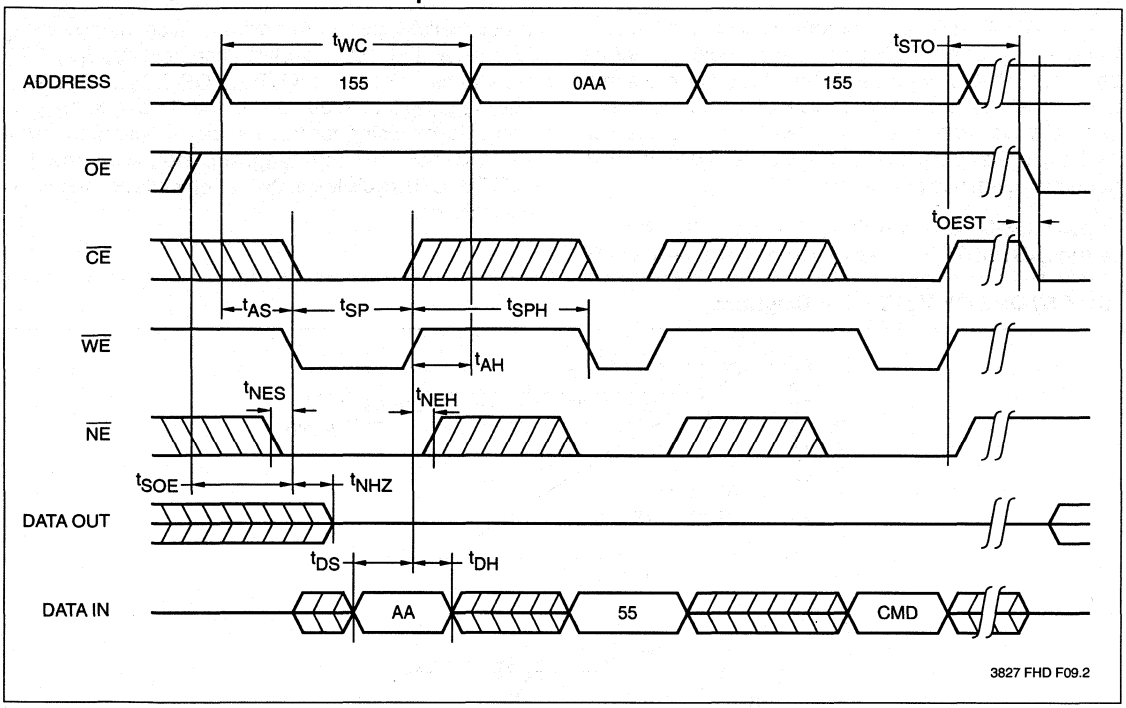
$\overline{CE}$ Controlled Software Command Sequence



3827 FHD F08.2

Notes: (6) The Store Pulse Width (t_{SP}) is a minimum time that $\overline{NE}$, $\overline{WE}$ and $\overline{CE}$ must be LOW simultaneously.
(7) t_{SOE}, t_{OEST} and t_{NHZ} are periodically sampled and not 100% tested.

$\overline{WE}$ Controlled Software Command Sequence

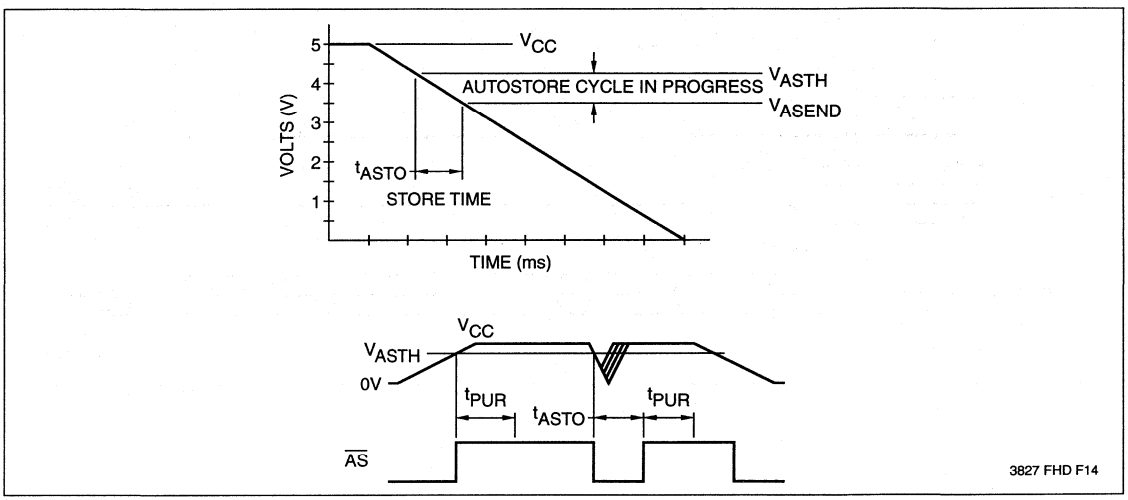


AUTOSTORE Feature

The AUTOSTORE feature automatically saves the contents of the X20C05's RAM to the on-board bit-for-bit shadow E²PROM at power-down. This circuitry insures that no data is lost during accidental power-downs or general system crashes, and is ideal for microprocessor caching systems, embedded software systems, and general system back-up memory.

The AUTOSTORE instruction (EAS) to the SDP register sets the AUTOSTORE enable latch, allowing the X20C05 to automatically perform a store operation whenever V_{CC} falls below the AUTOSTORE threshold (V_{ASTH}). V_{CC} must remain above the AUTOSTORE Cycle End Voltage (V_{ASEND}) for the duration of the store cycle (t_{ASTO}). The detailed timing for this feature is illustrated in the AUTOSTORE timing diagram, below. Once the AUTOSTORE cycle is initiated, all other device functions are inhibited.

AUTOSTORE CYCLE Timing Diagrams

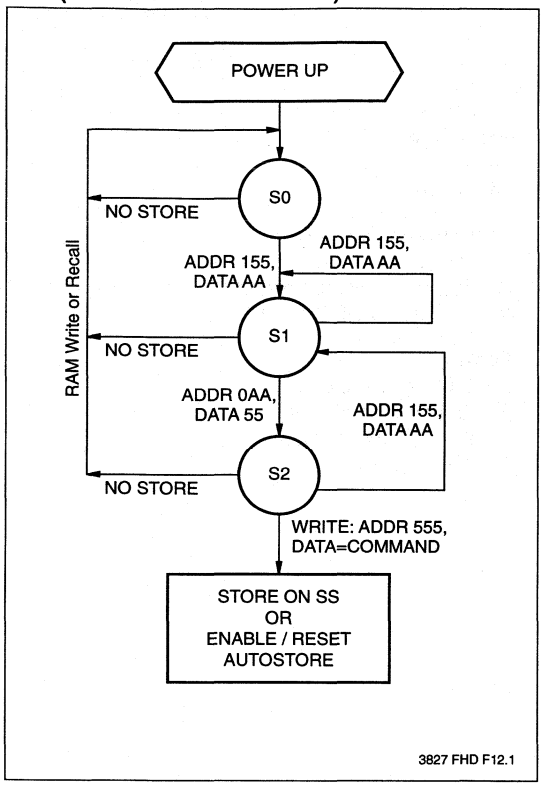


AUTOSTORE CYCLE LIMITS

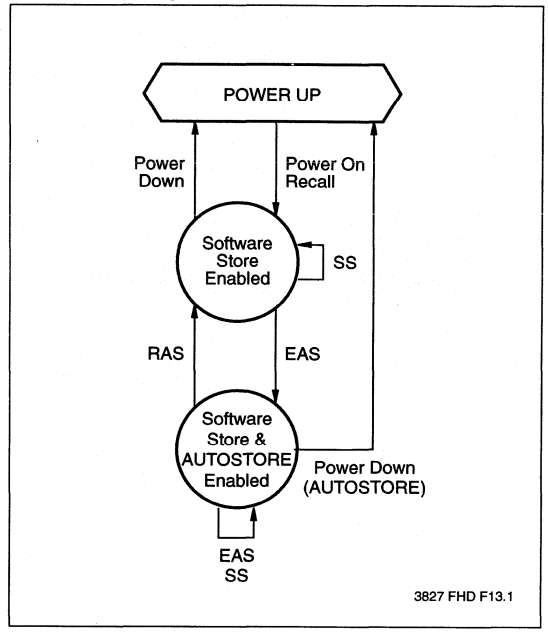
Symbol	Parameter	X20C05		Units
		Min.	Max.	
t_{ASTO}	AUTOSTORE Cycle Time		2.5	ms
V_{ASTH}	AUTOSTORE Threshold Voltage	4.0	4.3	V
V_{ASEND}	AUTOSTORE Cycle End Voltage	3.5		V

3827 PGM T15

SDP (Software Data Protection)



Store State Diagram

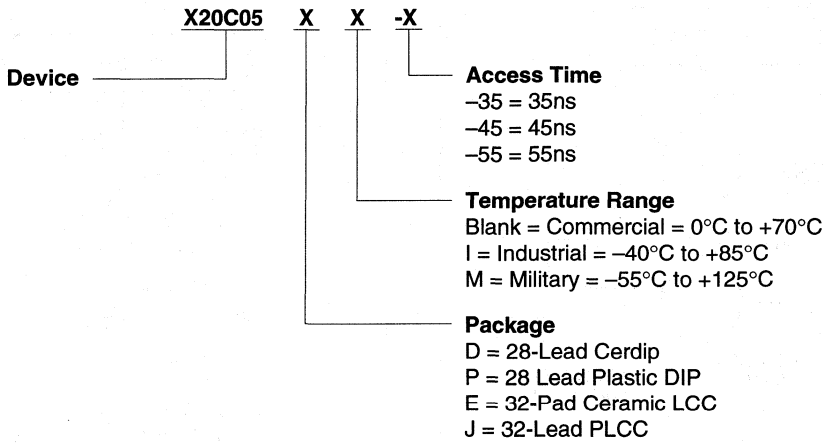


SOFTWARE DATA PROTECTION COMMANDS

Command		Data
EAS	Enable AUTOSTORE	CC[H]
RAS	Reset AUTOSTORE	CD[H]
SS	Software Store	33[H]

3827 PGM T14.1

ORDERING INFORMATION



16K X20C16 2K x 8 Bit

High Speed AUTOSTORE™ NOVRAM

FEATURES

- **Fast Access Time: 35ns, 45ns, 55ns**
- **High Reliability**
  - **—Endurance: 1,000,000 Nonvolatile Store Operations**
  - **—Retention: 100 Years Minimum**
- **AUTOSTORE™ NOVRAM**
  - **—Automatically Stores RAM Data Into the E^2PROM Array When V_{CC} Low Threshold is Detected**
  - **—User Enabled Option**
  - **—Open Drain AUTOSTORE Status Output Pin**
- **Power-on Recall**
  - **—E^2PROM Data Automatically Recalled Into RAM Upon Power-up**
- **Software Data Protection**
  - **—Locks Out Inadvertent Store Operations**
- **Low Power CMOS**
  - **—Standby: 250µA**
- **Infinite E^2PROM Array Recall, and RAM Read and Write Cycles**

DESCRIPTION

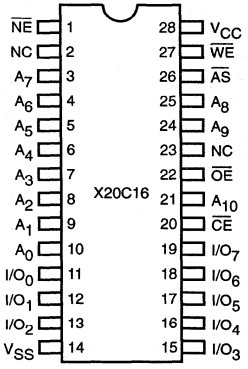
The Xicor X20C16 is a 2K x 8 NOVRAM featuring a high-speed static RAM overlaid bit-for-bit with a nonvolatile electrically erasable PROM (E^2PROM) and the AUTOSTORE feature which automatically saves the RAM contents to E^2PROM at power-down. The X20C16 is fabricated with advanced CMOS floating gate technology to achieve high speed with low power and wide power-supply margin. The X20C16 features a compatible JEDEC approved pinout for byte-wide memories, for industry standard RAMs, ROMs, EPROMs, and E^2PROMs.

The NOVRAM design allows data to be easily transferred from RAM to E^2PROM (store) and E^2PROM to RAM (recall). The store operation is completed in 5ms or less and the recall operation is completed in 10µs or less. An automatic array recall operation reloads the contents of the E^2PROM into RAM upon power-up.

Xicor NOVRAMS are designed for unlimited write operations to RAM, either from the host or recalls from E^2PROM, and a minimum 1,000,000 store operations to the E^2PROM. Data retention is specified to be greater than 100 years.

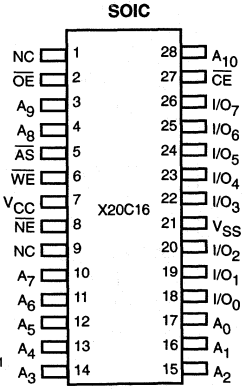
PIN CONFIGURATION

PLASTIC CERDIP



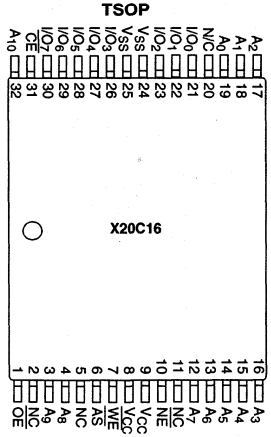
3826 FHD F02

SOIC



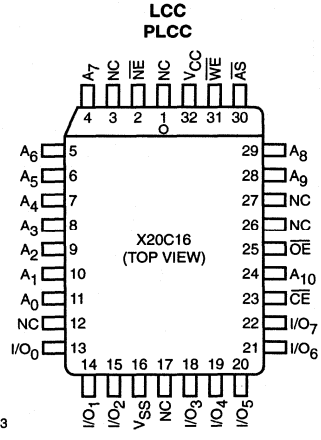
3826 FHD F15.1

TSOP



3826 ILL F17.2

LCC PLCC



3826 FHD F03

AUTOSTORE™ NOVRAM is a trademark of Xicor, Inc.

PIN DESCRIPTIONS

Addresses (A_0–A_{10})

The Address inputs select an 8-bit memory location during a read or write operation.

Chip Enable ($\overline{CE}$)

The Chip Enable input must be LOW to enable all read/write operations. When $\overline{CE}$ is HIGH, power consumption is reduced.

Output Enable ($\overline{OE}$)

The Output Enable input controls the data output buffers and is used to initiate read and recall operations. Output Enable LOW disables a store operation regardless of the state of $\overline{CE}$, $\overline{WE}$, or $\overline{NE}$.

Data In/Data Out (I/O_0–I/O_7)

Data is written to or read from the X20C16 through the I/O pins. The I/O pins are placed in the high impedance state when either $\overline{CE}$ or $\overline{OE}$ is HIGH or when $\overline{NE}$ is LOW.

Write Enable ($\overline{WE}$)

The Write Enable input controls the writing of data to the static RAM.

Nonvolatile Enable ($\overline{NE}$)

The Nonvolatile Enable input controls the recall function to the E²PROM array.

AUTOSTORE Output ($\overline{AS}$)

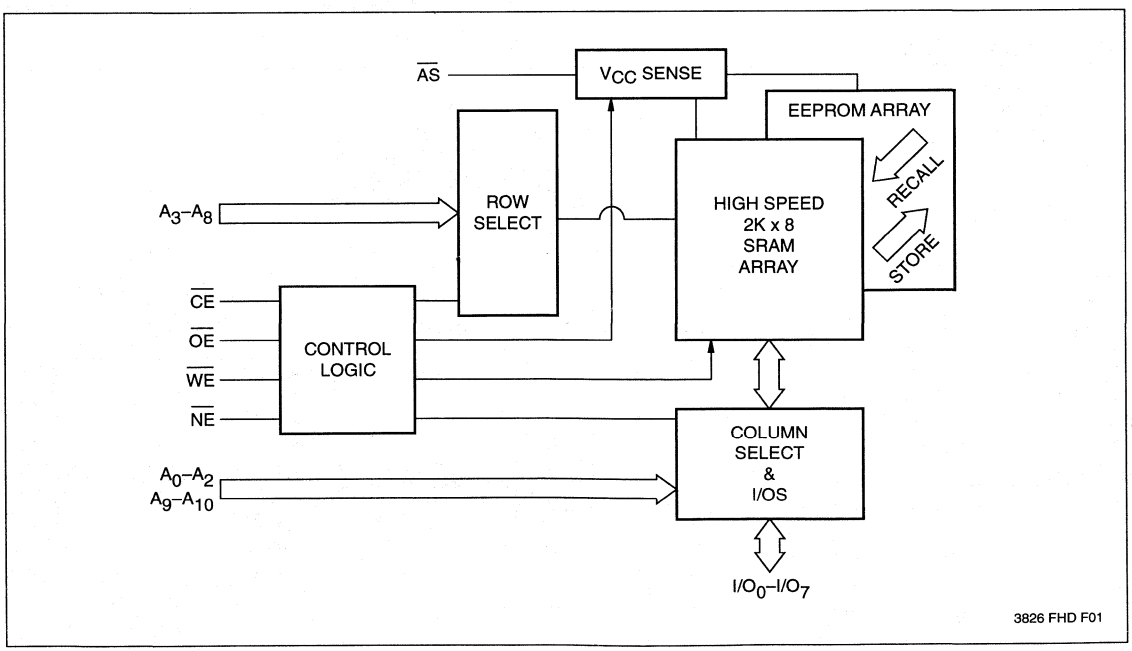
$\overline{AS}$ is an open drain output which, when asserted indicates V_{CC} has fallen below the AUTOSTORE threshold (V_{ASTH}). $\overline{AS}$ may be wire-ORed with multiple open drain outputs and used as an interrupt input to a microcontroller.

PIN NAMES

Symbol	Description
A_0–A_{10}	Address Inputs
I/O_0–I/O_7	Data Input/Output
$\overline{WE}$	Write Enable
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{NE}$	Nonvolatile Enable
$\overline{AS}$	AUTOSTORE Output
V_{CC}	+5V
V_{SS}	Ground
NC	No Connect

3826 PGM T01

FUNCTIONAL DIAGRAM



3826 FHD F01

DEVICE OPERATION

The $\overline{CE}$, $\overline{OE}$, $\overline{WE}$, and $\overline{NE}$ inputs control the X20C16 operation. The X20C16 byte-wide NOVRAM uses a 2-line control architecture to eliminate bus contention in a system environment. The I/O bus will be in a high impedance state when either $\overline{OE}$ or $\overline{CE}$ is HIGH, or when $\overline{NE}$ is LOW.

RAM Operations

RAM read and write operations are performed as they would be with any static RAM. A read operation requires $\overline{CE}$ and $\overline{OE}$ to be LOW with $\overline{WE}$ and $\overline{NE}$ HIGH. A write operation requires $\overline{CE}$ and $\overline{WE}$ to be LOW with $\overline{NE}$ HIGH. There is no limit to the number of read or write operations performed to the RAM portion of the X20C16.

Memory Transfer Operations

There are two memory transfer operations: a recall operation whereby the data stored in the E²PROM array is transferred to the RAM array; and a store operation which causes the entire contents of the RAM array to be stored in the E²PROM array.

Recall operations are performed automatically upon power-up and under host system control when $\overline{NE}$, $\overline{OE}$ and $\overline{CE}$ are LOW and $\overline{WE}$ is HIGH. The recall operation takes a maximum of 5µs.

SDP (Software Data Protection)

There are two methods of initiating a store operation. The first is the software store command. This command takes the place of the hardware store employed on the X20C04. This command is issued by entering into the special command mode: $\overline{NE}$, $\overline{CE}$, and $\overline{WE}$ strobe LOW while at the same time a specific address and data combination is sent to the device. This is a three step operation: the first address/data combination is 555[H]/AA[H]; the second combination is 2AA[H]/55[H]; and the final command combination is 555[H]/33[H]. This sequence of pseudo write operations will immediately initiate a store operation. Refer to the software command timing diagrams for details on set and hold times for the various signals.

The second method of storing data is with the AUTOSTORE command. When enabled, data is automatically stored from the RAM into the E²PROM array whenever V_{CC} falls below the preset Autostore threshold. This feature is enabled by performing the first two steps for the software store with the command combination being 555[H]/CC[H].

The AUTOSTORE feature is disabled by issuing the three step command sequence with the command combination being 555[H]/CD[H]. The AUTOSTORE feature will also be reset if V_{CC} falls below the power-up reset threshold (approximately 3.5V) and is then raised back into the operation range.

Write Protection

The X20C16 supports two methods of protecting the nonvolatile data.

—If after power-up the AUTOSTORE feature is not enabled, no AUTOSTORE can occur.

—V_{CC} Sense – All functions are inhibited when V_{CC} is ≤ 3.0V typical.

SYMBOL TABLE

The following symbol table provides a key to understanding the conventions used in the device timing diagrams. The diagrams should be used in conjunction with the device timing specifications to determine actual device operation and performance, as well as device suitability for user's application.

WAVEFORM	INPUTS	OUTPUTS
———	Must be steady	Will be steady
⟋⟋⟋	May change from LOW to HIGH	Will change from LOW to HIGH
⟍⟍⟍	May change from HIGH to LOW	Will change from HIGH to LOW
⟋⟍⟋⟍	Don't Care: Changes Allowed	Changing: State Not Known
⟋⟍⟋⟍	N/A	Center Line is High Impedance

ABSOLUTE MAXIMUM RATINGS*

Temperature under Bias ..... –65°C to +135°C
Storage Temperature ..... –65°C to +150°C
Voltage on any Pin with
Respect to V_{SS} ..... –1V to +7V
D.C. Output Current 10mA
Lead Temperature (Soldering, 10 seconds) ..... 300°C

***COMMENT**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any conditions other than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	+70°C
Industrial	–40°C	+85°C
Military	–55°C	+125°C

3826 PGM T02.1

Supply Voltage	Limits
X20C16	5V ±10%

3826 PGM T03.1

D.C. OPERATING CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits			Test Conditions
		Min.	Max.	Units	
I_{CC1}	V_{CC} Current (Active)		100	mA	$\overline{NE} = \overline{WE} = V_{IH}$, $\overline{CE} = \overline{OE} = V_{IL}$ Address Inputs = 0.4V/2.4V Levels @ f = 20MHz All I/Os = Open
I_{CC2}	V_{CC} Current During Store		5	mA	All Inputs = V_{IH}
I_{CC3}(2)	V_{CC} Current During AUTOSTORE		2.5	mA	All I/Os = Open
I_{SB1}	V_{CC} Standby Current (TTL Input)		10	mA	$\overline{CE} = V_{IH}$, All Other Inputs = V_{IH} All I/Os = Open
I_{SB2}	V_{CC} Standby Current (CMOS Input)		250	µA	All Inputs = V_{CC} – 0.3V All I/Os = Open
I_{LI}	Input Leakage Current		10	µA	$V_{IN} = V_{SS}$ to V_{CC}
I_{LO}	Output Leakage Current		10	µA	$V_{OUT} = V_{SS}$ to V_{CC}, $\overline{CE} = V_{IH}$
V_{IL}(1)	Input LOW Voltage	–1	0.8	V	
V_{IH}(1)	Input HIGH Voltage	2	V_{CC} + 0.5	V	
V_{OL}	Output LOW Voltage		0.4	V	I_{OL} = 4mA
V_{OLAS}	AUTOSTORE Output		0.4	V	I_{OLAS} = 1mA
V_{OH}	Output HIGH Voltage	2.4		V	I_{OH} = –4mA

3826 PGM T04.3

POWER-UP TIMING

Symbol	Parameter	Max.	Units
t_{PUR}(2)	Power-Up to RAM Operation	100	µs
t_{PUW}(2)	Power-Up to Nonvolatile Operation	5	ms

3826 PGM T05

CAPACITANCE T_A = +25°C, f = 1MHz, V_{CC} = 5V.

Symbol	Test	Max.	Units	Conditions
$C_{I/O}$(2)	Input/Output Capacitance	10	pF	$V_{I/O}$ = 0V
C_{IN}(2)	Input Capacitance	6	pF	V_{IN} = 0V

3826 PGM T06.1

Notes: (1) V_{IL} min. and V_{IH} max. are for reference only and are not tested.
(2) This parameter is periodically sampled and not 100% tested.

ENDURANCE AND DATA RETENTION

Parameter	Min.	Units
Endurance	100,000	Data Changes Per Bit
Store Cycles	1,000,000	Store Cycles
Data Retention	100	Years

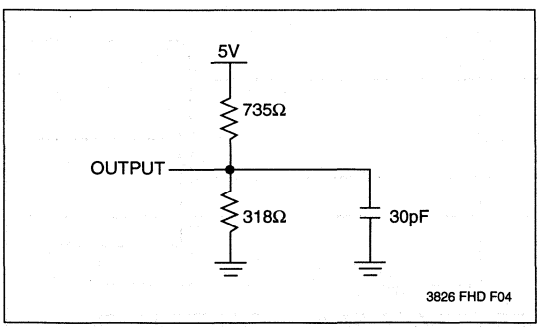
3826 PGM T07.1

MODE SELECTION

$\overline{CE}$	$\overline{WE}$	$\overline{NE}$	$\overline{OE}$	Mode	I/O	Power
H	X	X	X	Not Selected	Output High Z	Standby
L	H	H	L	Read RAM	Output Data	Active
L	L	H	X	Write "1" RAM	Input Data High	Active
L	L	H	X	Write "0" RAM	Input Data Low	Active
L	H	L	L	Array Recall	Output High Z	Active
L	L	L	H	Software Command	Input Data	Active
L	H	H	H	Output Disabled	Output High Z	Active
L	L	L	L	Not Allowed	Output High Z	Active
L	H	L	H	No Operation	Output High Z	Active

3826 PGM T09

EQUIVALENT A.C. LOAD CIRCUIT



3826 FHD F04

A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3V
Input Rise and Fall Times	5ns
Input and Output Timing Levels	1.5V

3826 PGM T08.1

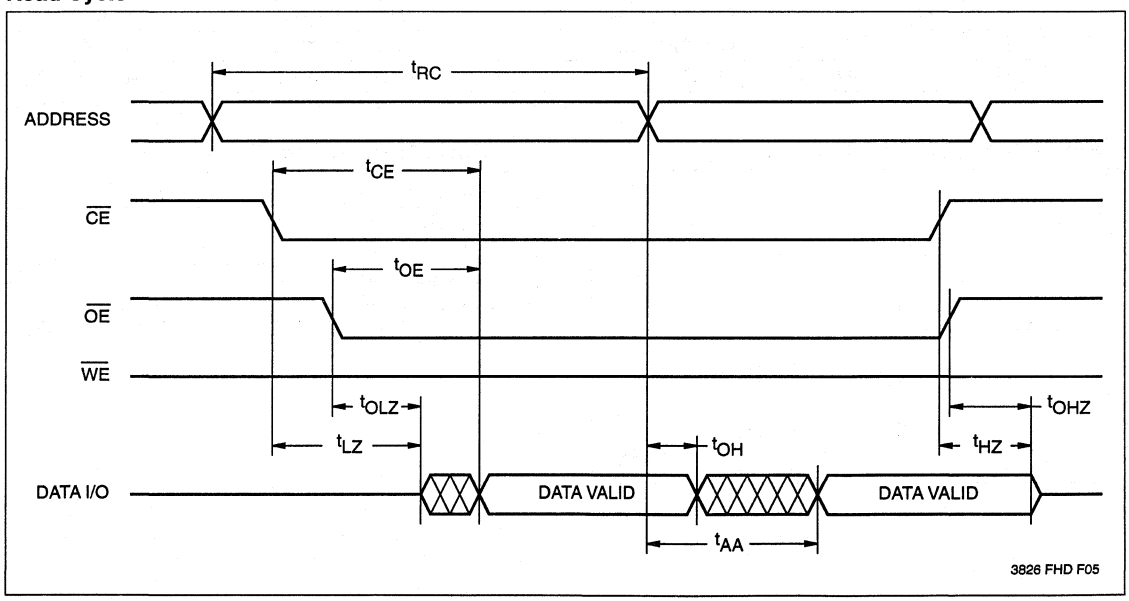
A.C. CHARACTERISTICS (Over the recommended operating conditions unless otherwise specified)

Read Cycle Limits

Symbol	Parameter	X20C16-35		X20C16-45		X20C16-55		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	35		45		55		ns
t_{CE}	Chip Enable Access Time		35		45		55	ns
t_{AA}	Address Access Time		35		45		55	ns
t_{OE}	Output Enable Access Time		20		25		30	ns
t_{LZ}(3)	Chip Enable to Output in Low Z	0		0		0		ns
t_{OLZ}(3)	Output Enable to Output in Low Z	0		0		0		ns
t_{HZ}(3)	Chip Disable to Output in High Z	0	15	0	20	0	25	ns
t_{OHZ}(3)	Output Disable to Output in High Z	0	15	0	20	0	25	ns
t_{OH}	Output Hold From Address Change	0		0		0		ns

3826 PGM T10

Read Cycle



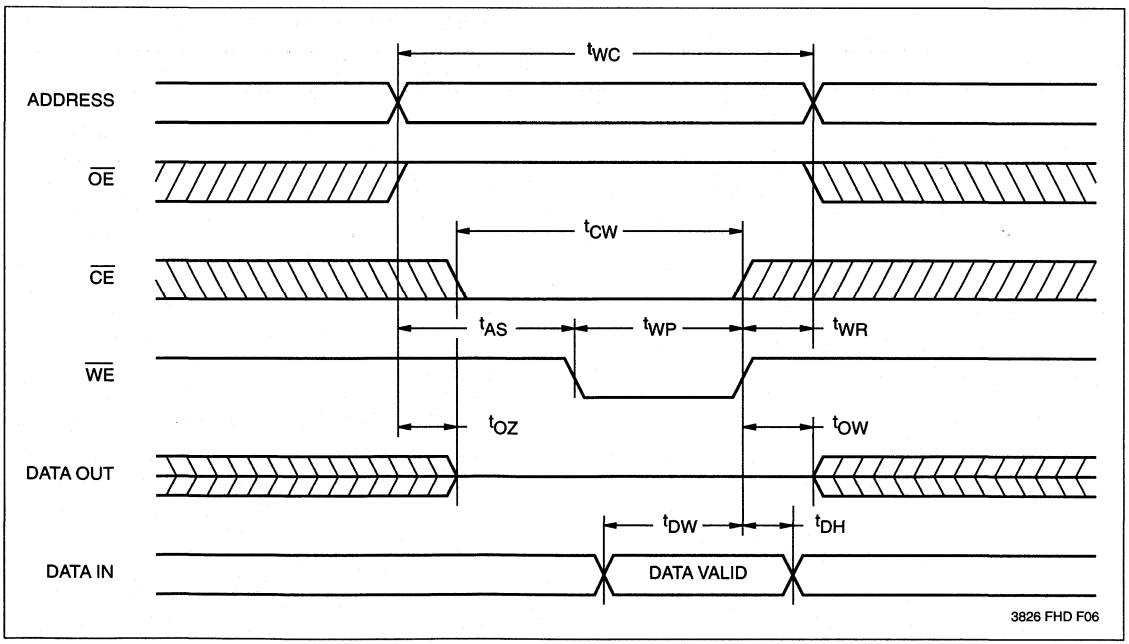
Note: (3) t_{LZ} min., t_{HZ}, t_{OLZ} min., and t_{OHZ} are periodically sampled and not 100% tested. t_{HZ} max. and t_{OHZ} max. are measured, with C_L = 5pF, from the point when $\overline{CE}$ or $\overline{OE}$ return HIGH (whichever occurs first) to the time when the outptus are no longer driven.

Write Cycle Limits

Symbol	Parameter	X20C16-35		X20C16-45		X20C16-55		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{WC}	Write Cycle Time	35		45		55		ns
t_{CW}	Chip Enable to End of Write Input	30		35		40		ns
t_{AS}	Address Setup Time	0		0		0		ns
t_{WP}	Write Pulse Width	30		35		40		ns
t_{WR}	Write Recovery Time	0		0		0		ns
t_{DW}	Data Setup to End of Write	15		20		25		ns
t_{DH}	Data Hold Time	3		3		3		ns
t_{WZ}(4)	Write Enable to Output in High Z		15		20		25	ns
t_{OW}(4)	Output Active from End of Write	5		5		5		ns
t_{OZ}(4)	Output Enable to Output in High Z		15		20		25	ns

3826 PGM T11

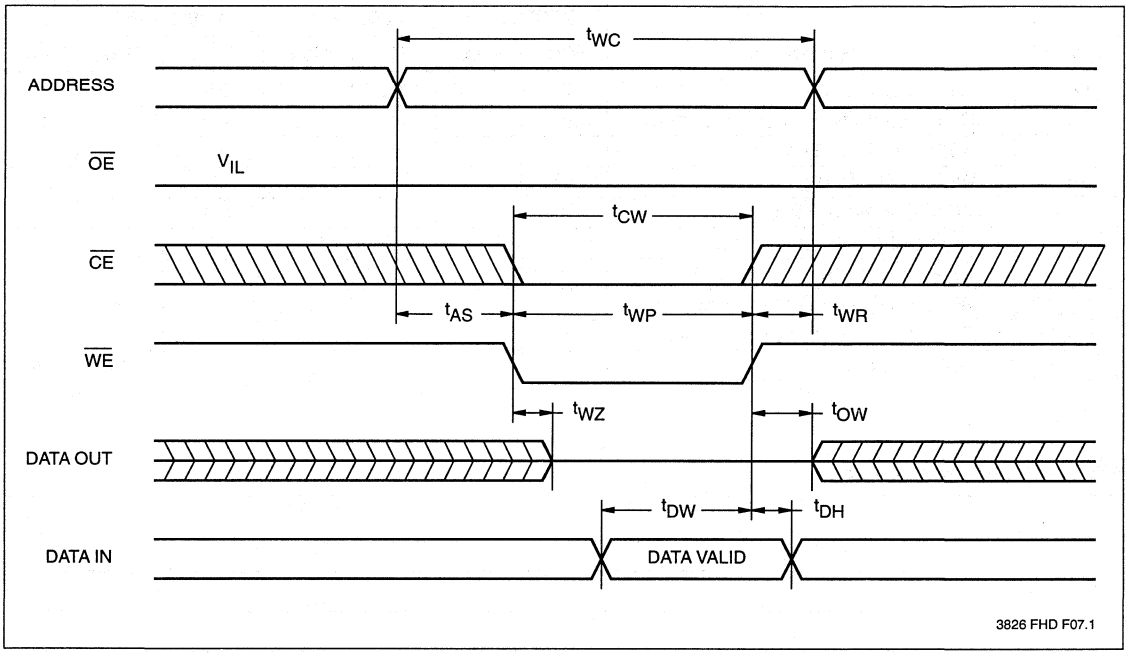
$\overline{WE}$ Controlled Write Cycle



3826 FHD F06

Note: (4) t_{WZ}, t_{OW}, t_{OZ} are periodically sampled and not 100% tested.

$\overline{CE}$ Controlled Write Cycle

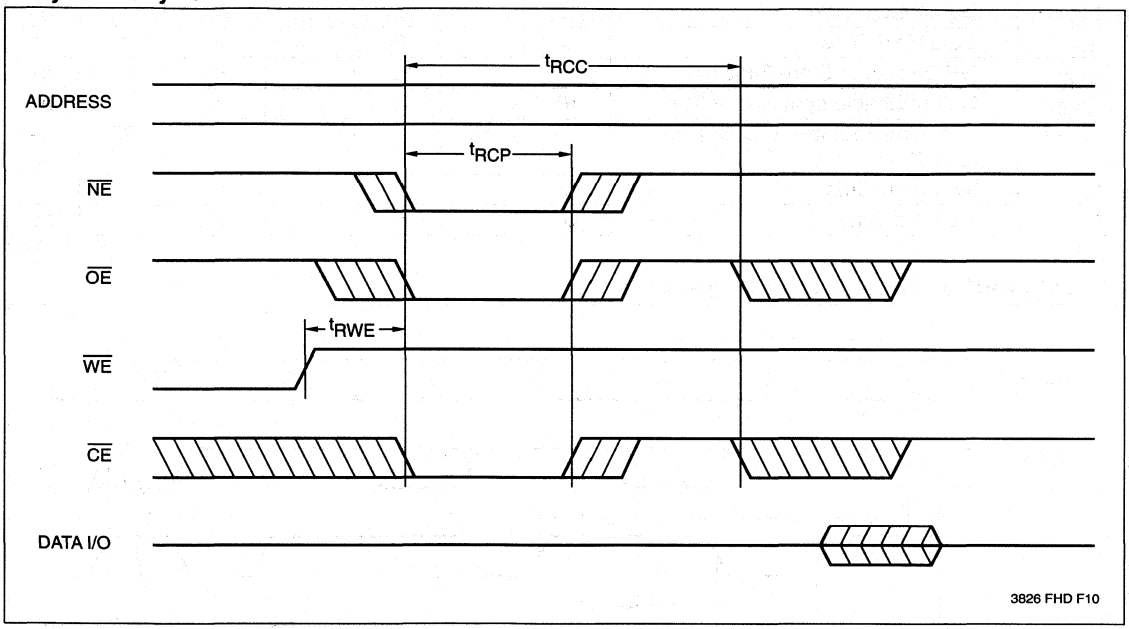


ARRAY RECALL CYCLE LIMITS

Symbol	Parameter	X20C16-35		X20C16-45		X20C16-55		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{RCC}	Array Recall Cycle Time		10		10		10	µs
t_{RCP}(5)	Recall Pulse Width to InitiateRecall	30		40		50		ns
t_{RWE}	$\overline{WE}$ Setup Time to $\overline{NE}$	0		0		0		ns

3826 PGM T13

Array Recall Cycle



3826 FHD F10

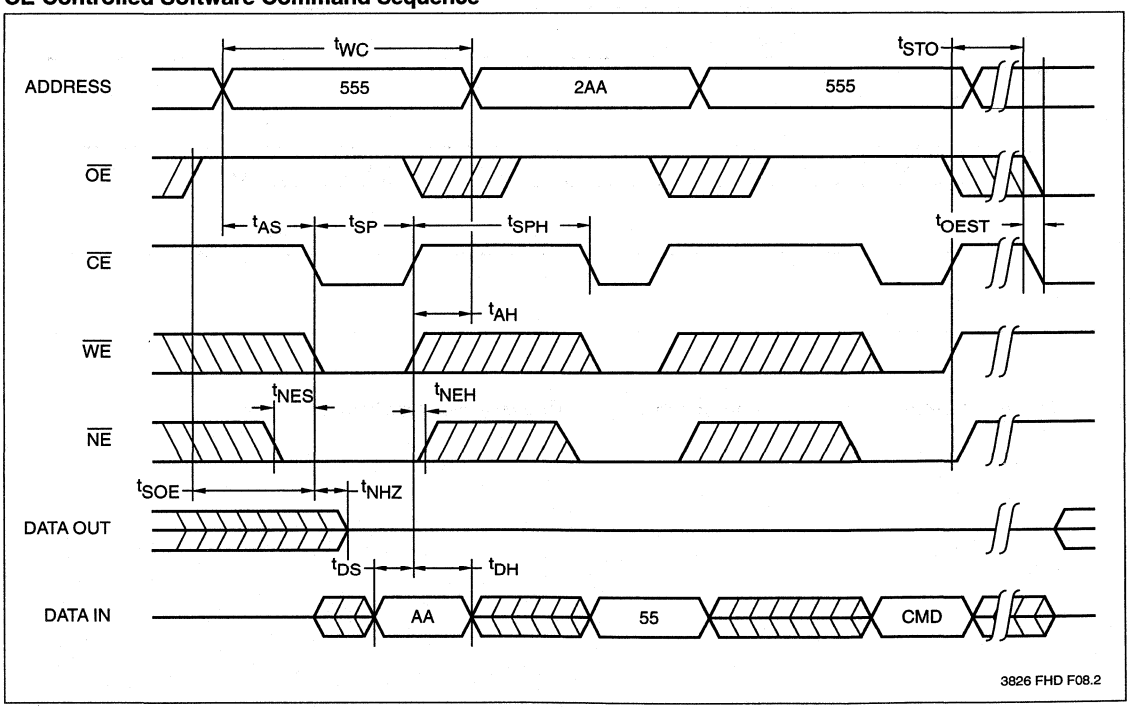
Note: (5) The Recall Pulse Width (t_{RCP}) is a minimum time that $\overline{NE}$, $\overline{OE}$ and $\overline{CE}$ must be LOW simultaneously.

Software Command Timing Limits

Symbol	Parameter	X20C16-35		X20C16-45		X20C16-55		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{STO}	Store Cycle Time		5		5		5	ms
t_{SP}(6)	Store Pulse Width	30		40		50		ns
t_{SPH}	Store Pulse Hold Time	35		45		55		ns
t_{WC}	Write Cycle Time	35		45		55		ns
t_{AS}	Address Setup Time	0		0		0		ns
t_{AH}	Address Hold time	0		0		0		ns
t_{DS}	Data Setup Time	15		20		25		ns
t_{DH}	Data Hold Time	3		3		3		ns
t_{SOE}(7)	$\overline{OE}$ Disable to Store Function	20		20		20		ns
t_{OEST}(7)	Output Enable from End of Store	10		10		10		ns
t_{NHZ}(7)	Nonvolatile Enable to Output in High Z		15		20		25	ns
t_{NES}	$\overline{NE}$ Setup Time	5		5		5		ns
t_{NEH}	$\overline{NE}$ Hold Time	5		5		5		ns

3826 PGM T12.2

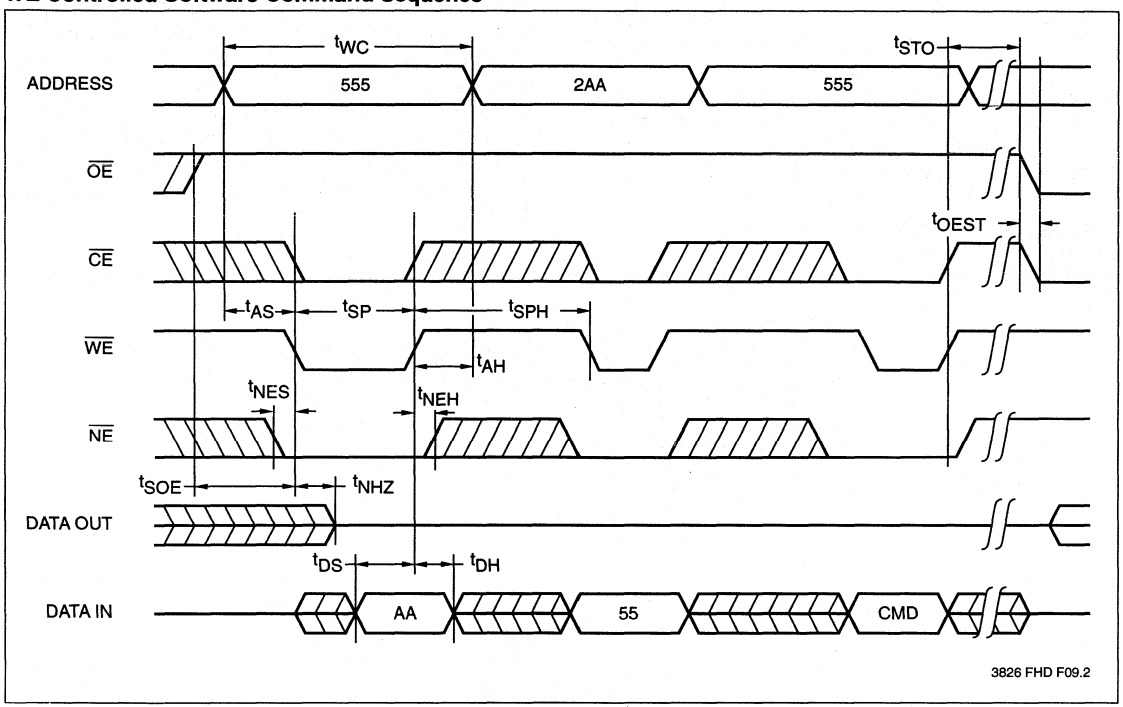
$\overline{CE}$ Controlled Software Command Sequence



3826 FHD F08.2

Note: (6) The Store Pulse Width (t_{SP}) is a minimum time that $\overline{NE}$, $\overline{WE}$ and $\overline{CE}$ must be LOW simultaneously.
(7) t_{SOE}, t_{OEST} and t_{NHZ} are periodically sampled and not 100% tested.

$\overline{WE}$ Controlled Software Command Sequence

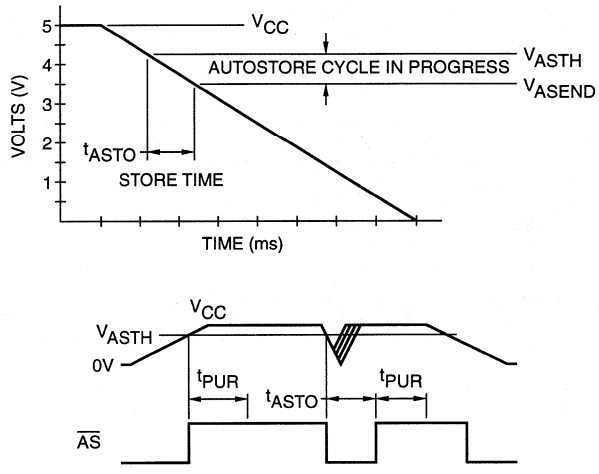


AUTOSTORE Feature

The AUTOSTORE feature automatically saves the contents of the X20C16's static RAM to the on-board bit-for-bit shadow E²PROM at power-down. This circuitry insures that no data is lost during accidental power-downs or general system crashes, and is ideal for microprocessor caching systems, embedded software systems, and general system back-up memory.

The AUTOSTORE instruction (EAS) to the SDP register sets the AUTOSTORE enable latch, allowing the X20C16 to automatically perform a store operation whenever V_{CC} falls below the AUTOSTORE threshold (V_{ASTH}). V_{CC} must remain above the AUTOSTORE Cycle End Voltage (V_{ASEND}) for the duration of the store cycle (t_{ASTO}). The detailed timing for this feature is illustrated in the AUTOSTORE timing diagram, below. Once the AUTOSTORE cycle is initiated, all other device functions are inhibited.

AUTOSTORE CYCLE Timing Diagrams



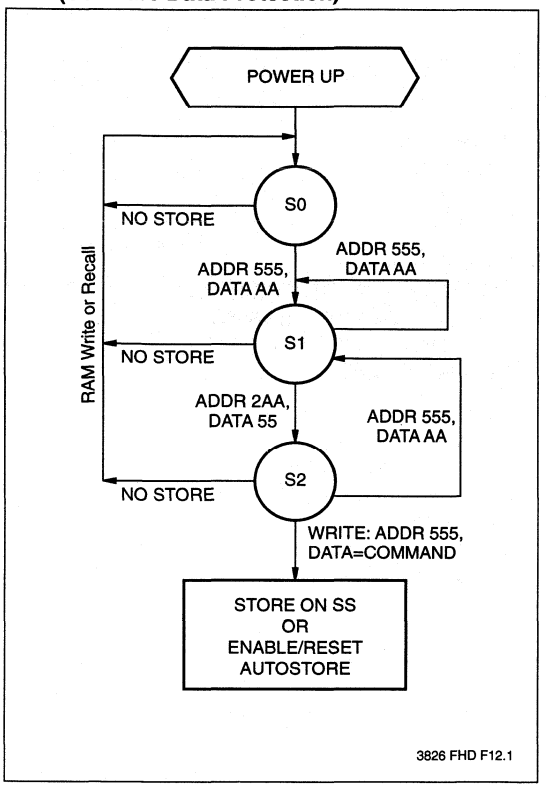
3826 FHD F14

AUTOSTORE CYCLE LIMITS

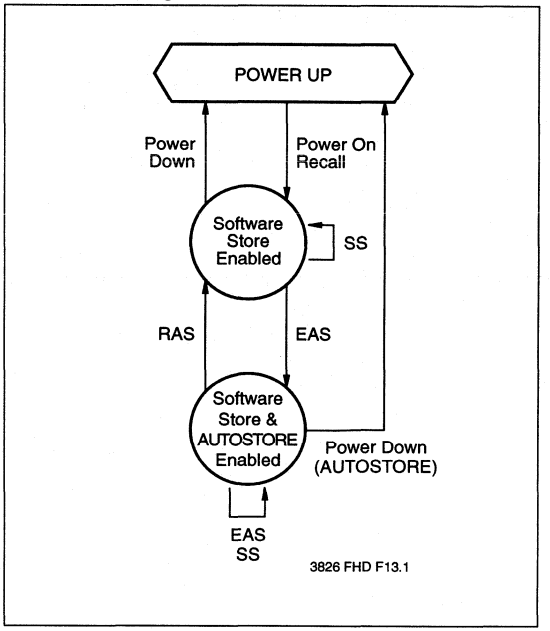
Symbol	Parameter	X20C16		Units
		Min.	Max.	
t_{ASTO}	AUTOSTORE Cycle Time		2.5	ms
V_{ASTH}	AUTOSTORE Threshold Voltage	4.0	4.3	V
V_{ASEND}	AUTOSTORE Cycle End Voltage	3.5		V

3826 PGM T15

SDP (Software Data Protection)



Store State Diagram

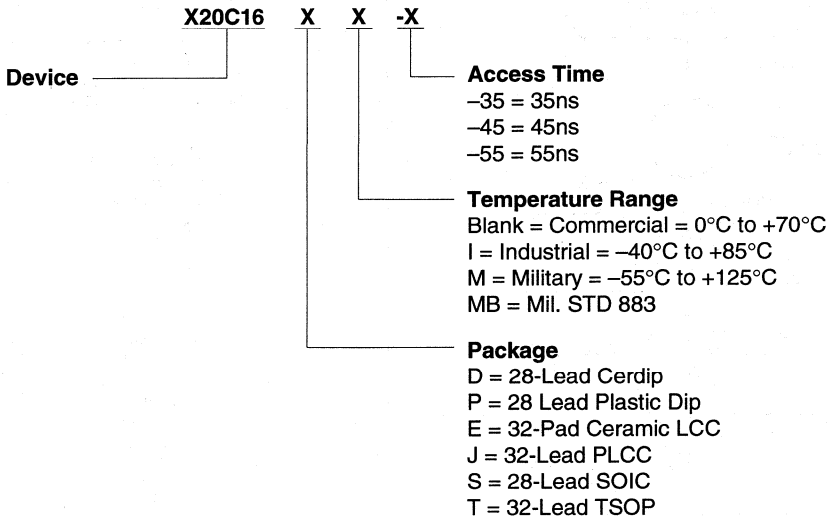


SOFTWARE DATA PROTECTION COMMANDS

Command		Data
EAS	Enable AUTOSTORE	CC[H]
RAS	Reset AUTOSTORE	CD[H]
SS	Software Store	33[H]

3826 PGM T14.1

ORDERING INFORMATION



APPLICATION NOTE
AVAILABLE
AN56

16K X20C17 2K x 8 Bit

High Speed AUTOSTORE™ NOVRAM

1

FEATURES

- 24-Pin Standard SRAM DIP Pinout
- Fast Access Time: 35ns, 45ns, 55ns
- High Reliability
  - —Endurance: 1,000,000 Nonvolatile Store Operations
  - —Retention: 100 Years Minimum
- AUTOSTORE™ NOVRAM
  - —Automatically Stores SRAM Data Into the E^2PROM Array When V_{CC} Low Threshold is Detected
  - —E^2PROM Data Automatically Recalled Into RAM Upon Power-up
- Low Power CMOS
  - —Standby: 250µA
- Infinite E^2PROM Array Recall, and RAM Read and Write Cycles

DESCRIPTION

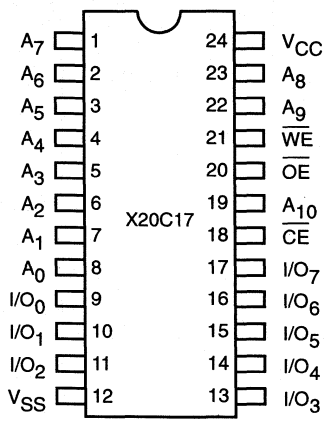
The Xicor X20C17 is a 2K x 8 NOVRAM featuring a high-speed static RAM overlaid bit-for-bit with a nonvolatile electrically erasable PROM (E^2PROM) and the AUTOSTORE feature which automatically saves the RAM contents to E^2PROM at power-down. The X20C17 is fabricated with advanced CMOS floating gate technology to achieve high speed with low power and wide power-supply margin. The X20C17 features a compatible JEDEC approved byte-wide memory pinout for industry standard SRAMs.

The NOVRAM design allows data to be easily transferred from RAM to E^2PROM (store) and E^2PROM to RAM (recall). The store operation is completed in 2.5ms or less. An automatic array recall operation reloads the contents of the E^2PROM into RAM upon power-up.

Xicor NOVRAMS are designed for unlimited write operations to RAM, either from the host or recalls from E^2PROM, and a minimum 1,000,000 store operations to the E^2PROM. Data retention is specified to be greater than 100 years.

PIN CONFIGURATION

PLASTIC
CERDIP



2015 ILL F02

AUTOSTORE™ NOVRAM is a trademark of Xicor, Inc.

PIN DESCRIPTIONS

Addresses (A_0–A_{10})

The Address inputs select an 8-bit memory location during a read or write operation.

Chip Enable ($\overline{CE}$)

The Chip Enable input must be LOW to enable all read/write operations. When $\overline{CE}$ is HIGH, power consumption is reduced.

Output Enable ($\overline{OE}$)

The Output Enable input controls the data output buffers and is used to initiate read and recall operations. Output Enable LOW disables a store operation regardless of the state of $\overline{CE}$, $\overline{WE}$.

Data In/Data Out (I/O_0–I/O_7)

Data is written to or read from the X20C17 through the I/O pins. The I/O pins are placed in the high impedance state when either $\overline{CE}$ or $\overline{OE}$ is HIGH.

Write Enable ($\overline{WE}$)

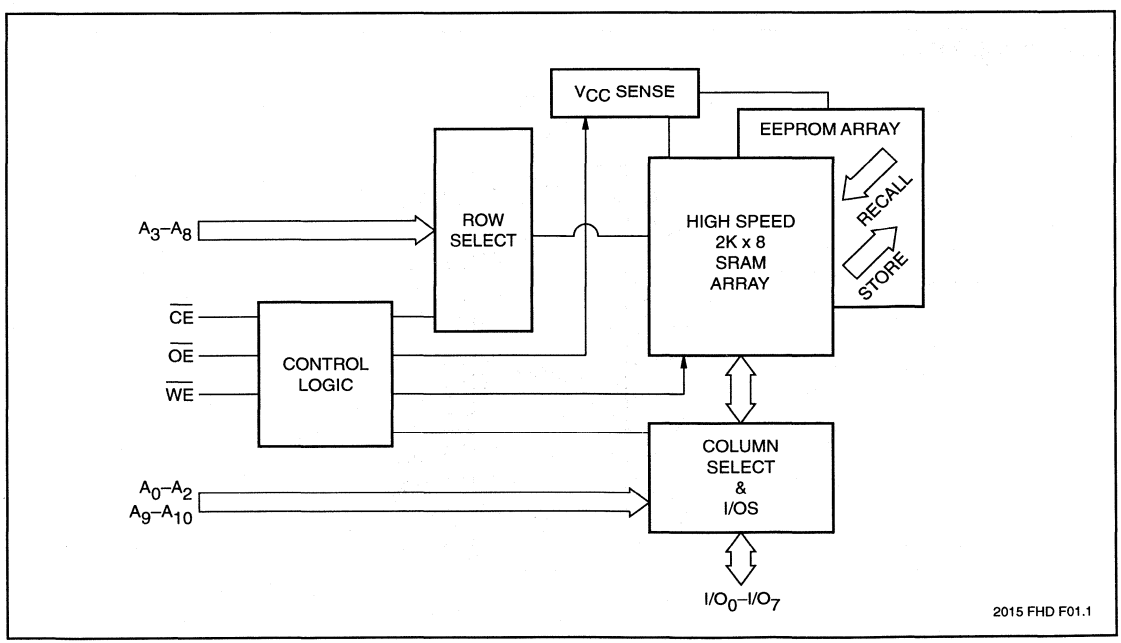
The Write Enable input controls the writing of data to the static RAM.

PIN NAMES

Symbol	Description
A_0–A_{10}	Address Inputs
I/O_0–I/O_7	Data Input/Output
$\overline{WE}$	Write Enable
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
V_{CC}	+5V
V_{SS}	Ground

2015 PGM T01

FUNCTIONAL DIAGRAM



2015 FHD F01.1

DEVICE OPERATION

The $\overline{CE}$, $\overline{OE}$, and $\overline{WE}$ inputs control the X20C17 operation. The X20C17 byte-wide NOVRAM uses a 2-line control architecture to eliminate bus contention in a system environment. The I/O bus will be in a high impedance state when either $\overline{OE}$ or $\overline{CE}$ is HIGH.

RAM Operations

RAM read and write operations are performed as they would be with any static RAM. A read operation requires $\overline{CE}$ and $\overline{OE}$ to be LOW. A write operation requires $\overline{CE}$ and $\overline{WE}$ to be LOW. There is no limit to the number of read or write operations performed to the RAM portion of the X20C17.

Memory Transfer Operations

There are two memory transfer operations: a recall operation whereby the data stored in the E^2PROM array is transferred to the RAM array; and a store operation which causes the entire contents of the RAM array to be stored in the E^2PROM array.

Recall operations are performed automatically upon power-up.

Store operations are performed automatically upon power-down. The store operation take a maximum of 2.5ms.

Write Protection

The X20C17 supports two methods of protecting the nonvolatile data.

—If after power-up no RAM write operations have occured, no AUTOSTORE operation can be initiated.

—V_{CC} Sense – All functions are inhibited when V_{CC} is ≤ 3V typical.

SYMBOL TABLE

The following symbol table provides a key to understanding the conventions used in the device timing diagrams. The diagrams should be used in conjunction with the device timing specifications to determine actual device operation and performance, as well as device suitability for user's application.

WAVEFORM	INPUTS	OUTPUTS
———	Must be steady	Will be steady
———		
///	May change from LOW to HIGH	Will change from LOW to HIGH
\\\	May change from HIGH to LOW	Will change from HIGH to LOW
XXX	Don't Care: Changes Allowed	Changing: State Not Known
><<	N/A	Center Line is High Impedance

ABSOLUTE MAXIMUM RATINGS*

Temperature under Bias ..... −65°C to +135°C
Storage Temperature ..... −65°C to +150°C
Voltage on any Pin with
Respect to V_{SS} ..... −1V to +7V
D.C. Output Current 10mA
Lead Temperature (Soldering, 10 seconds) ..... 300°C

***COMMENT**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any conditions other than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	+70°C
Industrial	−40°C	+85°C
Military	−55°C	+125°C

2015 PGM T02.1

Supply Voltage	Limits
X20C17	4.5V to 5.25V

2015 PGM T03.1

D.C. OPERATING CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits			Test Conditions
		Min.	Max.	Units	
I_{CC1}	V_{CC} Current (Active)		100	mA	$\overline{WE} = V_{IH}$, $\overline{CE} = \overline{OE} = V_{IL}$ Address Inputs = 0.4V/2.4V Levels @ f = 20MHz, All I/Os = Open
I_{CC2}(2)	V_{CC} Current During AUTOSTORE		2.5	mA	All I/Os = Open
I_{SB1}	V_{CC} Standby Current (TTL Input)		10	mA	All Inputs = V_{IH}, All I/Os = Open
I_{SB2}	V_{CC} Standby Current (CMOS Input)		250	µA	All Inputs = V_{CC} − 0.3V All I/Os = Open
I_{LI}	Input Leakage Current		10	µA	$V_{IN} = V_{SS}$ to V_{CC}
I_{LO}	Output Leakage Current		10	µA	$V_{OUT} = V_{SS}$ to V_{CC}, $\overline{CE} = V_{IH}$
V_{IL}(1)	Input LOW Voltage	−1	0.8	V	
V_{IH}(1)	Input HIGH Voltage	2	V_{CC} + 1	V	
V_{OL}	Output LOW Voltage		0.4	V	I_{OL} = 4mA
V_{OH}	Output HIGH Voltage	2.4		V	I_{OH} = −4mA

2015 PGM T04.3

POWER-UP TIMING

Symbol	Parameter	Max.	Units
t_{PUR}(2)	Power-Up to RAM Operation	100	µs
t_{PUW}(2)	Power-Up to Nonvolatile Operation	5	ms

2015 PGM T05

CAPACITANCE T_A = +25°C, f = 1MHz, V_{CC} = 5V.

Symbol	Test	Max.	Units	Conditions
$C_{I/O}$(2)	Input/Output Capacitance	10	pF	$V_{I/O}$ = 0V
C_{IN}(2)	Input Capacitance	6	pF	V_{IN} = 0V

2015 PGM T06.2

Notes: (1) V_{IL} min. and V_{IH} max. are for reference only and are not tested.
(2) This parameter is periodically sampled and not 100% tested.

ENDURANCE AND DATA RETENTION

Parameter	Min.	Units
Endurance	100,000	Data Changes Per Bit
Store Cycles	1,000,000	Store Cycles
Data Retention	100	Years

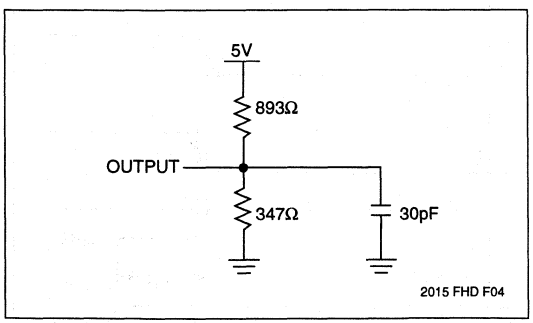
2015 PGM T07.1

MODE SELECTION

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O	Power
H	X	X	Not Selected	Output High Z	Standby
L	H	L	Read RAM	Output Data	Active
L	L	H	Write "1" RAM	Input Data High	Active
L	L	H	Write "0" RAM	Input Data Low	Active
L	L	L	Not Allowed	Output High Z	Active
L	H	H	No Operation	Output High Z	Active

2015 PGM T09

EQUIVALENT A.C. LOAD CIRCUIT



A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3V
Input Rise and Fall Times	5ns
Input and Output Timing Levels	1.5V

2015 PGM T08.1

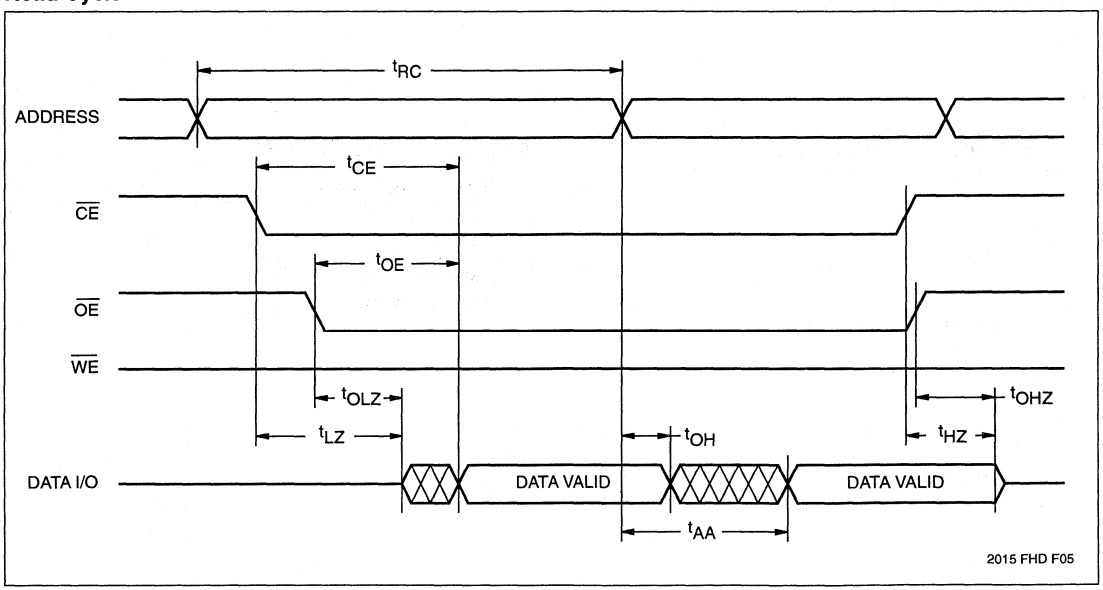
A.C. CHARACTERISTICS (Over the recommended operating conditions unless otherwise specified)

Read Cycle Limits

Symbol	Parameter	X20C17-35		X20C17-45		X20C17-55		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	35		45		55		ns
t_{CE}	Chip Enable Access Time		35		45		55	ns
t_{AA}	Address Access Time		35		45		55	ns
t_{OE}	Output Enable Access Time		20		25		30	ns
t_{LZ}(3)	Chip Enable to Output in Low Z	0		0		0		ns
t_{OLZ}(3)	Output Enable to Output in Low Z	0		0		0		ns
t_{HZ}(3)	Chip Disable to Output in High Z	0	15	0	20	0	25	ns
t_{OHZ}(3)	Output Disable to Output in High Z	0	15	0	20	0	25	ns
t_{OH}	Output Hold From Address Change	0		0		0		ns

2015 PGM T10

Read Cycle



2015 FHD F05

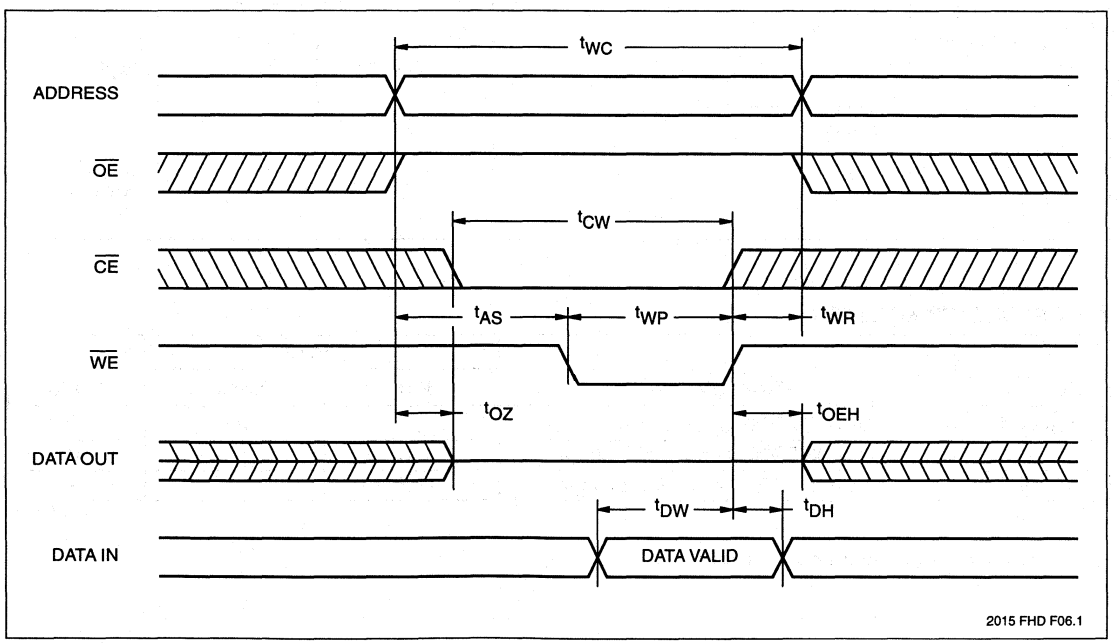
Note: (3) t_{LZ} min., t_{HZ}, t_{OLZ} min., and t_{OHZ} are periodically sampled and not 100% tested. t_{HZ} max. and t_{OHZ} max. are measured, with C_L = 5pF, from the point when $\overline{CE}$ or $\overline{OE}$ return HIGH (whichever occurs first) to the time when the Outputs are no longer driven.

Write Cycle Limits

Symbol	Parameter	X20C17-35		X20C17-45		X20C17-55		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{WC}	Write Cycle Time	35		45		55		ns
t_{CW}	Chip Enable to End of Write Input	30		35		40		ns
t_{AS}	Address Setup Time	0		0		0		ns
t_{WP}	Write Pulse Width	30		35		40		ns
t_{WR}	Write Recovery Time	0		0		0		ns
t_{DW}	Data Setup to End of Write	15		20		25		ns
t_{DH}	Data Hold Time	3		3		3		ns
t_{OEH}	$\overline{OE}$ High Hold Time	0		0		0		ns
t_{OES}	$\overline{OE}$ High Setup Time	0		0		0		ns
t_{OZ}(4)	Output Enable to Output in High Z		15		20		25	ns

2015 PGM T11

Write Cycle



2015 FHD F06.1

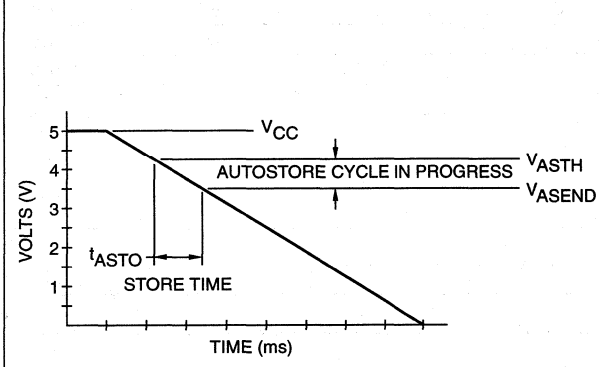
Note: (4) t_{OW}, t_{OZ} are periodically sampled and not 100% tested.

AUTOSTORE Feature

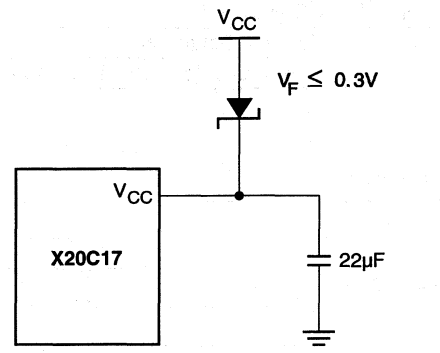
The AUTOSTORE feature automatically saves the contents of the X20C17's static RAM to the on-board bit-for-bit shadow E²PROM at power-down. This circuitry insures that no data is lost during accidental power-downs or general system crashes, and is ideal for microprocessor caching systems, embedded software systems, and general system back-up memory.

The X20C17 automatically initiates a nonvolatile store cycle whenever Vcc falls below the AUTOSTORE threshold voltage (V_{ASTH}). V_{CC} must remain above the AUTOSTORE Cycle End Voltage (V_{ASEND}) for the duration of the store cycle (t_{ASTO}). The detailed timing for this feature is illustrated in the AUTOSTORE timing diagram, below. Once the AUTOSTORE cycle is initiated, all other device functions are inhibited.

AUTOSTORE CYCLE Timing Diagram and Suggested AUTOSTORE Implementation Circuit



2015 FHD F14



2015 ILL F30.4

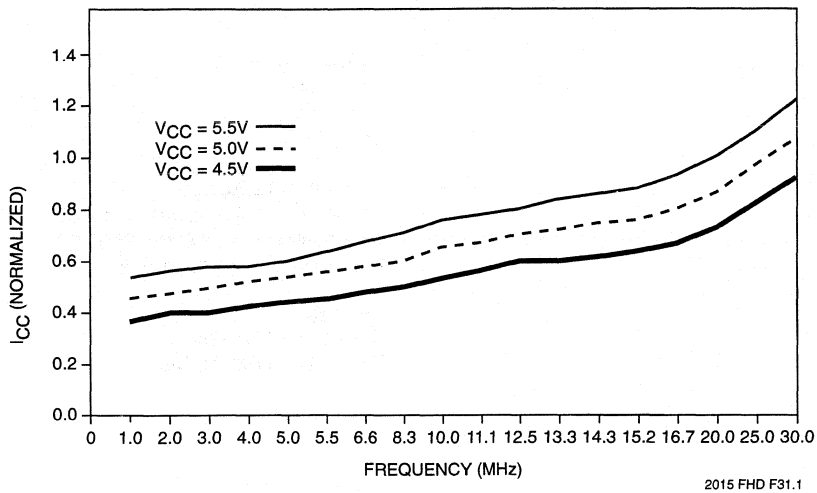
AUTOSTORE CYCLE LIMITS

Symbol	Parameter	X20C17 Min.	X20C17 Max.	Units
t_{ASTO} (5)	AUTOSTORE Cycle Time		2.5	ms
V_{ASTH}	AUTOSTORE Threshold Voltage	4.0	4.3	V
V_{ASEND} (5)	AUTOSTORE Cycle End Voltage	3.5		V

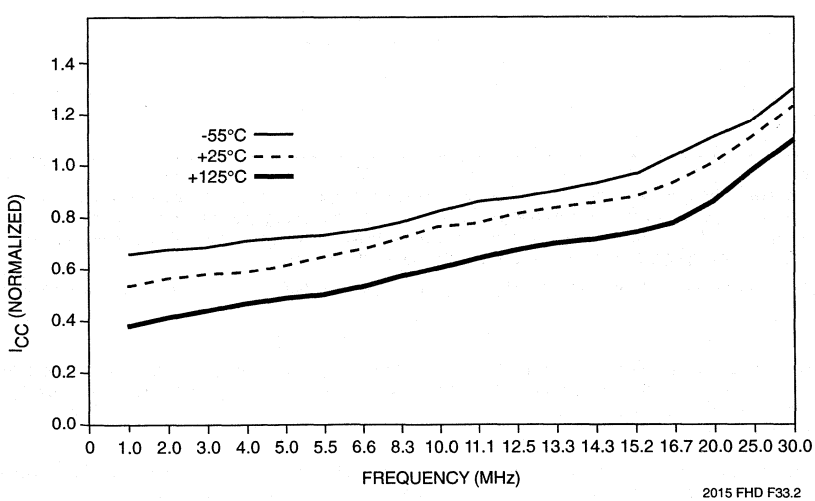
2015 PGM T15

Note: (5) t_{ASTO} and V_{ASEND} are periodically sampled and not 100% tested.

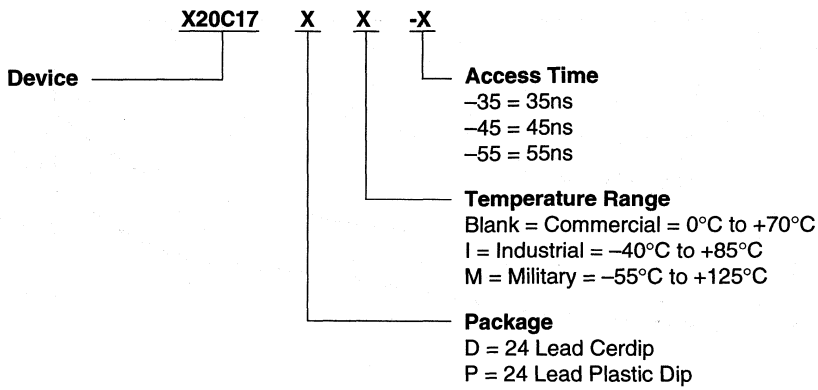
Normalized I_{CC} by Temperature over the V_{CC} Range and Frequency



Normalized I_{CC} by Temperature over Frequency



ORDERING INFORMATION



3807-2.3 12/4/95 T12/C0/D0 NS

APPLICATION NOTES
AVAILABLE
AN3 • AN7 • AN8 • AN15 • AN16 • AN25 • AN29 • AN30 • AN35 • AN36 • AN39 • AN56 • AN69

256 Bit X24C44 16 x 16 Bit

Serial Nonvolatile Static RAM

FEATURES

- **Advanced CMOS Version of Xicor's X2444**
- **16 x 16 Organization**
- **Single 5 Volt Supply**
- **Ideal for use with Single Chip Microcomputers**
  - **—Static Timing**
  - **—Minimum I/O Interface**
  - **—Serial Port Compatible (COPS™, 8051)**
  - **—Easily Interfaced to Microcontroller Ports**
- **Software and Hardware Control of Nonvolatile Functions**
- **Auto Recall on Power-Up**
- **TTL and CMOS Compatible**
- **Low Power Dissipation**
  - **—Active Current: 10mA Maximum**
  - **—Standby Current: 50µA Maximum**
- **8-Pin Mini-DIP and 8-Lead SOIC Packages**
- **High Reliability**
  - **—Store Cycles: 1,000,000**
  - **—Data Retention: 100 Years**

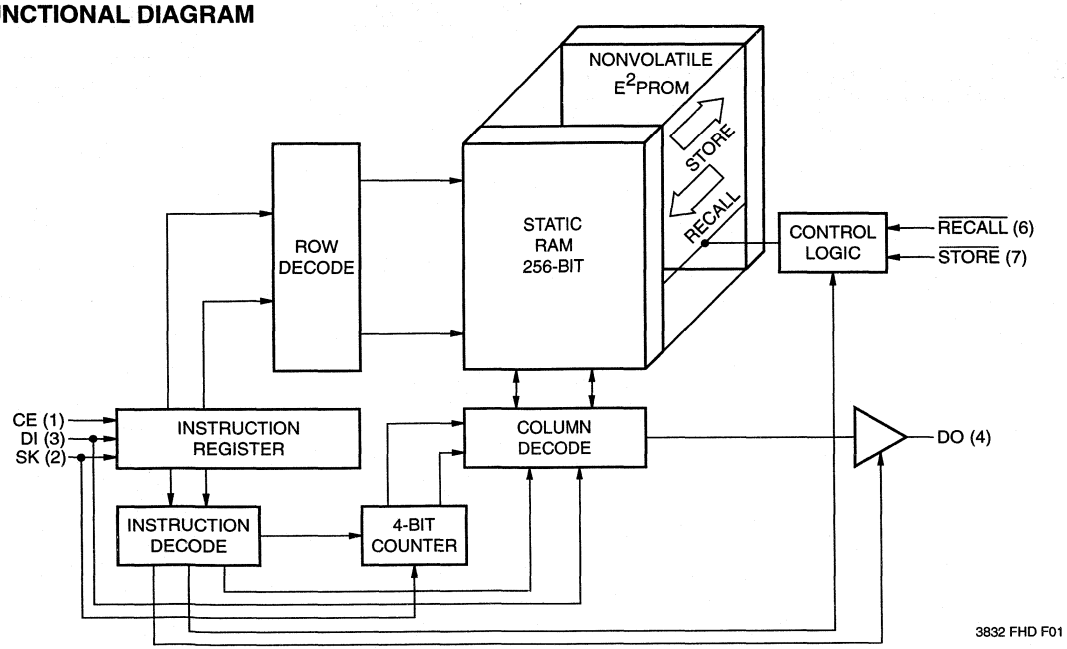
DESCRIPTION

The Xicor X24C44 is a serial 256 bit NOVRAM featuring a static RAM configured 16 x 16, overlaid bit-by-bit with a nonvolatile E²PROM array. The X24C44 is fabricated with Xicor's Advanced CMOS Floating Gate technology.

The Xicor NOVRAM design allows data to be transferred between the two memory arrays by means of software commands or external hardware inputs. A store operation (RAM data to E²PROM) is completed in 5ms or less and a recall operation (E²PROM data to RAM) is completed in 2µs or less.

Xicor NOVRAMs are designed for unlimited write operations to RAM, either from the host or recalls from E²PROM and a minimum 1,000,000 store operations. Inherent data retention is specified to be greater than 100 years.

FUNCTIONAL DIAGRAM



COPS is a trademark of National Semiconductor Corp.

PIN DESCRIPTIONS

Chip Enable (CE)

The Chip Enable input must be HIGH to enable all read/write operations. CE must remain HIGH following a Read or Write command until the data transfer is complete. CE LOW places the X24C44 in the low power standby mode and resets the instruction register. Therefore, CE must be brought LOW after the completion of an operation in order to reset the instruction register in preparation for the next command.

Serial Clock (SK)

The Serial Clock input is used to clock all data into and out of the device.

Data In (DI)

Data In is the serial data input.

Data Out (DO)

Data Out is the serial data output. It is in the high impedance state except during data output cycles in response to a READ instruction.

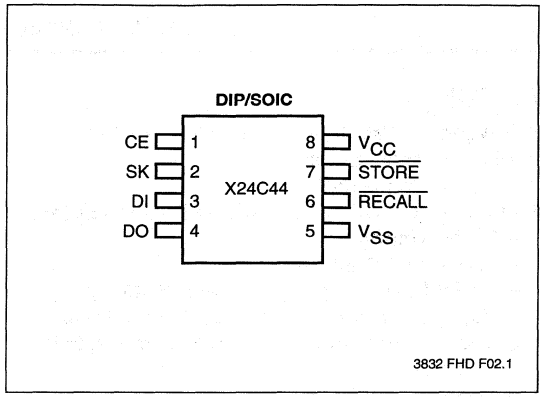
$\overline{\text{STORE}}$

$\overline{\text{STORE}}$ LOW will initiate an internal transfer of data from RAM to the E²PROM array.

$\overline{\text{RECALL}}$

$\overline{\text{RECALL}}$ LOW will initiate an internal transfer of data from E²PROM to the RAM array.

PIN CONFIGURATION



PIN NAMES

Symbol	Description
CE	Chip Enable
SK	Serial Clock
DI	Serial Data In
DO	Serial Data Out
$\overline{\text{RECALL}}$	Recall Input
$\overline{\text{STORE}}$	Store Input
V_{CC}	+5V
V_{SS}	Ground

3832 PGM T01

DEVICE OPERATION

The X24C44 contains an 8-bit instruction register. It is accessed via the DI input, with data being clocked in on the rising edge of SK. CE must be HIGH during the entire data transfer operation.

Table 1. contains a list of the instructions and their operation codes. The most significant bit (MSB) of all instructions is a logic one (HIGH), bits 6 through 3 are either RAM address bits (A) or don't cares (X) and bits 2 through 0 are the operation codes. The X24C44 requires the instruction to be shifted in with the MSB first.

After CE is HIGH, the X24C44 will not begin to interpret the data stream until a logic "1" has been shifted in on DI. Therefore, CE may be brought HIGH with SK running and DI LOW. DI must then go HIGH to indicate the start condition of an instruction before the X24C44 will begin any action.

In addition, the SK clock is totally static. The user can completely stop the clock and data shifting will be stopped. Restarting the clock will resume shifting of data.

RCL and $\overline{\text{RECALL}}$

Either a software RCL instruction or a LOW on the $\overline{\text{RECALL}}$ input will initiate a transfer of E²PROM data into RAM. This software or hardware recall operation sets an internal "previous recall" latch. This latch is reset upon power-up and must be intentionally set by the user to enable any write or store operations. Although a recall operation is performed upon power-up, the previous recall latch is not set by this operation.

WRDS and WREN

Internally the X24C44 contains a "write enable" latch. This latch must be set for either writes to the RAM or store operations to the E²PROM. The WREN instruction sets the latch and the WRDS instruction resets the latch, disabling both RAM writes and E²PROM stores, effectively protecting the nonvolatile data from corruption. The write enable latch is automatically reset on power-up.

STO and $\overline{\text{STORE}}$

Either the software STO instruction or a LOW on the $\overline{\text{STORE}}$ input will initiate a transfer of data from RAM to E²PROM. In order to safeguard against unwanted store operations, the following conditions must be true:

- STO instruction issued or $\overline{\text{STORE}}$ input is LOW.
- The internal "write enable" latch must be set (WREN instruction issued).
- The "previous recall" latch must be set (either a software or hardware recall operation).

Once the store cycle is initiated, all other device functions are inhibited. Upon completion of the store cycle, the write enable latch is reset. Refer to Figure 4 for a state diagram description of enabling/disabling conditions for store operations.

WRITE

The WRITE instruction contains the 4-bit address of the word to be written. The write instruction is immediately followed by the 16-bit word to be written. CE must remain HIGH during the entire operation. CE must go LOW before the next rising edge of SK. If CE is brought LOW prematurely (after the instruction but before 16 bits of data are transferred), the instruction register will be reset and the data that was shifted-in will be written to RAM.

If CE is kept HIGH for more than 24 SK clock cycles (8-bit instruction plus 16-bit data), the data already shifted-in will be overwritten.

Table 1. Instruction Set

Instruction	Format, I_2 I_1 I_0	Operation
WRDS (Figure 3)	1XXXX000	Reset Write Enable Latch (Disables Writes and Stores)
STO (Figure 3)	1XXXX001	Store RAM Data in E²PROM
Reserved	1XXXX010	N/A
WRITE (Figure 2)	1AAAA011	Write Data into RAM Address AAAA
WREN (Figure 3)	1XXXX100	Set Write Enable Latch (Enables Writes and Stores)
RCL (Figure 3)	1XXXX101	Recall E²PROM Data into RAM
READ (Figure 1)	1AAAA11X	Read Data from RAM Address AAAA

3832 PGM T13

X = Don't Care
A = Address

READ

The READ instruction contains the 4-bit address of the word to be accessed. Unlike the other six instructions, I_0 of the instruction word is a "don't care". This provides two advantages. In a design that ties both DI and DO together, the absence of an eighth bit in the instruction allows the host time to convert an I/O line from an output to an input. Secondly, it allows for valid data output during the ninth SK clock cycle.

D0, the first bit output during a read operation, is truncated. That is, it is internally clocked by the falling edge of the eighth SK clock; whereas, all succeeding bits are clocked by the rising edge of SK (refer to Read Cycle Diagram).

LOW POWER MODE

When CE is LOW, non-critical internal devices are powered-down, placing the device in the standby power mode, thereby minimizing power consumption.

SLEEP

Because the X24C44 is a low power CMOS device, the SLEEP instruction implemented on the first generation NMOS device has been deleted. For systems converting from the X2444 to the X24C44 the software need not be changed; the instruction will be ignored.

WRITE PROTECTION

The X24C44 provides two software write protection mechanisms to prevent inadvertent stores of unknown data.

Power-Up Condition

Upon power-up the "write enable" latch is in the reset state, disabling any store operation.

Unknown Data Store

The "previous recall" latch must be set after power-up. It may be set only by performing a software or hardware recall operation, which assures that data in all RAM locations is valid.

SYSTEM CONSIDERATIONS

Power-Up Recall

The X24C44 performs a power-up recall that transfers the E²PROM contents to the RAM array. Although the data may be read from the RAM array, this recall does not set the "previous recall" latch. During this power-up recall operation, all commands are ignored. Therefore, the host should delay any operations with the X24C44 a minimum of t_{PUR} after V_{CC} is stable.

Power-Down Data Protection

Because the X24C44 is a 5V only nonvolatile memory device it may be susceptible to inadvertent stores to the E²PROM array during power-down cycles. Power-up cycles are not a problem because the "previous recall" latch and "write enable" latch are reset, preventing any possible corruption of E²PROM data.

Software Power-Down Protection

If the $\overline{\text{STORE}}$ and $\overline{\text{RECALL}}$ pins are tied to V_{CC} through a pull-up resistor and only software operations are performed to initiate stores, there is little likelihood of an inadvertent store. However, if these two lines are under microprocessor control, positive action should be employed to negate the possibility of these control lines bouncing and generating an unwanted store. The safest method is to issue the WRDS command after a write sequence and also following store operations. Note: an internal store may take up to 5ms; therefore, the host microprocessor should delay 5ms after initiating the store prior to issuing the WRDS command.

Hardware Power-Down Protection

(when the "write enable" latch and "previous recall" latch are not in the reset state):

Holding either $\overline{\text{RECALL}}$ LOW, CE LOW or $\overline{\text{STORE}}$ HIGH during power-down will prevent an inadvertent store.

Figure 1. RAM Read

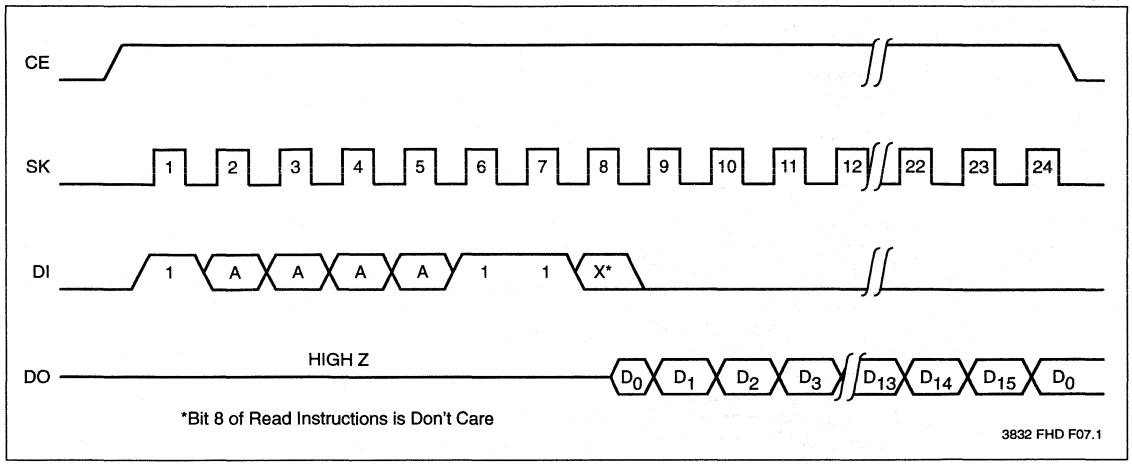


Figure 2. RAM Write

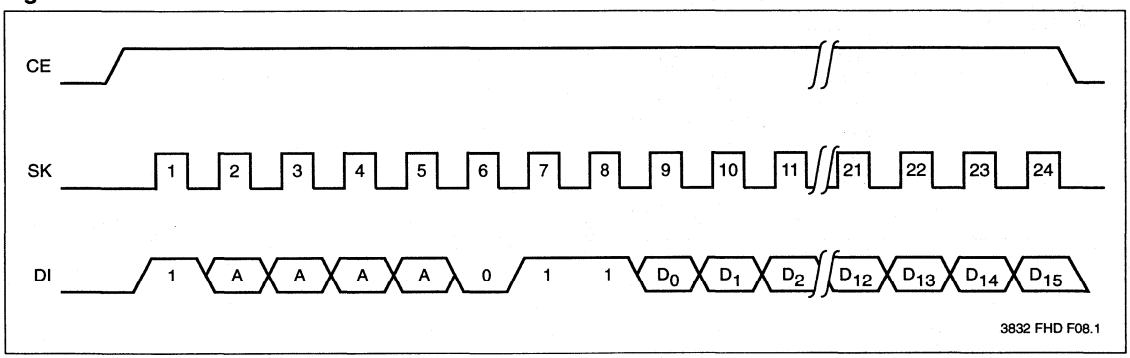


Figure 3. Non-Data Operations

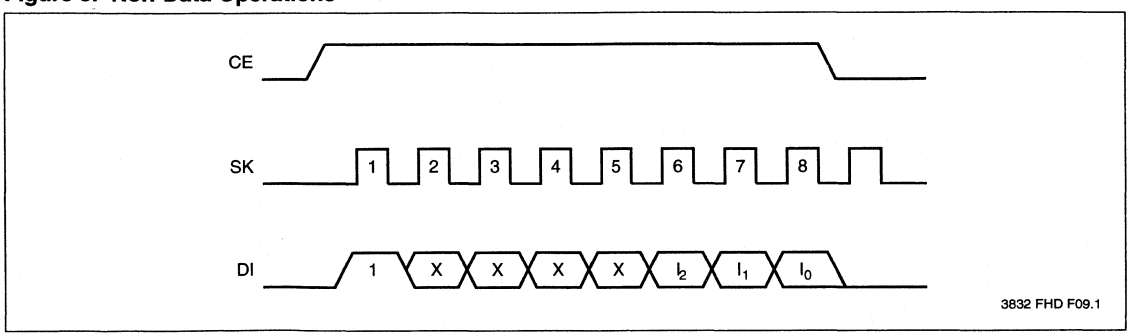
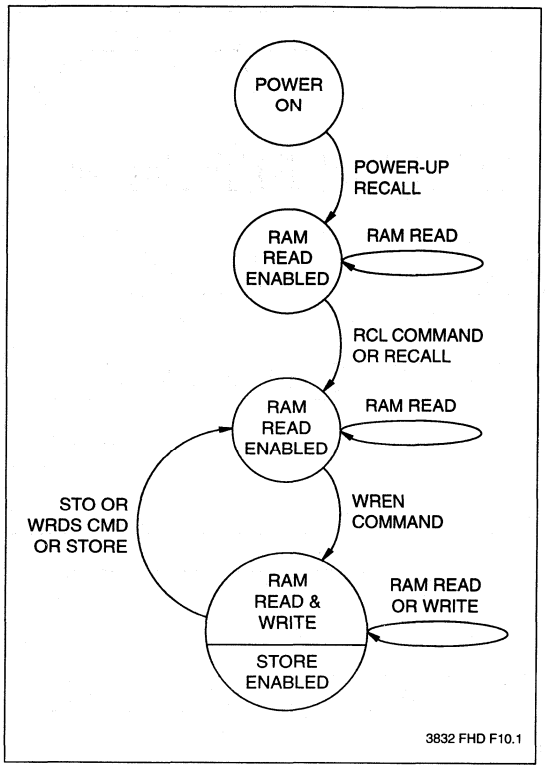


Figure 4. X24C44 State Diagram



ABSOLUTE MAXIMUM RATINGS*

Temperature under Bias ..... –65°C to +135°C
Storage Temperature ..... –65°C to +150°C
Voltage on any Pin with
Respect to V_{SS} ..... –1V to +7V
D.C. Output Current 5mA
Lead Temperature
(Soldering, 10 seconds) ..... 300°C

***COMMENT**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	+70°C
Industrial	–40°C	+85°C
Military	–55°C	+125°C

3832 PGM T02.1

Supply Voltage	Limits
X24C44	5V ±10%

3832 PGM T03.1

D.C. OPERATING CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
I_{CC}	V_{CC} Supply Current (TTL Inputs)		10	mA	SK = 0.4V/2.4V Levels @ 1MHz, DO = Open, All Other Inputs = V_{IH}
I_{SB1}	V_{CC} Standby Current (TTL Inputs)		1	mA	DO = Open, CE = V_{IL}, All Other Inputs = V_{IH}
I_{SB2}	V_{CC} Standby Current (CMOS Inputs)		50	µA	DO = Open, CE = V_{SS} All Other Inputs = V_{CC} – 0.3V
I_{LI}	Input Load Current		10	µA	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output Leakage Current		10	µA	V_{OUT} = V_{SS} to V_{CC}
V_{IL}(1)	Input LOW Voltage	–1	0.8	V	
V_{IH}(1)	Input HIGH Voltage	2	V_{CC} + 1	V	
V_{OL}	Output LOW Voltage		0.4	V	I_{OL} = 4.2mA
V_{OH}	Output HIGH Voltage	2.4		V	I_{OH} = –2mA

3832 PGM T04.3

ENDURANCE AND DATA RETENTION

Parameter	Min.	Units
Endurance	100,000	Data Changes Per Bit
Store Cycles	1,000,000	Store Cycles
Data Retention	100	Years

3832 PGM T05

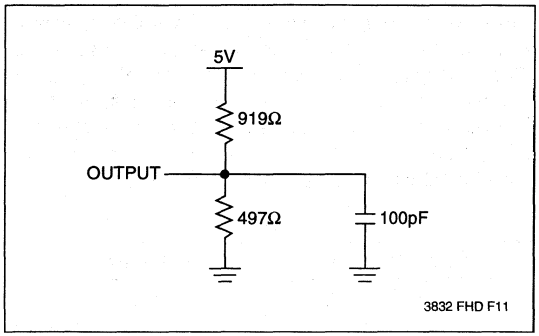
CAPACITANCE T_A = +25°C, f = 1MHz, V_{CC} = 5V

Symbol	Parameter	Max.	Units	Test Conditions
C_{OUT}(2)	Output Capacitance	8	pF	V_{OUT} = 0V
C_{IN}(2)	Input Capacitance	6	pF	V_{IN} = 0V

3832 PGM T06.1

Notes: (1) V_{IL} min. and V_{IH} max. are for reference only and are not tested.
(2) This parameter is periodically sampled and not 100% tested.

EQUIVALENT A.C. LOAD CIRCUIT



A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3V
Input Rise and Fall Times	10ns
Input and Output Timing Levels	1.5V

3832 PGM T07.1

A.C. CHARACTERISTICS (Over the recommended operating conditions unless otherwise specified.)

Read and Write Cycle Limits

Symbol	Parameter	Min.	Max.	Units
F_{SK}(3)	SK Frequency		1	MHz
t_{SKH}	SK Positive Pulse Width	400		ns
t_{SKL}	SK Negative Pulse Width	400		ns
t_{DS}	Data Setup Time	400		ns
t_{DH}	Data Hold Time	80		ns
t_{PD1}	SK to Data Bit 0 Valid		375	ns
t_{PD}	SK to Data Valid		375	ns
t_Z	Chip Enable to Output High Z		1	µs
t_{CES}	Chip Enable Setup	800		ns
t_{CEH}	Chip Enable Hold	350		ns
t_{CDS}	Chip Deselect	800		ns

3832 PGM T08.1

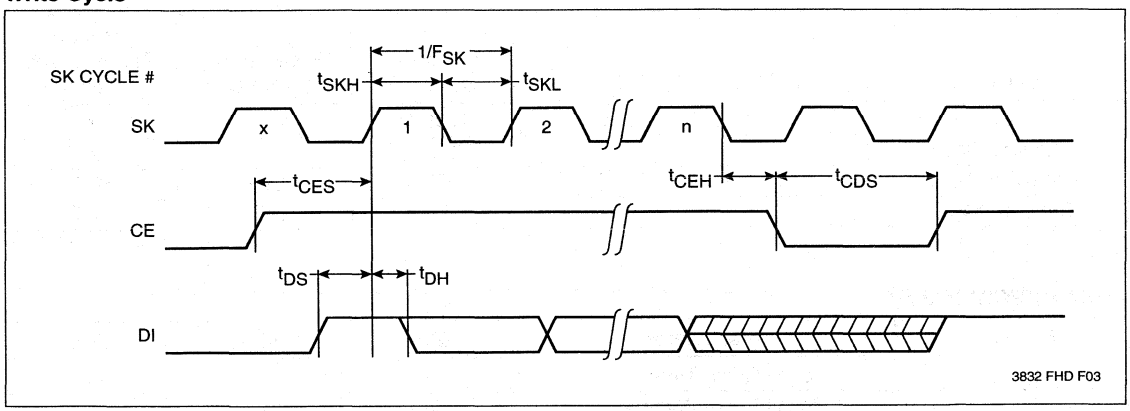
POWER-UP TIMING

Symbol	Parameter	Max.	Units
t_{PUR}(4)	Power-up to Read Operation	200	µs
t_{PUW}(4)	Power-up to Write or Store Operation	5	ms

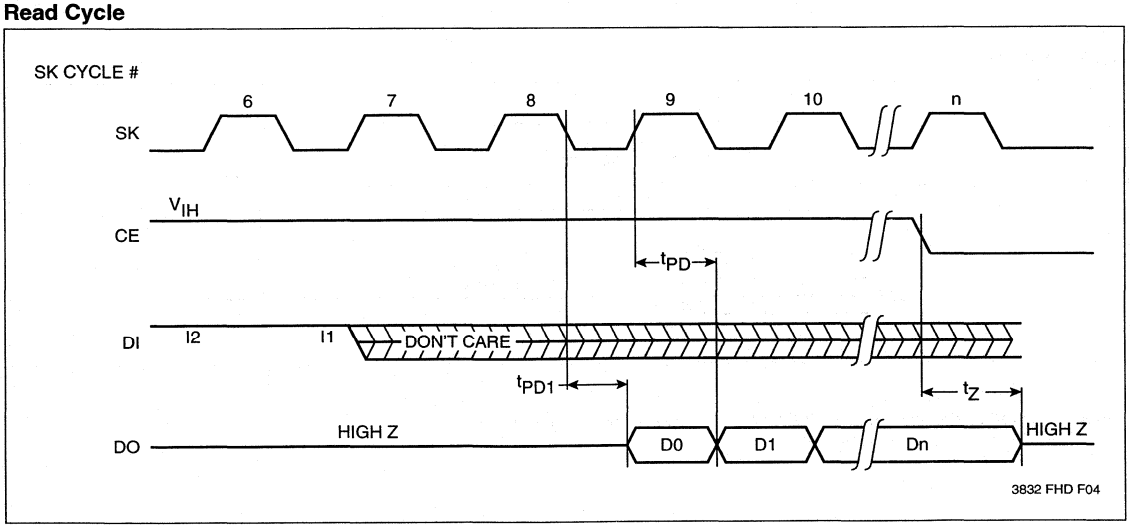
3832 PGM T09

Notes: (3) SK rise and fall times must be less than 50ns.
(4) t_{PUR} and t_{PUW} are the delays required from the time V_{CC} is stable until the specified operation can be initiated. These parameters are periodically sampled and not 100% tested.

Write Cycle



Read Cycle



NONVOLATILE OPERATIONS

Operation	$\overline{\text{STORE}}$	$\overline{\text{RECALL}}$	Software Instruction	Write Enable Latch State	Previous Recall Latch State
Hardware Recall	1	0	NOP(5)	X	X
Software Recall	1	1	RCL	X	X
Hardware Store	0	1	NOP(5)	SET	SET
Software Store	1	1	STO	SET	SET

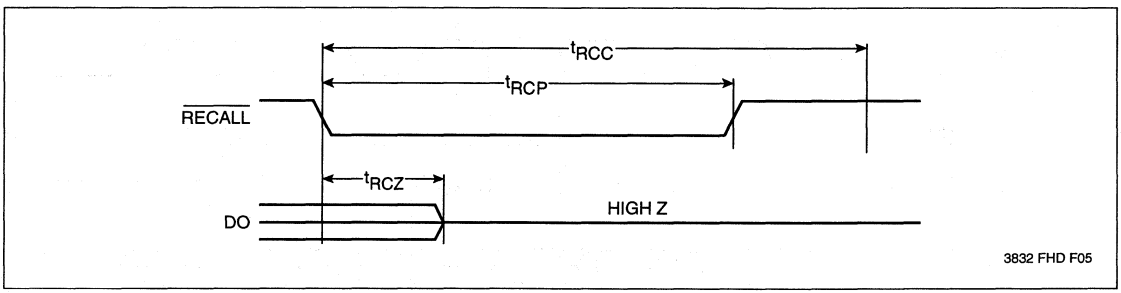
3832 PGM T10

ARRAY RECALL LIMITS

Symbol	Parameter	Min.	Max.	Units
t_{RCC}	Recall Cycle Time	2		µs
t_{RCP}	Recall Pulse Width(6)	500		ns
t_{RCZ}	Recall to Output in High Z		500	ns

3832 PGM T11

Recall Timing



3832 FHD F05

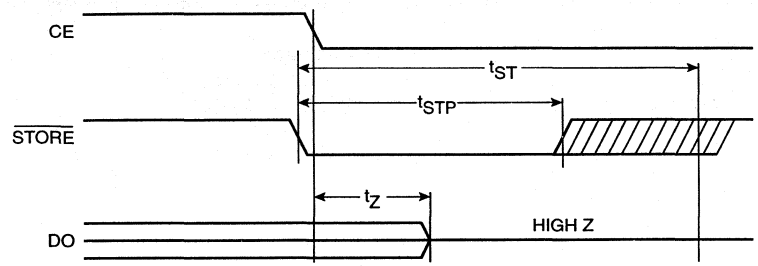
Notes: (5) NOP designates when the X24C44 is not currently executing an instruction.
(6) Recall rise time must be <10µs.

STORE CYCLE LIMITS

Symbol	Parameter	Min.	Typ.(7)	Max.	Units
t_{ST}	Store Time		2	5	ms
t_{STP}	Store Pulse Width	200			ns
t_Z	CE to Output in High Z			1	µs
V_{CC}	Store Inhibit		3		V

3832 PGM T12

Store Timing



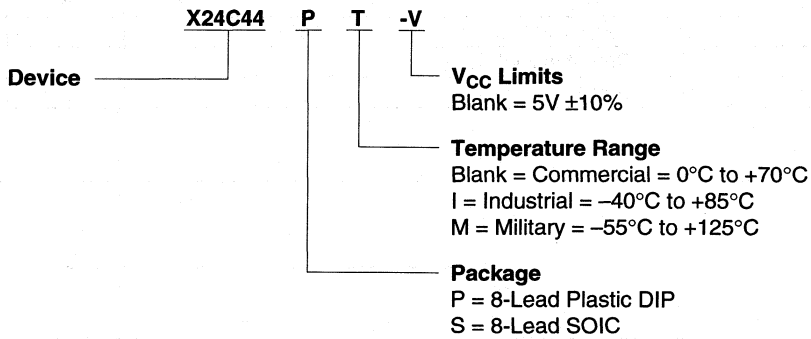
3832 FHD F06

Note: (7) Typical values are for T_A = 25°C and nominal supply voltage.

SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

ORDERING INFORMATION



256 Bit X24C45 16 x 16 Bit

Serial AUTOSTORE™ NOVRAM

FEATURES

- **AUTOSTORE™ NOVRAM**
  - **—Automatically Performs a Store Operation Upon Loss of V_{CC}**
- **Single 5 Volt Supply**
- **Ideal for use with Single Chip Microcomputers**
  - **—Minimum I/O Interface**
  - **—Serial Port Compatible (COPS™, 8051)**
  - **—Easily Interfaced to Microcontroller Ports**
- **Software and Hardware Control of Nonvolatile Functions**
- **Auto Recall on Power-Up**
- **TTL and CMOS Compatible**
- **Low Power Dissipation**
  - **—Active Current: 10mA**
  - **—Standby Current: 50μA**
- **8-Pin Mini-DIP and 8-Lead SOIC Packages**
- **High Reliability**
  - **—Store Cycles: 1,000,000**
  - **—Data Retention: 100 Years**

DESCRIPTION

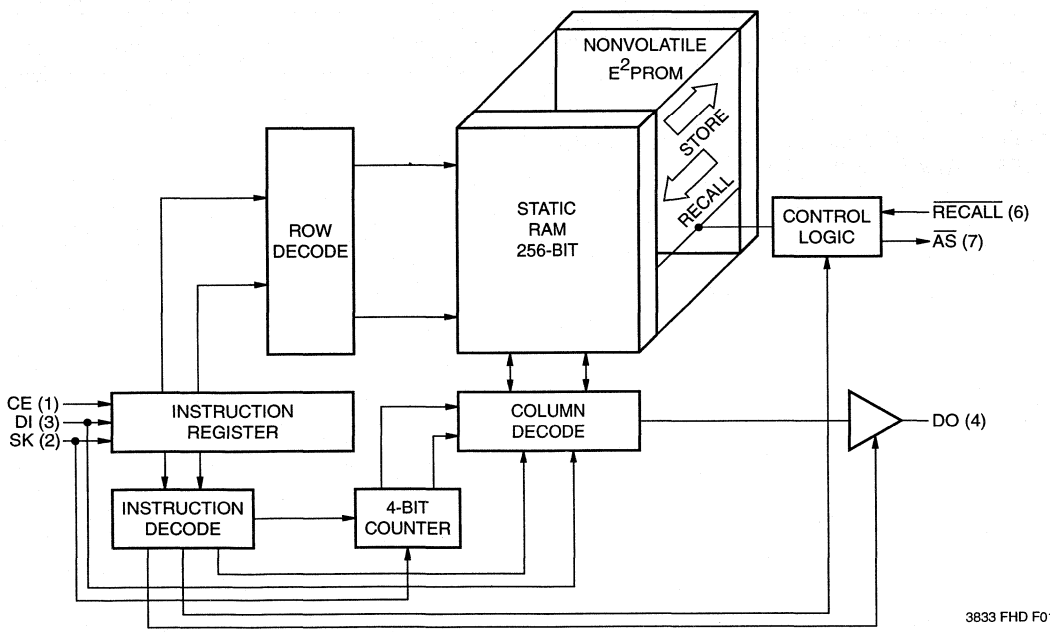
The Xicor X24C45 is a serial 256 bit NOVRAM featuring a static RAM configured 16 x 16, overlaid bit-by-bit with a nonvolatile E^2PROM array. The X24C45 is fabricated with Xicor's Advanced CMOS Floating Gate technology.

The Xicor NOVRAM design allows data to be transferred between the two memory arrays by means of software commands or external hardware inputs. A store operation (RAM data to E^2PROM) is completed in 5ms or less and a recall operation (E^2PROM data to RAM) is completed in 2μs or less.

The X24C45 also includes the AUTOSTORE feature, a user selectable feature that automatically performs a store operation when V_{CC} falls below a preset threshold.

Xicor NOVRAMs are designed for unlimited write operations to RAM, either from the host or recalls from E^2PROM and a minimum 1,000,000 store operations. Inherent data retention is specified to be greater than 100 years.

FUNCTIONAL DIAGRAM



AUTOSTORE™ NOVRAM is a trademark of Xicor, Inc.
COPS is a trademark of National Semiconductor Corp.

PIN DESCRIPTIONS

Chip Enable (CE)

The Chip Enable input must be HIGH to enable all read/write operations. CE must remain HIGH following a Read or Write command until the data transfer is complete. CE LOW places the X24C45 in the low power standby mode and resets the instruction register. Therefore, CE must be brought LOW after the completion of an operation in order to reset the instruction register in preparation for the next command.

Serial Clock (SK)

The Serial Clock input is used to clock all data into and out of the device.

Data In (DI)

Data In is the serial data input.

Data Out (DO)

Data Out is the serial data output. It is in the high impedance state except during data output cycles in response to a READ instruction.

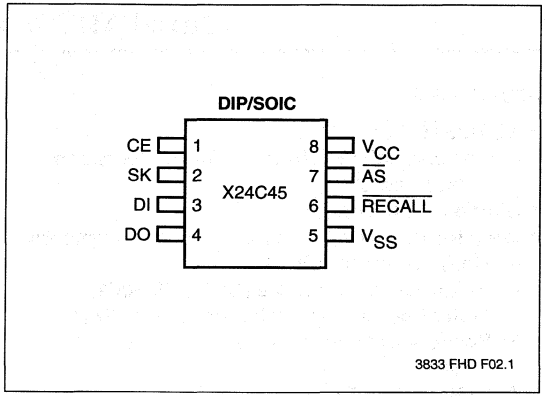
AUTOSTORE Output ($\overline{AS}$)

$\overline{AS}$ is an open drain output which, when asserted indicates V_{CC} has fallen below the AUTOSTORE threshold (V_{ASTH}). $\overline{AS}$ may be wire-ORed with multiple open drain outputs and used as an interrupt input to a microcontroller or as an input to a low power reset circuit.

$\overline{RECALL}$

$\overline{RECALL}$ LOW will initiate an internal transfer of data from E²PROM to the RAM array.

PIN CONFIGURATION



PIN NAMES

Symbol	Description
CE	Chip Enable
SK	Serial Clock
DI	Serial Data In
DO	Serial Data Out
$\overline{RECALL}$	Recall Input
$\overline{AS}$	AUTOSTORE Output
V_{CC}	+5V
V_{SS}	Ground

3833 PGM T01

DEVICE OPERATION

The X24C45 contains an 8-bit instruction register. It is accessed via the DI input, with data being clocked in on the rising edge of SK. CE must be HIGH during the entire data transfer operation.

Table 1. contains a list of the instructions and their operation codes. The most significant bit (MSB) of all instructions is a logic one (HIGH), bits 6 through 3 are either RAM address bits (A) or don't cares (X) and bits 2 through 0 are the operation codes. The X24C45 requires the instruction to be shifted in with the MSB first.

After CE is HIGH, the X24C45 will not begin to interpret the data stream until a logic "1" has been shifted in on DI. Therefore, CE may be brought HIGH with SK running and DI LOW. DI must then go HIGH to indicate the start condition of an instruction before the X24C45 will begin any action.

In addition, the SK clock is totally static. The user can completely stop the clock and data shifting will be stopped. Restarting the clock will resume shifting of data.

RCL and $\overline{\text{RECALL}}$

Either a software RCL instruction or a LOW on the $\overline{\text{RECALL}}$ input will initiate a transfer of E²PROM data into RAM. This software or hardware recall operation sets an internal "previous recall" latch. This latch is reset upon power-up and must be intentionally set by the user to enable any write or store operations. Although a recall operation is performed upon power-up, the previous recall latch is not set by this operation.

WRDS and WREN

Internally the X24C45 contains a "write enable" latch. This latch must be set for either writes to the RAM or store operations to the E²PROM. The WREN instruction sets the latch and the WRDS instruction resets the latch, disabling both RAM writes and E²PROM stores, effectively protecting the nonvolatile data from corruption. The write enable latch is automatically reset on power-up.

STO

The software STO instruction will initiate a transfer of data from RAM to E²PROM. In order to safeguard against unwanted store operations, the following conditions must be true:

- STO instruction issued.
- The internal "write enable" latch must be set (WREN instruction issued).
- The "previous recall" latch must be set (either a software or hardware recall operation).

Once the store cycle is initiated, all other device functions are inhibited. Upon completion of the store cycle, the write enable latch is reset. Refer to Figure 4 for a state diagram description of enabling/disabling conditions for store operations.

TABLE 1. INSTRUCTION SET

Instruction	Format, I_2 I_1 I_0	Operation
WRDS (Figure 3)	1XXXX000	Reset Write Enable Latch (Disables Writes and Stores)
STO (Figure 3)	1XXXX001	Store RAM Data in E²PROM
ENAS	1XXXX010	Enable AUTOSTORE Feature
WRITE (Figure 2)	1AAAA011	Write Data into RAM Address AAAA
WREN (Figure 3)	1XXXX100	Set Write Enable Latch (Enables Writes and Stores)
RCL (Figure 3)	1XXXX101	Recall E²PROM Data into RAM
READ (Figure 1)	1AAAA11X	Read Data from RAM Address AAAA

3833 PGM T11

X = Don't Care
A = Address

WRITE

The WRITE instruction contains the 4-bit address of the word to be written. The write instruction is immediately followed by the 16-bit word to be written. CE must remain HIGH during the entire operation. CE must go LOW before the next rising edge of SK. If CE is brought LOW prematurely (after the instruction but before 16 bits of data are transferred), the instruction register will be reset and the data that was shifted-in will be written to RAM.

If CE is kept HIGH for more than 24 SK clock cycles (8-bit instruction plus 16-bit data), the data already shifted-in will be overwritten.

READ

The READ instruction contains the 4-bit address of the word to be accessed. Unlike the other six instructions, I_0 of the instruction word is a "don't care". This provides two advantages. In a design that ties both DI and DO together, the absence of an eighth bit in the instruction allows the host time to convert an I/O line from an output to an input. Secondly, it allows for valid data output during the ninth SK clock cycle.

D0, the first bit output during a read operation, is truncated. That is, it is internally clocked by the falling edge of the eighth SK clock; whereas, all succeeding bits are clocked by the rising edge of SK (refer to Read Cycle Diagram).

LOW POWER MODE

When CE is LOW, non-critical internal devices are powered-down, placing the device in the standby power mode, thereby minimizing power consumption.

AUTOSTORE Feature

The AUTOSTORE instruction (ENAS) sets the "AUTOSTORE enable" latch, allowing the X24C45 to automatically perform a store operation when V_{CC} falls below the AUTOSTORE threshold (V_{ASTH}).

WRITE PROTECTION

The X24C45 provides two software write protection mechanisms to prevent inadvertent stores of unknown data.

Power-Up Condition

Upon power-up the "write enable" and "AUTOSTORE enable" latches are in the reset state, disabling any store operation.

Unknown Data Store

The "previous recall" latch must be set after power-up. It may be set only by performing a software or hardware recall operation, which assures that data in all RAM locations is valid.

SYSTEM CONSIDERATIONS

Power-Up Recall

The X24C45 performs a power-up recall that transfers the E²PROM contents to the RAM array. Although the data may be read from the RAM array, this recall does not set the "previous recall" latch. During this power-up recall operation, all commands are ignored. Therefore, the host should delay any operations with the X24C45 a minimum of t_{PUR} after V_{CC} is stable.

Figure 1. RAM Read

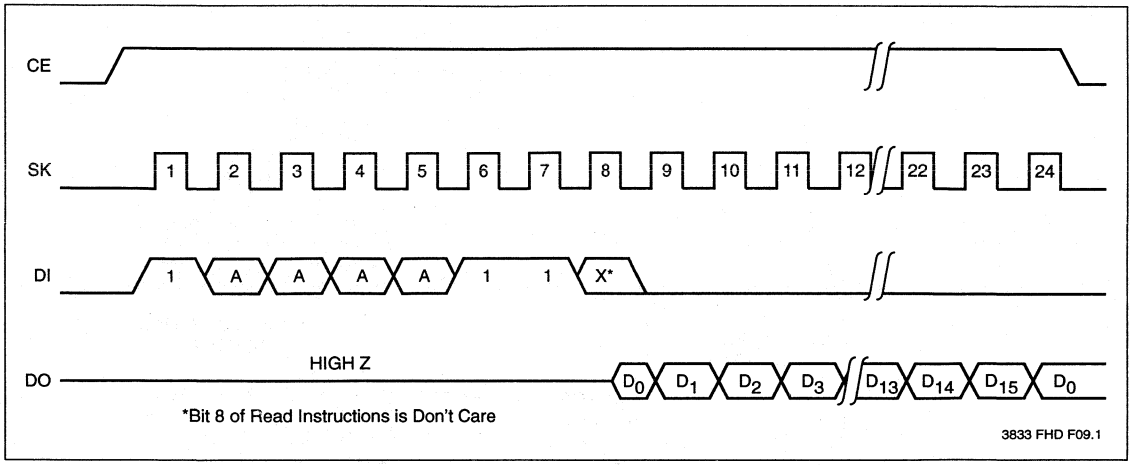


Figure 2. RAM Write

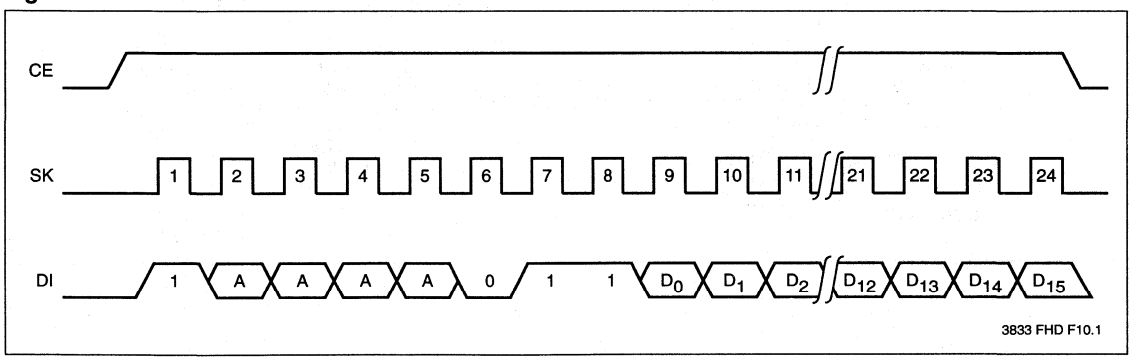


Figure 3. Non-Data Operations

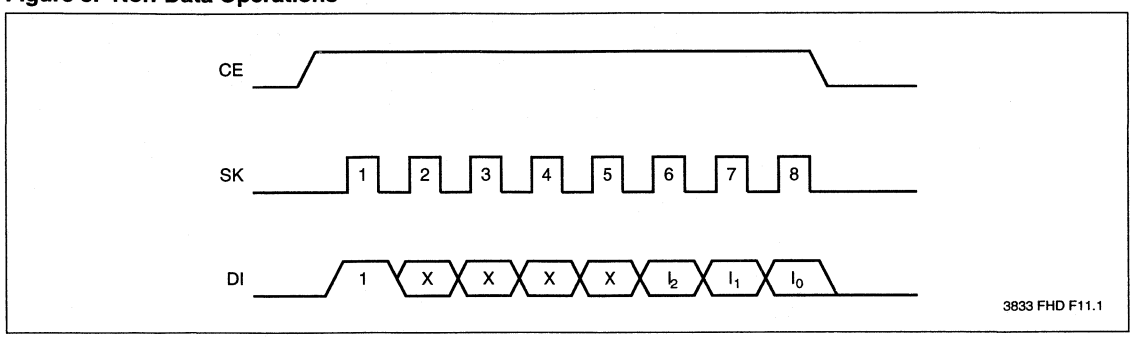
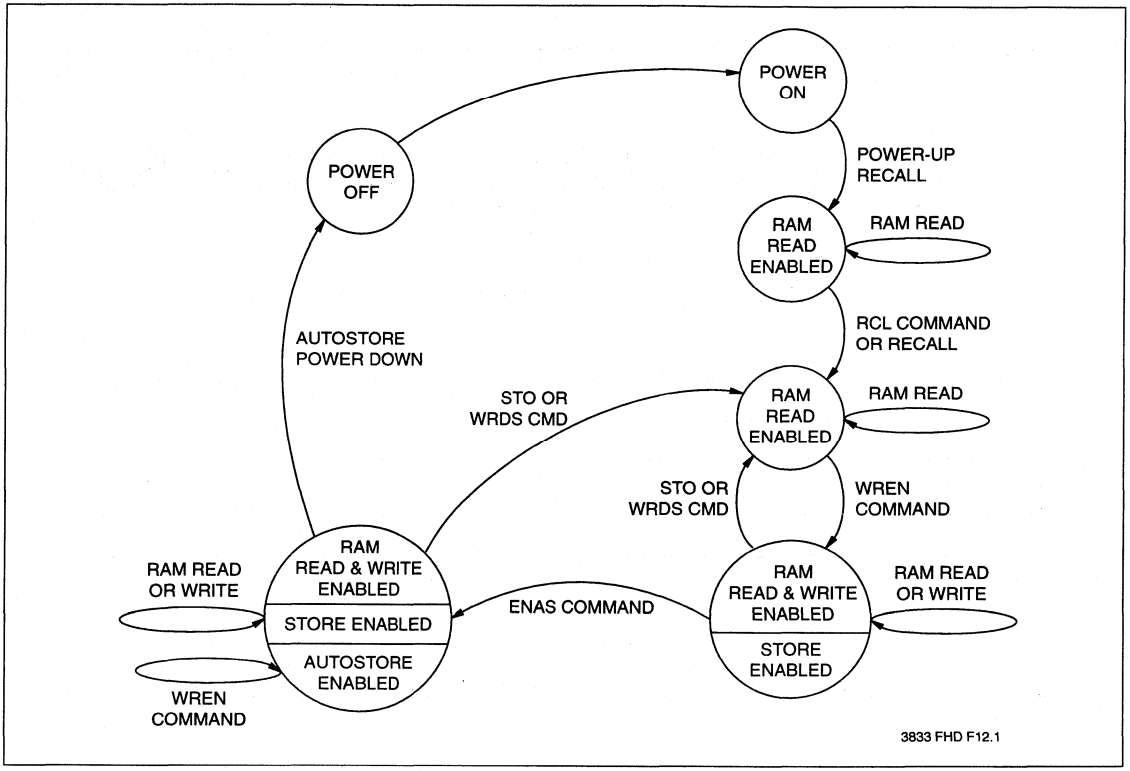


Figure 4. X24C45 State Diagram



ABSOLUTE MAXIMUM RATINGS*

Temperature under Bias ..... –65°C to +135°C
Storage Temperature ..... –65°C to +150°C
Voltage on any Pin with
Respect to V_{SS} ..... –1V to +7V
D.C. Output Current 5mA
Lead Temperature
(Soldering, 10 seconds) ..... 300°C

***COMMENT**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	+70°C
Industrial	–40°C	+85°C
Military	–55°C	+125°C

3833 PGM T02.1

Supply Voltage	Limits
X24C45	5V ±10%

3833 PGM T03.1

D.C. OPERATING CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
I_{CC1}	V_{CC} Supply Current (TTL Inputs)		10	mA	SK = 0.4V/2.4V Levels @ 1MHz, DO = Open, All Other Inputs = V_{IH}
I_{CC2}	V_{CC} Supply Current (During AUTOSTORE)		2	mA	All Inputs = V_{IH}, CE = V_{IL} DO = Open, V_{CC} = 4.3V
I_{SB1}	V_{CC} Standby Current (TTL Inputs)		1	mA	DO = Open, CE = V_{IL}, All Other Inputs = V_{IH}
I_{SB2}	V_{CC} Standby Current (CMOS Inputs)		50	µA	DO = Open, CE = V_{SS} All Other Inputs = V_{CC} – 0.3V
I_{LI}	Input Load Current		10	µA	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output Leakage Current		10	µA	V_{OUT} = V_{SS} to V_{CC}
V_{IL}(1)	Input LOW Voltage	–1	0.8	V	
V_{IH}(1)	Input HIGH Voltage	2	V_{CC} + 1	V	
V_{OL}	Output LOW Voltage		0.4	V	I_{OL} = 4.2mA
V_{OH}	Output HIGH Voltage	2.4		V	I_{OH} = –2mA
$V_{OL(AS)}$	Output LOW Voltage (AS)		0.4	V	$I_{OL\ (AS)}$ = 1mA

3833 PGM T04.3

ENDURANCE AND DATA RETENTION

Parameter	Min.	Units
Endurance	100,000	Data Changes Per Bit
Store Cycles	1,000,000	Store Cycles
Data Retention	100	Years

3833 PGM T05

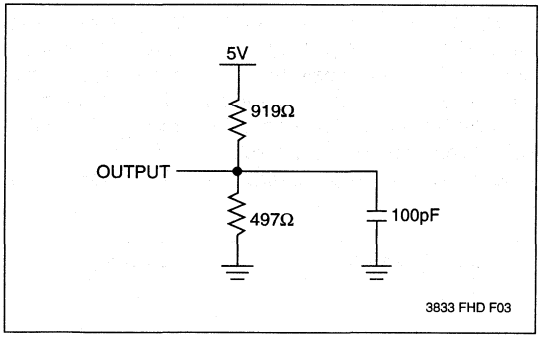
CAPACITANCE T_A = +25°C, f = 1MHz, V_{CC} = 5V

Symbol	Parameter	Max.	Units	Test Conditions
C_{OUT}(2)	Output Capacitance	8	pF	V_{OUT} = 0V
C_{IN}(2)	Input Capacitance	6	pF	V_{IN} = 0V

3833 PGM T06.1

Notes: (1) V_{IL} min. and V_{IH} max. are for reference only and are not tested.
(2) This parameter is periodically sampled and not 100% tested.

EQUIVALENT A.C. LOAD CIRCUIT



A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3V
Input Rise and Fall Times	10ns
Input and Output Timing Levels	1.5V

3833 PGM T07.1

A.C. CHARACTERISTICS (Over the recommended operating conditions unless otherwise specified.)

Read and Write Cycle Limits

Symbol	Parameter	Min.	Max.	Units
F_{SK}(3)	SK Frequency		1	MHz
t_{SKH}	SK Positive Pulse Width	400		ns
t_{SKL}	SK Negative Pulse Width	400		ns
t_{DS}	Data Setup Time	400		ns
t_{DH}	Data Hold Time	80		ns
t_{PD1}	SK to Data Bit 0 Valid		375	ns
t_{PD}	SK to Data Valid		375	ns
t_Z	Chip Enable to Output High Z		1	µs
t_{CES}	Chip Enable Setup	800		ns
t_{CEH}	Chip Enable Hold	350		ns
t_{CDS}	Chip Deselect	800		ns

3833 PGM T08.1

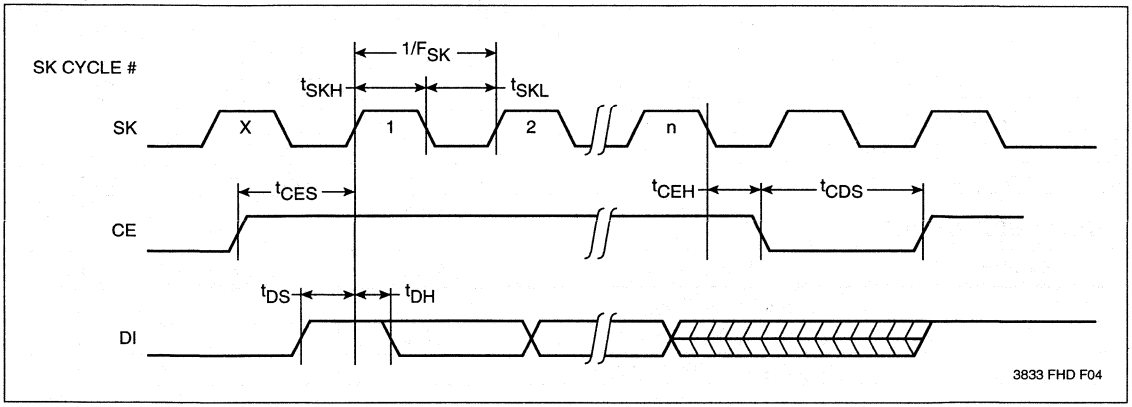
POWER-UP TIMING

Symbol	Parameter	Max.	Units
t_{PUR}(4)	Power-up to Read Operation	200	µs
t_{PUW}(4)	Power-up to Write or Store Operation	5	ms

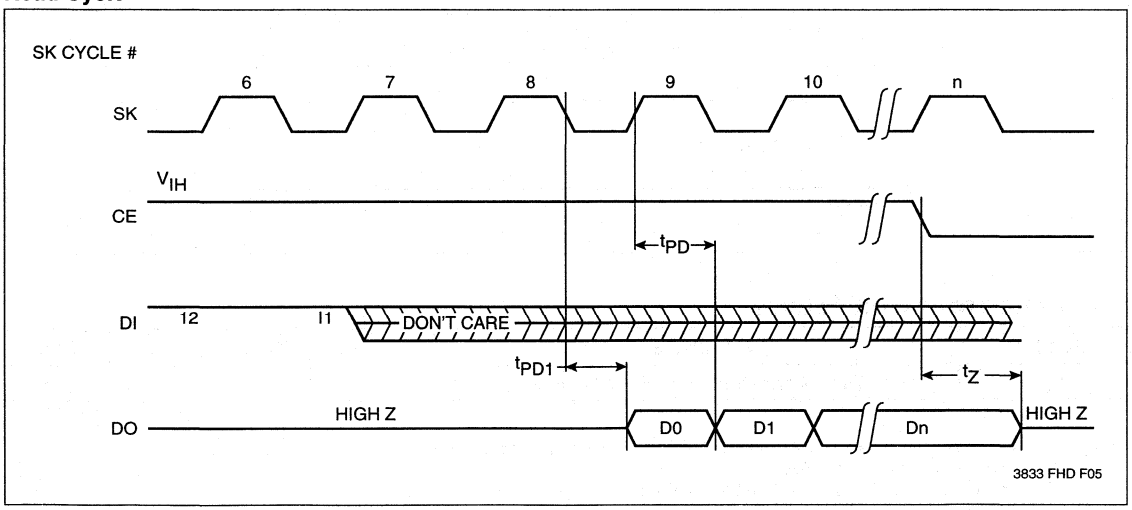
3833 PGM T09

Notes: (3) SK rise and fall times must be less than 50ns.
(4) t_{PUR} and t_{PUW} are the delays required from the time V_{CC} is stable until the specified operation can be initiated. These parameters are periodically sampled and not 100% tested.

Write Cycle



Read Cycle



NONVOLATILE OPERATIONS

Operation	$\overline{\text{RECALL}}$	Software Instruction	Write Enable Latch State	Previous Recall Latch State
Hardware Recall	0	NOP(5)	X	X
Software Recall	1	RCL	X	X
Software Store	1	STO	SET	SET

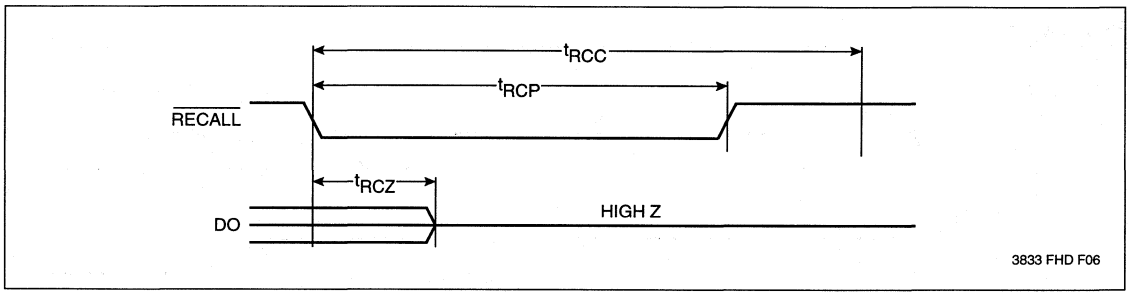
3833 PGM T10

ARRAY RECALL LIMITS

Symbol	Parameter	Min.	Max.	Units
t_{RCC}	Recall Cycle Time	2		µs
t_{RCP}	Recall Pulse Width(6)	500		ns
t_{RCZ}	Recall to Output in High Z		500	ns

3833 PGM T11

Recall Timing



3833 FHD F06

SOFTWARE STORE CYCLE LIMITS

Symbol	Parameter	Min.	Typ.(7)	Max.	Units
t_{ST}	Store Time After Clock 8 of STO Command		2	5	ms

3833 PGM T12.1

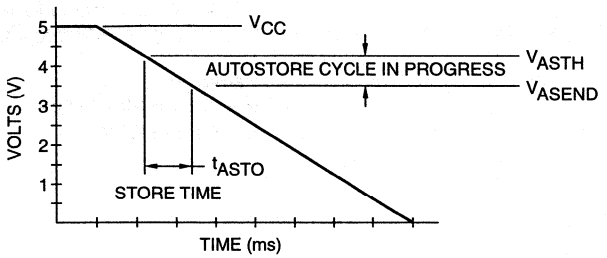
Notes: (5) NOP designates when the X24C45 is not currently executing an instruction.
(6) Recall rise time must be <10µs.
(7) Typical values are for T_A = 25°C and nominal supply voltage.

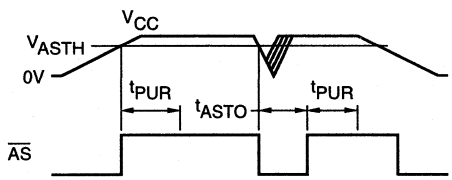
AUTOSTORE Cycle Limits

Symbol	Parameter	Min.	Max.	Units
t_{ASTO}	AUTOSTORE Cycle Time		5	ms
V_{ASTH}	AUTOSTORE Threshold Voltage	4.0	4.3	V
V_{ASEND}	AUTOSTORE Cycle End Voltage	3.5		V

3833 PGM T13.1

AUTOSTORE Cycle Timing Diagrams



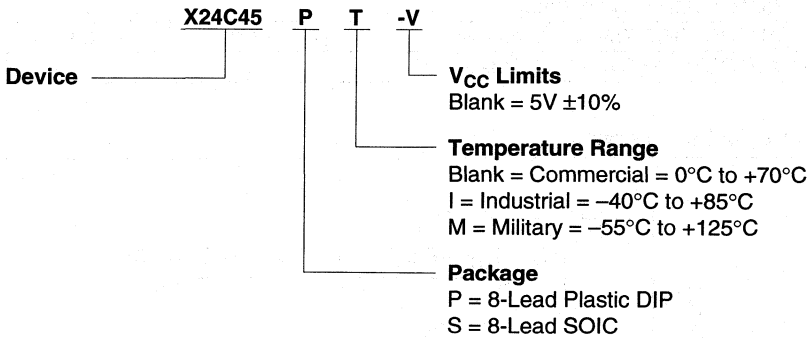


3833 FHD F08

SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

ORDERING INFORMATION



NOTES

Xicor®

#3

Design Engineers Bulletin

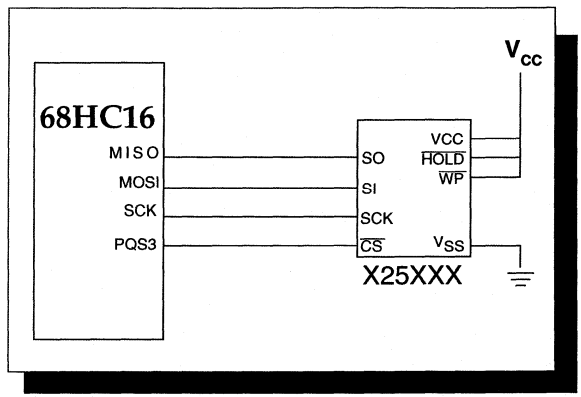
New Product and Applications Information for Design Engineers

New Generation Serial Nonvolatile Memories

The Missing Link for M68HC16 / MC68302 Designs: QSPI Serial Nonvolatile Memories

Migrating in the Motorola microcontroller family beyond the M68HC11 presents a problem for those applications which require nonvolatile memory since the advanced 16 and 32 bit microcontrollers do not feature integrated E²PROM. Xicor's full line of QSPI serial memories fills the void present in the M68HC16/68302 architecture. These serial devices are fully compatible with the QSPI port on the M68HC16 and operate at speeds up to 1MHz. The QSPI interface reduces the software overhead of the serial communication by handling much of the supervision in the interface itself rather than through software intervention.

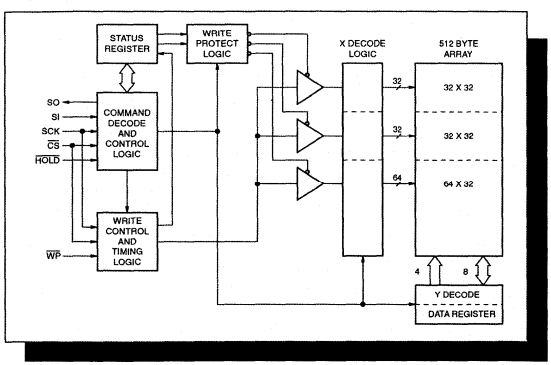
Xicor's Serial SPI memories are available as either Autostore™ NOVRAMS or E²PROMS in densities from 256 Bits to 4K Bits with operating voltage ranges from 2.7 to 5.0 Volts.



X25XXX Family Interfaces Directly to M68HC16 QSPI Ports.

BLOCK LOCK™ Protection and Security Key Code Provides Hierarchical Approach to Data Security

In many applications, it is desirable to provide different levels of alterability to various parameters of data in the system. Certain data, such as calibration or configuration data should only be alterable during initial manufacture or service, while other data may be altered during system operation. This hierarchy of alterability was impossible to provide with older generation nonvolatile memories without resorting to the separation of the data into separate memory devices.



X25040 Advanced Software Configurable Block Lock™ Provides a Fail-Safe Mechanism to Protect Data.

Xicor's SPI family of Serial E²PROMs feature the advanced *BLOCK LOCK* capability. *BLOCK LOCK* divides the memory array into three sections or blocks. The ability to alter data in each section is controlled by the value in a nonvolatile configuration register. Depending upon the value or "Key Code" stored in this register, either none, 1/4, 1/2 or all of the memory can be secured against alteration. In this manner, the "Key Code" for enabling the alteration of calibration data is passed to the system only at time of calibration, which prevents accidental or intentional data modifications or corruption.

APPLICATION NOTE
A V A I L A B L E
AN56

256 Bit X25401 16 x 16 Bit

SPI Serial AUTOSTORE™ NOVRAM

FEATURES

- 1MHz Clock Rate
- AUTOSTORE™ NOVRAM
  - —Automatically Performs a Store Operation Upon Loss of V_{CC}
- Single 5 Volt Supply
- Ideal for use with Single Chip Microcomputers
  - —Minimum I/O Interface
  - —SPI Mode (0,0 & 1,1) Serial Port Compatible
  - —Easily Interfaced to Microcontroller Ports
- Software and Hardware Control of Nonvolatile Functions
- Auto Recall on Power-Up
- TTL and CMOS Compatible
- Low Power Dissipation
  - —Active Current: 10mA
  - —Standby Current: 50µA
- 8-Pin Mini-DIP and 8-Lead SOIC Packages
- High Reliability
  - —Store Cycles: 1,000,000
  - —Data Retention: 100 Years

DESCRIPTION

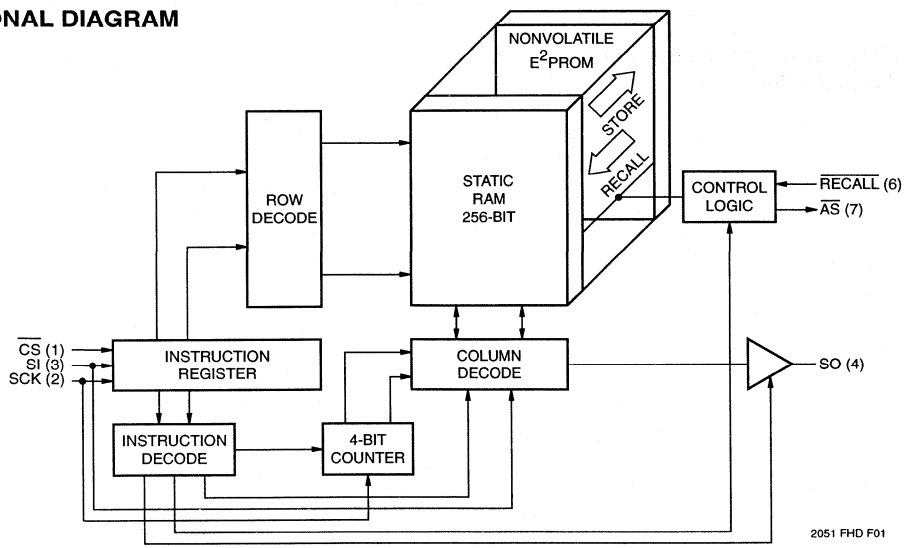
The Xicor X25401 is a serial 256 bit NOVRAM featuring a static RAM configured 16 x 16, overlaid bit-by-bit with a nonvolatile E^2PROM array. The X25401 features a Serial Peripheral Interface (SPI) and software protocol allowing operation on a simple three-wire bus. The bus signals are a clock input (SCK) plus separate data in (SI) and data out (SO) lines. Access to the device is controlled through a chip select ($\overline{CS}$) input, allowing any number of devices to share the same bus.

The Xicor NOVRAM design allows data to be transferred between the two memory arrays by means of software commands or external hardware inputs. A store operation (RAM data to E^2PROM) is completed in 5ms or less and a recall operation (E^2PROM data to RAM) is completed in 2µs or less.

The X25401 also includes the AUTOSTORE feature, a user selectable feature that automatically performs a store operation when V_{CC} falls below a preset threshold.

Xicor NOVRAMs are designed for unlimited write operations to RAM, either from the host or recalls from E^2PROM and a minimum 1,000,000 store operations. Inherent data retention is specified to be greater than 100 years.

FUNCTIONAL DIAGRAM



AUTOSTORE™ NOVRAM is a trademark of Xicor, Inc.
COPS is a trademark of National Semiconductor Corp.

PIN DESCRIPTIONS

Chip Select ($\overline{CS}$)

The Chip Select input must be LOW to enable all read/write operations. $\overline{CS}$ must remain LOW following a Read or Write command until the data transfer is complete. $\overline{CS}$ HIGH places the X25401 in the low power standby mode and resets the instruction register. Therefore, $\overline{CS}$ must be brought HIGH after the completion of an operation in order to reset the instruction register in preparation for the next command.

Serial Clock (SCK)

The Serial Clock input is used to clock all data into and out of the device.

Serial Data In (SI)

SI is the serial data input.

Serial Data Out (SO)

SO is the serial data output. It is in the high impedance state except during data output cycles in response to a READ instruction.

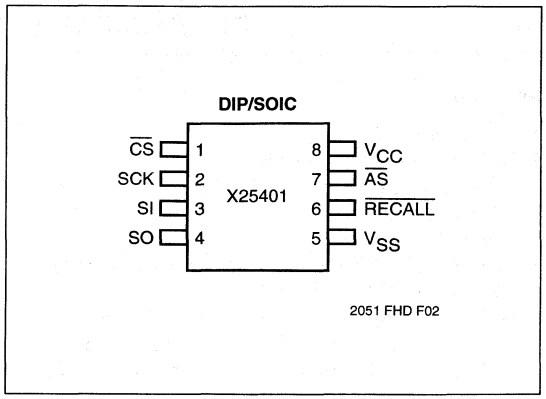
AUTOSTORE Output ($\overline{AS}$)

$\overline{AS}$ is an open drain output which, when asserted indicates V_{CC} has fallen below the AUTOSTORE threshold (V_{ASTH}). $\overline{AS}$ may be wire-ORed with multiple open drain outputs and used as an interrupt input to a microcontroller or as an input to a low power reset circuit.

$\overline{RECALL}$

$\overline{RECALL}$ LOW will initiate an internal transfer of data from E^2PROM to the RAM array.

PIN CONFIGURATION



PIN NAMES

Symbol	Description
$\overline{CS}$	Chip Enable
SCK	Serial Clock
SI	Serial Data In
SO	Serial Data Out
$\overline{RECALL}$	Recall Input
$\overline{AS}$	AUTOSTORE Output
V_{CC}	+5V
V_{SS}	Ground

2051 PGM T01

DEVICE OPERATION

The X25401 contains an 8-bit instruction register. It is accessed via the SI input, with data being clocked in on the rising edge of SCK. $\overline{CS}$ must be LOW during the entire data transfer operation.

Table 1 contains a list of the instructions and their operation codes. The most significant bit (MSB) of all instructions is a logic one (HIGH), bits 6 through 3 are either RAM address bits (A) or don't cares (X) and bits 2 through 0 are the operation codes. The X25401 requires the instruction to be shifted in with the MSB first.

After $\overline{CS}$ is LOW, the X25401 will not begin to interpret the data stream until a logic "1" has been shifted in on SI. Therefore, $\overline{CS}$ may be brought LOW with SCK running and SI LOW. SI must then go HIGH to indicate the start condition of an instruction before the X25401 will begin any action.

In addition, the SCK clock is totally static. The user can completely stop the clock and data shifting will be stopped. Restarting the clock will resume shifting of data.

RCL and $\overline{RECALL}$

Either a software RCL instruction or a LOW on the $\overline{RECALL}$ input will initiate a transfer of E²PROM data into RAM. This software or hardware recall operation sets an internal "previous recall" latch. This latch is reset upon power-up and must be intentionally set by the user to enable any write or store operations. Although a recall operation is performed upon power-up, the previous recall latch is not set by this operation.

WRDS and WREN

Internally the X25401 contains a "write enable" latch. This latch must be set for either writes to the RAM or store operations to the E²PROM. The WREN instruction sets the latch and the WRDS instruction resets the latch, disabling both RAM writes and E²PROM stores, effectively protecting the nonvolatile data from corruption. The write enable latch is automatically reset on power-up.

STO

The software STO instruction will initiate a transfer of data from RAM to E²PROM. In order to safeguard against unwanted store operations, the following conditions must be true:

- STO instruction issued.
- The internal "write enable" latch must be set (WREN instruction issued).
- The "previous recall" latch must be set (either a software or hardware recall operation).

Once the store cycle is initiated, all other device functions are inhibited. Upon completion of the store cycle, the write enable latch is reset. Refer to Figure 4 for a state diagram description of enabling/disabling conditions for store operations.

TABLE 1. INSTRUCTION SET

Instruction	Format, I_2 I_1 I_0	Operation
WRDS (Figure 3)	1XXXX000	Reset Write Enable Latch (Disables Writes and Stores)
STO (Figure 3)	1XXXX001	Store RAM Data in E²PROM
ENAS	1XXXX010	Enable AUTOSTORE Feature
WRITE (Figure 2)	1AAAA011	Write Data into RAM Address AAAA
WREN (Figure 3)	1XXXX100	Set Write Enable Latch (Enables Writes and Stores)
RCL (Figure 3)	1XXXX101	Recall E²PROM Data into RAM
READ (Figure 1)	1AAAA11X	Read Data from RAM Address AAAA

2051 PGM T11

X = Don't Care
A = Address

WRITE

The WRITE instruction contains the 4-bit address of the word to be written. The write instruction is immediately followed by the 16-bit word to be written. $\overline{CS}$ must remain LOW during the entire operation. $\overline{CS}$ must go HIGH before the next rising edge of SCK. If $\overline{CS}$ is brought HIGH prematurely (after the instruction but before 16 bits of data are transferred), the instruction register will be reset and the data that was shifted-in will be written to RAM.

If $\overline{CS}$ is kept LOW for more than 24 SCK clock cycles (8-bit instruction plus 16-bit data), the data already shifted-in will be overwritten.

READ

The READ instruction contains the 4-bit address of the word to be accessed. Unlike the other six instructions, I_0 of the instruction word is a "don't care". This provides two advantages. In a design that ties both SI and SO together, the absence of an eighth bit in the instruction allows the host time to convert an I/O line from an output to an input. Secondly, it allows for valid data output during the ninth SCK clock cycle.

All data bits are clocked by the falling edge of SCK (refer to Read Cycle Diagram).

LOW POWER MODE

When $\overline{CS}$ is HIGH, non-critical internal devices are powered-down, placing the device in the standby power mode, thereby minimizing power consumption.

AUTOSTORE Feature

The AUTOSTORE instruction (ENAS) sets the "AUTOSTORE enable" latch, allowing the X25401 to automatically perform a store operation when V_{CC} falls below the AUTOSTORE threshold (V_{ASTH}).

WRITE PROTECTION

The X25401 provides two software write protection mechanisms to prevent inadvertent stores of unknown data.

Power-Up Condition

Upon power-up the "write enable" and "AUTOSTORE enable" latches are in the reset state, disabling any store operation.

Unknown Data Store

The "previous recall" latch must be set after power-up. It may be set only by performing a software or hardware recall operation, which assures that data in all RAM locations is valid.

SYSTEM CONSIDERATIONS

Power-Up Recall

The X25401 performs a power-up recall that transfers the E²PROM contents to the RAM array. Although the data may be read from the RAM array, this recall does not set the "previous recall" latch. During this power-up recall operation, all commands are ignored. Therefore, the host should delay any operations with the X25401 a minimum of t_{PUR} after V_{CC} is stable.

Figure 1. RAM Read

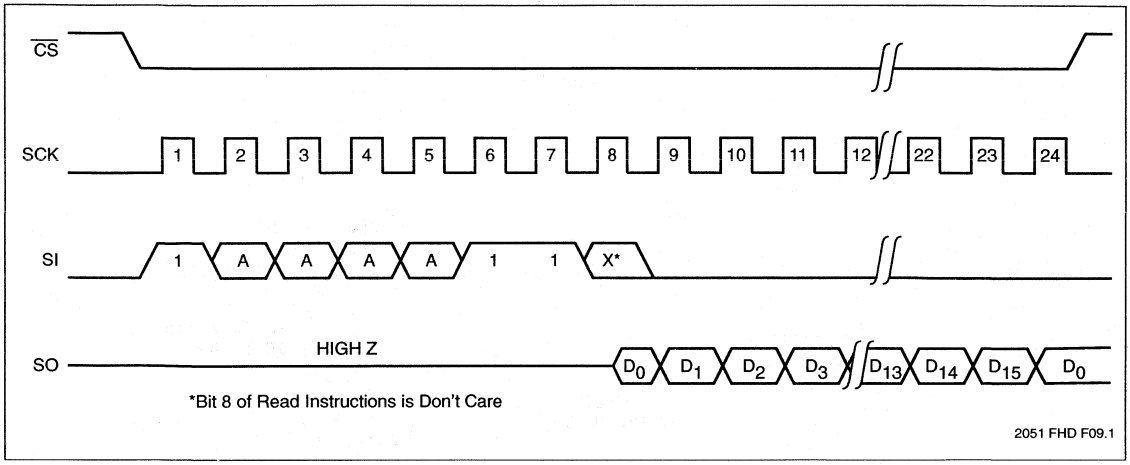


Figure 2. RAM Write

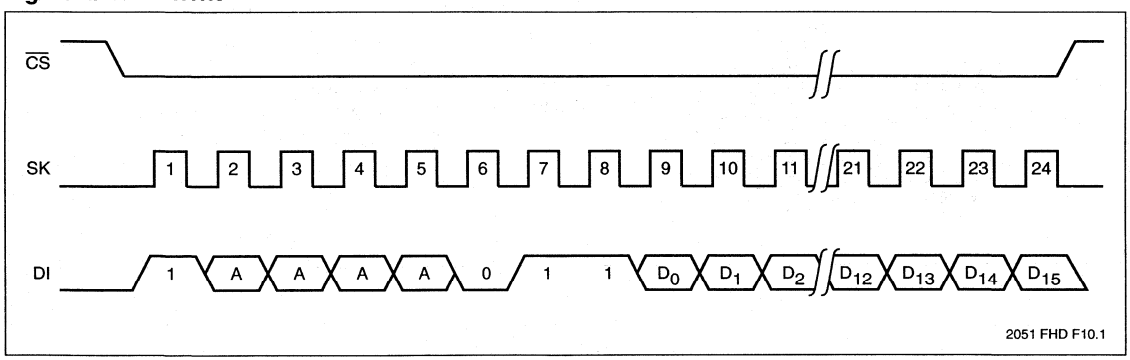


Figure 3. Non-Data Operations

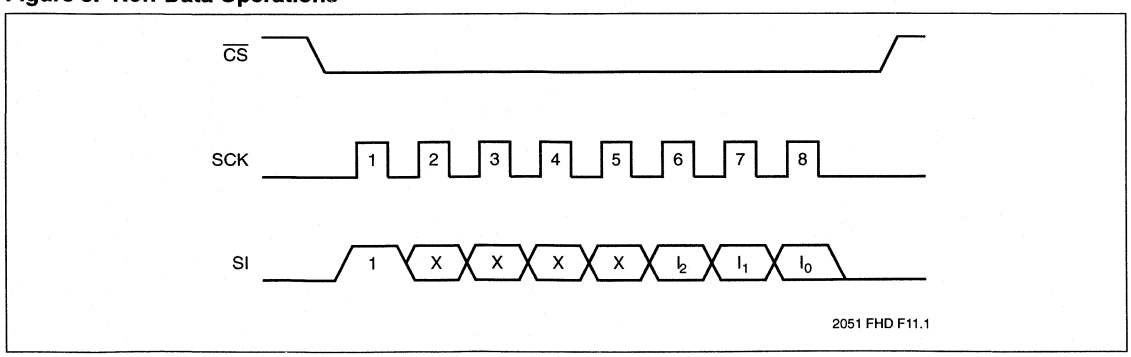
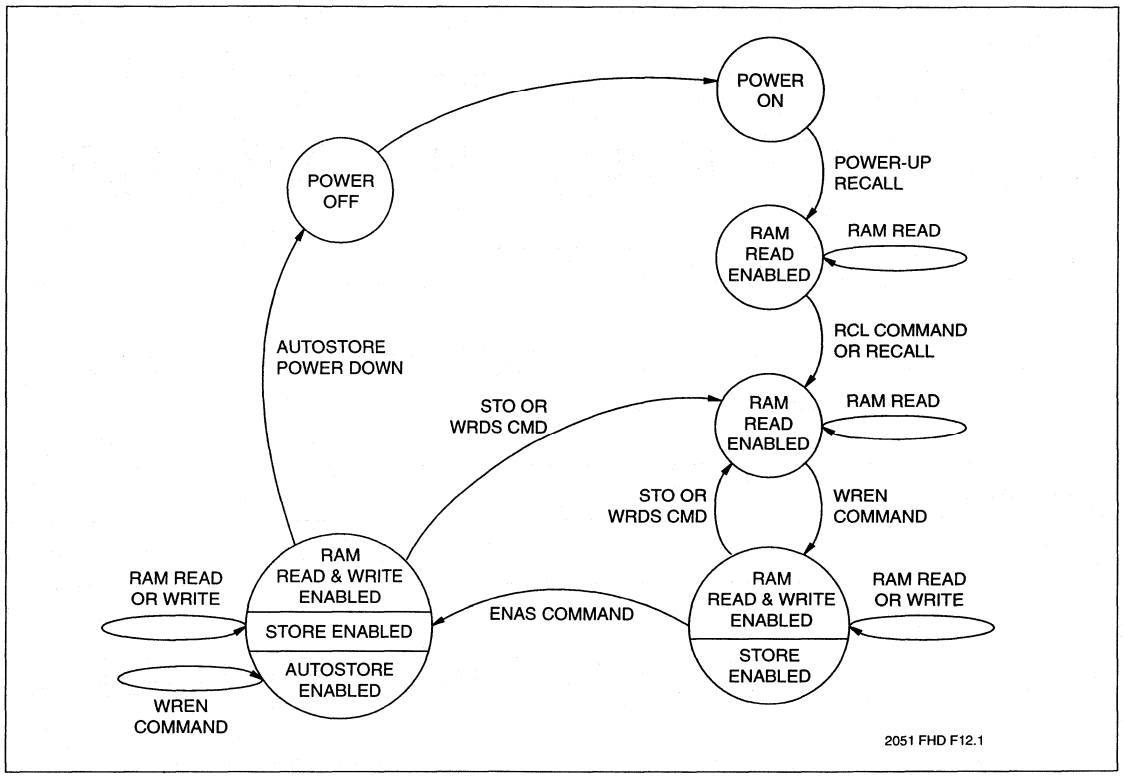


Figure 4. X25401 State Diagram



ABSOLUTE MAXIMUM RATINGS*

Temperature under Bias ..... –65°C to +135°C
Storage Temperature ..... –65°C to +150°C
Voltage on any Pin with
Respect to V_{SS} ..... –1V to +7V
D.C. Output Current 5mA
Lead Temperature
(Soldering, 10 seconds) ..... 300°C

***COMMENT**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	+70°C
Industrial	–40°C	+85°C
Military	–55°C	+125°C

2051 PGM T02.1

Supply Voltage	Limits
X25401	5V ±10%

2051 PGM T03.2

D.C. OPERATING CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
I_{CC1}	V_{CC} Supply Current (TTL Inputs)		10	mA	SCK = 0.4V/2.4V Levels @ 1MHz, SO = Open, All Other Inputs = V_{IH}
I_{CC2}	V_{CC} Supply Current (During AUTOSTORE)		2	mA	All Inputs = V_{IH}, $\overline{CS}$ = V_{IL} SO = Open, V_{CC} = 4.3V
I_{SB1}	V_{CC} Standby Current (TTL Inputs)		1	mA	SO = Open, $\overline{CS}$ = V_{IL}, All Other Inputs = V_{IH}
I_{SB2}	V_{CC} Standby Current (CMOS Inputs)		50	µA	SO = Open, $\overline{CS}$ = V_{SS} All Other Inputs = V_{CC} – 0.3V
I_{LI}	Input Load Current		10	µA	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output Leakage Current		10	µA	V_{OUT} = V_{SS} to V_{CC}
V_{IL}(1)	Input LOW Voltage	–1	0.8	V	
V_{IH}(1)	Input HIGH Voltage	2	V_{CC} + 1	V	
V_{OL}	Output LOW Voltage		0.4	V	I_{OL} = 4.2mA
V_{OH}	Output HIGH Voltage	2.4		V	I_{OH} = –2mA
$V_{OL(AS)}$	Output LOW Voltage (AS)		0.4	V	$I_{OL\ (AS)}$ = 1mA

2051 PGM T04.3

ENDURANCE AND DATA RETENTION

Parameter	Min.	Units
Endurance	100,000	Data Changes Per Bit
Store Cycles	1,000,000	Store Cycles
Data Retention	100	Years

2051 PGM T05

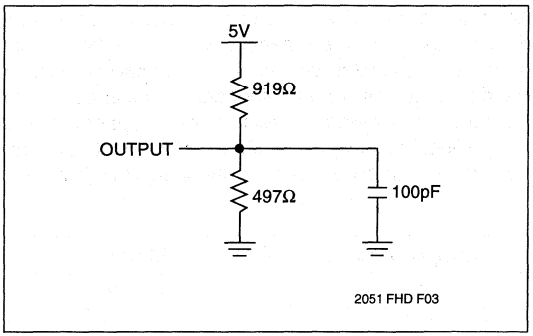
CAPACITANCE T_A = +25°C, f = 1MHz, V_{CC} = 5V

Symbol	Parameter	Max.	Units	Test Conditions
C_{OUT}(2)	Output Capacitance	8	pF	V_{OUT} = 0V
C_{IN}(2)	Input Capacitance	6	pF	V_{IN} = 0V

2051 PGM T06.2

Notes: (1) V_{IL} min. and V_{IH} max. are for reference only and are not tested.
(2) This parameter is periodically sampled and not 100% tested.

EQUIVALENT A.C. LOAD CIRCUIT



A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3V
Input Rise and Fall Times	10ns
Input and Output Timing Levels	1.5V

2051 PGM T07.1

A.C. CHARACTERISTICS (Over the recommended operating conditions unless otherwise specified.)

Read and Write Cycle Limits

Symbol	Parameter	Min.	Max.	Units
F_{SK}(3)	SCK Frequency		1	MHz
t_{SCKH}	SCK Positive Pulse Width	400		ns
t_{SCKL}	SCK Negative Pulse Width	400		ns
t_{DS}	Data Setup Time	400		ns
t_{DH}	Data Hold Time	80		ns
t_{PD1}	SCK to Data Bit 0 Valid		375	ns
t_{PD}	SCK to Data Valid		375	ns
t_Z	Chip Select to Output High Z		1	µs
t_{CSS}	Chip Select Setup	800		ns
t_{CSH}	Chip Select Hold	350		ns
t_{CDS}	Chip Deselect	800		ns

2051 PGM T08.1

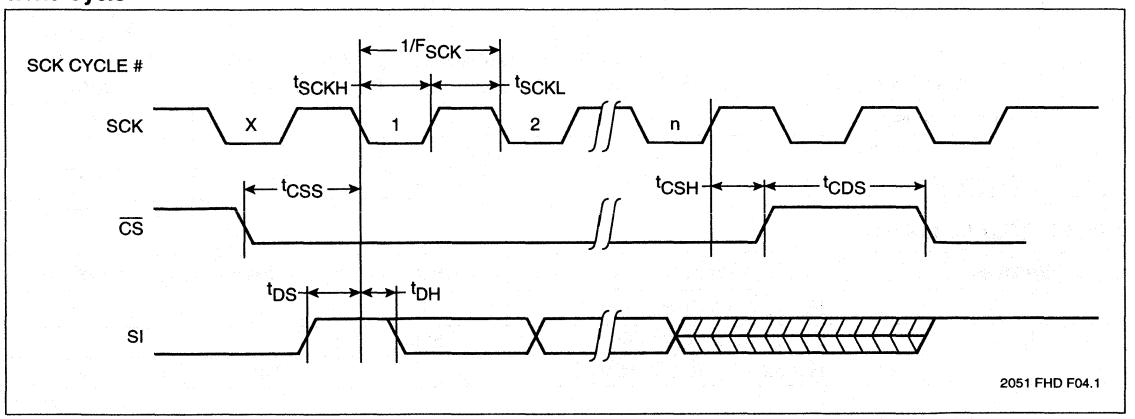
POWER-UP TIMING

Symbol	Parameter	Max.	Units
t_{PUR}(4)	Power-up to Read Operation	200	µs
t_{PUW}(4)	Power-up to Write or Store Operation	5	ms

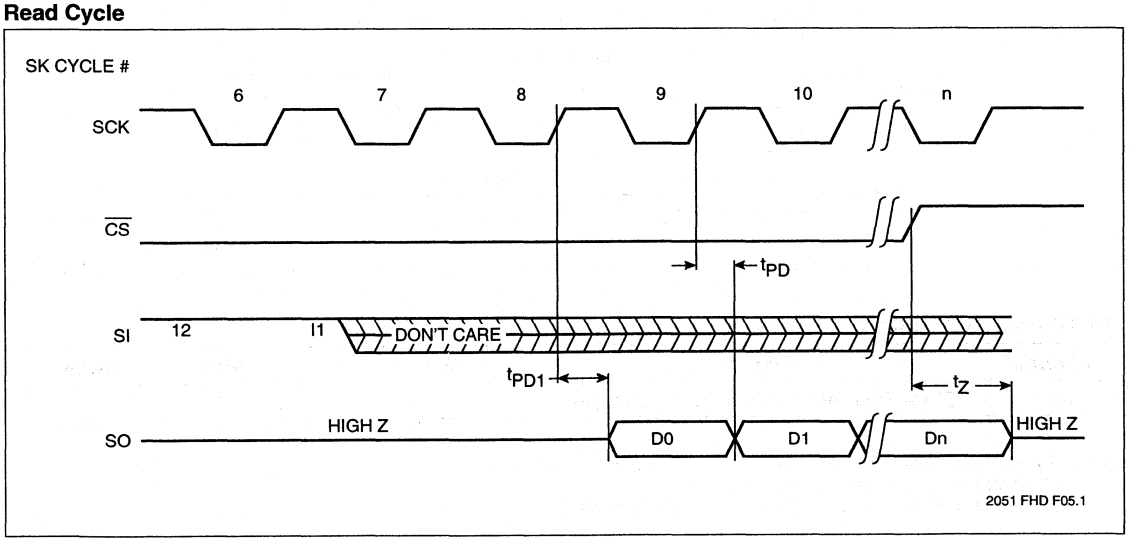
2051 PGM T09

Notes: (3) SCK rise and fall times must be less than 50ns.
(4) t_{PUR} and t_{PUW} are the delays required from the time V_{CC} is stable until the specified operation can be initiated. These parameters are periodically sampled and not 100% tested.

Write Cycle



Read Cycle



NONVOLATILE OPERATIONS

Operation	$\overline{\text{RECALL}}$	Software Instruction	Write Enable Latch State	Previous Recall Latch State
Hardware Recall	0	NOP(5)	X	X
Software Recall	1	RCL	X	X
Software Store	1	STO	SET	SET

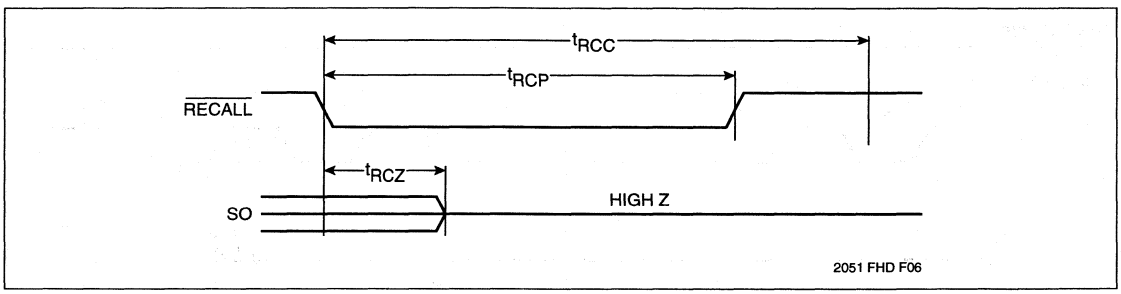
2051 PGM T10

ARRAY RECALL LIMITS

Symbol	Parameter	Min.	Max.	Units
t_{RCC}	Recall Cycle Time	2		µs
t_{RCP}	Recall Pulse Width(6)	500		ns
t_{RCZ}	Recall to Output in High Z		500	ns

2051 PGM T11

Recall Timing



2051 FHD F06

SOFTWARE STORE CYCLE LIMITS

Symbol	Parameter	Min.	Typ.(7)	Max.	Units
t_{ST}	Store Time After Clock 8 of STO Command		2	5	ms

2051 PGM T12.1

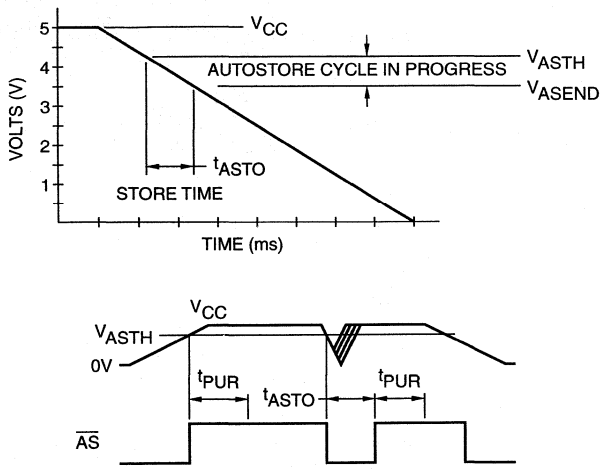
Notes: (5) NOP designates when the X25401 is not currently executing an instruction.
(6) Recall rise time must be <10µs.
(7) Typical values are for T_A = 25°C and nominal supply voltage.

AUTOSTORE Cycle Limits

Symbol	Parameter	Min.	Max.	Units
V_{ASTO}	AUTOSTORE Cycle Time		5	ms
V_{ASTH}	AUTOSTORE Threshold Voltage	4.0	4.3	V
V_{ASEND}	AUTOSTORE Cycle End Voltage	3.5		V

2051 PGM T13

AUTOSTORE Cycle Timing Diagrams

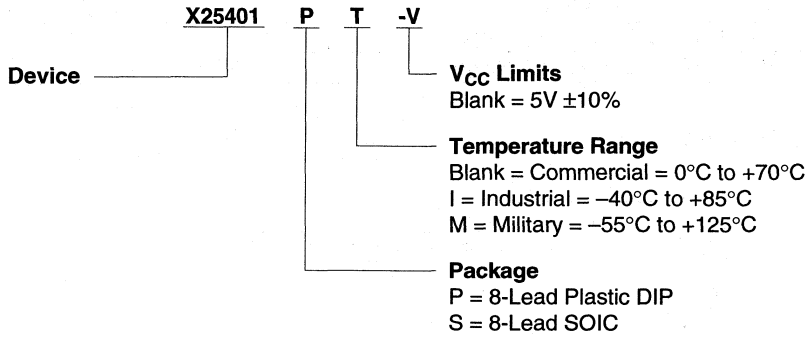


2051 FHD F08

SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

ORDERING INFORMATION



128 Bit X24C00 16 x 8 Bit

Serial E²PROM

FEATURES

- 2.7V to 5.5V Power Supply
- 128 Bit Serial E²PROM
- Low Power CMOS
  - —Active Current Less Than 3mA
  - —Standby Current Less Than 50µA
- Internally Organized 16 x 8
- 2 Wire Serial Interface
  - —Bidirectional Data Transfer Protocol
- Byte Mode Write
- Self Timed Write Cycle
  - —Typical Write Cycle Time of 5ms
- Push/Pull Output
- High Reliability
  - —Endurance: 100,000 Cycles
  - —Data Retention: 100 Years
- 8-Pin Mini-DIP and 8-Lead SOIC Packages

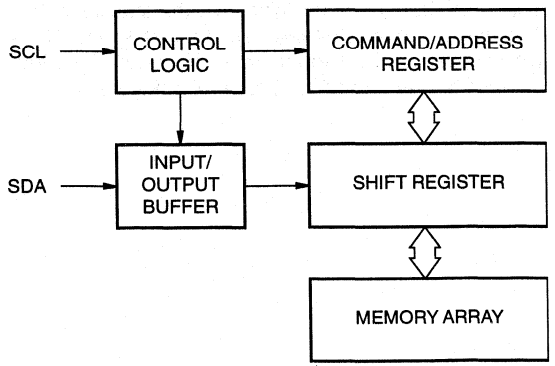
DESCRIPTION

The X24C00 is a CMOS 128 bit serial E²PROM, internally organized as 16 x 8. The X24C00 features a serial interface and software protocol allowing operation on a simple two wire bus.

Xicor E²PROMs are designed and tested for applications requiring extended endurance. Inherent data retention is greater than 100 years.

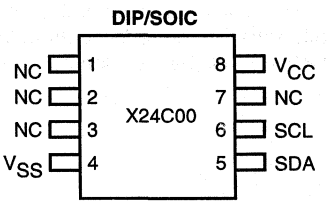
The X24C00 is fabricated with Xicor's Advanced CMOS Floating Gate technology.

FUNCTIONAL DIAGRAM



3836 FHD F01

PIN CONFIGURATION



3836 FHD F03

PIN DESCRIPTIONS

Serial Clock (SCL)

The SCL input is used to clock all data into and out of the device.

Serial Data (SDA)

SDA is a bidirectional pin used to transfer data into and out of the device. It is a push/pull output and does not require the use of a pull-up resistor.

PIN NAMES

Symbol	Description
NC	No Connect
V_{SS}	Ground
V_{CC}	Supply Voltage
SDA	Serial Data
SCL	Serial Clock

3836 PGM T01

DEVICE OPERATION

The X24C00 supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is a master and the device being controlled is the slave. The master will always initiate data transfers and provide the clock for both transmit and receive operations. Therefore, the X24C00 will be considered a slave in all applications.

Clock and Data Conventions

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions. Refer to Figures 1 and 2.

Start Condition

All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The X24C00 continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

A start may be issued to terminate the input of a control word or the input of data to be written. This will reset the device and leave it ready to begin a new read or write command. Because of the push/pull output, a start cannot be generated while the part is outputting data. Starts are also inhibited while a write is in progress.

Stop Condition

The stop condition is a LOW to HIGH transition of SDA when SCL is HIGH. The stop condition is used to reset the device during a command or data input sequence and will leave the device in the standby mode. As with starts, stops are inhibited when outputting data and while a write is in progress.

Write Operation

The byte write operation is initiated with a start condition. The start condition is followed by an eight bit control byte which consists of a two bit write command (0,1), four address bits, and two "don't care" bits (Figure 3).

Figure 1. Data Validity

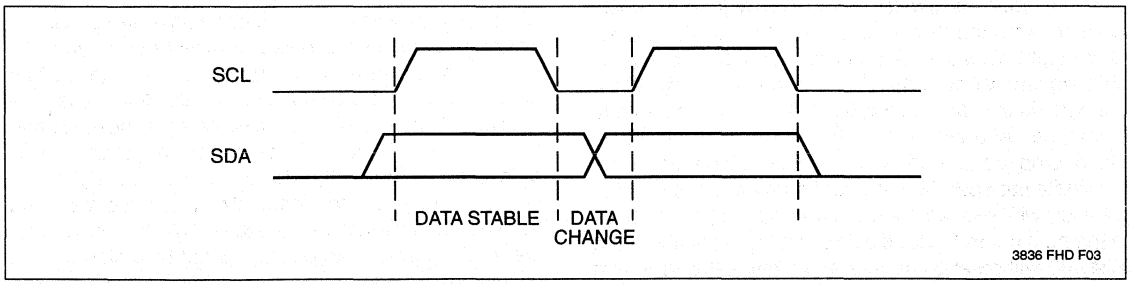


Figure 2. Definition of Start and Stop Conditions

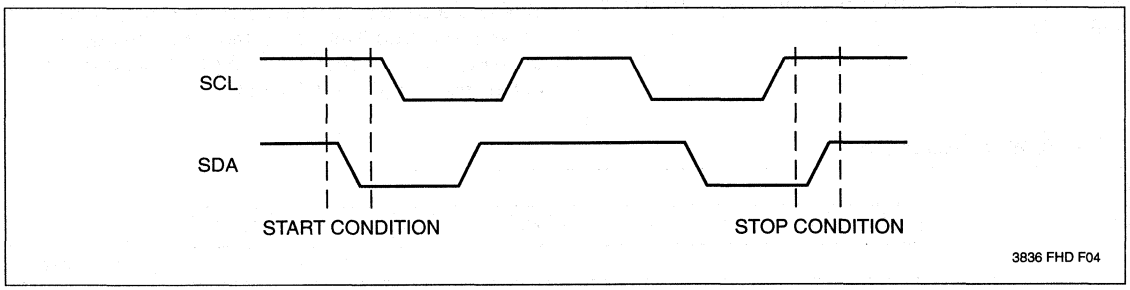
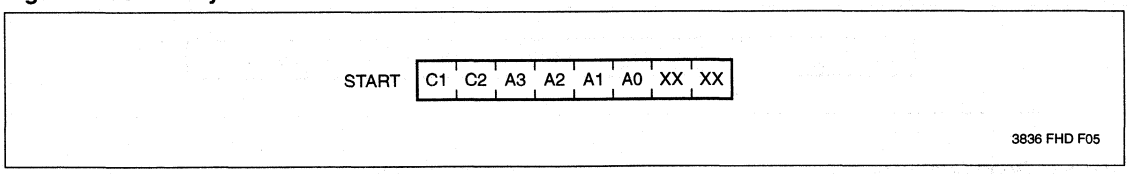


Figure 3. Control Byte



After receipt of the control byte, the X24C00 will enter the write mode and await the data to be written. This data is shifted into the device on the next eight SCL clocks. Once eight clocks have been received, the data in the shift register will be written into the memory array. While the write is in progress the X24C00 will not respond to any inputs. At any time prior to clocking in the last data bit, a stop command or a new start command will terminate the operation. If a start command is given, the X24C00 will reset all counters and will prepare to clock in the next control byte. If a stop command is given, the X24C00 will reset all counters and await the next start command.

At the end of the write the X24C00 will automatically reset all counters and enter the standby mode. (Figure 4).

Read Operation

The byte read operation is initiated with a start condition. The start condition is followed by an eight-bit control byte which consists of a two-bit read command (1,0), four address bits, and two "don't care" bits. After receipt of the control byte the X24C00 will enter the read mode and transfer data into the shift register from the array. This data is shifted out of the device on the next eight SCL clocks. At the end of the read, all counters are reset and the X24C00 will enter the standby mode. As with a write, the read operation can be interrupted by a start or stop condition while the command or address is being clocked in. While clocking data out, starts or stops cannot be generated.

During the second don't care clock cycle, starts and stops are ignored. The master must free the bus prior to the end of this clock cycle to allow the X24C00 to begin outputting data (Figures 5 and 6).

Figure 4. Write Sequence

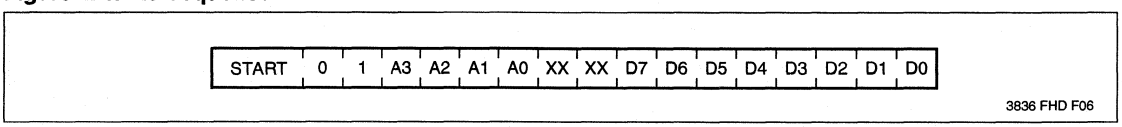


Figure 5. Read Sequence

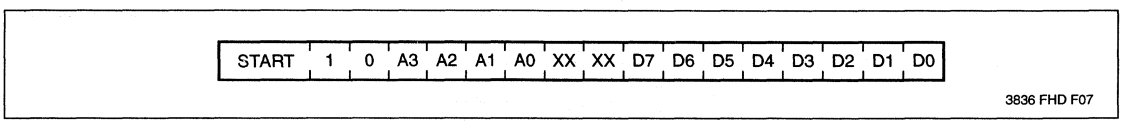
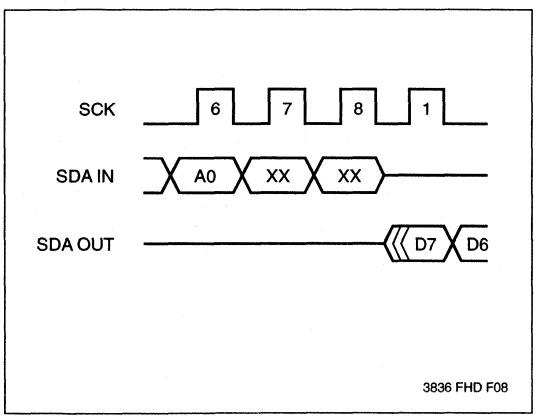


Figure 6. Read Cycle Timing



SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

ABSOLUTE MAXIMUM RATINGS*

Temperature under Bias
X24C00 ..... –65°C to +135°C
Storage Temperature ..... –65°C to +150°C
Voltage on any Pin with
Respect to V_{SS} ..... –1V to +7V
D.C. Output Current 5mA
Lead Temperature
(Soldering, 10 seconds) ..... 300°C

***COMMENT**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2

RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	+70°C
Industrial	–40°C	+85°C
Military	–55°C	+125°C

3836 PGM T02.1

Supply Voltage	Limits
X24C00	5V ±10%
X24C00-3	3V to 5.5V
X24C00-2.7	2.7V to 5.5V

3836 PGM T03.1

D.C. OPERATING CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
I_{CC1}	V_{CC} Supply Current Read		1	mA	SCL = VCC x 0.1/VCC x 0.9
I_{CC2}	V_{CC} Supply Current Write		3		Levels @ 1MHz, SDA = Open
I_{SB1}	V_{CC} Standby Current		100	µA	SCL = SDA = V_{CC} V_{CC} = 5V ±10%
I_{SB2}	V_{CC} Standby Current		50	µA	SCL = SDA = V_{CC} V_{CC} = 2.7V
I_{LI}	Input Leakage Current		10	µA	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output Leakage Current		10	µA	V_{OUT} = V_{SS} to V_{CC}
V_{IL}(1)	Input LOW Voltage	–1	V_{CC} x 0.3	V	
V_{IH}(1)	Input HIGH Voltage	V_{CC} x 0.7	V_{CC} + 0.5	V	
V_{OL}	Output LOW Voltage		0.4	V	I_{OL} = 2.1mA
V_{OH}	Output HIGH Voltage	V_{CC} – 0.8		V	I_{OH} = 1mA

3841 PGM T04.3

CAPACITANCE T_A = +25°C, f = 1MHz, V_{CC} = 5V

Symbol	Parameter	Max.	Units	Test Conditions
$C_{I/O}$(2)	Input/Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}(2)	Input Capacitance (SCL)	6	pF	V_{IN} = 0V

3836 PGM T05.1

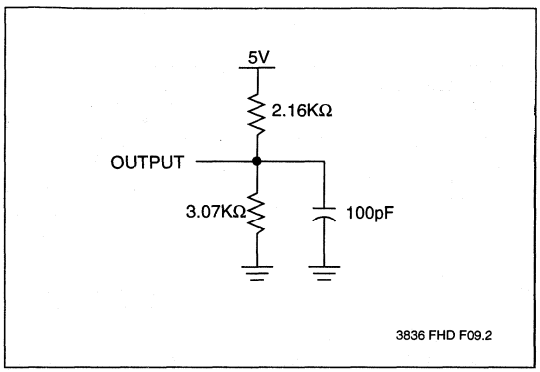
Notes: (1) V_{IL} min. and V_{IH} max. are for reference only and are not tested.
(2) This parameter is periodically sampled and not 100% tested.

POWER-UP TIMING

Symbol	Parameter	Max.	Units
t_{PUR}(3)	Power-up to Read Operation	2	ms
t_{PUW}(3)	Power-up to Write Operation	5	ms

3836 PGM T08

EQUIVALENT A.C. LOAD CIRCUIT



3836 FHD F09.2

A.C. CONDITIONS OF TEST

Input Pulse Levels	V_{CC} x 0.1 to V_{CC} x 0.9
Input Rise and Fall Times	10ns
Input and Output Timing Levels	V_{CC} x 0.5

3836 PGM T06.1

A.C. CHARACTERISTICS (Over the recommended operating conditions unless otherwise specified.)

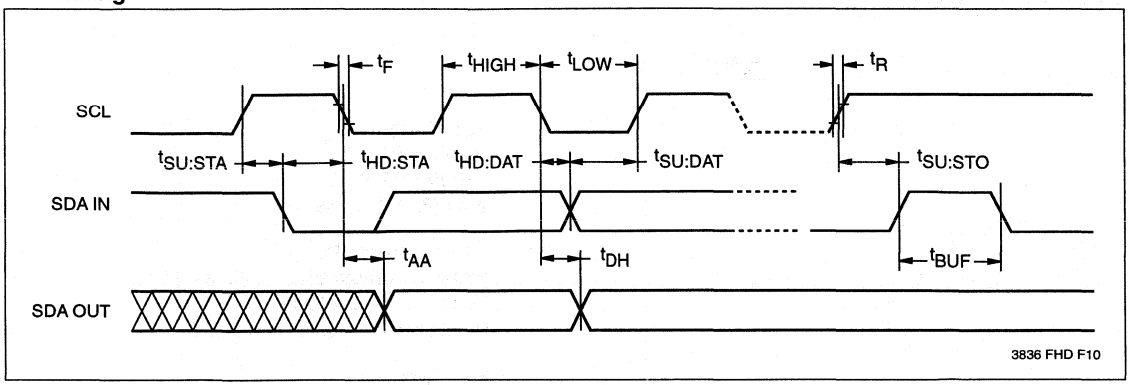
Read & Write Cycle Limits

Symbol	Parameter	Min.	Max.	Units
f_{SCL}	SCL Clock Frequency	0	1	MHz
t_{AA}	SCL LOW to SDA Data Out Valid		350	ns
t_{BUF}	Time the Bus Must Be Free Before a New Transmission Can Start	500		ns
$t_{HD:STA}$	Start Condition Hold Time	250		ns
t_{LOW}	Clock LOW Period	500		ns
t_{HIGH}	Clock HIGH Period	500		ns
$t_{SU:STA}$	Start Condition Setup Time	250		ns
$t_{HD:DAT}$	Data In Hold Time	0		µs
$t_{SU:DAT}$	Data in Setup Time	250		ns
t_R	SDA and SCL Rise Time		1	µs
t_F	SDA and SCL Fall Time		300	ns
$t_{SU:STO}$	Stop Condition Setup Time	250		ns
t_{DH}	Data Out Hold Time	50		ns

3836 PGM T07.1

Note: (3) t_{PUR} and t_{PUW} are the delays required from the time V_{CC} is stable until the specified operation can be initiated. These parameters are periodically sampled and not 100% tested.

Bus Timing

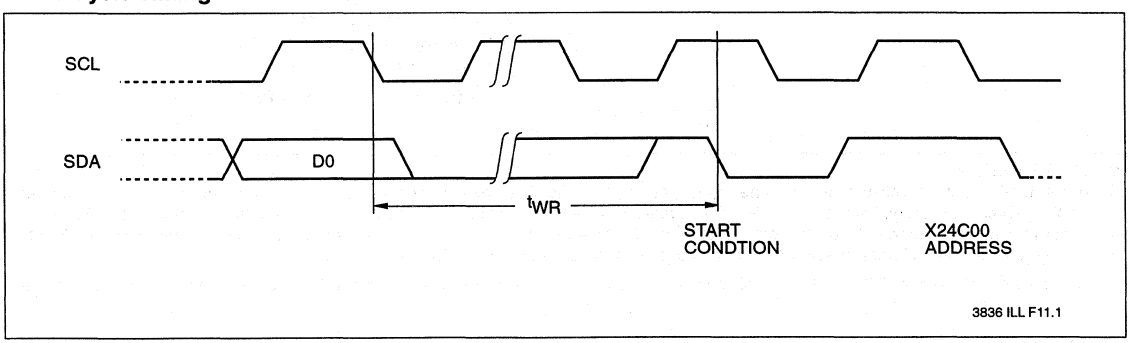


WRITE CYCLE LIMITS

Symbol	Parameter	Min.	Max.	Units
t_{WR}(4)	Write Cycle Time		5	ms

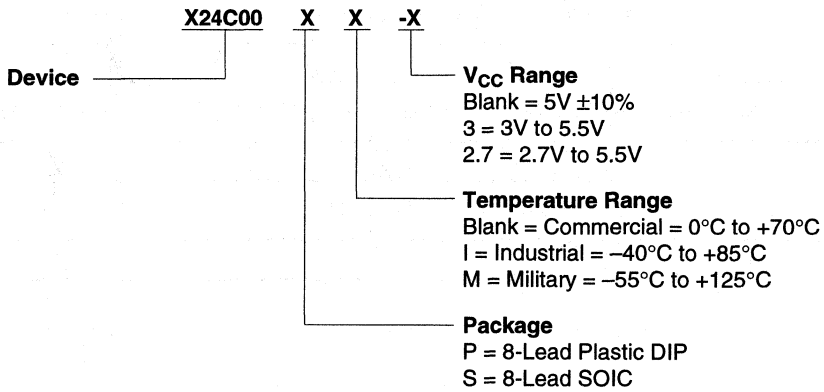
3836 PGM T09

Write Cycle Timing

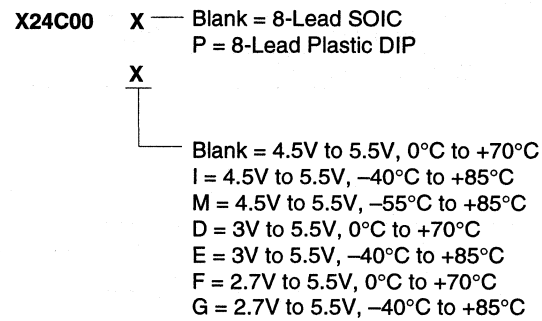


Note: (4) The write cycle time is the time from the initiation of a write sequence to the end of the internal erase/program cycle. During the write cycle, the X24C00 bus interface circuits are disabled, SDA is high impedance, and the device does not respond to start conditions.

ORDERING INFORMATION



Part Mark Convention



Identi™PROM

FEATURES

- 2.7V to 5.5V Power Supply
- 128 Bit Serial E²PROM
- Low Power CMOS
  - —Active Current Less Than 1mA
  - —Standby Current Less Than 50µA
- Internally Organized 16 x 8
- 2 Wire Serial Interface
- High Voltage Programmable Only
  - —V_{PGM}, 12V to 15V
- Push/Pull Output
- High Reliability
  - —Data Retention: 100 Years
- 8-Pin Mini-DIP and 8-Lead SOIC Packages

DESCRIPTION

The X24001 is a CMOS 128 bit serial E²PROM, internally organized as 16 x 8. The X24001 features a serial interface and software protocol allowing operation on a simple two wire bus.

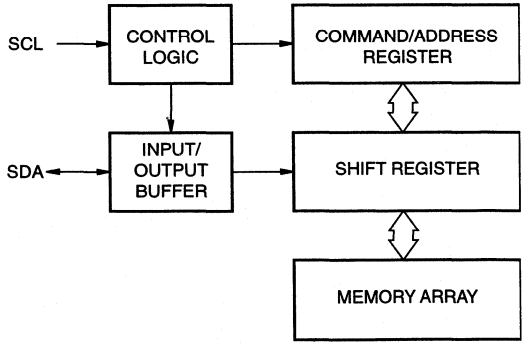
The X24001 is ideally suited for identification applications such as serial numbers or device revision numbers which need to be stored and retrieved electronically.

V_{PGM} is used to enable writes to the device. This provides full protection of the data in the user's environment where V_{PGM} is not available.

Xicor E²PROMs are designed and tested for applications requiring extended endurance. Inherent data retention is greater than 100 years.

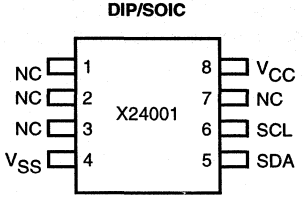
The X24001 is fabricated with Xicor's Advanced CMOS Floating Gate technology.

FUNCTIONAL DIAGRAM



3830 FHD F01

PIN CONFIGURATION



3830 FHD F02

IDENTI™ PROM is a trademark of Xicor, Inc.

3830-1.4 11/30/95 T0/C2/D2 NS

PIN DESCRIPTIONS

Serial Clock (SCL)

The SCL input is used to clock all data into and out of the device.

Serial Data (SDA)

SDA is a bidirectional pin used to transfer data into and out of the device. It is a push/pull output and does not require the use of a pull-up resistor. During the programming operation, SDA is an input.

PIN NAMES

Symbol	Description
NC	No Connect
V_{SS}	Ground
V_{CC}	Supply Voltage
SDA	Serial Data
SCL	Serial Clock

3830 PGM T01

DEVICE OPERATION

The X24001 supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is a master and the device being controlled is the slave. The master will always initiate data transfers and provide the clock for both transmit and receive operations. Therefore, the X24001 will be considered a slave in all applications.

Clock and Data Conventions

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions. Refer to Figures 1 and 2.

Start Condition

All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The X24001 continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

A start may be issued to terminate the input of a control word or the input of data to be written. This will reset the device and leave it ready to begin a new read or write command. Because of the push/pull output, a start cannot be generated while the part is outputting data. Starts are also inhibited while a write is in progress.

Stop Condition

The stop condition is a LOW to HIGH transition of SDA when SCL is HIGH. The stop condition is used to reset the device during a command or data input sequence and will leave the device in the standby mode. As with starts, stops are inhibited when outputting data and while a write is in progress.

Figure 1. Data Validity

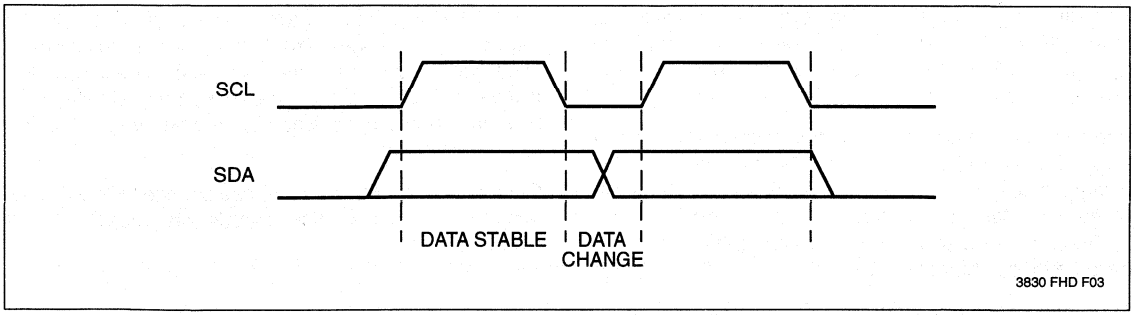
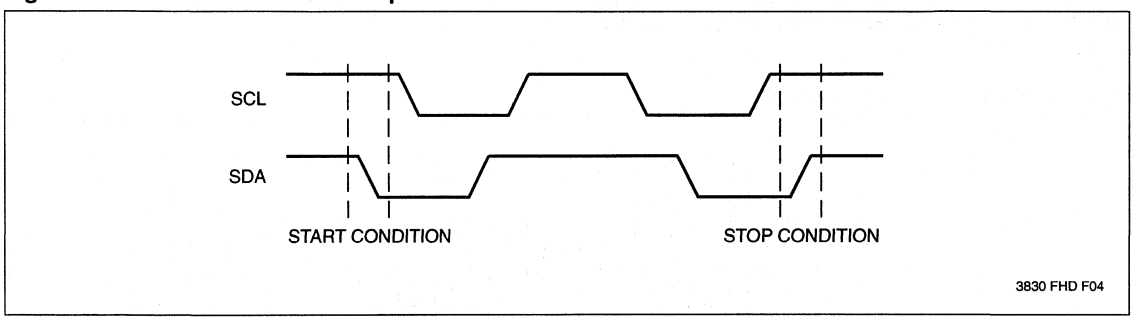


Figure 2. Definition of Start and Stop Conditions



Programming Operation

Programming of the X24001 is performed one byte at a time. After each byte is written, a delay equal to the write cycle time of 5ms must be observed before initiating the next write cycle.

The sequence of operations is: first raise the SCL pin to V_{PGM} and generate a HIGH to LOW transition of SDA (programming mode start). This is followed by eight bits of data containing the program command bits, four address bits and two don't care bits, immediately followed by the 8-bit data byte.

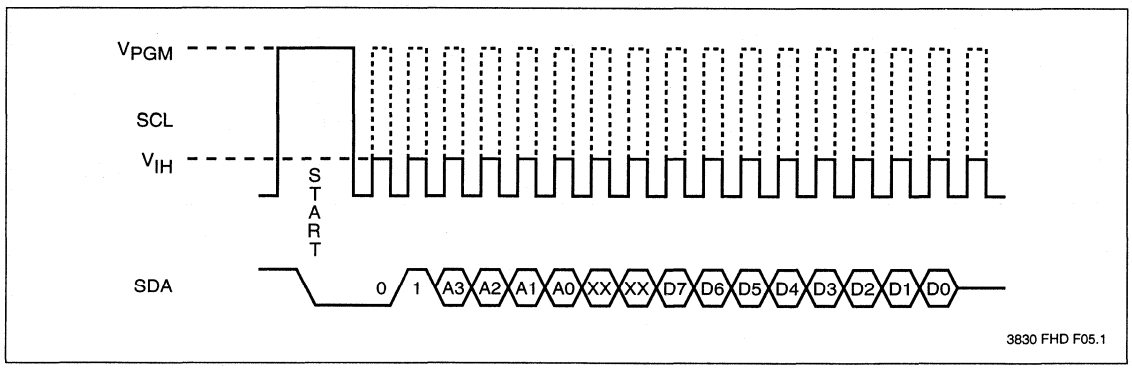
The timing of the operation conforms to the standard A.C. timing requirements and follows the sequence shown below. After generating the Programming Mode start condition the SCL HIGH level can be either V_{IH} or V_{PGM}.

Factory Programming Service

The X24001 can be programmed with customer specific data prior to shipment. The data programmed can be in two forms: static data pattern where there is no change in the data in a group of devices or sequential data, such as a base number incremented by one for each device tested and shipped.

Customers requiring one of these services should contact their local sales office for ordering procedures and service charges.

Figure 3. Programming Sequence

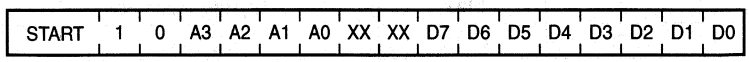


Read Operation

The byte read operation is initiated with a start condition. The start condition is followed by an eight-bit control byte which consists of a two-bit read command (1,0), four address bits, and two "don't care" bits. After receipt of the control byte, the X24001 will enter the read mode and transfer data into the shift register from the array. This data is shifted out of the device on the next eight SCL clocks. At the end of the read, all counters are reset and the X24001 will enter the standby mode. As with a write, the read operation can be interrupted by a start or stop condition while the command or address is being clocked in. While clocking data out, starts or stops cannot be generated.

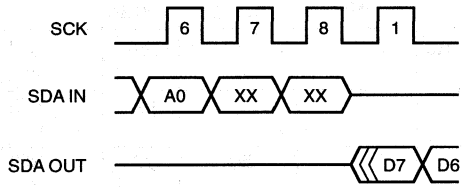
During the second don't care clock cycle, starts and stops are ignored. The master must free the bus prior to the end of this clock cycle to allow the X24001 to begin outputting data (Figures 4 and 5).

Figure 4. Read Sequence



3830 FHD F06

Figure 5. Read Cycle Timing



3830 FHD F07

SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

ABSOLUTE MAXIMUM RATINGS*

Temperature under Bias
X24001 ..... –65°C to +135°C
Storage Temperature ..... –65°C to +150°C
Voltage on any Pin with
Respect to V_{SS} ..... –1V to +7V
Voltage on SCL with
Respect to V_{SS} ..... –1V to +17V
D.C. Output Current 5mA
Lead Temperature
(Soldering, 10 seconds) ..... 300°C

***COMMENT**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	+70°C
Industrial	–40°C	+85°C
Military	–55°C	+125°C

3830 PGM T02.1

Supply Voltage	Limits
X24001	5V ±10%
X24001-3	3V to 5.5V
X24001-2.7	2.7V to 5.5V

3830 PGM T03.1

D.C. OPERATING CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
I_{CC1}	V_{CC} Supply Current Read		1	mA	SCL = V_{CC} x 0.1/V_{CC} x 0.9 Levels @ 1MHz, SDA = Open
I_{SB1}	V_{CC} Standby Current		100	µA	SCL = SDA = V_{CC} V_{CC} = 5V ±10%
I_{SB2}	V_{CC} Standby Current		50	µA	SCL = SDA = V_{CC} V_{CC} = 3V
I_{LI}	Input Leakage Current		10	µA	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output Leakage Current		10	µA	V_{OUT} = V_{SS} to V_{CC}
V_{IL}(1)	Input LOW Voltage	–1.0	V_{CC} x 0.3	V	
V_{IH}(1)	Input HIGH Voltage	V_{CC} x 0.7	V_{CC} + 0.5	V	
V_{OL}	Output LOW Voltage		0.4	V	I_{OL} = 2.1mA
V_{OH}	Output HIGH Voltage	V_{CC} – 0.8		V	I_{OH} = 1mA
V_{PGM}	Program Enable Voltage	12	15	V	

3830 PGM T04.3

CAPACITANCE T_A = +25°C, f = 1MHz, V_{CC} = 5V

Symbol	Parameter	Max.	Units	Test Conditions
$C_{I/O}$(2)	Input/Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}(2)	Input Capacitance (SCL)	6	pF	V_{IN} = 0V

3830 PGM T05.1

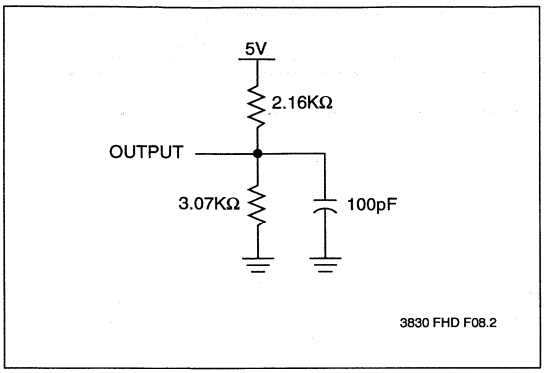
Notes: (1) V_{IL} min. and V_{IH} max. are for reference only and are not tested.
(2) This parameter is periodically sampled and not 100% tested.

POWER-UP TIMING

Symbol	Parameter	Max.	Units
t_{PUR}[3]	Power-up to Read Operation	2	ms
t_{PUW}[3]	Power-up to Write Operation	5	ms

3830 PGM T06

EQUIVALENT A.C. LOAD CIRCUIT



3830 FHD F08.2

A.C. CONDITIONS OF TEST

Input Pulse Levels	V_{CC} x 0.1 to V_{CC} x 0.9
Input Rise and Fall Times	10ns
Input and Output Timing Levels	V_{CC} x 0.5

3830 PGM T07.1

2

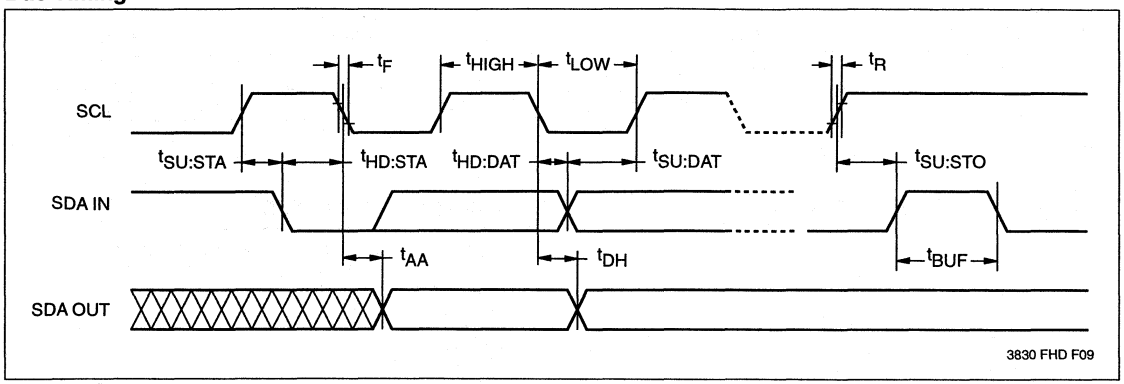
A.C. CHARACTERISTICS (Over the recommended operating conditions unless otherwise specified.)

Read & Write Cycle Limits

Symbol	Parameter	Min.	Max.	Units
f_{SCL}	SCL Clock Frequency	0	1	MHz
t_{AA}	SCL LOW to SDA Data Out Valid		350	ns
t_{BUF}	Time the Bus Must Be Free Before a New Transmission Can Start	500		ns
$t_{HD:STA}$	Start Condition Hold Time	250		ns
t_{LOW}	Clock LOW Period	500		ns
t_{HIGH}	Clock HIGH Period	500		ns
$t_{SU:STA}$	Start Condition Setup Time	250		ns
$t_{HD:DAT}$	Data In Hold Time	0		µs
$t_{SU:DAT}$	Data in Setup Time	250		ns
t_R	SDA and SCL Rise Time		1	µs
t_F	SDA and SCL Fall Time		300	ns
$t_{SU:STO}$	Stop Condition Setup Time	250		ns
t_{DH}	Data Out Hold Time	50		ns

3830 PGM T08.1

Bus Timing

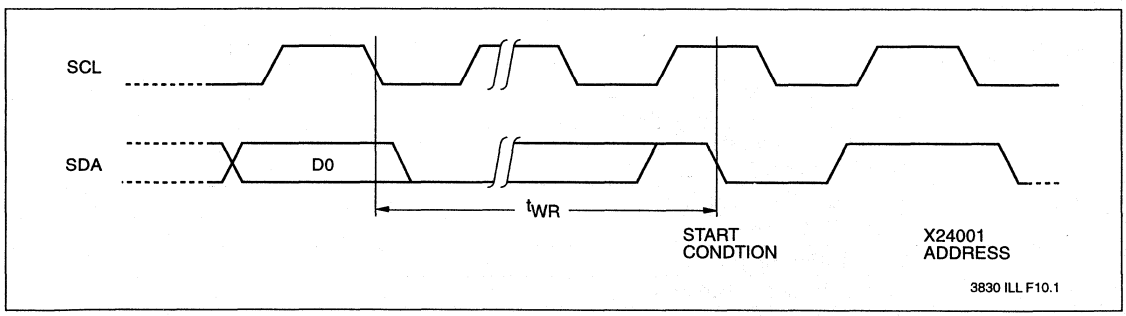


WRITE CYCLE LIMITS

Symbol	Parameter	Min.	Max.	Units
t_{WR}(4)	Write Cycle Time		5	ms

3830 PGM T09

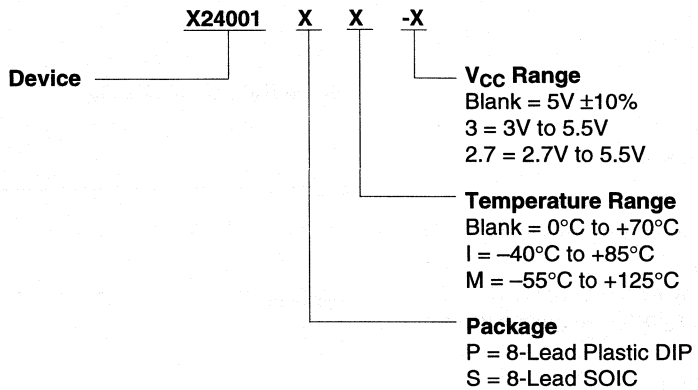
Write Cycle Timing



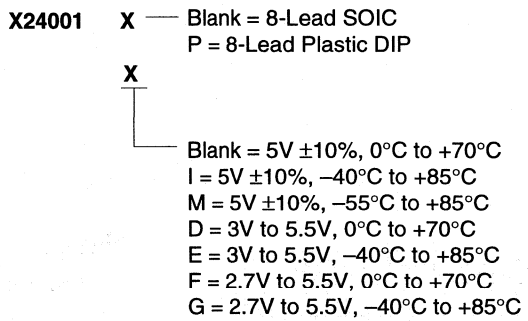
Note: (3) t_{PUR} and t_{PUW} are the delays required from the time V_{CC} is stable until the specified operation can be initiated. These parameters are periodically sampled and not 100% tested.

(4) The write cycle time is the time from the initiation of a write sequence to the end of the internal erase/program cycle. During the write cycle, the X24001 bus interface circuits are disabled, SDA is high impedance, and the device does not respond to start conditions.

ORDERING INFORMATION



Part Mark Convention



X24001 PROGRAMMING ORDER INFORMATION

Customer Name: .....

Address: .....

.....

.....

Complete Device Part Number: .....

☐ Static Pattern
Fill in matrix A below

☐ Incrementing Pattern
Indicate in Matix A any static pattern and indicate in Matrix B beginning sequence value to be incremented.

☐ Totally Random Pattern

AUTHORIZATION

Programming Information Supplied By

_____
Print or Type Clearly Full Name

_____
Title

_____
Signature **Date**

Matrix A

Address	Data Pattern MSB First							
	7	6	5	4	3	2	1	0
0								
1								
2								
3								
4								
5								
6								
7								
8								
9								
A								
B								
C								
D								
E								
F								

Matrix B

Address	Data Pattern MSB First							
	7	6	5	4	3	2	1	0
0								
1								
2								
3								
4								
5								
6								
7								
8								
9								
A								
B								
C								
D								
E								
F								

Advanced 2-Wire Serial E²PROM with Block Lock™ Protection

FEATURES

- 2.7V to 5.5V Power Supply
- Low Power CMOS
  - —Active Read Current Less Than 1mA
  - —Active Write Current Less Than 3mA
  - —Standby Current Less Than 1μA
- Internally Organized 2048 x 8
- New Programmable Block Lock Protection
  - —Software Write Protection
  - —Programmable Hardware Write Protect
- Block Lock (0, 1/4, 1/2, or all of the E²PROM array)
- 2 Wire Serial Interface
- Bidirectional Data Transfer Protocol
- 32 Byte Page Write Mode
  - —Minimizes Total Write Time Per Byte
- Self Timed Write Cycle
  - —Typical Write Cycle Time of 5ms
- High Reliability
  - —Endurance: 100,000 Cycles
  - —Data Retention: 100 Years
- Available Packages
  - —8-Lead Mini-DIP
  - —8-Lead SOIC (JEDEC)
  - —14-Lead TSSOP

DESCRIPTION

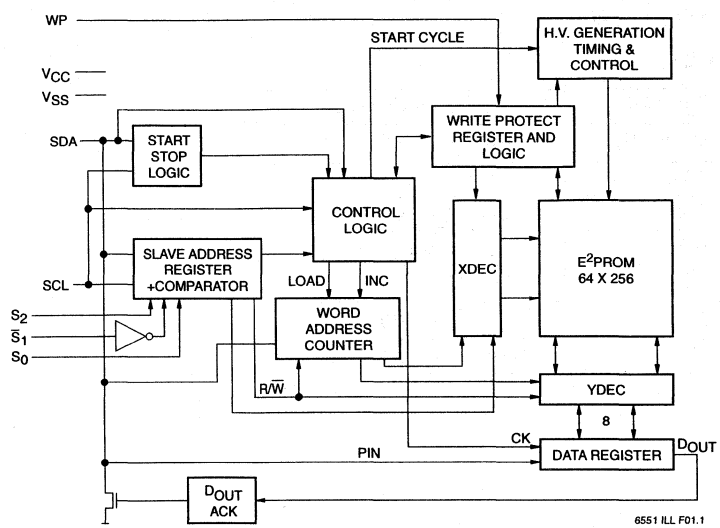
The X24165 is a CMOS 16,384 bit serial E²PROM, internally organized 2048 x 8. The X24165 features a serial interface and software protocol allowing operation on a simple two wire bus.

Three device select inputs (S_0, $\overline{S}_1$, S_2) allow up to eight devices to share a common two wire bus.

A Write Protect Register at the highest address location, 7FFh, provides three new write protection features: Software Write Protect, Block Write Protect, and Hardware Write Protect. The Software Write Protect feature prevents any nonvolatile writes to the X24165 until the WEL bit in the write protect register is set. The Block Write Protection feature allows the user to individually write protect four blocks of the array by programming two bits in the write protect register. The Programmable Hardware Write Protect feature allows the user to install the X24165 with WP tied to V_{CC}, program the entire memory array in place, and then enable the hardware write protection by programming a WPEN bit in the write protect register. After this, selected blocks of the array, including the write protect register itself, are permanently write protected.

Xicor E²PROMs are designed and tested for applications requiring extended endurance. Inherent data retention is greater than 100 years.

FUNCTIONAL DIAGRAM



PIN DESCRIPTIONS

Serial Clock (SCL)

The SCL input is used to clock all data into and out of the device.

Serial Data (SDA)

SDA is a bidirectional pin used to transfer data into and out of the device. It is an open drain output and may be wire-ORed with any number of open drain or open collector outputs.

An open drain output requires the use of a pull-up resistor. For selecting typical values, refer to the Pull-Up Resistor selection graph at the end of this data sheet.

Device Select (S0, $\overline{S}_1$, S_2)

The device select inputs (S0, $\overline{S}_1$, S_2) are used to set the first three bits of the 8-bit slave address. This allows up to eight X24165's to share a common bus. These inputs can be static or actively driven. If used statically they must be tied to V_{SS} or V_{CC} as appropriate. If actively driven, they must be driven with CMOS levels (driven to V_{CC} or V_{SS}).

Write Protect (WP)

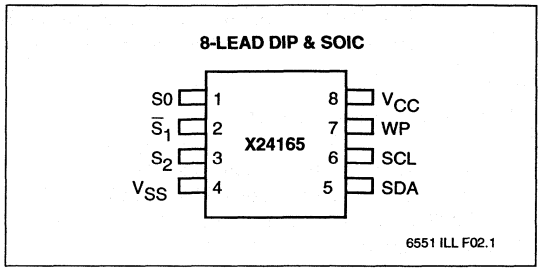
The write protect input controls the hardware write protect feature. When held LOW, hardware write protection is disabled and the X24165 can be written normally. When this input is held HIGH, and the WPEN bit in the write protect register is set HIGH, write protection is enabled, and nonvolatile writes are disabled to the selected blocks as well as the write protect register itself.

PIN NAMES

Symbol	Description
S0, $\overline{S}_1$, S_2	Device Select Inputs
SDA	Serial Data
SCL	Serial Clock
WP	Write Protect
V_{SS}	Ground
V_{CC}	Supply Voltage
NC	No Connect

6551 FRM T01.1

PIN CONFIGURATION



DEVICE OPERATION

The X24165 supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter, and the receiving device as the receiver. The device controlling the transfer is a master and the device being controlled is the slave. The master will always initiate data transfers, and provide the clock for both transmit and receive operations. Therefore, the X24165 will be considered a slave in all applications.

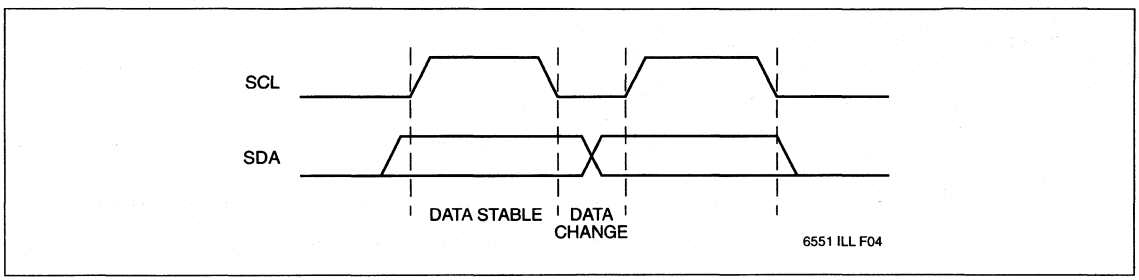
Clock and Data Conventions

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions. Refer to Figures 1 and 2.

Start Condition

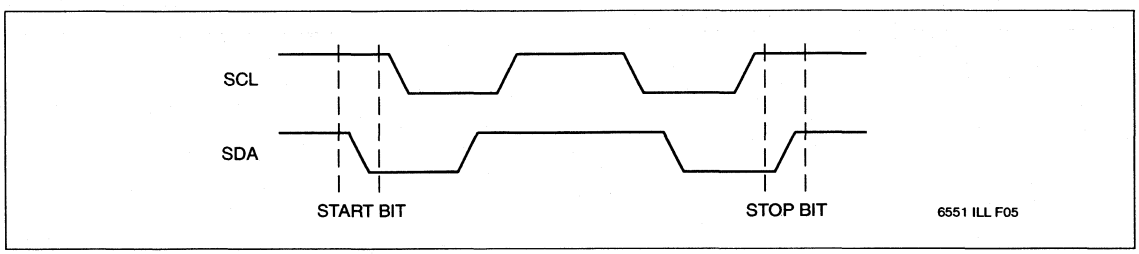
All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The X24165 continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

Figure 1. Data Validity



Notes: (5) Typical values are for $T_A = 25°C$ and nominal supply voltage (5V)
(6) t_{WR} is the minimum cycle time from the system perspective when polling techniques are not used. It is the maximum time the device requires to perform the internal write operation.

Figure 2. Definition of Start and Stop



Stop Condition

All communications must be terminated by a stop condition, which is a LOW to HIGH transition of SDA when SCL is HIGH. The stop condition is also used to place the device into the standby power mode after a read sequence. A stop condition can only be issued after the transmitting device has released the bus.

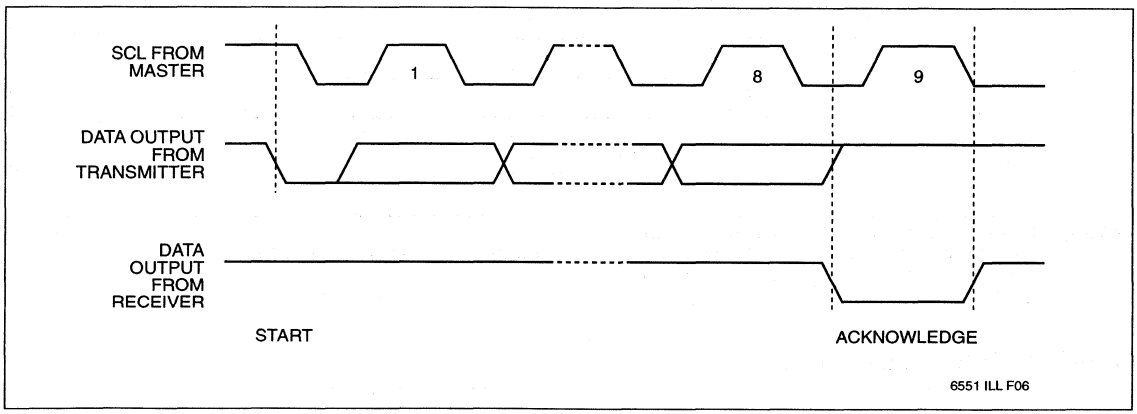
Acknowledge

Acknowledge is a software convention used to indicate successful data transfer. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data. Refer to Figure 3.

The X24165 will respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a write operation have been selected, the X24165 will respond with an acknowledge after the receipt of each subsequent eight-bit word.

In the read mode the X24165 will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the X24165 will continue to transmit data. If an acknowledge is not detected, the X24165 will terminate further data transmissions. The master must then issue a stop condition to return the X24165 to the standby power mode and place the device into a known state.

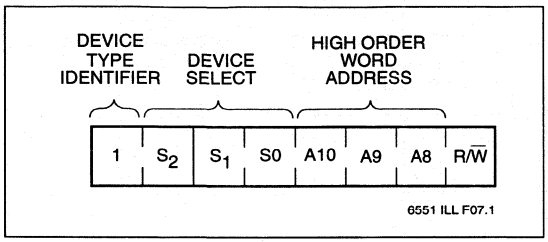
Figure 3. Acknowledge Response From Receiver



DEVICE ADDRESSING

Following a start condition the master must output the address of the slave it is accessing (see Figure 4). The next three bits are the device select bits. A system could have up to eight X24165's on the bus. The eight addresses are defined by the state of the S0, $\overline{S_1}$ and S_2 inputs. S_1 of the slave address must be the inverse of the $\overline{S_1}$ input pin.

Figure 4. Slave Address



The next three bits of the slave address are an extension of the array's address and are concatenated with the eight bits of address in the word address field, providing direct access to the whole 2048 x 8 array.

The last bit of the slave address defines the operation to be performed. When set HIGH a read operation is selected, when set LOW a write operation is selected.

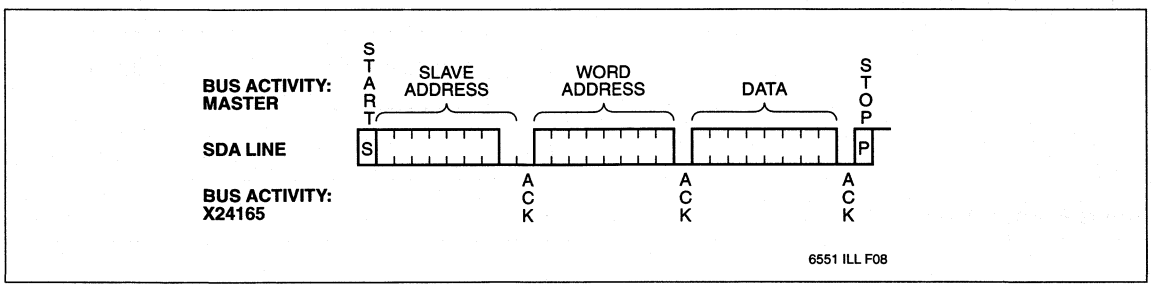
Following the start condition, the X24165 monitors the SDA bus comparing the slave address being transmitted with its slave address device type identifier. Upon a correct compare the X24165 outputs an acknowledge on the SDA line. Depending on the state of the R/$\overline{W}$ bit, the X24165 will execute a read or write operation.

WRITE OPERATIONS

Byte Write

For a write operation, the X24165 requires a second address field. This address field is the word address, comprised of eight bits, providing access to any one of 2048 words in the array. Upon receipt of the word address, the X24165 responds with an acknowledge and awaits the next eight bits of data, again responding with an acknowledge. The master then terminates the transfer by generating a stop condition, at which time the X24165 begins the internal write cycle to the nonvolatile memory. While the internal write cycle is in progress the X24165 inputs are disabled, and the device will not respond to any requests from the master. Refer to Figure 5 for the address, acknowledge and data transfer sequence.

Figure 5. Byte Write



Page Write

The X24165 is capable of a 32 byte page write operation. It is initiated in the same manner as the byte write operation, but instead of terminating the write cycle after the first data word is transferred, the master can transmit up to fifteen more words. After the receipt of each word, the X24165 will respond with an acknowledge.

After the receipt of each word, the five low order address bits are internally incremented by one. The high order bits of the word address remain constant. If the master should transmit more than 32 words prior to generating the stop condition, the address counter will "roll over" and the previously written data will be overwritten. As with the byte write operation, all inputs are disabled until completion of the internal write cycle. Refer to Figure 6 for the address, acknowledge and data transfer sequence.

Acknowledge Polling

The 10ms Max Write Cycle Time (5ms Typical) can be significantly reduced using Acknowledge Polling. To initiate Acknowledge Polling, the master issues a start condition followed by the Slave Address Byte for a write or read operation. If the device is still busy with the high voltage cycle, then no ACK will be returned. If the device has completed the write operation, an ACK will be returned and the host can then proceed with the read or write operation. Refer to Flow 1.

Flow 1. ACK Polling Sequence

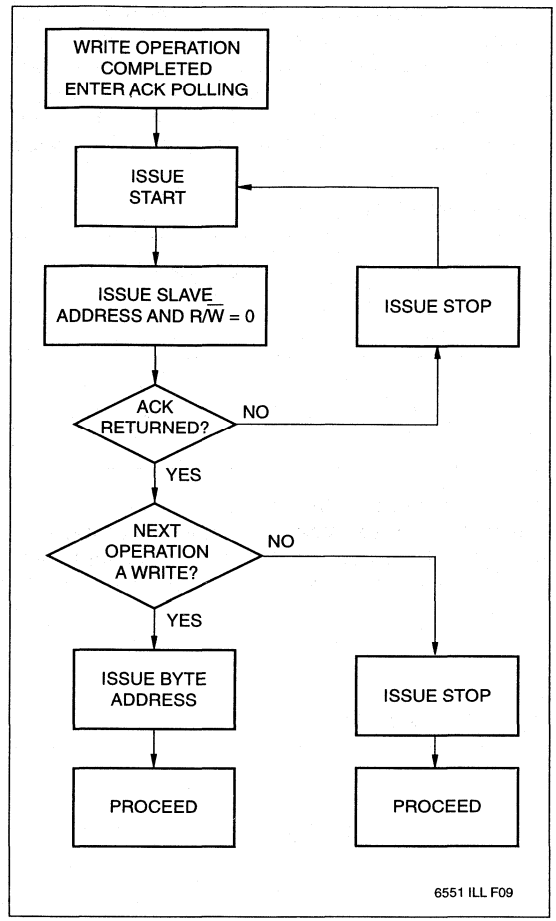
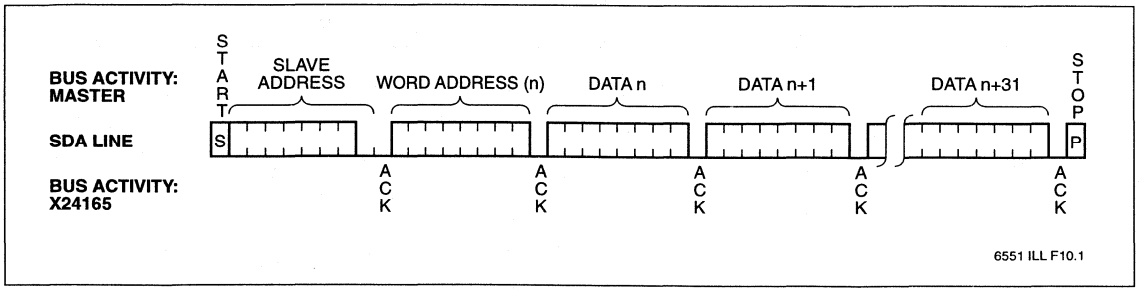


Figure 6. Page Write



READ OPERATIONS

Read operations are initiated in the same manner as write operations with the exception that the R/$\overline{W}$ bit of the slave address is set HIGH. There are three basic read operations: current address read, random read and sequential read.

It should be noted that the ninth clock cycle of the read operation is not a "don't care." To terminate a read operation, the master must either issue a stop condition during the ninth cycle or hold SDA HIGH during the ninth clock cycle and then issue a stop condition.

Current Address Read

Internally the X24165 contains an address counter that maintains the address of the last word read, incremented by one or the exact address of the last word written. Therefore, if the last access read was to address n, the next read operation would access data from address n + 1. Upon receipt of the slave address with the R/$\overline{W}$ set HIGH, the X24165 issues an acknowledge and transmits the eight-bit word. The read operation is terminated by the master; by not responding with an acknowledge and by issuing a stop condition. Refer to Figure 7 for the sequence of address, acknowledge and data transfer.

Random Read

Random read operations allow the master to access any memory location in a random manner. Prior to issuing the slave address with the R/$\overline{W}$ bit set HIGH, the master must first perform a "dummy" write operation. The master issues the start condition, and the slave address with the R/$\overline{W}$ bit set LOW, followed by the word address it is to read. After the word address acknowledge, the master immediately reissues the start condition and the slave address with the R/$\overline{W}$ bit set HIGH. This will be followed by an acknowledge from the X24165 and then by the eight-bit word. The read operation is terminated by the master; by not responding with an acknowledge and by issuing a stop condition. Refer to Figure 8 for the address, acknowledge and data transfer sequence.

Figure 7. Current Address Read

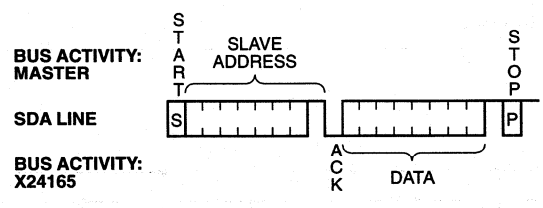
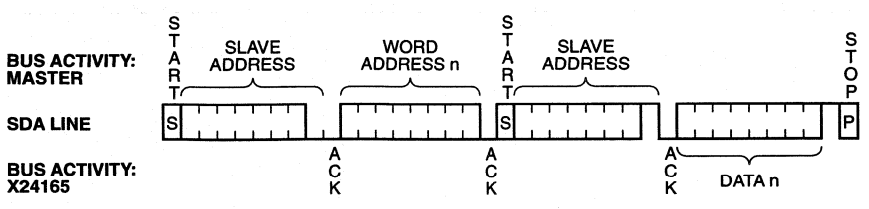


Figure 8. Random Read



Sequential Read

Sequential reads can be initiated as either a current address read or random access read. The first word is transmitted as with the other modes, however, the master now responds with an acknowledge, indicating it requires additional data. The X24165 continues to output data for each acknowledge received. The read operation is terminated by the master; by not responding with an acknowledge and then issuing a stop condition.

The data output is sequential, with the data from address n followed by the data from n + 1. The address counter for read operations increments all address bits, allowing the entire memory contents to be serially read during one operation. At the end of the address space (address 2047), the counter "rolls over" to 0 and the X24165 continues to output data for each acknowledge received. Refer to Figure 9 for the address, acknowledge and data transfer sequence.

Figure 9. Sequential Read

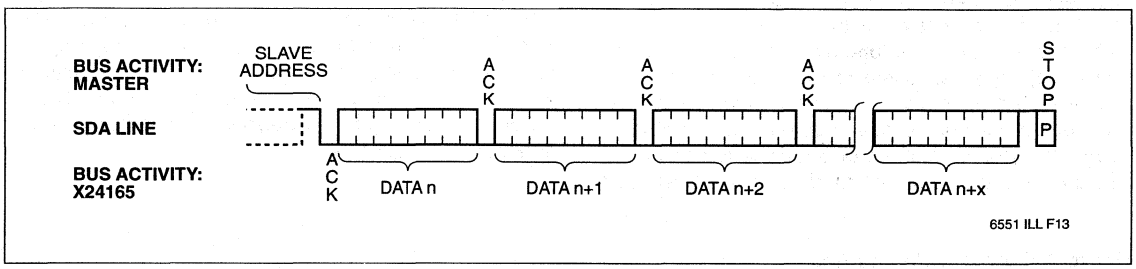
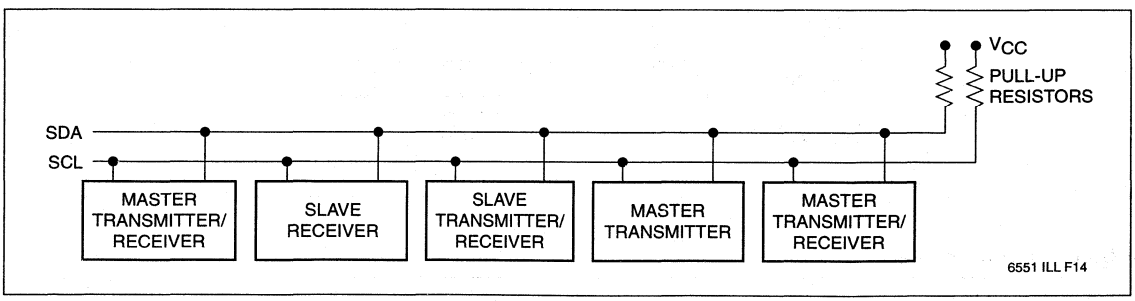


Figure 10. Typical System Configuration



WRITE PROTECT REGISTER

The Write Protect Register (WPR) is located at the highest address, 7FFh.

Figure 11. Write Protect Register

WPR (Addr = 7FFh)

7	6	5	4	3	2	1	0
WPEN	0	0	BP1	BP0	RWEL	WEL	0

6551 ILL F15.1

WPR.1 = WEL
- Write Enable Latch (Volatile)
  0 = Write enable latch reset, writes disabled
  1 = Write enable latch set, writes enabled

If WEL = 0 then "no ACK" after first byte of input data.

WPR.2 = RWEL
- Register Write Enable Latch (Volatile)
  0 = Register write enable latch reset, writes disabled
  1 = Register write enable latch set, writes enabled

WPR.3, WPR.4 = BP0, BP1
- Block Protect Bits (Nonvolatile)

(See Block Protect section for definition)

WPR.7 = WPEN
- Write Protect Enable Bit (Nonvolatile)

(See Hardware Write Protect section for definition)

Writing to the Write Protect Register

The Write Protect Register is written by performing a random write of one byte directly to address, 7FFh. If a page write is performed starting with any address other than 7FFh, the byte in the array at address 7FFh will be written instead of the Write Protect Register (assuming writes are not disabled by the block protect register).

The state of the Write Protect Register can be read by performing a random read at address 7FFh at any time. If a sequential read starting at any other address than 7FFh is performed, the contents of the byte in the array at 7FFh is read out instead of the Write Protect Register.

WEL and RWEL are volatile latches that power-up in the LOW (disabled) state. A write to any address other than 7FFh, where the Write Protect Register is located, will be ignored (no ack) until the WEL bit is set HIGH. The WEL bit is set by writing 0000001x to address 7FFh. Once set, WEL remains HIGH until either reset (by writing 00000000 to 7FFh) or until the part powers-up again. The RWEL bit controls writes to the block protect bits. RWEL is set by first setting WEL = 1 and then writing 0000011x to address 7FFh. RWEL must be set in order to change the block protect bits, BP0 and BP1, or the WPEN bit. RWEL is reset when the block protect or WPEN bits are changed, or when the part powers-up again.

Programming the BP or WPEN Bits

A three step sequence is required to change the nonvoltaile Block Protect or Write Protect Enable:

1) Set WEL = 1 (write 00000010 to address 7FFh, volatile write cycle)

(Start)

2) Set RWEL = 1 (write 00000110 to address 7FFh, volatile write cycle)

(Start)

3) Set BP1, BP0, and/or WPEN bits (Write w00yz010 to address 7FFh)

w = WPEN, y = BP1, Z = BP0,

(Stop)

Step 3 is a nonvolatile write cycle, requiring 10ms to complete. RWEL is reset (0) by this write cycle, requiring another write cycle to set RWEL again before the block protect bits can be changed. RWEL must be 0 in step 3; if w00yz110 is written to address 7FFh, RWEL is set but WPEN, BP1 and BP0 are not changed (the device remains at step 2).

Block Protect Bits

The Block Protect Bits BP0 and BP1 determine which blocks of the memory are write-protected:

Table 1. Block Protect Bits

BP1	BP0	Protected Addresses	
0	0	None	
0	1	600h–7FFh	Upper 1/4
1	0	400h–7FFh	Upper 1/2
1	1	0000h–7FFh	Full Array (WPR not included)

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Programmable Hardware Write Protect

The Write Protect (WP) pin and the Write Protect Enable (WPEN) bit in the Write Protect Register control the programmable hardware write protect feature. Hardware write protection is enabled when the WP pin and the WPEN bit are both HIGH, and disabled when either the WP pin is LOW or the WPEN bit is LOW. When the chip is hardware write-protected, nonvolatile writes are disabled to the Write Protect Register, including the BP bits and the WPEN bit itself, as well as to block-protected sections in the memory array. Only the sections of the memory array that are not block-protected can be written. Note that since the WPEN bit is write-protected, it cannot be changed back to a LOW state, and write protection is disabled as long as the the WP pin is held HIGH. Table 2 defines the write protection status for each state of WPEN and WP.

Table 2. Write Protect Status Table

WP	WPEN	Memory Array (Not Block Protected)	Memory Array (Block Protected)	BP Bits	WPEN Bit
0	X	Writable	Protected	Writable	Writable
X	0	Writable	Protected	Writable	Writable
1	1	Writable	Protected	Protected	Protected

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ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias
X24165 ..... –65°C to +135°C
Storage Temperature ..... –65°C to +150°C
Voltage on any Pin with
Respect to V_{SS} ..... –1V to +7V
D.C. Output Current 5mA
Lead Temperature (Soldering, 10 Seconds) ..... 300°C

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2

RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	+70°C
Industrial	–40°C	+85°C
Military	–55°C	+125°C

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Supply Voltage	Limits
X24165	4.5V to 5.5V
X24165-2.7	2.7V to 5.5V

6551 FRM T05

D.C. OPERATING CHARACTERISTICS

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
I_{CC1}	V_{CC} Supply Current (Read)		1	mA	SCL = V_{CC} X 0.1/V_{CC} X 0.9 Levels @ 100KHz, SDA = Open, All Other Inputs = V_{SS} or V_{CC} – 0.3V
I_{CC2}	V_{CC} Supply Current (Write)		3	mA	
I_{SB1}(1)	V_{CC} Standby Current		50	µA	SCL = SDA = V_{CC}, All Other Inputs = V_{SS} or V_{CC} – 0.3V, V_{CC} = 5V ± 10%
I_{SB2}(1)	V_{CC} Standby Current		1	µA	SCL = SDA = V_{CC}, All Other Inputs = V_{SS} or V_{CC} – 0.3V, V_{CC} = 2.7V
I_{LI}	Input Leakage Current		10	µA	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output Leakage Current		10	µA	V_{OUT} = V_{SS} to V_{CC}
V_{IL}(2)	Input LOW Voltage	–1	V_{CC} x 0.3	V	
V_{IH}(2)	Input HIGH Voltage	V_{CC} x 0.7	V_{CC} + 0.5	V	
V_{OL}	Output LOW Voltage		0.4	V	I_{OL} = 3mA, V_{CC} = 4.5V

6551 FRM T06.1

CAPACITANCE T_A = +25°C, f = 1MHz, V_{CC} = 5V

Symbol	Parameter	Max.	Units	Test Conditions
$C_{I/O}$(3)	Input/Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}(3)	Input Capacitance (S_1, $\overline{S}_2$, SCL)	6	pF	V_{IN} = 0V

6551 FRM T07.1

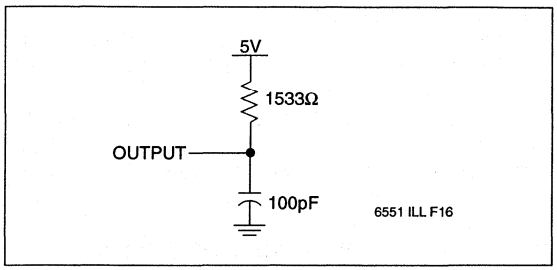
Notes: (1) Must perform a stop command prior to measurement.
(2) V_{IL} min. and V_{IH} max. are for reference only and are not 100% tested.
(3) This parameter is periodically sampled and not 100% tested.

A.C. CONDITIONS OF TEST

Input Pulse Levels	V_{CC} x 0.1 to V_{CC} x 0.9
Input Rise and Fall Times	10ns
Input and Output Timing Levels	V_{CC} X 0.5

6551 FRM T08.1

EQUIVALENT A.C. LOAD CIRCUIT



A.C. OPERATING CHARACTERISTICS (Over the recommended operating conditions, unless otherwise specified.)

Read & Write Cycle Limits

Symbol	Parameter	Min.	Max.	Units
f_{SCL}	SCL Clock Frequency	0	100	KHz
T_I	Noise Suppression Time Constant at SCL, SDA Inputs		100	ns
t_{AA}	SCL LOW to SDA Data Out Valid	0.3	3.5	µs
t_{BUF}	Time the Bus Must Be Free Before a New Transmission Can Start	4.7		µs
$t_{HD:STA}$	Start Condition Hold Time	4		µs
t_{LOW}	Clock LOW Period	4.7		µs
t_{HIGH}	Clock HIGH Period	4		µs
$t_{SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	4.7		µs
$t_{HD:DAT}$	Data In Hold Time	0		µs
$t_{SU:DAT}$	Data In Setup Time	250		ns
t_R	SDA and SCL Rise Time		1	µs
t_F	SDA and SCL Fall Time		300	ns
$t_{SU:STO}$	Stop Condition Setup Time	4.7		µs
t_{DH}	Data Out Hold Time	300		ns

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POWER-UP TIMING(4)

Symbol	Parameter	Max.	Units
t_{PUR}	Power-up to Read Operation	1	ms
t_{PUW}	Power-up to Write Operation	5	ms

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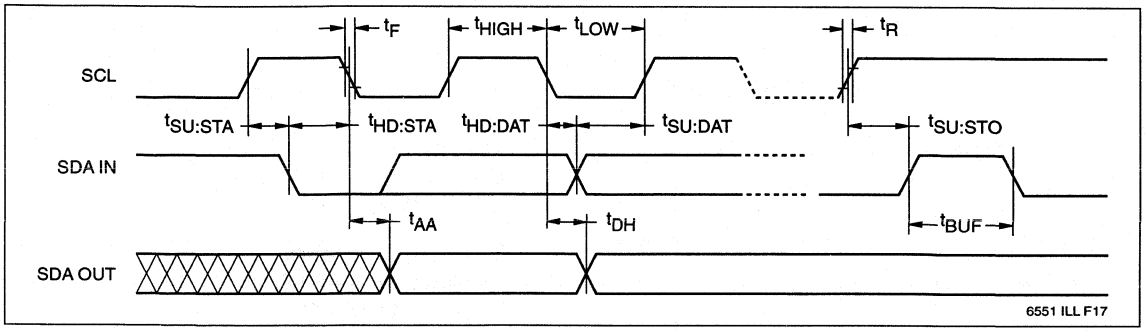
Notes: (4) t_{PUR} and t_{PUW} are the delays required from the time V_{CC} is stable until the specified operation can be initiated. These parameters are periodically sampled and not 100% tested.

Bus Timing



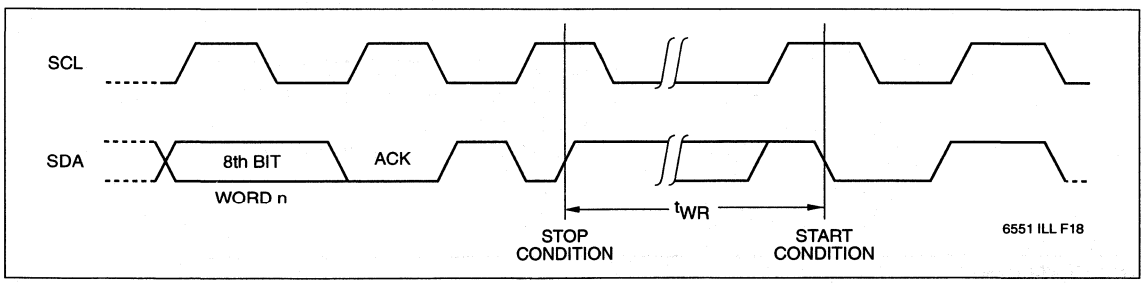
Write Cycle Limits

Symbol	Parameter	Min.	Typ.(5)	Max.	Units
t_{WR}(6)	Write Cycle Time		5	10	ms

6551 FRM T11.1

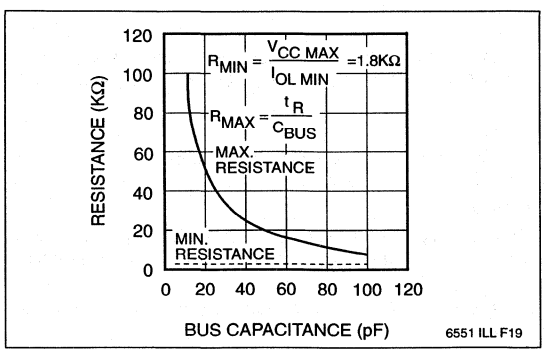
The write cycle time is the time from a valid stop condition of a write sequence to the end of the internal erase/program cycle. During the write cycle, the X24165 bus interface circuits are disabled, SDA is allowed to remain HIGH, and the device does not respond to its slave address.

Bus Timing



Notes: (5) Typical values are for $T_A = 25°C$ and nominal supply voltage (5V).
(6) t_{WR} is the minimum cycle time to be allowed from the system perspective unless polling techniques are used. It is the maximum time the device requires to automatically complete the internal write operation.

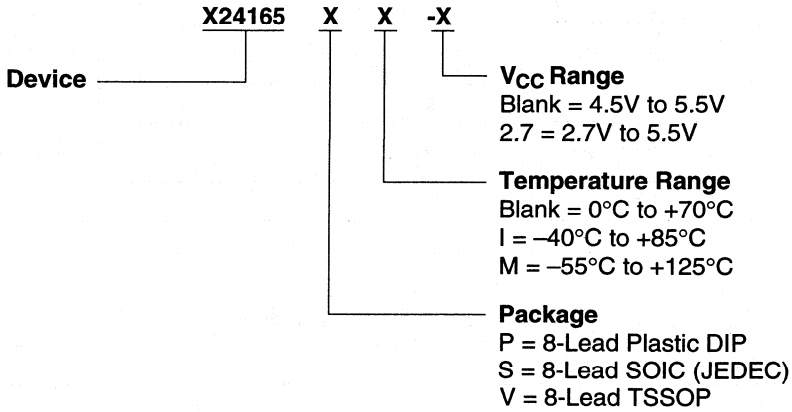
Guidelines for Calculating Typical Values of Bus Pull-Up Resistors



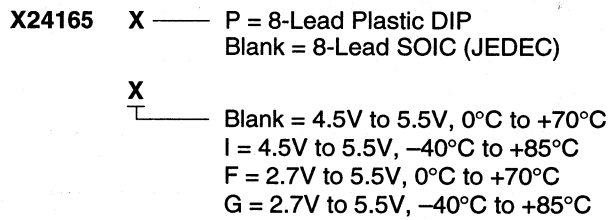
SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

ORDERING INFORMATION



Part Mark Convention



Advanced 2-Wire Serial E²PROM with Block Lock™ Protection

FEATURES

- 2.7V to 5.5V Power Supply
- Low Power CMOS
  - —Active Read Current Less Than 1mA
  - —Active Write Current Less Than 3mA
  - —Standby Current Less Than 1μA
- Internally Organized 4096 x 8
- New Programmable Block Lock Protection
  - —Software Write Protection
  - —Programmable hardware Write Protect
- Block Lock (0, 1/4, 1/2, or all of the E²PROM array)
- 2 Wire Serial Interface
- Bidirectional Data Transfer Protocol
- 32 Byte Page Write Mode
  - —Minimizes Total Write Time Per Byte
- Self Timed Write Cycle
  - —Typical Write Cycle Time of 5ms
- High Reliability
  - —Endurance: 100,000 Cycles
  - —Data Retention: 100 Years
- Available Packages
  - —8-Lead Mini-DIP
  - —8-Lead SOIC (JEDEC)
  - —14-Lead TSSOP

DESCRIPTION

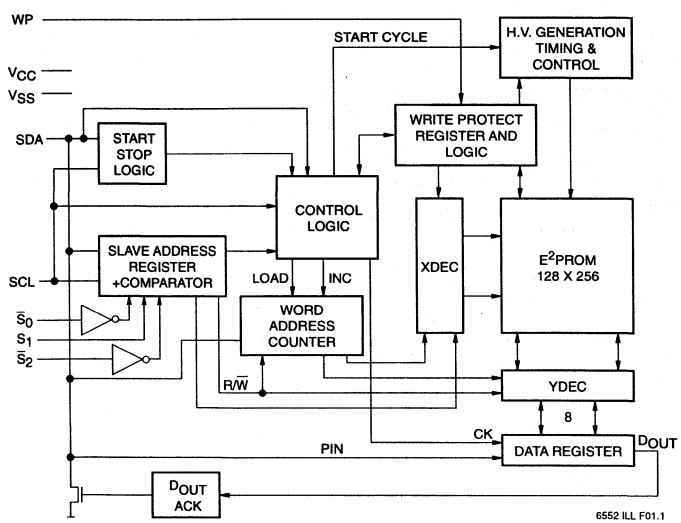
The X24325 is a CMOS 32,768 bit serial E²PROM, internally organized 4096 x 8. The X24325 features a serial interface and software protocol allowing operation on a simple two wire bus.

Three device select inputs ($\overline{S}_0$, S_1, $\overline{S}_2$) allow up to eight devices to share a common two wire bus.

A Write Protect Register at the highest address location, FFFh, provides three new write protection features: Software Write Protect, Block Write Protect, and Hardware Write Protect. The Software Write Protect feature prevents any nonvolatile writes to the X24325 until the WEL bit in the write protect register is set. The Block Write Protection feature allows the user to individually write protect four blocks of the array by programming two bits in the write protect register. The Programmable Hardware Write Protect feature allows the user to install the X24325 with WP tied to V_{CC}, program the entire memory array in place, and then enable the hardware write protection by programming a WPEN bit in the write protect register. After this, selected blocks of the array, including the write protect register itself, are permanently write protected.

Xicor E²PROMs are designed and tested for applications requiring extended endurance. Inherent data retention is greater than 100 years.

FUNCTIONAL DIAGRAM



PIN DESCRIPTIONS

Serial Clock (SCL)

The SCL input is used to clock all data into and out of the device.

Serial Data (SDA)

SDA is a bidirectional pin used to transfer data into and out of the device. It is an open drain output and may be wire-ORed with any number of open drain or open collector outputs.

An open drain output requires the use of a pull-up resistor. For selecting typical values, refer to the Pull-Up Resistor selection graph at the end of this data sheet.

Device Select ($\overline{S0}$, S_1, $\overline{S_2}$)

The device select inputs ($\overline{S0}$, S_1, $\overline{S_2}$) are used to set the first three bits of the 8-bit slave address. This allows up to eight X24325's to share a common bus. These inputs can be static or actively driven. If used statically they must be tied to V_{SS} or V_{CC} as appropriate. If actively driven, they must be driven with CMOS levels (driven to V_{CC} or V_{SS}).

Write Protect (WP)

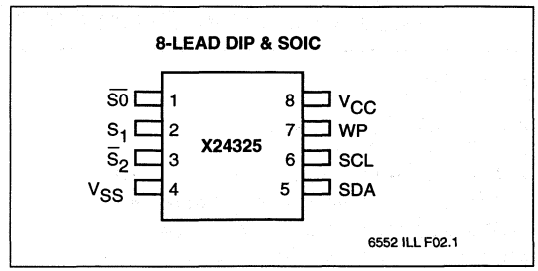
The write protect input controls the hardware write protect feature. When held LOW, hardware write protection is disabled and the X24325 can be written normally. When this input is held HIGH, and the WPEN bit in the write protect register is set HIGH, write protection is enabled, and nonvolatile writes are disabled to the selected blocks as well as the write protect register itself.

PIN NAMES

Symbol	Description
$\overline{S0}$, S_1, $\overline{S_2}$	Device Select Inputs
SDA	Serial Data
SCL	Serial Clock
WP	Write Protect
V_{SS}	Ground
V_{CC}	Supply Voltage
NC	No Connect

6552 FRM T01.1

PIN CONFIGURATION



DEVICE OPERATION

The X24325 supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter, and the receiving device as the receiver. The device controlling the transfer is a master and the device being controlled is the slave. The master will always initiate data transfers, and provide the clock for both transmit and receive operations. Therefore, the X24325 will be considered a slave in all applications.

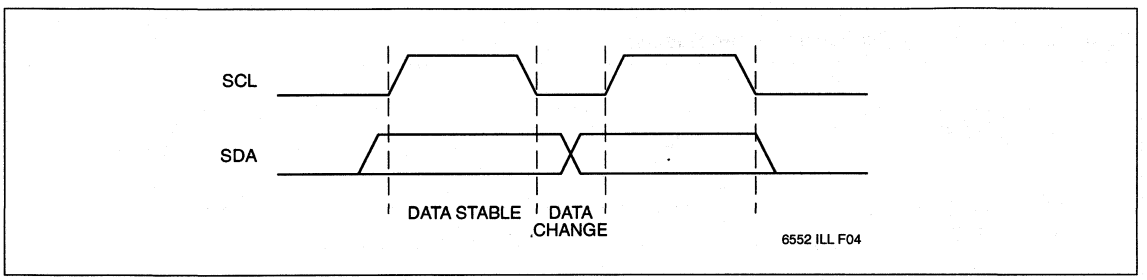
Clock and Data Conventions

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions. Refer to Figures 1 and 2.

Start Condition

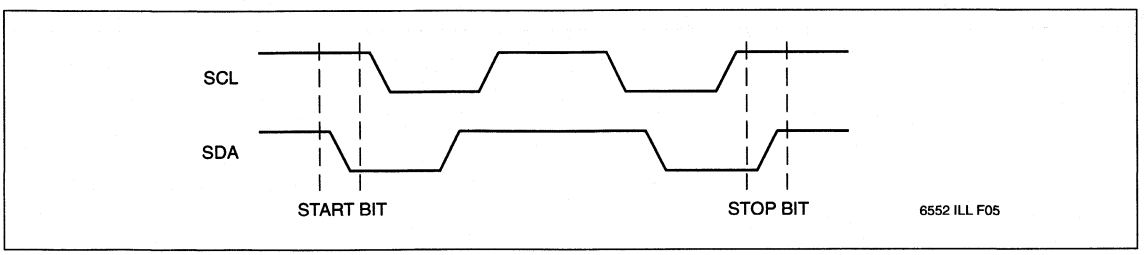
All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The X24325 continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

Figure 1. Data Validity



Notes: (5) Typical values are for $T_A = 25°C$ and nominal supply voltage (5V)
(6) t_{WR} is the minimum cycle time from the system perspective when polling techniques are not used. It is the maximum time the device requires to perform the internal write operation.

Figure 2. Definition of Start and Stop



Stop Condition

All communications must be terminated by a stop condition, which is a LOW to HIGH transition of SDA when SCL is HIGH. The stop condition is also used to place the device into the standby power mode after a read sequence. A stop condition can only be issued after the transmitting device has released the bus.

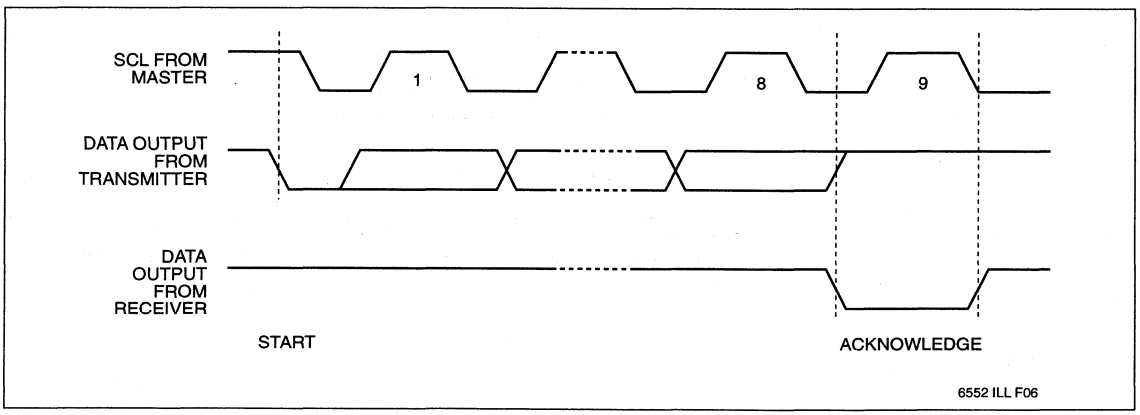
Acknowledge

Acknowledge is a software convention used to indicate successful data transfer. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data. Refer to Figure 3.

The X24325 will respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a write operation have been selected, the X24325 will respond with an acknowledge after the receipt of each subsequent eight-bit word.

In the read mode the X24325 will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the X24325 will continue to transmit data. If an acknowledge is not detected, the X24325 will terminate further data transmissions. The master must then issue a stop condition to return the X24325 to the standby power mode and place the device into a known state.

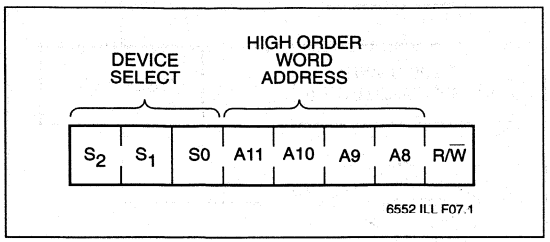
Figure 3. Acknowledge Response From Receiver



DEVICE ADDRESSING

Following a start condition the master must output the address of the slave it is accessing (see Figure 4). The next three bits are the device select bits. A system could have up to eight X24325's on the bus. The eight addresses are defined by the state of the $\overline{S0}$, S_1 and $\overline{S}_2$ inputs. S0 and S_2 of the slave address must be the inverse of the $\overline{S0}$ and $\overline{S}_2$ input pins.

Figure 4. Slave Address



The next four bits of the slave address are an extension of the array's address and are concatenated with the eight bits of address in the word address field, providing direct access to the whole 4096 x 8 array.

The last bit of the slave address defines the operation to be performed. When set HIGH a read operation is selected, when set LOW a write operation is selected.

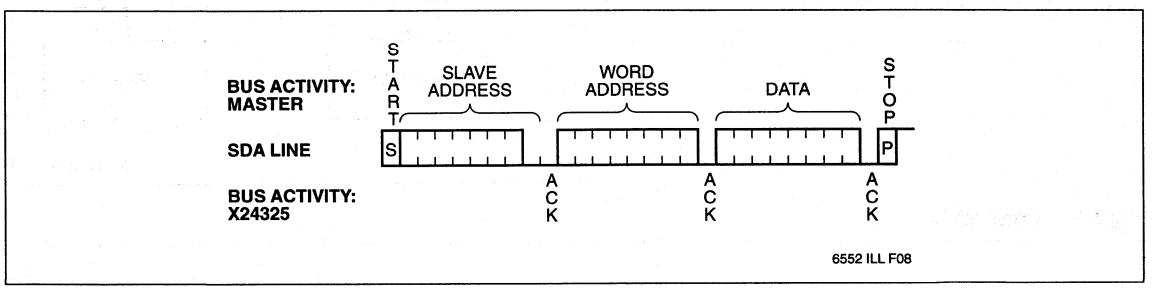
Following the start condition, the X24325 monitors the SDA bus comparing the slave address being transmitted with its slave address device type identifier. Upon a correct compare the X24325 outputs an acknowledge on the SDA line. Depending on the state of the R/$\overline{W}$ bit, the X24325 will execute a read or write operation.

WRITE OPERATIONS

Byte Write

For a write operation, the X24325 requires a second address field. This address field is the word address, comprised of eight bits, providing access to any one of 4096 words in the array. Upon receipt of the word address, the X24325 responds with an acknowledge and awaits the next eight bits of data, again responding with an acknowledge. The master then terminates the transfer by generating a stop condition, at which time the X24325 begins the internal write cycle to the nonvolatile memory. While the internal write cycle is in progress the X24325 inputs are disabled, and the device will not respond to any requests from the master. Refer to Figure 5 for the address, acknowledge and data transfer sequence.

Figure 5. Byte Write



Page Write

The X24325 is capable of a 32 byte page write operation. It is initiated in the same manner as the byte write operation, but instead of terminating the write cycle after the first data word is transferred, the master can transmit up to fifteen more words. After the receipt of each word, the X24325 will respond with an acknowledge.

After the receipt of each word, the five low order address bits are internally incremented by one. The high order bits of the word address remain constant. If the master should transmit more than 32 words prior to generating the stop condition, the address counter will "roll over" and the previously written data will be overwritten. As with the byte write operation, all inputs are disabled until completion of the internal write cycle. Refer to Figure 6 for the address, acknowledge and data transfer sequence.

Acknowledge Polling

The 10ms Max Write Cycle Time (5ms Typical) can be significantly reduced using Acknowledge Polling. To initiate Acknowledge Polling, the master issues a start condition followed by the Slave Address Byte for a write or read operation. If the device is still busy with the high voltage cycle, then no ACK will be returned. If the device has completed the write operation, an ACK will be returned and the host can then proceed with the read or write operation. Refer to Flow 1.

Flow 1. ACK Polling Sequence

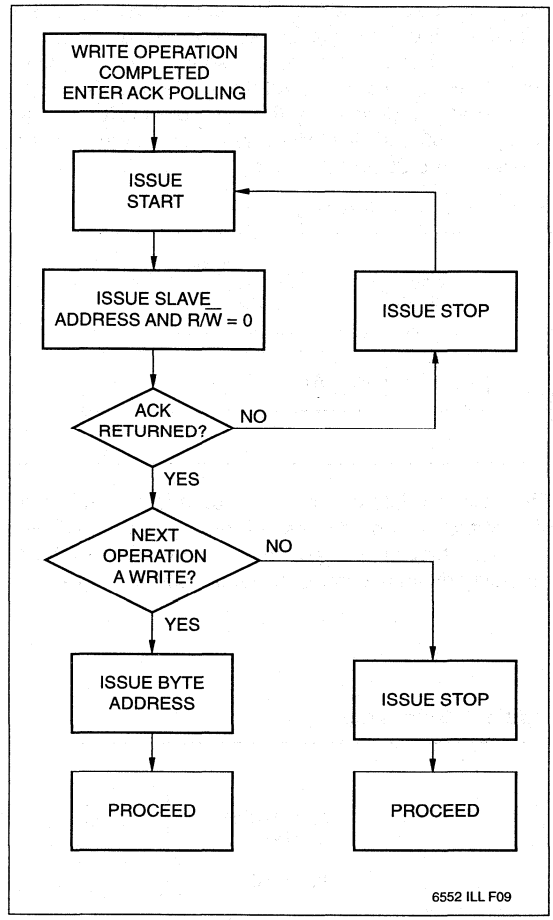
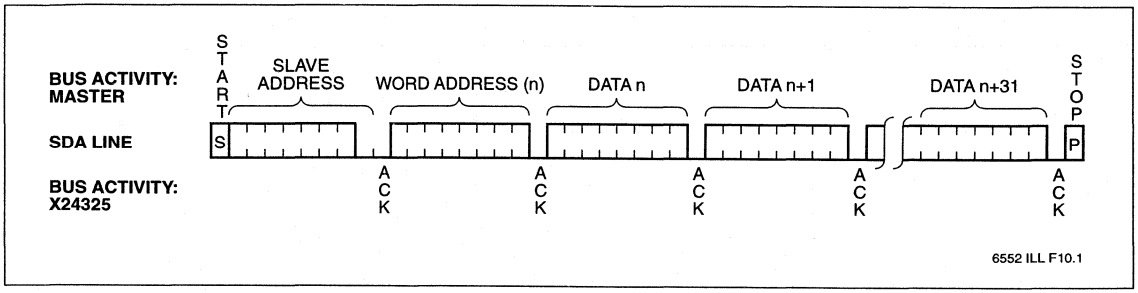


Figure 6. Page Write



READ OPERATIONS

Read operations are initiated in the same manner as write operations with the exception that the R/$\overline{W}$ bit of the slave address is set HIGH. There are three basic read operations: current address read, random read and sequential read.

It should be noted that the ninth clock cycle of the read operation is not a "don't care." To terminate a read operation, the master must either issue a stop condition during the ninth cycle or hold SDA HIGH during the ninth clock cycle and then issue a stop condition.

Current Address Read

Internally the X24325 contains an address counter that maintains the address of the last word read, incremented by one or the exact address of the last word written. Therefore, if the last access read was to address n, the next read operation would access data from address n + 1. Upon receipt of the slave address with the R/$\overline{W}$ set HIGH, the X24325 issues an acknowledge and transmits the eight-bit word. The read operation is terminated by the master; by not responding with an acknowledge and by issuing a stop condition. Refer to Figure 7 for the sequence of address, acknowledge and data transfer.

Random Read

Random read operations allow the master to access any memory location in a random manner. Prior to issuing the slave address with the R/$\overline{W}$ bit set HIGH, the master must first perform a "dummy" write operation. The master issues the start condition, and the slave address with the R/$\overline{W}$ bit set LOW, followed by the word address it is to read. After the word address acknowledge, the master immediately reissues the start condition and the slave address with the R/$\overline{W}$ bit set HIGH. This will be followed by an acknowledge from the X24325 and then by the eight-bit word. The read operation is terminated by the master; by not responding with an acknowledge and by issuing a stop condition. Refer to Figure 8 for the address, acknowledge and data transfer sequence.

Figure 7. Current Address Read

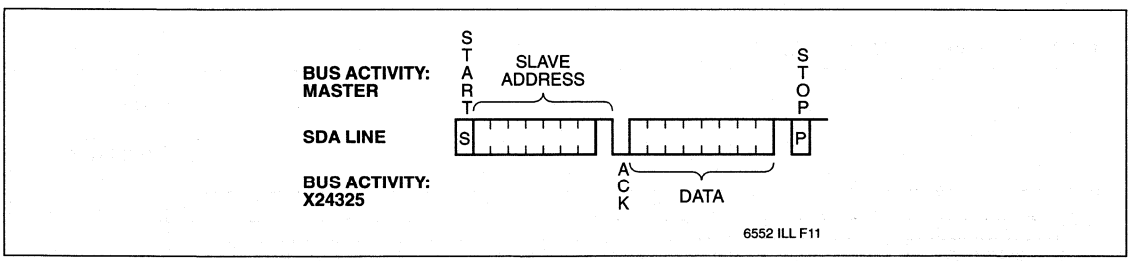
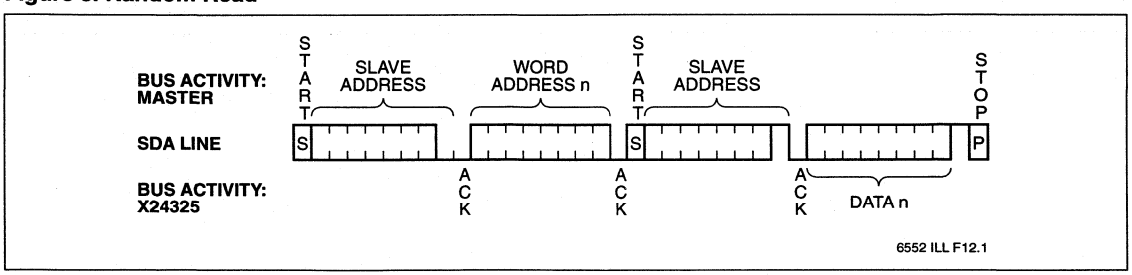


Figure 8. Random Read



Sequential Read

Sequential reads can be initiated as either a current address read or random access read. The first word is transmitted as with the other modes, however, the master now responds with an acknowledge, indicating it requires additional data. The X24325 continues to output data for each acknowledge received. The read operation is terminated by the master; by not responding with an acknowledge and then issuing a stop condition.

The data output is sequential, with the data from address n followed by the data from n + 1. The address counter for read operations increments all address bits, allowing the entire memory contents to be serially read during one operation. At the end of the address space (address 4095), the counter "rolls over" to 0 and the X24325 continues to output data for each acknowledge received. Refer to Figure 9 for the address, acknowledge and data transfer sequence.

Figure 9. Sequential Read

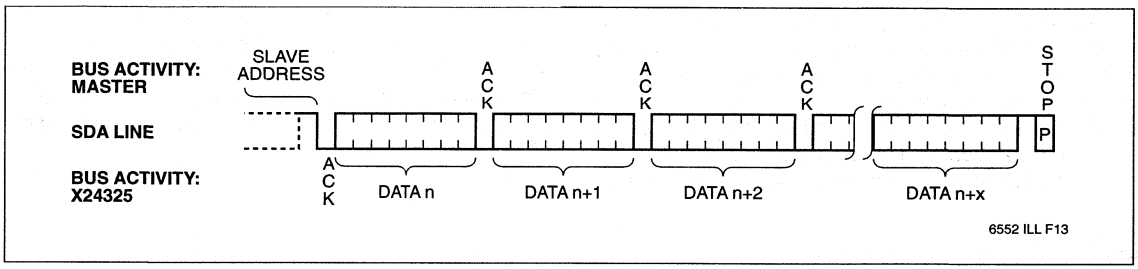
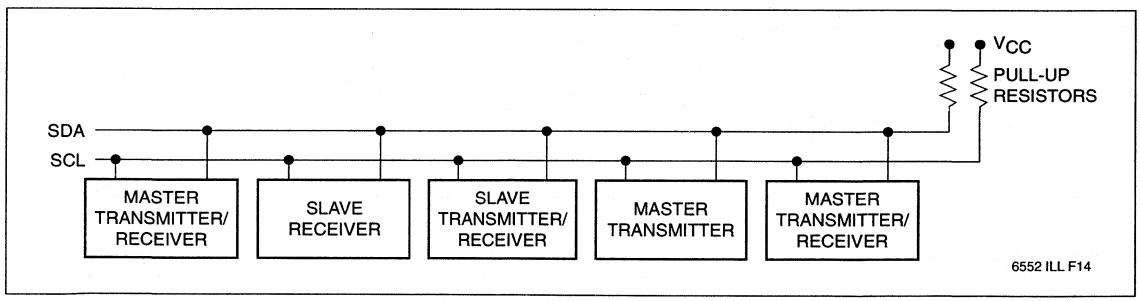


Figure 10. Typical System Configuration



WRITE PROTECT REGISTER

The Write Protect Register (WPR) is located at the highest address, FFFh.

Figure 11. Write Protect Register

WPR (Addr = FFFh)

7	6	5	4	3	2	1	0
WPEN	0	0	BP1	BP0	RWEL	WEL	0

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WPR.1 = WEL
- Write Enable Latch (Volatile)
  0 = Write enable latch reset, writes disabled
  1 = Write enable latch set, writes enabled

If WEL = 0 then "no ACK" after first byte of input data.

WPR.2 = RWEL
- Register Write Enable Latch (Volatile)
  0 = Register write enable latch reset, writes disabled
  1 = Register write enable latch set, writes enabled

WPR.3, WPR.4 = BP0, BP1
- Block Protect Bits (Nonvolatile)

(See Block Protect section for definition)

WPR.7 = WPEN
- Write Protect Enable Bit (Nonvolatile)

(See Hardware Write Protect section for definition)

Writing to the Write Protect Register

The Write Protect Register is written by performing a random write of one byte directly to address, FFFh. If a page write is performed starting with any address other than FFFh, the byte in the array at address FFFh will be written instead of the Write Protect Register (assuming writes are not disabled by the block protect register).

The state of the Write Protect Register can be read by performing a random read at address FFFh at any time. If a sequential read starting at any other address than FFFh is performed, the contents of the byte in the array at FFFh is read out instead of the Write Protect Register.

WEL and RWEL are volatile latches that power-up in the LOW (disabled) state. A write to any address other than FFFh, where the Write Protect Register is located, will be ignored (no ack) until the WEL bit is set HIGH. The WEL bit is set by writing 0000001x to address FFFh. Once set, WEL remains HIGH until either reset (by writing 00000000 to FFFh) or until the part powers-up again. The RWEL bit controls writes to the block protect bits. RWEL is set by first setting WEL = 1 and then writing 0000011x to address FFFh. RWEL must be set in order to change the block protect bits, BP0 and BP1, or the WPEN bit. RWEL is reset when the block protect or WPEN bits are changed, or when the part powers-up again.

Programming the BP or WPEN Bits

A three step sequence is required to change the nonvoltaile Block Protect or Write Protect Enable:

1) Set WEL = 1 (write 00000010 to address FFFh, volatile write cycle)

(Start)

2) Set RWEL = 1 (write 00000110 to address FFFh, volatile write cycle)

(Start)

3) Set BP1, BP0, and/or WPEN bits (Write w00yz010 to address FFFh)

w = WPEN, y = BP1, Z = BP0,

(Stop)

Step 3 is a nonvolatile write cycle, requiring 10ms to complete. RWEL is reset (0) by this write cycle, requiring another write cycle to set RWEL again before the block protect bits can be changed. RWEL must be 0 in step 3; if w00yz110 is written to address FFFh, RWEL is set but WPEN, BP1 and BP0 are not changed (the device remains at step 2).

Block Protect Bits

The Block Protect Bits BP0 and BP1 determine which blocks of the memory are write-protected:

Table 1. Block Protect Bits

BP1	BP0	Protected Addresses	
0	0	None	
0	1	C00h–FFFh	Upper 1/4
1	0	800h–FFFh	Upper 1/2
1	1	0000h–FFFh	Full Array (WPR not included)

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Programmable Hardware Write Protect

The Write Protect (WP) pin and the Write Protect Enable (WPEN) bit in the Write Protect Register control the programmable hardware write protect feature. Hardware write protection is enabled when the WP pin and the WPEN bit are both HIGH, and disabled when either the WP pin is LOW or the WPEN bit is LOW. When the chip is hardware write-protected, nonvolatile writes are disabled to the Write Protect Register, including the BP bits and the WPEN bit itself, as well as to block-protected sections in the memory array. Only the sections of the memory array that are not block-protected can be written. Note that since the WPEN bit is write-protected, it cannot be changed back to a LOW state, and write protection is disabled as long as the the WP pin is held HIGH. Table 2 defines the write protection status for each state of WPEN and WP.

Table 2. Write Protect Status Table

WP	WPEN	Memory Array (Not Block Protected)	Memory Array (Block Protected)	BP Bits	WPEN Bit
0	X	Writable	Protected	Writable	Writable
X	0	Writable	Protected	Writable	Writable
1	1	Writable	Protected	Protected	Protected

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ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias
X24325 ..... –65°C to +135°C
Storage Temperature ..... –65°C to +150°C
Voltage on any Pin with
Respect to V_{SS} ..... –1V to +7V
D.C. Output Current 5mA
Lead Temperature (Soldering, 10 Seconds) ..... 300°C

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2

RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	+70°C
Industrial	–40°C	+85°C
Military	–55°C	+125°C

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Supply Voltage	Limits
X24325	4.5V to 5.5V
X24325-2.7	2.7V to 5.5V

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D.C. OPERATING CHARACTERISTICS

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
I_{CC1}	V_{CC} Supply Current (Read)		1	mA	SCL = V_{CC} X 0.1/V_{CC} X 0.9 Levels @ 100KHz, SDA = Open, All Other Inputs = V_{SS} or V_{CC} – 0.3V
I_{CC2}	V_{CC} Supply Current (Write)		3	mA	
I_{SB1}(1)	V_{CC} Standby Current		50	µA	SCL = SDA = V_{CC}, All Other Inputs = V_{SS} or V_{CC} – 0.3V, V_{CC} = 5V ± 10%
I_{SB2}(1)	V_{CC} Standby Current		1	µA	SCL = SDA = V_{CC}, All Other Inputs = V_{SS} or V_{CC} – 0.3V, V_{CC} = 2.7V
I_{LI}	Input Leakage Current		10	µA	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output Leakage Current		10	µA	V_{OUT} = V_{SS} to V_{CC}
V_{IL}(2)	Input LOW Voltage	–1	V_{CC} x 0.3	V	
V_{IH}(2)	Input HIGH Voltage	V_{CC} x 0.7	V_{CC} + 0.5	V	
V_{OL}	Output LOW Voltage		0.4	V	I_{OL} = 3mA, V_{CC} = 4.5V

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CAPACITANCE T_A = +25°C, f = 1MHz, V_{CC} = 5V

Symbol	Parameter	Max.	Units	Test Conditions
$C_{I/O}$(3)	Input/Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}(3)	Input Capacitance (S_1, $\overline{S_2}$, SCL)	6	pF	V_{IN} = 0V

6552 FRM T07.1

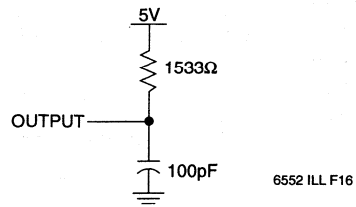
Notes: (1) Must perform a stop command prior to measurement.
(2) V_{IL} min. and V_{IH} max. are for reference only and are not 100% tested.
(3) This parameter is periodically sampled and not 100% tested.

A.C. CONDITIONS OF TEST

Input Pulse Levels	V_{CC} x 0.1 to V_{CC} x 0.9
Input Rise and Fall Times	10ns
Input and Output Timing Levels	V_{CC} X 0.5

6552 FRM T08.1

EQUIVALENT A.C. LOAD CIRCUIT



6552 ILL F16

A.C. OPERATING CHARACTERISTICS (Over the recommended operating conditions, unless otherwise specified.)

Read & Write Cycle Limits

Symbol	Parameter	Min.	Max.	Units
f_{SCL}	SCL Clock Frequency	0	100	KHz
T_I	Noise Suppression Time Constant at SCL, SDA Inputs		100	ns
t_{AA}	SCL LOW to SDA Data Out Valid	0.3	3.5	µs
t_{BUF}	Time the Bus Must Be Free Before a New Transmission Can Start	4.7		µs
$t_{HD:STA}$	Start Condition Hold Time	4		µs
t_{LOW}	Clock LOW Period	4.7		µs
t_{HIGH}	Clock HIGH Period	4		µs
$t_{SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	4.7		µs
$t_{HD:DAT}$	Data In Hold Time	0		µs
$t_{SU:DAT}$	Data In Setup Time	250		ns
t_R	SDA and SCL Rise Time		1	µs
t_F	SDA and SCL Fall Time		300	ns
$t_{SU:STO}$	Stop Condition Setup Time	4.7		µs
t_{DH}	Data Out Hold Time	300		ns

6552 FRM T09.1

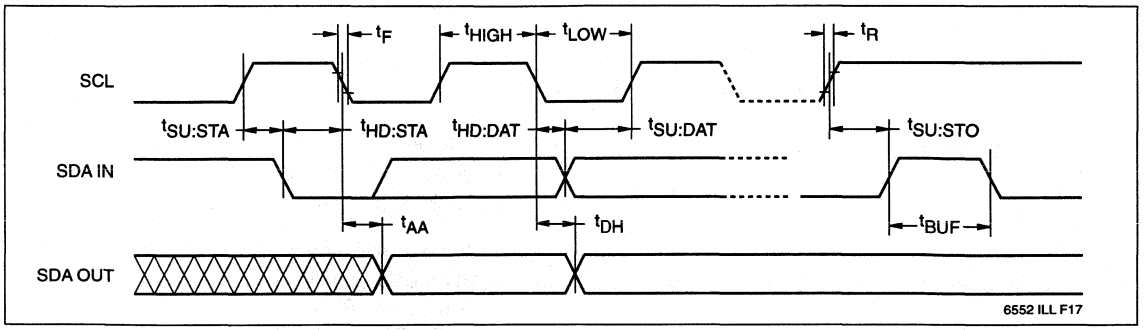
POWER-UP TIMING(4)

Symbol	Parameter	Max.	Units
t_{PUR}	Power-up to Read Operation	1	ms
t_{PUW}	Power-up to Write Operation	5	ms

6552 FRM T10

Notes: (4) t_{PUR} and t_{PUW} are the delays required from the time V_{CC} is stable until the specified operation can be initiated. These parameters are periodically sampled and not 100% tested.

Bus Timing



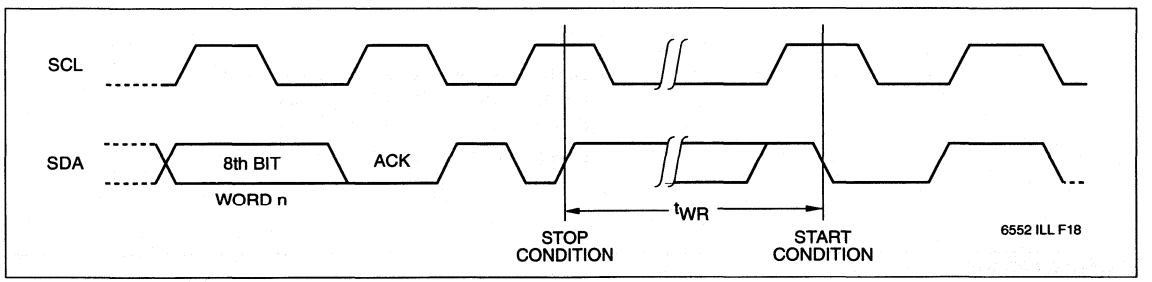
Write Cycle Limits

Symbol	Parameter	Min.	Typ.(5)	Max.	Units
t_{WR}(6)	Write Cycle Time		5	10	ms

6552 FRM T11.1

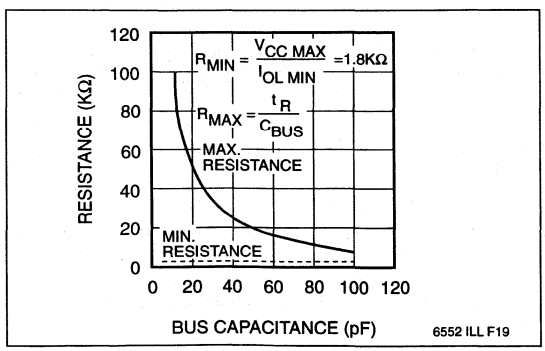
The write cycle time is the time from a valid stop condition of a write sequence to the end of the internal erase/program cycle. During the write cycle, the X24325 bus interface circuits are disabled, SDA is allowed to remain HIGH, and the device does not respond to its slave address.

Bus Timing



Notes: (5) Typical values are for T_A = 25°C and nominal supply voltage (5V).
(6) t_{WR} is the minimum cycle time to be allowed from the system perspective unless polling techniques are used. It is the maximum time the device requires to automatically complete the internal write operation.

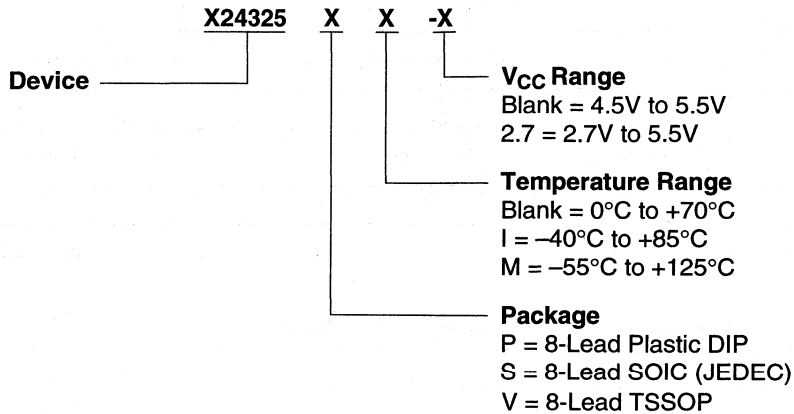
Guidelines for Calculating Typical Values of Bus Pull-Up Resistors



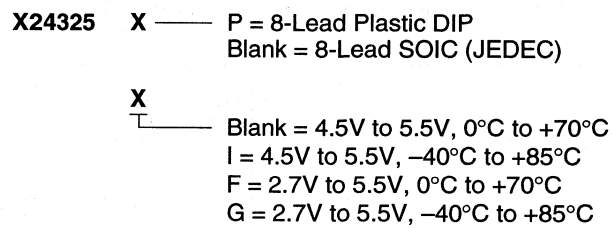
SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

ORDERING INFORMATION



Part Mark Convention



Advanced 2-Wire Serial E²PROM with Block Lock™ Protection

FEATURES

- 2.7V to 5.5V Power Supply
- Low Power CMOS
  - —Active Read Current Less Than 1mA
  - —Active Write Current Less Than 3mA
  - —Standby Current Less Than 1μA
- Internally Organized 8192 x 8
- New Programmable Block Lock Protection
  - —Software Write Protection
  - —Programmable hardware Write Protect
- Block Lock (0, 1/4, 1/2, or all of the E²PROM array)
- 2 Wire Serial Interface
- Bidirectional Data Transfer Protocol
- 32 Byte Page Write Mode
  - —Minimizes Total Write Time Per Byte
- Self Timed Write Cycle
  - —Typical Write Cycle Time of 5ms
- High Reliability
  - —Endurance: 100,000 Cycles
  - —Data Retention: 100 Years
- Available Packages
  - —8-Lead Mini-DIP
  - —8-Lead SOIC (JEDEC)
  - —14-Lead SOIC (JEDEC)
  - —8-Lead SOIC (EIAJ)
  - —20-Lead TSSOP

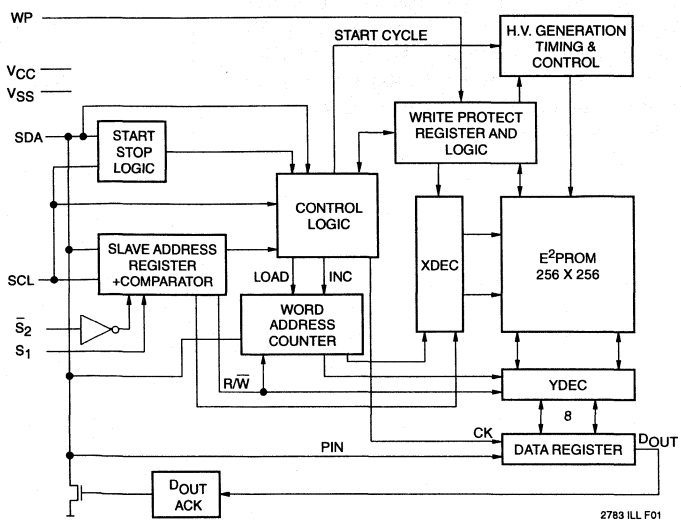
DESCRIPTION

The X24645 is a CMOS 65,536-bit serial E²PROM, internally organized 8192 x 8. The X24645 features a serial interface and software protocol allowing operation on a simple two wire bus.

Two device select inputs (S_1, $\overline{S}_2$) allow up to four devices to share a common two wire bus.

A Write Protect Register at the highest address location, 1FFFh, provides three new write protection features: Software Write Protect, Block Write Protect, and Hardware Write Protect. The Software Write Protect feature prevents any nonvolatile writes to the X24645 until the WEL bit in the write protect register is set. The Block Write Protection feature allows the user to individually write protect four blocks of the array by programming two bits in the write protect register. The Programmable Hardware Write Protect feature allows the user to install the X24645 with WP tied to V_{CC}, program the entire memory array in place, and then enable the hardware write protection by programming a WPEN bit in the write protect register. After this, selected blocks of the array, including the write protect register itself, are permanently write protected, as long as WP remains HIGH.

FUNCTIONAL DIAGRAM



Xicor E^2PROMs are designed and tested for applications requiring extended endurance. Inherent data retention is greater than 100 years.

PIN DESCRIPTIONS

Serial Clock (SCL)

The SCL input is used to clock all data into and out of the device.

Serial Data (SDA)

SDA is a bidirectional pin used to transfer data into and out of the device. It is an open drain output and may be wire-ORed with any number of open drain or open collector outputs.

An open drain output requires the use of a pull-up resistor. For selecting typical values, refer to the Pull-up resistor selection graph at the end of this data sheet.

Device Select (S_1, $\overline{S}_2$)

The device select inputs (S_1, $\overline{S}_2$) are used to set the first and second bits of the 8-bit slave address. This allows up to four X24645 devices to share a common bus. These inputs can be static or actively driven. If used statically they must be tied to V_{SS} or V_{CC} as appropriate. If actively driven, they must be driven with CMOS levels (driven to V_{CC} or V_{SS}).

Write Protect (WP)

The write protect input controls the hardware write protect feature. When held LOW, hardware write protection is disabled and the X24645 can be written normally. When this input is held HIGH, and the WPEN bit in the write protect register is set HIGH, write protection is enabled, and nonvolatile writes are disabled to the selected blocks as well as the write protect register itself.

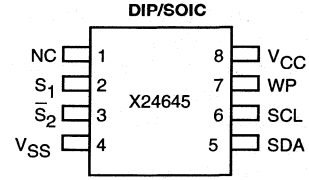
PIN NAMES

Symbol	Description
S_1, $\overline{S}_2$	Device Select Inputs
SDA	Serial Data
SCL	Serial Clock
WP	Write Protect
V_{SS}	Ground
V_{CC}	Supply Voltage
NC	No Connect

2783 FRM T01.1

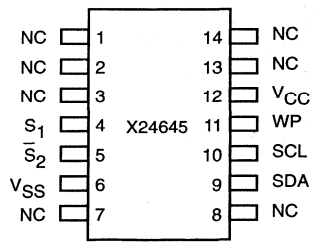
PIN CONFIGURATION

DIP/SOIC



2783 ILL F02.2

14-LEAD SOIC



2783 ILL F03.2

DEVICE OPERATION

The X24645 supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter, and the receiving device as the receiver. The device controlling the transfer is a master and the device being controlled is the slave. The master will always initiate data transfers, and provide the clock for both transmit and receive operations. Therefore, the X24645 will be considered a slave in all applications.

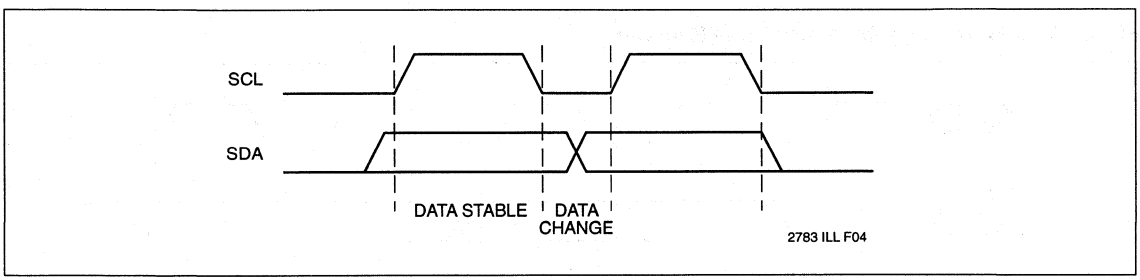
Clock and Data Conventions

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions. Refer to Figures 1 and 2.

Start Condition

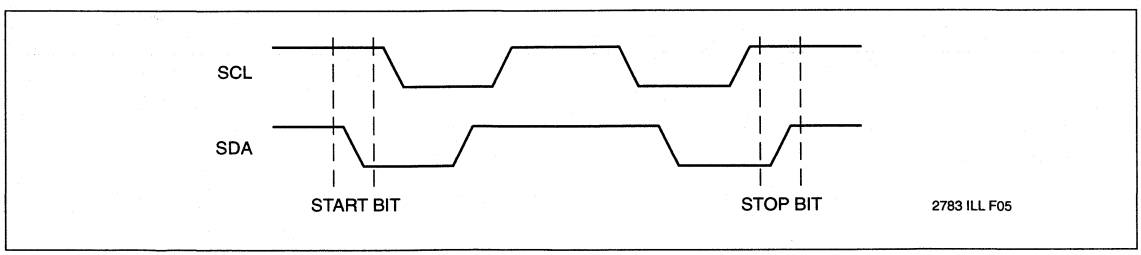
All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The X24645 continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

Figure 1. Data Validity



Notes: (5) Typical values are for $T_A = 25°C$ and nominal supply voltage (5V)
(6) t_{WR} is the minimum cycle time from the system perspective when polling techniques are not used. It is the maximum time the device requires to perform the internal write operation.

Figure 2. Definition of Start and Stop



Stop Condition

All communications must be terminated by a stop condition, which is a LOW to HIGH transition of SDA when SCL is HIGH. The stop condition is also used to place the device into the standby power mode after a read sequence. A stop condition can only be issued after the transmitting device has released the bus.

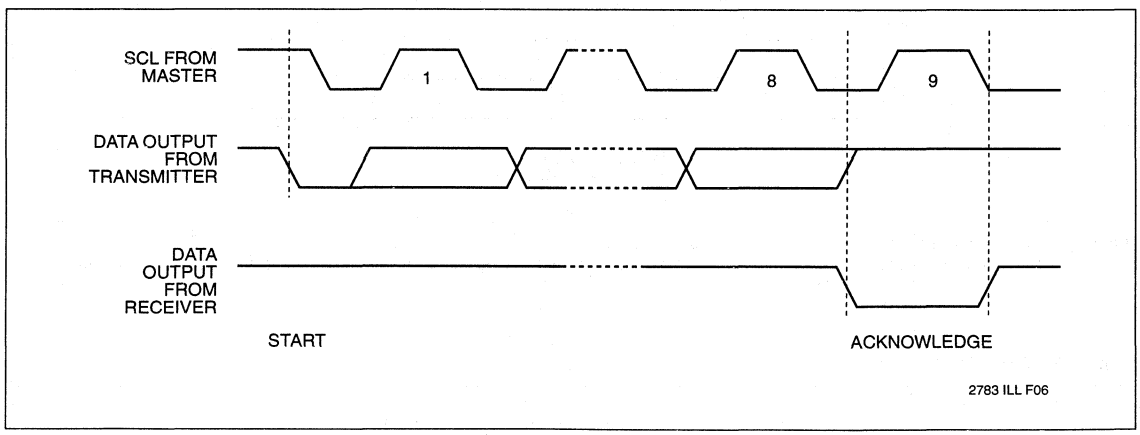
Acknowledge

Acknowledge is a software convention used to indicate successful data transfer. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data. Refer to Figure 3.

The X24645 will respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a write operation have been selected, the X24645 will respond with an acknowledge after the receipt of each subsequent 8-bit word.

In the read mode the X24645 will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the X24645 will continue to transmit data. If an acknowledge is not detected, the X24645 will terminate further data transmissions. The master must then issue a stop condition to return the X24645 to the standby power mode and place the device into a known state.

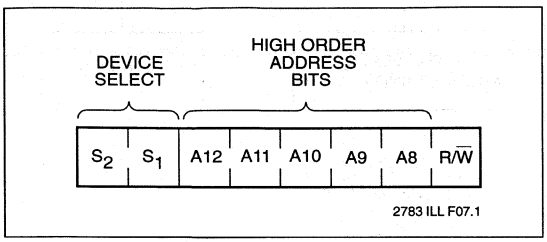
Figure 3. Acknowledge Response From Receiver



DEVICE ADDRESSING

Following a start condition the master must output the address of the slave it is accessing (see Figure 4). The next two bits are the device select bits. A system could have up to four X24645's on the bus. The four addresses are defined by the state of the S_1 and $\overline{S_2}$ inputs. S_2 of the slave address must be the inverse of the $\overline{S_2}$ input pin.

Figure 4. Slave Address



The next five bits of the slave address are an extension of the array's address and are concatenated with the eight bits of address in the byte address field, providing direct access to the whole 8192 x 8 array.

The last bit of the slave address defines the operation to be performed. When set HIGH a read operation is selected, when set LOW, a write operation is selected.

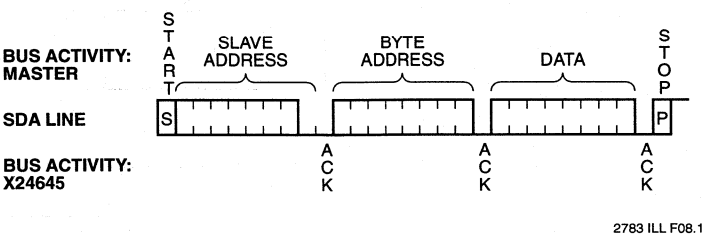
Following the start condition, the X24645 monitors the SDA bus comparing the slave address being transmitted with its slave address device type identifier. Upon a correct compare the X24645 outputs an acknowledge on the SDA line. Depending on the state of the R/$\overline{W}$ bit, the X24645 will execute a read or write operation.

WRITE OPERATIONS

Byte Write

For a write operation, the X24645 requires a second address field. This address field is the byte address, comprised of eight bits, providing access to any one of 8192 words in the array. Upon receipt of the byte address, the X24645 responds with an acknowledge and awaits the next eight bits of data, again responding with an acknowledge. The master then terminates the transfer by generating a stop condition, at which time the X24645 begins the internal write cycle to the nonvolatile memory. While the internal write cycle is in progress the X24645 inputs are disabled, and the device will not respond to any requests from the master. Refer to Figure 5 for the address, acknowledge and data transfer sequence.

Figure 5. Byte Write



Page Write

The X24645 is capable of a 32-byte page write operation. It is initiated in the same manner as the byte write operation, but instead of terminating the write cycle after the first data word is transferred, the master can transmit up to thirty-one more bytes. After the receipt of each byte, the X24645 will respond with an acknowledge.

After the receipt of each byte, the five low order address bits are internally incremented by one. The high order eight bits of the address remain constant. If the master should transmit more than 32 bytes prior to generating the stop condition, the address counter will "roll over" and the previously written data will be overwritten. As with the byte write operation, all inputs are disabled until completion of the internal write cycle. Refer to Figure 6 for the address, acknowledge, and data transfer sequence.

Acknowledge Polling

The 10ms Max Write Cycle Time (5ms Typical) can be significantly reduced using Acknowledge Polling. To initiate Acknowledge Polling, the master issues a start condition followed by the Slave Address Byte for a write or read operation. If the device is still busy with the high voltage cycle, then no ACK will be returned. If the device has completed the write operation, an ACK will be returned and the host can then proceed with the read or write operation. Refer to Flow 1.

Flow 1. ACK Polling Sequence

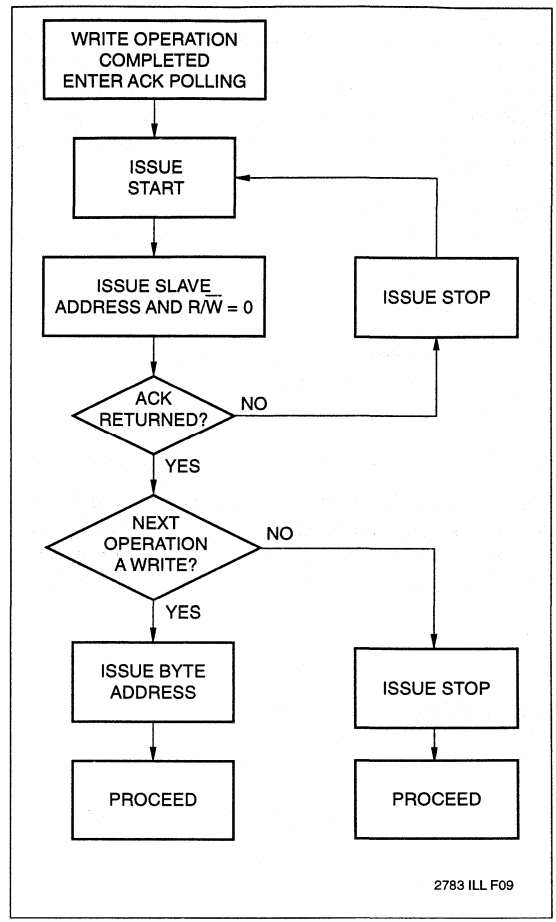
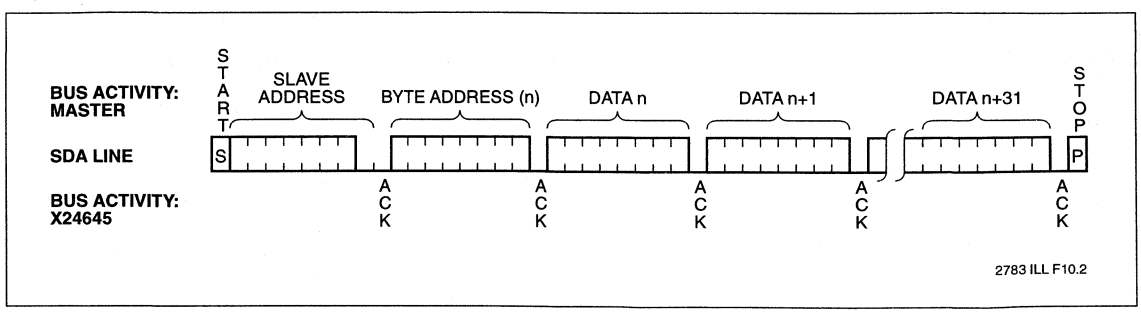


Figure 6. Page Write



READ OPERATIONS

Read operations are initiated in the same manner as write operations with the exception that the R/W bit of the slave address is set HIGH. There are three basic read operations: current address read, random read and sequential read.

It should be noted that the ninth clock cycle of the read operation is not a "don't care." To terminate a read operation, the master must either issue a stop condition during the ninth cycle or hold SDA HIGH during the ninth clock cycle and then issue a stop condition.

Current Address Read

Internally the X24645 contains an address counter that maintains the address of the last byte read, incremented by one or the exact address of the last byte written. Therefore, if the last access read was to address n, the next read operation would access data from address n + 1. Upon receipt of the slave address with the R/$\overline{W}$ set HIGH, the X24645 issues an acknowledge and transmits the byte. The read operation is terminated by the master; by not responding with an acknowledge and by issuing a stop condition. Refer to Figure 7 for the sequence of address, acknowledge and data transfer.

Random Read

Random read operations allow the master to access any memory location in a random manner. Prior to issuing the slave address with the R/$\overline{W}$ bit set HIGH, the master must first perform a "dummy" write operation. The master issues the start condition, and the slave address with the R/$\overline{W}$ bit set LOW, followed by the byte address it is to read. After the word address acknowledge, the master immediately reissues the start condition and the slave address with the R/$\overline{W}$ bit set HIGH. This will be followed by an acknowledge from the X24645 and then by the data byte. The read operation is terminated by the master; by not responding with an acknowledge and by issuing a stop condition. Refer to Figure 8 for the address, acknowledge and data transfer sequence.

Figure 7. Current Address Read

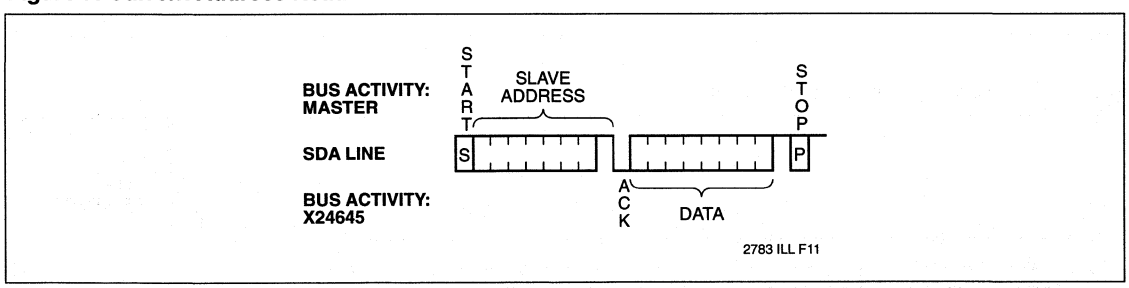
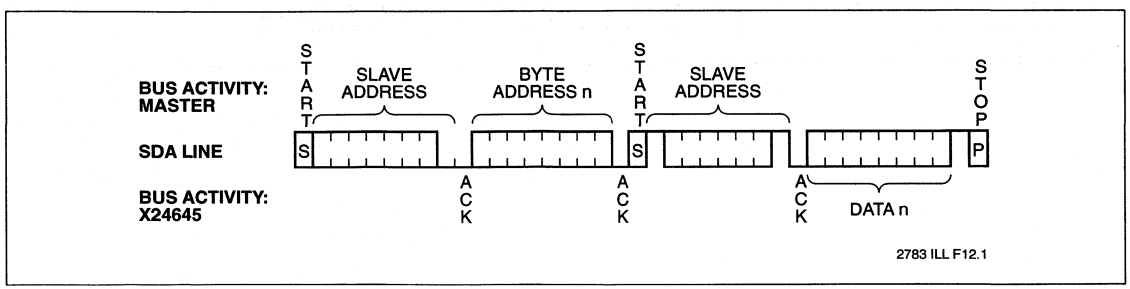


Figure 8. Random Read



Sequential Read

Sequential reads can be initiated as either a current address read or random access read. The first byte is transmitted as with the other modes, however, the master now responds with an acknowledge, indicating it requires additional data. The X24645 continues to output data for each acknowledge received. The read operation is terminated by the master; by not responding with an acknowledge and then issuing a stop condition.

The data output is sequential, with the data from address n followed by the data from n + 1. The address counter for read operations increments all address bits, allowing the entire memory contents to be serially read during one operation. At the end of the address space (address 8191), the counter "rolls over" to 0 and the X24645 continues to output data for each acknowledge received. Refer to Figure 9 for the address, acknowledge and data transfer sequence.

Figure 9. Sequential Read

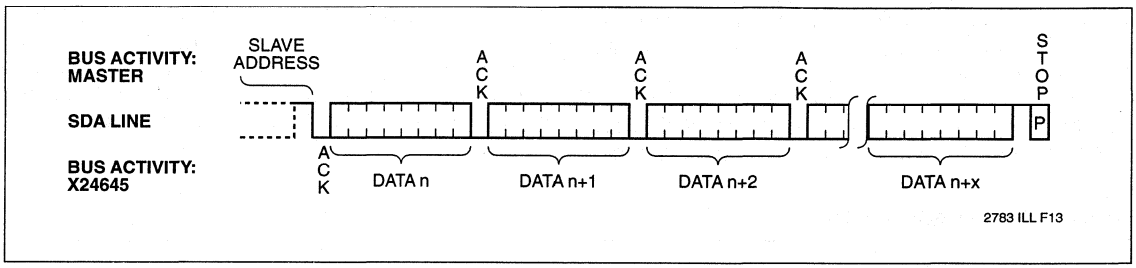
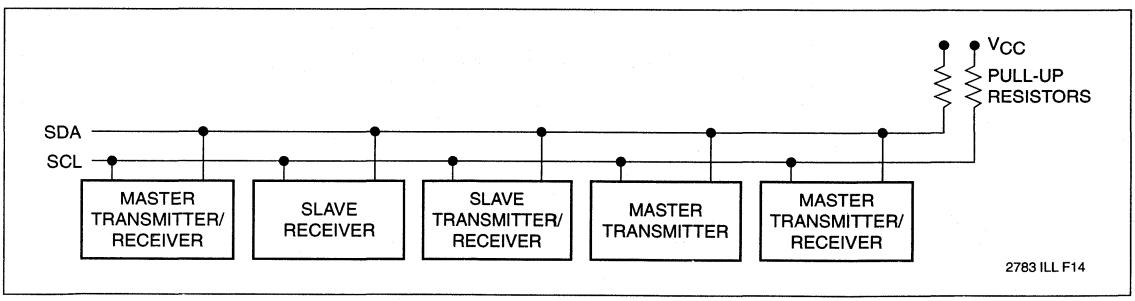


Figure 10. Typical System Configuration



WRITE PROTECT REGISTER

The Write Protect Register (WPR) is located at the highest address, 1FFFh.

Figure 11. Write Protect Register

WPR (ADDR = 1FFFh)

7	6	5	4	3	2	1	0
WPEN	0	0	BP1	BP0	RWEL	WEL	0

2783 ILL F15.1

WPR.1 = WEL
– "Write Enable" Latch (Volatile)
0 = Write enable latch reset, writes disabled
1 = Write enable latch set, writes enabled

If WEL = "0" then "no ACK" after first byte of input data.

WPR.2 = RWEL
– "Register Write Enable" Latch (Volatile)
0 = Register write enable latch reset, writes disabled
1 = Register write enable latch set, writes enabled

WPR.3, WPR.4 = BP0, BP1
– Block Protect Bits (Nonvolatile)
(See Block Protect section for definition)

WPR.7 = WPEN
– Write Protect Enable Bit (Nonvolatile)
(See Hardware Write Protect section for definition)

Writing to the Write Protect Register

The Write Protect Register is written by performing a random write of one byte directly to address, 1FFFh. If a page write is performed starting with any address other than 1FFF, the byte in the array at address 1FFFh will be written instead of the Write Protect Register (assuming writes are not disabled by the block protect register).

The state of the Write Protect Register can be read by performing a random read at address 1FFFh at any time. If a sequential read starting at any other address than 1FFFh is performed, the contents of the byte in the array at 1FFFh is read out instead of the Write Protect Register.

WEL and RWEL are volatile latches that power-up in the LOW (disabled) state. A write to any address other than 1FFFh, where the Write Protect Register is located, will be ignored (no ack) until the WEL bit is set HIGH. The WEL bit is set by writing 0000001x to address 1FFFh. Once set, WEL remains HIGH until either reset (by writing 00000000 to 1FFFh) or until the part powers-up again. The RWEL bit controls writes to the block protect bits. RWEL is set by first setting WEL to "1" and then writing 0000011x to address 1FFFh. RWEL must be set in order to change the block protect bits, BP0 and BP1, or the WPEN bit. RWEL is reset when the block protect or WPEN bits are changed, or when the part powers-up again.

Programming the BP or WPEN Bits

A three step sequence is required to change the nonvolatile Block Protect or Write Protect Enable:

1) Set WEL = 1 (write 00000010 to address 1FFFh, volatile write cycle)

(Start)

2) Set RWEL = 1 (write 00000110 to address 1FFFh, volatile write cycle)

(Start)

3) Set BP1, BP0, and/or WPEN bits (Write w00yz010 to address 1FFFh)

w = WPEN, y = BP1, Z = BP0,

(Stop)

Step 3 is a nonvolatile write cycle, requiring 10ms to complete. RWEL is reset to "0" by this write cycle, requiring another write cycle to set RWEL again before the block protect bits can be changed. RWEL must be "0" in step 3; if w00yz110 is written to address 1FFFh, RWEL is set but WPEN, BP1 and BP0 are not changed (the device remains at step 2).

Block Protect Bits

The Block Protect Bits BP0 and BP1 determine which blocks of the memory are write-protected:

Table 1. Block Protect Bits

BP1	BP0	Protected Addresses	
0	0	None	
0	1	1800h–1FFFh	Upper 1/4
1	0	1000h–1FFFh	Upper 1/2
1	1	0000h–1FFFh	Full Array (WPR not included)

2783 FRM T02

Programmable Hardware Write Protect

The Write Protect (WP) pin and the Write Protect Enable (WPEN) bit in the Write Protect Register control the programmable hardware write protect feature. Hardware write protection is enabled when the WP pin is HIGH and the WPEN bit is "1", and disabled when either the WP pin is LOW or the WPEN bit is "0". When the chip is hardware write-protected, nonvolatile writes are disabled to the Write Protect Register, including the BP bits and the WPEN bit itself, as well as to block-protected sections in the memory array. Only the sections of the memory array that are not block-protected can be written. Note that since the WPEN bit is write-protected, it cannot be changed back to a LOW state, and write protection is disabled as long as the the WP pin is held HIGH. Table 2 defines the write protection status for each state of WPEN and WP.

Table 2. Write Protect Status Table

WP	WPEN	Memory Array (Not Block Protected)	Memory Array (Block Protected)	BP Bits	WPEN Bit
L	X	Writable	Protected	Writable	Writable
X	0	Writable	Protected	Writable	Writable
H	1	Writable	Protected	Protected	Protected

2783 FRM T03.1

ABSOLUTE MAXIMUM RATINGS*

Temperature under Bias
X24645 ..... –65°C to +135°C
Storage Temperature ..... –65°C to +150°C
Voltage on any Pin with
Respect to V_{SS} ..... –1V to +7V
D.C. Output Current 5mA
Lead Temperature
(Soldering, 10 seconds) ..... 300°C

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2

RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	+70°C
Industrial	–40°C	+85°C
Military	–55°C	+125°C

2783 FRM T04

Supply Voltage	Limits
X24645	4.5V to 5.5V
X24645-2.7	2.7V to 5.5V

2783 FRM T05

D.C. OPERATING CHARACTERISTICS

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
I_{CC1}	V_{CC} Supply Current (Read)		1	mA	SCL = V_{CC} X 0.1/V_{CC} X 0.9 Levels @ 100KHz, SDA = Open, All Other Inputs = V_{SS} or V_{CC} – 0.3V
I_{CC2}	V_{CC} Supply Current (Write)		3	mA	
I_{SB1}(1)	V_{CC} Standby Current		50	µA	SCL = SDA = V_{CC}, All Other Inputs = V_{SS} or V_{CC} – 0.3V, V_{CC} = 5V ± 10%
I_{SB2}(1)	V_{CC} Standby Current		1	µA	SCL = SDA = V_{CC}, All Other Inputs = V_{SS} or V_{CC} – 0.3V, V_{CC} = 2.7V
I_{LI}	Input Leakage Current		10	µA	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output Leakage Current		10	µA	V_{OUT} = V_{SS} to V_{CC}
V_{IL}(2)	Input LOW Voltage	–1	V_{CC} x 0.3	V	
V_{IH}(2)	Input HIGH Voltage	V_{CC} x 0.7	V_{CC} + 0.5	V	
V_{OL}	Output LOW Voltage		0.4	V	I_{OL} = 3mA, V_{CC} = 4.5V

2783 FRM T06.2

CAPACITANCE T_A = +25°C, f = 1MHz, V_{CC} = 5V

Symbol	Parameter	Max.	Units	Test Conditions
$C_{I/O}$(3)	Input/Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}(3)	Input Capacitance (S_1, $\overline{S_2}$, SCL)	6	pF	V_{IN} = 0V

2783 FRM T07.1

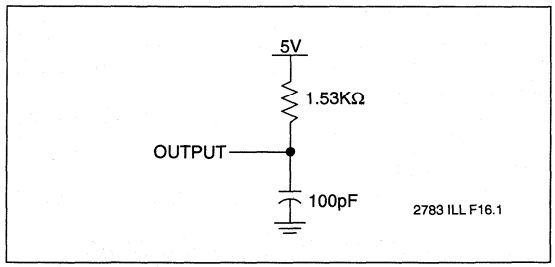
Notes: (1) Must perform a stop command prior to measurement.
(2) V_{IL} min. and V_{IH} max. are for reference only and are not 100% tested.
(3) This parameter is periodically sampled and not 100% tested.

A.C. CONDITIONS OF TEST

Input Pulse Levels	V_{CC} x 0.1 to V_{CC} x 0.9
Input Rise and Fall Times	10ns
Input and Output Timing Levels	V_{CC} X 0.5

2783 FRM T08

EQUIVALENT A.C. LOAD CIRCUIT



A.C. OPERATING CHARACTERISTICS (Over the recommended operating conditions, unless otherwise specified.)

Read & Write Cycle Limits

Symbol	Parameter	Min.	Max.	Units
f_{SCL}	SCL Clock Frequency	0	100	KHz
T_I	Noise Suppression Time Constant at SCL, SDA Inputs		100	ns
t_{AA}	SCL LOW to SDA Data Out Valid	0.3	3.5	µs
t_{BUF}	Time the Bus Must Be Free Before a New Transmission Can Start	4.7		µs
$t_{HD:STA}$	Start Condition Hold Time	4		µs
t_{LOW}	Clock LOW Period	4.7		µs
t_{HIGH}	Clock HIGH Period	4		µs
$t_{SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	4.7		µs
$t_{HD:DAT}$	Data In Hold Time	0		µs
$t_{SU:DAT}$	Data In Setup Time	250		ns
t_R	SDA and SCL Rise Time		1	µs
t_F	SDA and SCL Fall Time		300	ns
$t_{SU:STO}$	Stop Condition Setup Time	4.7		µs
t_{DH}	Data Out Hold Time	300		ns

2783 FRM T09.2

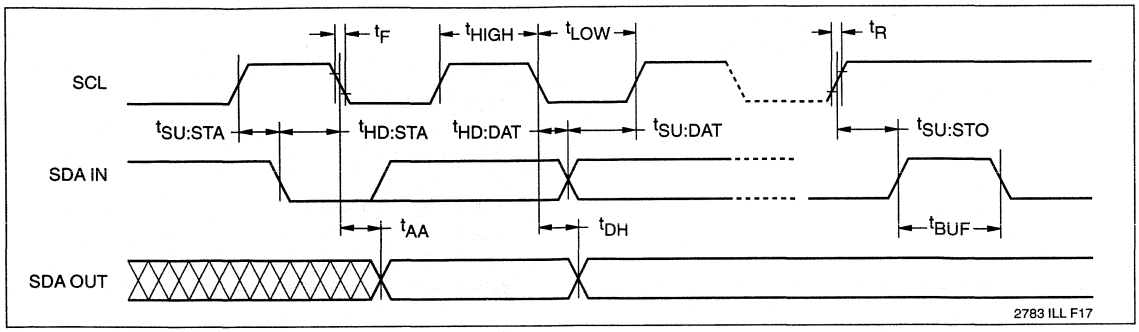
POWER-UP TIMING(4)

Symbol	Parameter	Max.	Units
t_{PUR}	Power-up to Read Operation	1	ms
t_{PUW}	Power-up to Write Operation	5	ms

2783 FRM T10

Notes: (4) t_{PUR} and t_{PUW} are the delays required from the time V_{CC} is stable until the specified operation can be initiated. These parameters are periodically sampled and not 100% tested.

Bus Timing



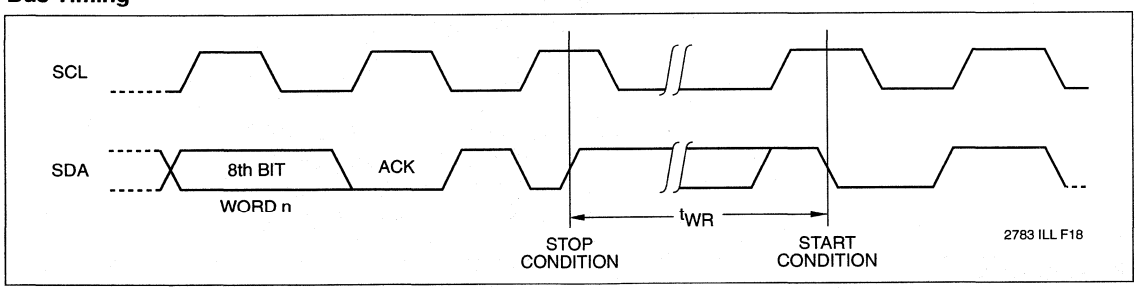
Write Cycle Limits

Symbol	Parameter	Min.	Typ.(5)	Max.	Units
T_{WR}(6)	Write Cycle Time		5	10	ms

2783 FRM T11

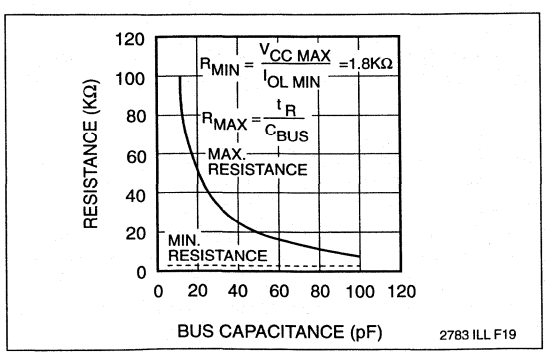
The write cycle time is the time from a valid stop condition of a write sequence to the end of the internal erase/program cycle. During the write cycle, the X24645 bus interface circuits are disabled, SDA is allowed to remain HIGH, and the device does not respond to its slave address.

Bus Timing



Notes: (5) Typical values are for $T_A = 25°C$ and nominal supply voltage (5V).
(6) t_{WR} is the minimum cycle time to be allowed from the system perspective unless polling techniques are used. It is the maximum time the device requires to automatically complete the internal write operation.

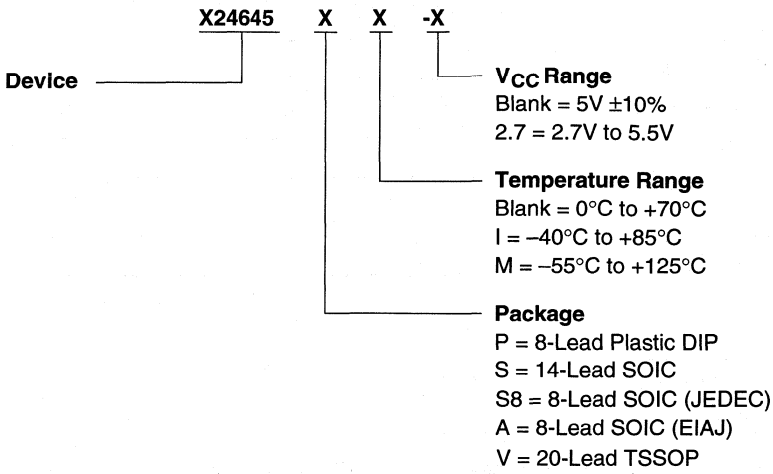
Guidelines for Calculating Typical Values of Bus Pull-Up Resistors



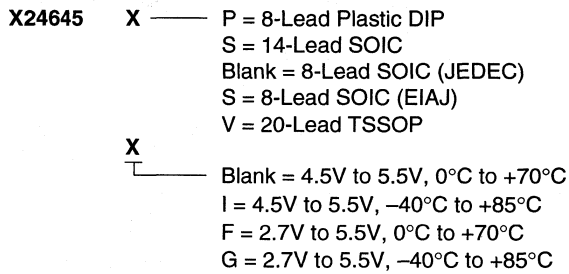
SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

ORDERING INFORMATION



Part Mark Convention



2K X25C02 256 x 8 Bit

SPI Serial E²PROM

FEATURES

- 1MHz Clock Rate
- 256 X 8 Bits
  - —4 Byte Page Mode
- Low Power CMOS
  - —150μA Standby Current
  - —2mA Active Current
- 5V Power Supply
- Built-in Inadvertent Write Protection
  - —Power-Up/Power-Down protection circuitry
  - —Write Latch
  - —Write Protect Pin
- Self-Timed Write Cycle
  - —5ms Write Cycle Time (Typical)
- High Reliability
  - —Endurance: 100,000 cycles per byte
  - —Data Retention: 100 Years
  - —ESD protection: 2000V on all pins
- 8-Pin Mini-DIP Package
- 8-Pin SOIC Package

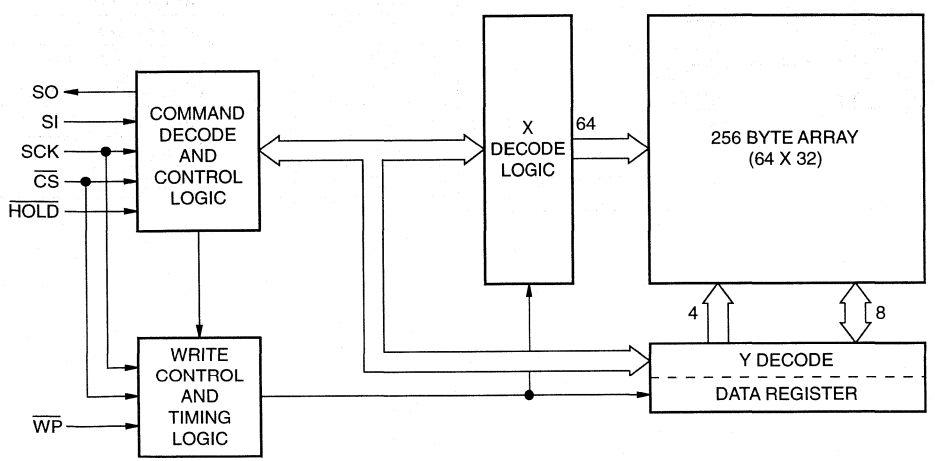
DESCRIPTION

The X25C02 is a CMOS 2048-bit serial E²PROM, internally organized as 256 x 8. The X25C02 features a serial interface and software protocol allowing operation on a simple three-wire bus. The bus signals are a clock input (SCK) plus separate data in (SI) and data out (SO) lines. Access to the device is controlled through a chip select ($\overline{CS}$) input, allowing any number of devices to share the same bus.

The X25C02 also features two additional inputs that provide the end user with added flexibility. By asserting the $\overline{HOLD}$ input, the X25C02 will ignore transitions on its inputs, thus allowing the host to service higher priority interrupts. The $\overline{WP}$ input can be used as a hardwire input to the X25C02 disabling all write attempts, thus providing a mechanism for limiting end user capability of altering the memory.

The X25C02 utilizes Xicor's proprietary Direct Write™ cell, providing a minimum endurance of 100,000 cycles per byte and a minimum data retention of 100 years.

FUNCTIONAL DIAGRAM



3843 FHD F01

Direct Write™ is a trademark of Xicor, Inc.

3843-1.5 5/25/95 T8/C5/D0 TD

PIN DESCRIPTIONS

Serial Output (SO)

SO is a push/pull serial data output pin. During a read cycle, data is shifted out on this pin. Data is clocked out by the falling edge of the serial clock.

Serial Input (SI)

SI is the serial data input pin. All data, opcodes, byte addresses, and data to be written to the memory are input on this pin. Data is latched by the rising edge of the serial clock.

Serial Clock (SCK)

The Serial Clock controls the serial bus timing for data input and output. Opcodes, addresses, or data present on the SI pin are sampled or latched on the rising edge of the clock input, while data on the SO pin change after the falling edge of the clock input.

Chip Select ($\overline{CS}$)

When $\overline{CS}$ is HIGH, the X25C02 is deselected and the SO output pin is at HIGH impedance and unless an internal write operation is underway, the X25C02 will be in the standby power mode. $\overline{CS}$ LOW enables the X25C02, placing it in the active power mode. It should be noted that after power-up, a HIGH to LOW transition on $\overline{CS}$ is required prior to the start of any operation.

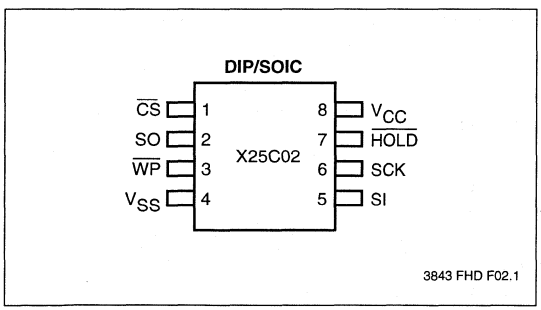
Write Protect ($\overline{WP}$)

When $\overline{WP}$ is LOW, nonvolatile writes to the X25C02 are disabled, but the part otherwise functions normally. When $\overline{WP}$ is held HIGH, all functions, including nonvolatile writes operate normally. $\overline{WP}$ going LOW while $\overline{CS}$ is still LOW will interrupt a write to the X25C02. If the internal write cycle has already been initiated, $\overline{WP}$ going LOW will have no affect on a write.

Hold ($\overline{HOLD}$)

$\overline{HOLD}$ is used in conjunction with the $\overline{CS}$ pin to select the device. Once the part is selected and a serial sequence is underway, $\overline{HOLD}$ may be used to pause the serial communication with the controller without resetting the serial sequence. To pause, $\overline{HOLD}$ must be brought LOW while SCK is LOW. To resume communication, $\overline{HOLD}$ is brought HIGH, again while SCK is LOW. If the pause feature is not used, $\overline{HOLD}$ should be held HIGH at all times.

PIN CONFIGURATION



PIN NAMES

Symbol	Description
$\overline{CS}$	Chip Select Input
SO	Serial Output
SI	Serial Input
SCK	Serial Clock Input
$\overline{WP}$	Write Protect Input
V_{SS}	Ground
V_{CC}	Supply Voltage
$\overline{HOLD}$	Hold Input

3843 PGM T01

PRINCIPLES OF OPERATION

The X25C02 is a 256 x 8 E^2PROM designed to interface directly with the synchronous serial peripheral interface (SPI) of many popular microcontroller families.

The X25C02 contains an 8-bit instruction register. It is accessed via the SI input, with data being clocked in on the rising SCK. $\overline{CS}$ must be LOW and the $\overline{HOLD}$ and $\overline{WP}$ inputs must be HIGH during the entire operation.

Table 1 contains a list of the instructions and their opcodes. All instructions, addresses and data are transferred MSB first.

Data input is sampled on the first rising edge of SCK after $\overline{CS}$ goes LOW. SCK is static, allowing the user to stop the clock and then resume operations. If the clock line is shared with other peripheral devices on the SPI bus, the user can assert the $\overline{HOLD}$ input to place the X25C02 into a "PAUSE" condition. After releasing $\overline{HOLD}$, the X25C02 will resume operation from the point when $\overline{HOLD}$ was first asserted.

Write Enable (WREN) and Write Disable (WRDI)

The X25C02 contains a "write enable" latch. This latch must be SET before a write operation will be completed internally. The WREN instruction will set the latch and the WRDI instruction will reset the latch. This latch is automatically reset upon a power-up condition and after the completion of a byte or page write cycle. The latch is also reset if $\overline{WP}$ is brought LOW.

Table 1. Instruction Set

Instruction Name	Instruction Format*	Operation
WREN	0000 0110	Set the Write Enable Latch (Enable Write Operations)
WRDI	0000 0100	Reset the Write Enable Latch (Disable Write Operations)
READ	0000 0011	Read Data from Memory Array beginning at selected address
WRITE	0000 0010	Write Data to Memory Array beginning at Selected Address (1 to 4 Bytes)

3843 PGM T02

*Instructions are shown MSB in leftmost position. Instructions are transferred MSB first.

DEVICE OPERATION

Clock and Data Timing

Data input on the SI line is sampled and latched on the rising edge of SCK. Data is output on the SO line by the falling edge of SCK.

Read Sequence

The $\overline{CS}$ line is first pulled LOW to select the device. The 8-bit read opcode is transmitted to the X25C02, followed by the 8-bit address. After the READ opcode and byte address are sent, the data stored in the memory at the selected address is shifted out on the SO line. The data stored in memory at the next address can be read sequentially by continuing to provide clock pulses. The byte address is automatically incremented to the next higher address after each byte of data is shifted out. When the highest address is reached ($FF) the address counter rolls over to address $00 allowing the read cycle to be continued indefinitely. The read operation is terminated by taking $\overline{CS}$ HIGH. Refer to the read operation sequence illustrated in Figure 1.

Write Sequence

Prior to any attempt to write data into the X25C02, the "write enable" latch must first be set by issuing the WREN instruction (See Fig. 2). $\overline{CS}$ is first taken LOW, then the instruction is clocked into the X25C02. After all eight bits of the instruction are transmitted, $\overline{CS}$ must then be taken HIGH. If the user continues the write operation without taking $\overline{CS}$ HIGH after issuing the WREN instruction, the write operation will be ignored.

Once the "write enable" latch is set, the user may proceed by issuing the write instruction, followed by the address and then the data to be written. This is minimally a twenty-four clock operation. $\overline{CS}$ must go LOW and remain LOW for the duration of the operation. The host may continue to write up to four bytes of data to the X25C02. The only restriction is the four bytes must reside on the same page. A page address begins with address XXXX XX00 and ends with XXXX XX11. If the byte address counter reaches XXXX XX11 and the clock continues the counter will "roll over" to the first address of the page and overwrite any data that may have been written.

For the write operation (byte or page write) to be completed, $\overline{CS}$ can only be brought HIGH after the twenty-fourth, thirty-second, fourtieth or fourty-eighth clock. If it is brought HIGH at any other time, the write operation will not be completed. Refer to Figure 4 for a detailed illustration of the page write sequence and time frames in which $\overline{CS}$ going HIGH are valid.

Hold Operation

The $\overline{HOLD}$ input should be HIGH (at V_{IH}) under normal operation. If a data transfer is to be interrupted $\overline{HOLD}$ can be pulled LOW to suspend the transfer until it can be resumed. The only restriction is the SCK input must be LOW when $\overline{HOLD}$ is first pulled low and SCK must also be LOW when $\overline{HOLD}$ is released.

The $\overline{HOLD}$ input may be tied HIGH either directly to V_{CC} or tied to V_{CC} through a resistor.

Operational Notes

The X25C02 powers-up in the following state:

- The device is in the low power standby state.
- A HIGH to LOW transition on $\overline{CS}$ is required to enter an active state and receive an instruction.
- SO pin is high impedance.
- The "write enable" latch is reset.

Data Protection

The following circuitry has been included to prevent inadvertent writes:

- The "write enable" latch is reset upon power-up.
- A WREN instruction must be issued to set the "write enable" latch.
- $\overline{CS}$ must come HIGH at the proper clock count in order to start a write cycle.

The "write enable" latch is reset when $\overline{WP}$ is brought LOW.

Figure 1. Read Operation Sequence

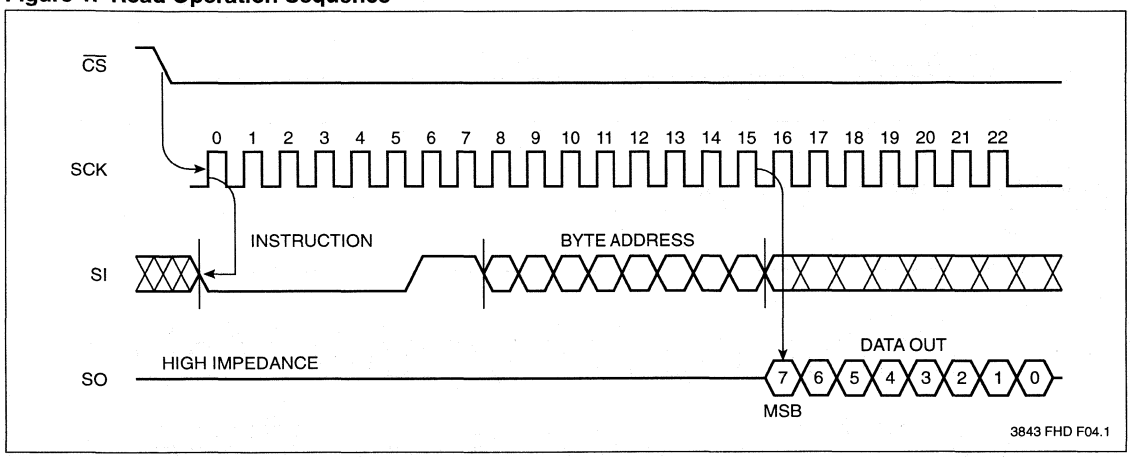


Figure 2. Set Write Enable Latch Sequence

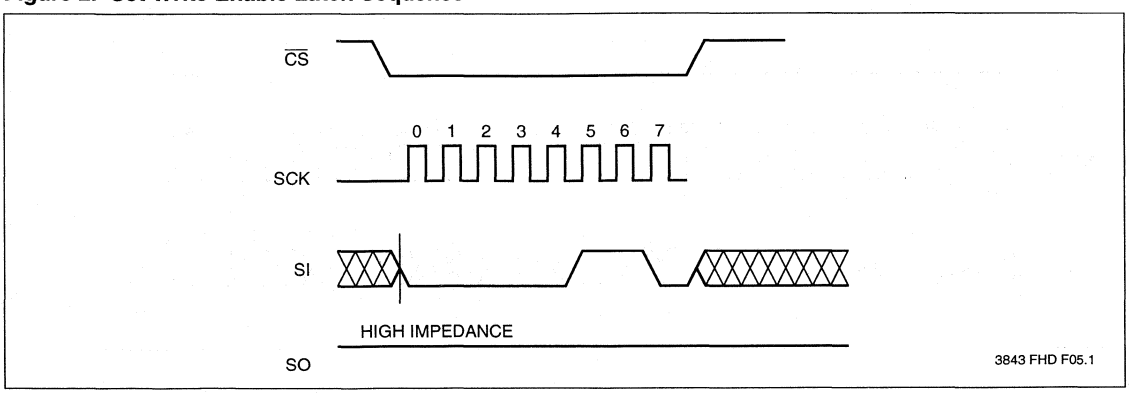


Figure 3. Byte Write Operation Sequence

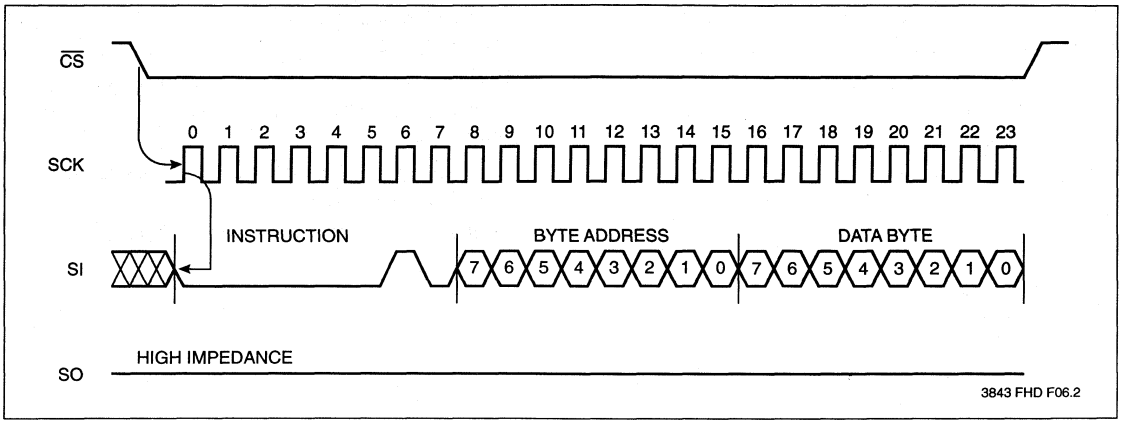
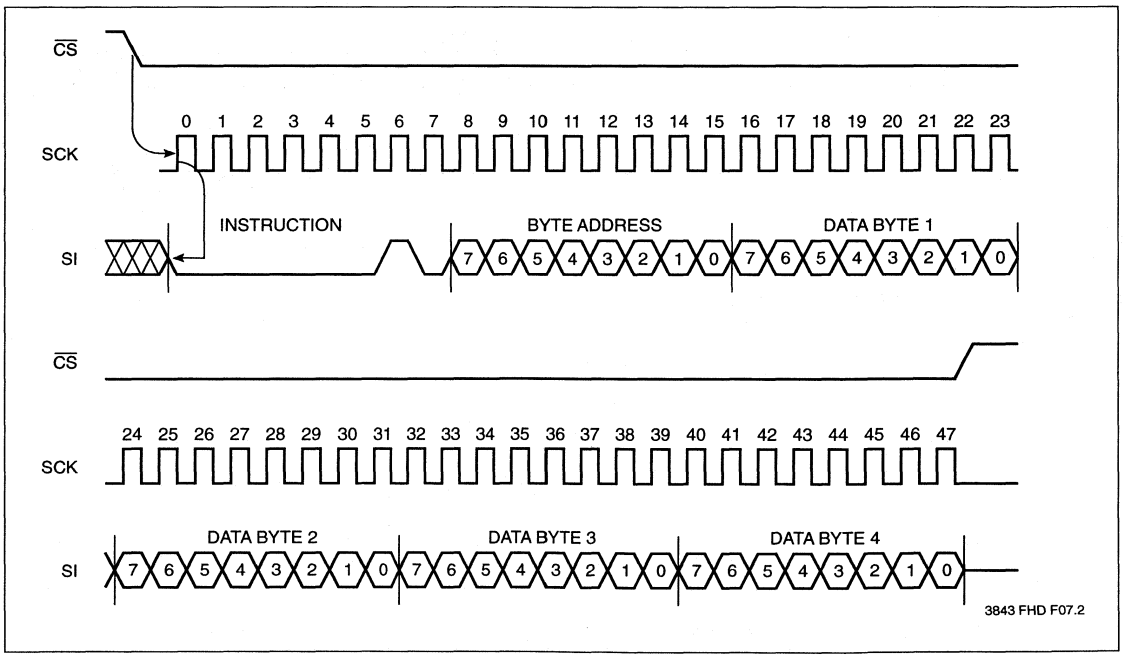


Figure 4. Page Write Operation Sequence



ABSOLUTE MAXIMUM RATINGS*

Temperature under Bias ..... –65°C to +135°C
Storage Temperature ..... –65°C to +150°C
Voltage on any Pin with Respect to V_{SS} ..... –1V to +7V
D.C. Output Current 5mA
Lead Temperature
(Soldering, 10 seconds) ..... 300°C

***COMMENT**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2

RECOMMENDED OPERATING CONDITIONS

Temp	Min.	Max.
Commercial	0°C	+70°C
Industrial	–40°C	+85°C
Military	–55°C	+125°C

3843 PGM T03.1

Supply Voltage	Limits
X25C02	5V ±10%

3843 PGM T04.1

D.C. OPERATING CHARACTERISTICS (Over the recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
I_{CC}	V_{CC} Supply Current (Active)		2	mA	SCK = V_{CC} x 0.1/V_{CC} x 0.9 @ 1MHz, SO = Open
I_{SB}	V_{CC} Supply Current (Standby)		150	µA	$\overline{CS}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC} – 0.3V
I_{LI}	Input Leakage Current		10	µA	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output Leakage Current		10	µA	V_{OUT} = V_{SS} to V_{CC}
V_{IL}(1)	Input LOW Voltage	–1	V_{CC} x 0.3	V	
V_{IH}(1)	Input HIGH Voltage	V_{CC} x 0.7	V_{CC} + 0.5	V	
V_{OL}	Output LOW Voltage		0.4	V	I_{OL} = 2mA
V_{OH}	Output HIGH Voltage	V_{CC}–0.8		V	I_{OH} = –1mA

3843 PGM T05.3

POWER-UP TIMING

Symbol	Parameter	Min.	Max.	Units
t_{PUR}(1)	Power-up to Read Operation		1	ms
t_{PUW}(1)	Power-up to Write Operation		5	ms

3843 PGM T09

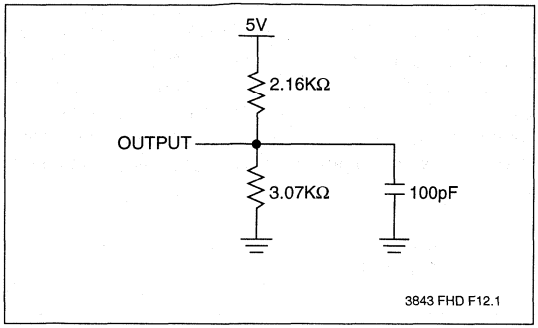
CAPACITANCE T_A = +25°C, f = 1MHz, V_{CC} = 5V.

Symbol	Test	Max.	Units	Conditions
C_{OUT}(2)	Output Capacitance (SO)	8	pF	V_{OUT} = 0V
C_{IN}(2)	Input Capacitance (SCK, SI, $\overline{CS}$, $\overline{WP}$, $\overline{HOLD}$)	6	pF	V_{IN} = 0V

3843 PGM T06.1

Notes: (1) V_{IL} min. and V_{IH} max. are for reference only and are not tested.
(2) This parameter is periodically sampled and not 100% tested.

EQUIVALENT A.C. LOAD CIRCUIT



A.C. TEST CONDITIONS

Input Pulse Levels	V_{CC} x 0.1 to V_{CC} x 0.9
Input Rise and Fall Times	10ns
Input and Output Timing Level	V_{CC} x 0.5

3843 PGM T07

A.C. CHARACTERISTICS (Over recommended operating conditions, unless otherwise specified)

Data Input Timing

Symbol	Parameter	Min.	Max.	Units
f_{SCK}	Clock Frequency	0	1	MHz
t_{CYC}	Cycle Time	1000		ns
t_{LEAD}	$\overline{CS}$ Lead Time	500		ns
t_{LAG}	$\overline{CS}$ Lag Time	500		ns
t_{WH}	Clock HIGH Time	400		ns
t_{WL}	Clock LOW Time	400		ns
t_{SU}	Data Setup Time	100		ns
t_H	Data Hold Time	100		ns
t_{RI}	Data In Rise Time		2	µs
t_{FI}	Data In Fall Time		2	µs
t_{HD}	$\overline{HOLD}$ Setup Time	200		ns
t_{CD}	$\overline{HOLD}$ Hold Time	200		ns
t_{CS}	$\overline{CS}$ Deselect Time	500		ns
t_{WC}(3)	Write Cycle Time		10	ms

3843 PGM T08.2

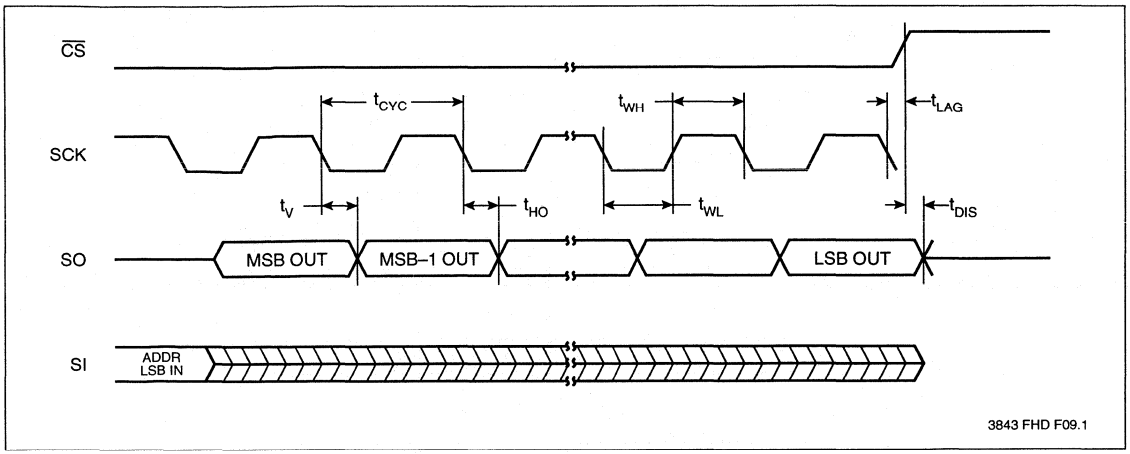
Data Output Timing

Symbol	Parameter	Min.	Max.	Units
f_{SCK}	Clock Frequency	0	1	MHz
t_{DIS}	Output Disable Time		500	ns
t_V	Output Valid from clock Low		400	ns
t_{HO}	Output Hold Time	0		ns
t_{RO}(1)	Output Rise Time		300	ns
t_{FO}(1)	Output Fall Time		300	ns
t_{LZ}	$\overline{HOLD}$ HIGH to Output in Low Z	100		ns
t_{HZ}	$\overline{HOLD}$ LOW to Output in High Z	100		ns

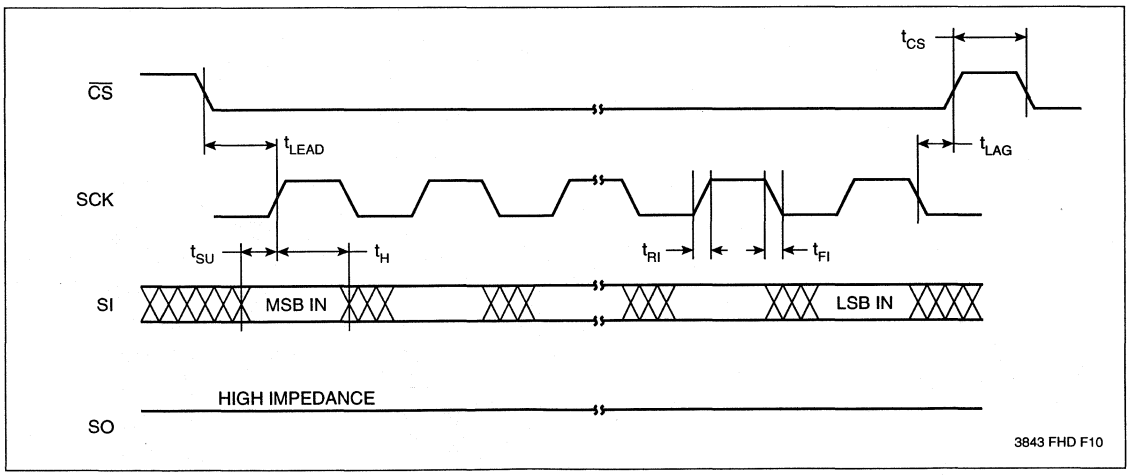
3843 PGM T09.1

Notes: (3) t_{WC} is the time from the rising edge of $\overline{CS}$ after a valid write sequence has been sent to the end of the self-timed internal nonvolatile write cycle.

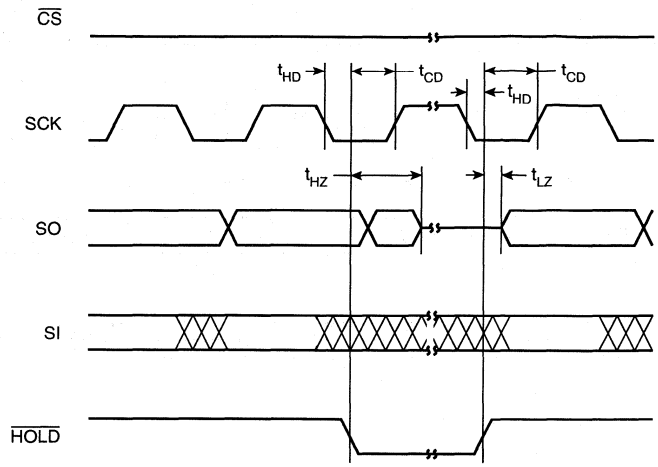
Serial Output Timing



Serial Input Timing



Hold Timing

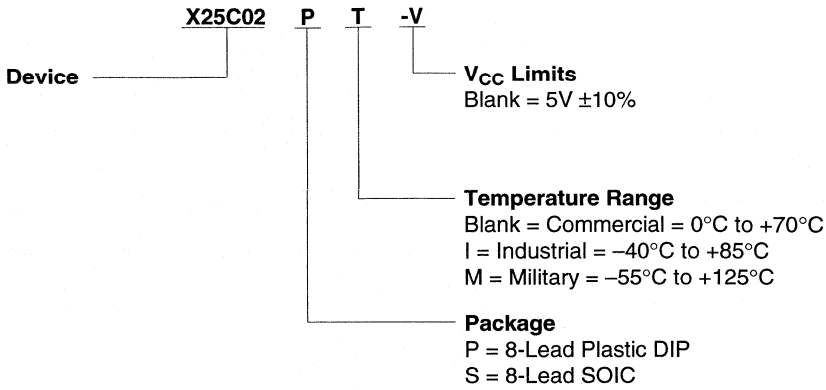


3843 FHD F11

SYMBOL TABLE

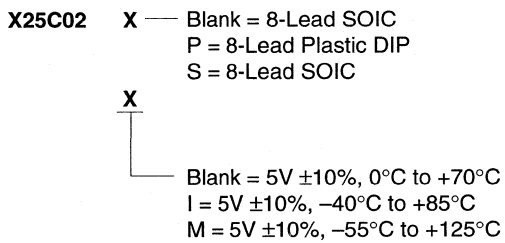
WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

ORDERING INFORMATION



2

Part Mark Convention



NOTES

Xicor®

2K X25020 256 x 8 Bit

SPI Serial E²PROM with Block Lock™ Protection

FEATURES

- 1MHz Clock Rate
- SPI Modes (0,0 & 1,1)
- 256 X 8 Bits
  - —4 Byte Page Mode
- Low Power CMOS
  - —10µA Standby Current
  - —3mA Active Write Current
- 2.7V To 5.5V Power Supply
- Block Lock Protection
  - —Protect 1/4, 1/2 or all of E²PROM Array
- Built-in Inadvertent Write Protection
  - —Power-Up/Power-Down protection circuitry
  - —Write Latch
  - —Write Protect Pin
- Self-Timed Write Cycle
  - —5ms Write Cycle Time (Typical)
- High Reliability
  - —Endurance: 100,000 cycles per byte
  - —Data Retention: 100 Years
  - —ESD protection: 2000V on all pins
- 8-Pin Mini-DIP Package
- 8-Lead SOIC Package
- 8-Lead TSSOP

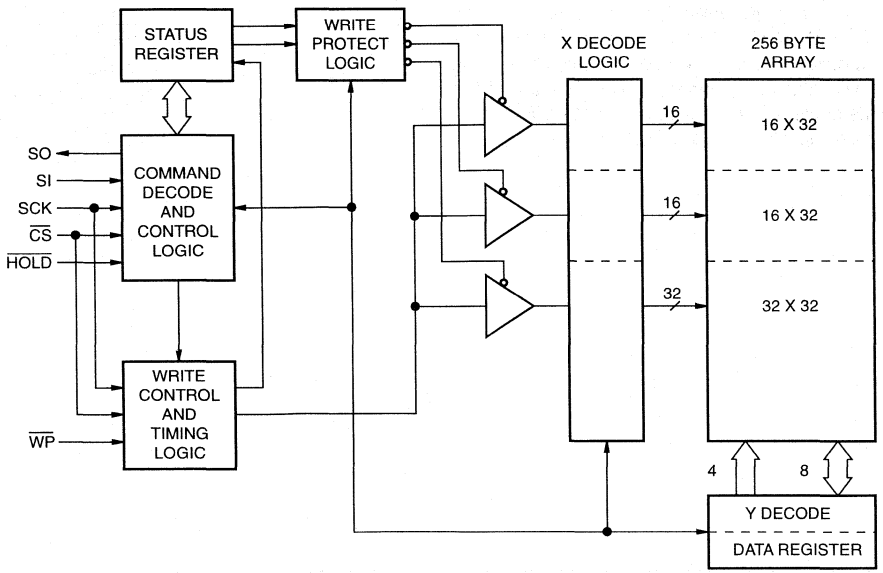
DESCRIPTION

The X25020 is a CMOS 2048-bit serial E²PROM, internally organized as 256 x 8. The X25020 features a serial interface and software protocol allowing operation on a simple three-wire bus. The bus signals are a clock input (SCK) plus separate data in (SI) and data out (SO) lines. Access to the device is controlled through a chip select ($\overline{CS}$) input, allowing any number of devices to share the same bus.

The X25020 also features two additional inputs that provide the end user with added flexibility. By asserting the $\overline{HOLD}$ input, the X25020 will ignore transitions on its inputs, thus allowing the host to service higher priority interrupts. The $\overline{WP}$ input can be used as a hardwire input to the X25020 disabling all write attempts, thus providing a mechanism for limiting end user capability of altering the memory.

The X25020 utilizes Xicor's proprietary Direct Write™ cell, providing a minimum endurance of 100,000 cycles per byte and a minimum data retention of 100 years.

FUNCTIONAL DIAGRAM



3834 FHD F01

Direct Write™ and Block Lock™ Protection is a trademark of Xicor, Inc.

PIN DESCRIPTIONS

Serial Output (SO)

SO is a push/pull serial data output pin. During a read cycle, data is shifted out on this pin. Data is clocked out by the falling edge of the serial clock.

Serial Input (SI)

SI is the serial data input pin. All opcodes, byte addresses, and data to be written to the memory are input on this pin. Data is latched by the rising edge of the serial clock.

Serial Clock (SCK)

The Serial Clock controls the serial bus timing for data input and output. Opcodes, addresses, or data present on the SI pin are latched on the rising edge of the clock input, while data on the SO pin change after the falling edge of the clock input.

Chip Select ($\overline{CS}$)

When $\overline{CS}$ is HIGH, the X25020 is deselected and the SO output pin is at high impedance and unless an internal write operation is underway, the X25020 will be in the standby power mode. $\overline{CS}$ LOW enables the X25020, placing it in the active power mode. It should be noted that after power-up, a HIGH to LOW transition on $\overline{CS}$ is required prior to the start of any operation.

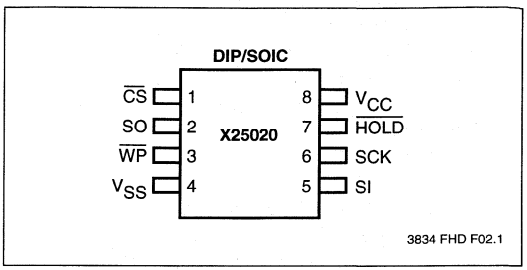
Write Protect ($\overline{WP}$)

When $\overline{WP}$ is LOW, nonvolatile writes to the X25020 are disabled, but the part otherwise functions normally. When $\overline{WP}$ is held HIGH, all functions, including nonvolatile writes operate normally. $\overline{WP}$ going LOW while $\overline{CS}$ is still LOW will interrupt a write to the X25020. If the internal write cycle has already been initiated, $\overline{WP}$ going LOW will have no affect on a write.

Hold ($\overline{HOLD}$)

$\overline{HOLD}$ is used in conjunction with the $\overline{CS}$ pin to select the device. Once the part is selected and a serial sequence is underway, $\overline{HOLD}$ may be used to pause the serial communication with the controller without resetting the serial sequence. To pause, $\overline{HOLD}$ must be brought LOW while SCK is LOW. To resume communication, $\overline{HOLD}$ is brought HIGH, again while SCK is LOW. If the pause feature is not used, $\overline{HOLD}$ should be held HIGH at all times.

PIN CONFIGURATION



3834 FHD F02.1

PIN NAMES

Symbol	Description
$\overline{CS}$	Chip Select Input
SO	Serial Output
SI	Serial Input
SCK	Serial Clock Input
$\overline{WP}$	Write Protect Input
V_{SS}	Ground
V_{CC}	Supply Voltage
$\overline{HOLD}$	Hold Input

3834 PGM T01.1

PRINCIPLES OF OPERATION

The X25020 is a 256 x 8 E^2PROM designed to interface directly with the synchronous serial peripheral interface (SPI) of many popular microcontroller families.

The X25020 contains an 8-bit instruction register. It is accessed via the SI input, with data being clocked in on the rising SCK. $\overline{CS}$ must be LOW and the $\overline{HOLD}$ and $\overline{WP}$ inputs must be HIGH during the entire operation.

Table 1 contains a list of the instructions and their opcodes. All instructions, addresses and data are transferred MSB first.

Data input is sampled on the first rising edge of SCK after $\overline{CS}$ goes LOW. SCK is static, allowing the user to stop the clock and then resume operations. If the clock line is shared with other peripheral devices on the SPI bus, the user can assert the $\overline{HOLD}$ input to place the X25020 into a "PAUSE" condition. After releasing $\overline{HOLD}$, the X25020 will resume operation from the point when $\overline{HOLD}$ was first asserted.

Write Enable Latch

The X25020 contains a "write enable" latch. This latch must be SET before a write operation will be completed internally. The WREN instruction will set the latch and the WRDI instruction will reset the latch. This latch is automatically reset upon a power-up condition and after the completion of a byte, page, or status register write cycle.

Status Register

The RDSR instruction provides access to the status register. The status register may be read at any time, even during a write cycle. The status register is formatted as follows:

7	6	5	4	3	2	1	0
X	X	X	X	BP1	BP0	WEL	WIP

3834 PGM T02

BP0 and BP1 are set by the WRSR instruction. WEL and WIP are read-only and automatically set by other operations.

The Write-In-Process (WIP) bit indicates whether the X25020 is busy with a write operation. When set to a "1", a write is in progress, when set to a "0", no write is in progress. During a write, all other bits are set to "1".

The Write Enable Latch (WEL) bit indicates the status of the "write enable" latch. When set to a "1", the latch is set, when set to a "0", the latch is reset.

The Block Protect (BP0 and BP1) bits are nonvolatile and allow the user to select one of four levels of protection. The X25020 is divided into four 512-bit segments. One, two, or all four of the segments may be protected. That is, the user may read the segments but will be unable to alter (write) data within the selected segments. The partitioning is controlled as illustrated below.

Status Register Bits		Array Addresses Protected
BP1	BP0	
0	0	None
0	1	$C0–$FF
1	0	$80–$FF
1	1	$00–$FF

3834 PGM T03

Table 1. Instruction Set

Instruction Name	Instruction Format*	Operation
WREN	0000 0110	Set the Write Enable Latch (Enable Write Operations)
WRDI	0000 0100	Reset the Write Enable Latch (Disable Write Operations)
RDSR	0000 0101	Read Status Register
WRSR	0000 0001	Write Status Register
READ	0000 0011	Read Data from Memory Array beginning at selected address
WRITE	0000 0010	Write Data to Memory Array beginning at Selected Address (1 to 32 Bytes)

3834 PGM T04

*Instructions are shown MSB in leftmost position. Instructions are transferred MSB first.

Clock and Data Timing

Data input on the SI line is latched on the rising edge of SCK. Data is output on the SO line by the falling edge of SCK.

Read Sequence

When reading from the E²PROM memory array, $\overline{CS}$ is first pulled LOW to select the device. The 8-bit READ instruction is transmitted to the X25020, followed by the 8-bit address. After the READ opcode and address are sent, the data stored in the memory at the selected address is shifted out on the SO line. The data stored in memory at the next address can be read sequentially by continuing to provide clock pulses. The address is automatically incremented to the next higher address after each byte of data is shifted out. When the highest address is reached ($FF) the address counter rolls over to address $00 allowing the read cycle to be continued indefinitely. The read operation is terminated by taking $\overline{CS}$ HIGH. Refer to the read E²PROM array operation sequence illustrated in Figure 1.

To read the status register $\overline{CS}$ line is first pulled LOW to select the device followed by the 8-bit RDSR instruction. After the read status register opcode is sent, the contents of the status register are shifted out on the SO line. Figure 2 illustrates the read status register sequence.

Write Sequence

Prior to any attempt to write data into the X25020 the "write enable" latch must first be set by issuing the WREN instruction (See Figure 3). $\overline{CS}$ is first taken LOW, then the WREN instruction is clocked into the X25020. After all eight bits of the instruction are transmitted, $\overline{CS}$ must then be taken HIGH. If the user continues the write operation without taking $\overline{CS}$ HIGH after issuing the WREN instruction, the write operation will be ignored.

To write data to the E²PROM memory array, the user issues the WRITE instruction, followed by the address and then the data to be written. This is minimally a thirty-two clock operation. $\overline{CS}$ must go LOW and remain LOW for the duration of the operation. The host may continue to write up to 4 bytes of data to the X25020. The only restriction is that the 4 bytes must reside on the same page. If the address counter reaches the end of the page and the clock continues, the counter will "roll over" to the first address of the page and overwrite any data that may have been written.

For the write operation (byte or page write) to be completed, $\overline{CS}$ can only be brought HIGH after bit 0 of data byte N is clocked in. If it is brought HIGH at any other time the write operation will not be completed. Refer to Figures 4 and 5 below for a detailed illustration of the write sequences and time frames in which $\overline{CS}$ going HIGH are valid.

To write to the status register, the WRSR instruction is followed by the data to be written. Data bits 0, 1, 4, 5, 6 and 7 must be "0". Figure 6 illustrates this sequence.

While the write is in progress following a status register or E²PROM write sequence, the status register may be read to check the WIP bit. During this time the WIP bit will be HIGH.

Hold Operation

The $\overline{HOLD}$ input should be HIGH (at V_{IH}) under normal operation. If a data transfer is to be interrupted $\overline{HOLD}$ can be pulled LOW to suspend the transfer until it can be resumed. The only restriction is the SCK input must be LOW when $\overline{HOLD}$ is first pulled LOW and SCK must also be LOW when $\overline{HOLD}$ is released.

The HOLD input may be tied HIGH either directly to V_{CC} or tied to V_{CC} through a resistor.

Operational Notes

The X25020 powers-up in the following state:

- The device is in the low power standby state.
- A HIGH to LOW transition on $\overline{CS}$ is required to enter an active state and receive an instruction.
- SO pin is high impedance.
- The "write enable" latch is reset.

Data Protection

The following circuitry has been included to prevent inadvertent writes:

- The "write enable" latch is reset upon power-up.
- A WREN instruction must be issued to set the "write enable" latch.
- $\overline{CS}$ must come HIGH at the proper clock count in order to start a write cycle.

Figure 1. Read E²PROM Array Operation Sequence

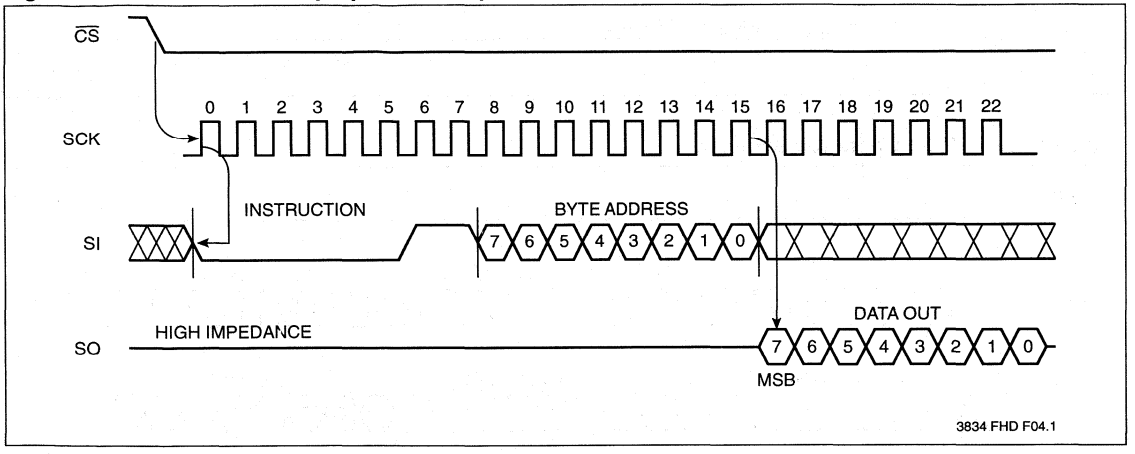


Figure 2. Read Status Register Operation Sequence

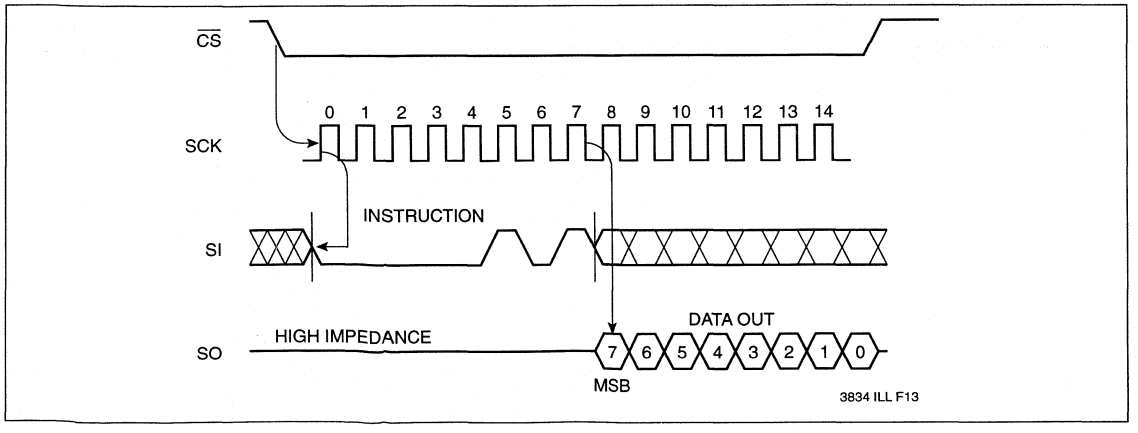


Figure 3. Write Enable Latch Sequence

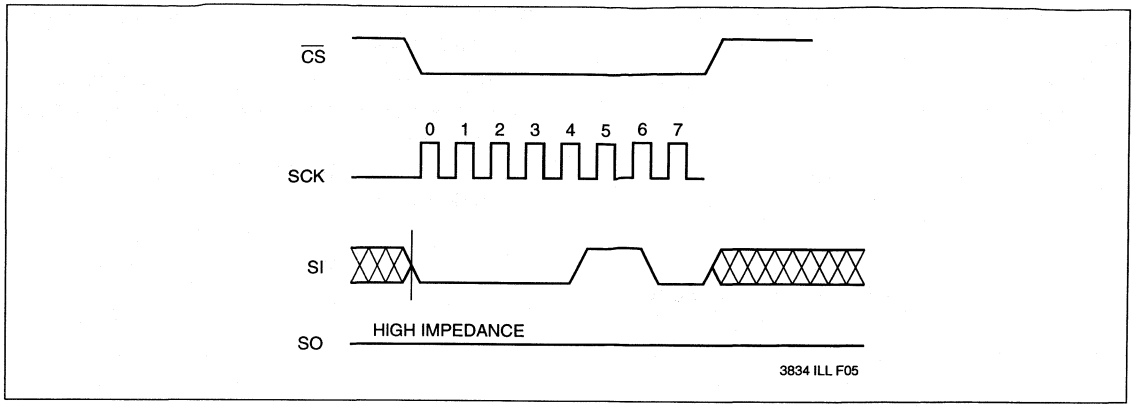


Figure 4. Byte Write Operation Sequence

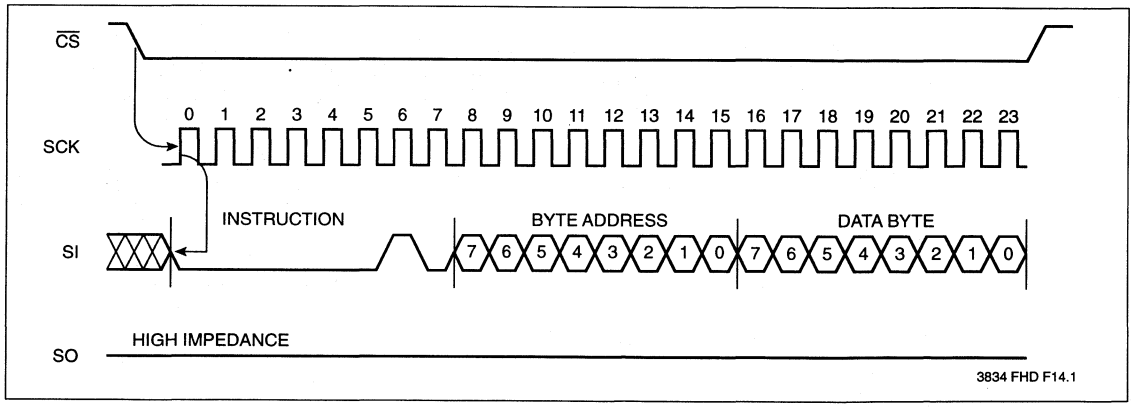


Figure 5. Page Write Operation Sequence

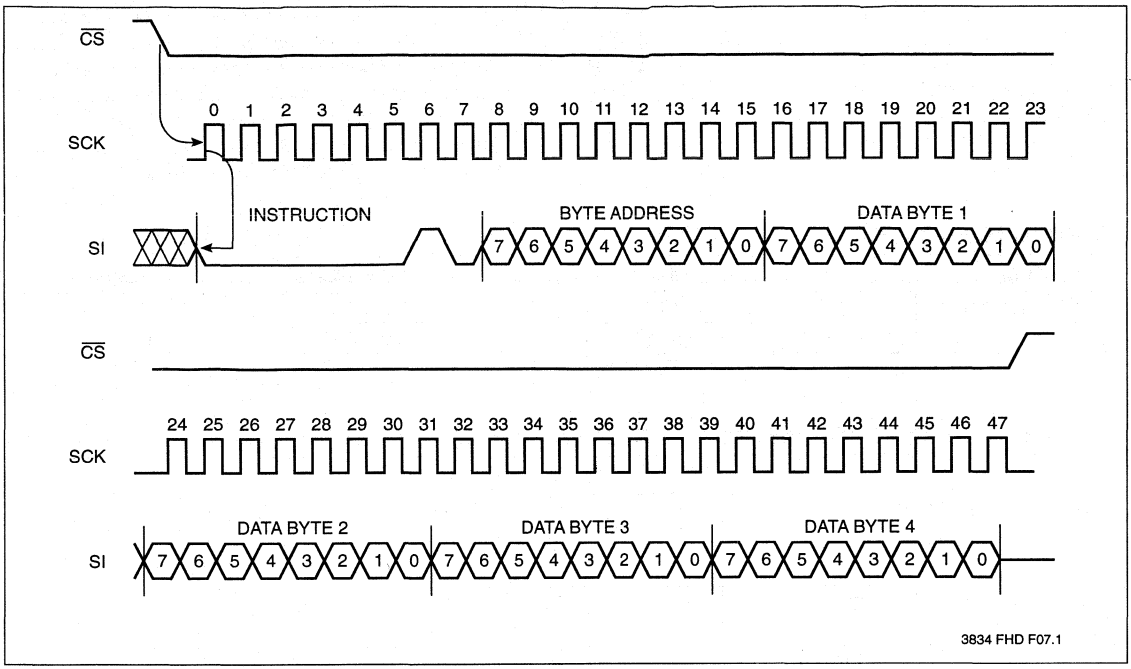
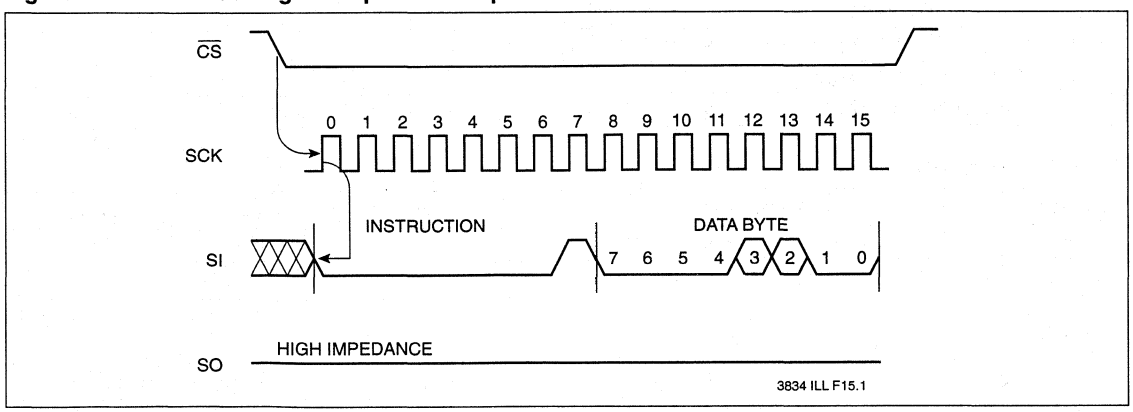


Figure 6. Write Status Register Operation Sequence



ABSOLUTE MAXIMUM RATINGS*

Temperature under Bias ..... –65°C to +135°C
Storage Temperature ..... –65°C to +150°C
Voltage on any Pin with Respect to V_{SS} ..... –1V to +7V
D.C. Output Current 5mA
Lead Temperature
(Soldering, 10 seconds) ..... 300°C

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temp	Min.	Max.
Commercial	0°C	+70°C
Industrial	–40°C	+85°C

3834 PGM T05.2

Supply Voltage	Limits
X25020	5V ±10%
X25020–3	3V to 5.5V
X25020–2.7	2.7V to 5.5V

3834 PGM T06.1

D.C. OPERATING CHARACTERISTICS (Over the recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
I_{CC}	V_{CC} Supply Current (Active)		3	mA	SCK = V_{CC} x 0.1/V_{CC} x 0.9 @ 1MHz, SO = Open
I_{SB}	V_{CC} Supply Current (Standby)		10	µA	$\overline{CS}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC} – 0.3V
I_{LI}	Input Leakage Current		10	µA	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output Leakage Current		10	µA	V_{OUT} = V_{SS} to V_{CC}
V_{IL}(1)	Input LOW Voltage	–0.5	V_{CC} x 0.3	V	
V_{IH}(1)	Input HIGH Voltage	V_{CC} x 0.7	V_{CC} + 0.5	V	
V_{OL}	Output LOW Voltage		0.4	V	I_{OL} = 2mA
V_{OH}	Output HIGH Voltage	V_{CC} – 0.8		V	I_{OH} = –1mA

3834 PGM T07.5

POWER-UP TIMING

Symbol	Parameter	Min.	Max.	Units
t_{PUR}(2)	Power-up to Read Operation		1	ms
t_{PUW}(2)	Power-up to Write Operation		5	ms

3834 PGM T08

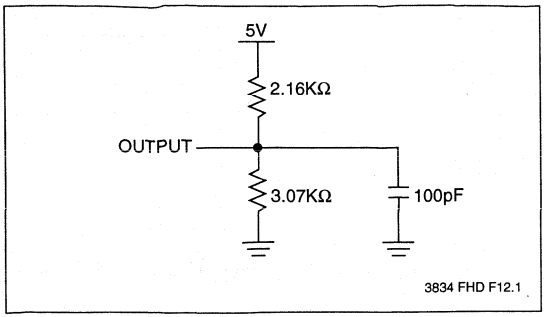
CAPACITANCE T_A = +25°C, f = 1MHz, V_{CC} = 5V.

Symbol	Test	Max.	Units	Conditions
C_{OUT}(2)	Output Capacitance (SO)	8	pF	V_{OUT} = 0V
C_{IN}(2)	Input Capacitance (SCK, SI, $\overline{CS}$, $\overline{WP}$, $\overline{HOLD}$)	6	pF	V_{IN} = 0V

3834 PGM T09.1

Notes: (1) V_{IL} min. and V_{IH} max. are for reference only and are not tested.
(2) This parameter is periodically sampled and not 100% tested.

EQUIVALENT A.C. LOAD CIRCUIT AT 5V V_{CC}



A.C. TEST CONDITIONS

Input Pulse Levels	V_{CC} x 0.1 to V_{CC} x 0.9
Input Rise and Fall Times	10ns
Input and Output Timing Level	V_{CC} x 0.5

3834 PGM T10

2

A.C. CHARACTERISTICS (Over recommended operating conditions, unless otherwise specified)

Data Input Timing

Symbol	Parameter	Min.	Max.	Units
f_{SCK}	Clock Frequency	0	1	MHz
t_{CYC}	Cycle Time	1000		ns
t_{LEAD}	$\overline{CS}$ Lead Time	500		ns
t_{LAG}	$\overline{CS}$ Lag Time	500		ns
t_{WH}	Clock HIGH Time	400		ns
t_{WL}	Clock LOW Time	400		ns
t_{SU}	Data Setup Time	100		ns
t_H	Data Hold Time	100		ns
t_{RI}	Data In Rise Time		2	µs
t_{FI}	Data In Fall Time		2	µs
t_{HD}	HOLD Setup Time	200		ns
t_{CD}	HOLD Hold Time	200		ns
t_{CS}	$\overline{CS}$ Deselect Time	500		ns
t_{WC}(3)	Write Cycle Time		10	ms

3834 PGM T11.2

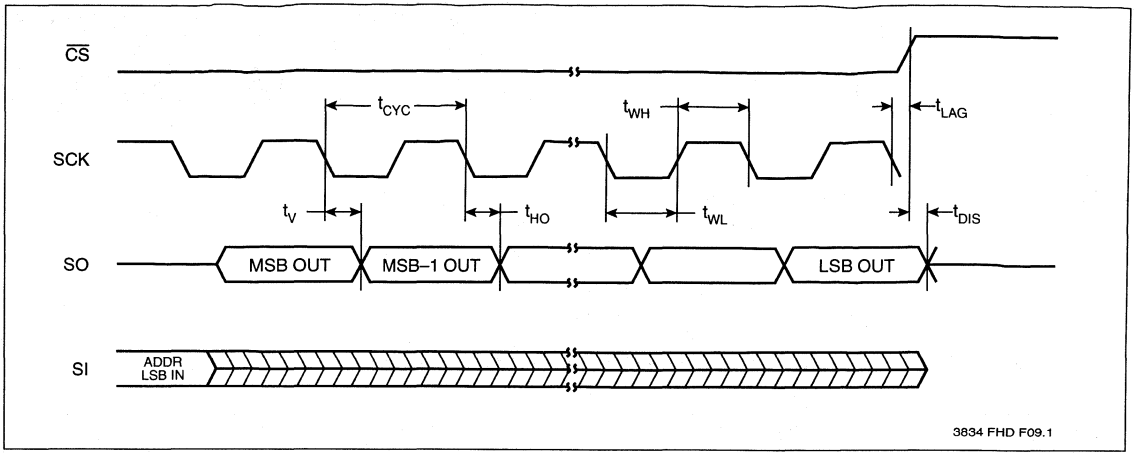
Data Output Timing

Symbol	Parameter	Min.	Max.	Units
f_{SCK}	Clock Frequency	0	1	MHz
t_{DIS}	Output Disable Time		500	ns
t_V	Output Valid from Clock LOW		360	ns
t_{HO}	Output Hold Time	0		ns
t_{RO}	Output Rise Time		300	ns
t_{FO}	Output Fall Time		300	ns
t_{LZ}	HOLD HIGH to Output in Low Z	100		ns
t_{HZ}	HOLD LOW to Output in High Z	100		ns

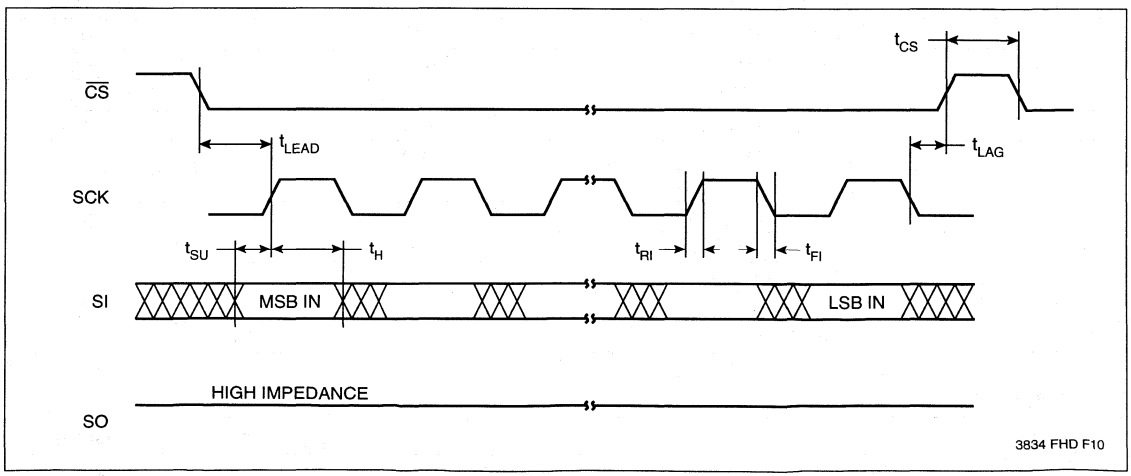
3834 PGM T12.1

Notes: (3) t_{WC} is the time from the rising edge of $\overline{CS}$ after a valid write sequence has been sent to the end of the self-timed internal nonvolatile write cycle.

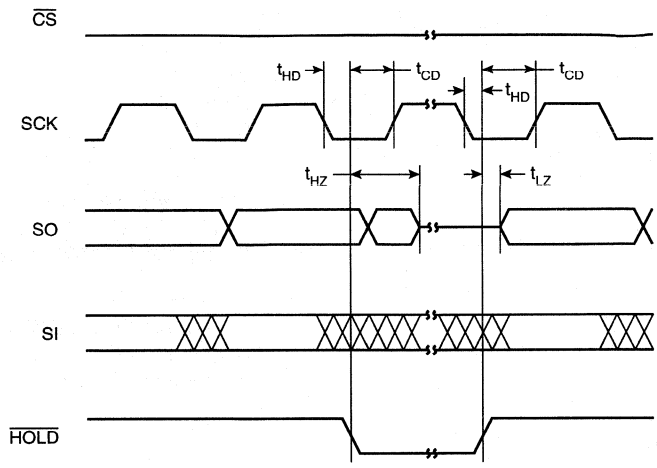
Serial Output Timing



Serial Input Timing



Hold Timing

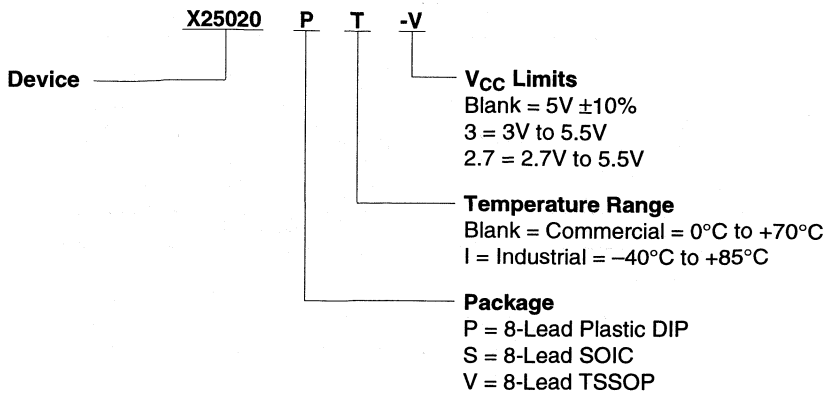


3834 FHD F11

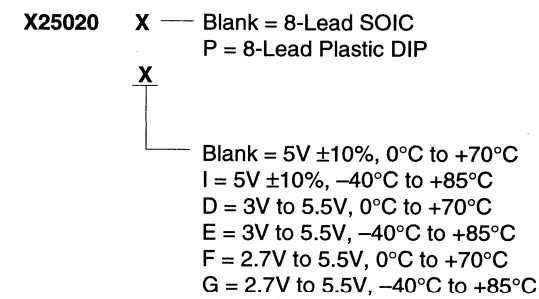
SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

ORDERING INFORMATION



Part Mark Convention



SPI Serial E²PROM with Block Lock™ Protection

FEATURES

- 1MHz Clock Rate
- SPI Modes (0,1 & 1,0)
- 256 X 8 Bits
  - —4 Byte Page Mode
- Low Power CMOS
  - —10μA Standby Current
  - —3mA Active Current
- 2.7V To 5.5V Power Supply
- Block Lock Protection
  - —Protect 1/4, 1/2 or all of E²PROM Array
- Built-in Inadvertent Write Protection
  - —Power-Up/Power-Down protection circuitry
  - —Write Latch
  - —Write Protect Pin
- Self-Timed Write Cycle
  - —5ms Write Cycle Time (Typical)
- High Reliability
  - —Endurance: 100,000 cycles per byte
  - —Data Retention: 100 Years
  - —ESD protection: 2000V on all pins
- 8-Pin Mini-DIP Package
- 8-Lead SOIC Package
- 8-Lead TSSOP

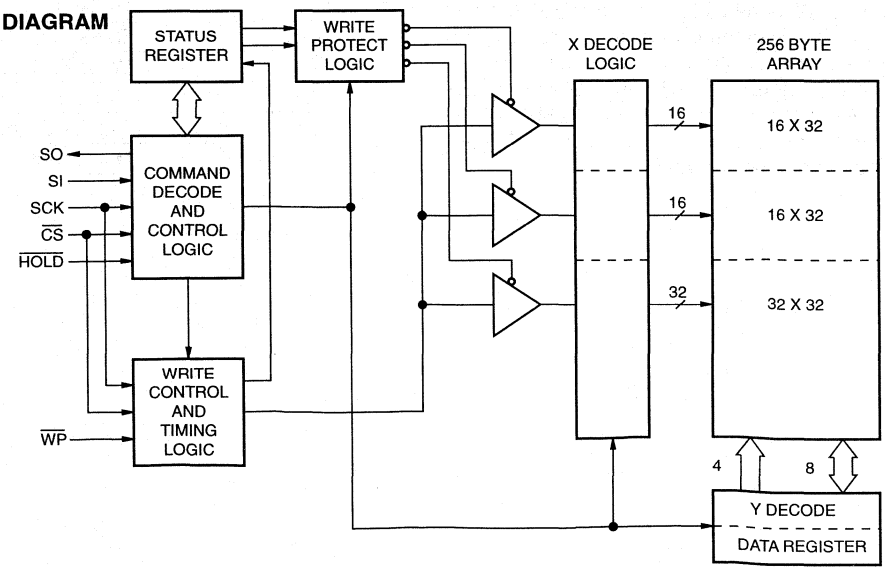
DESCRIPTION

The X25021 is a CMOS 2048-bit serial E²PROM, internally organized as 256 x 8. The X25021 features a Serial Peripheral Interface (SPI) and software protocol allowing operation on a simple three-wire bus. The bus signals are a clock input (SCK) plus separate data in (SI) and data out (SO) lines. Access to the device is controlled through a chip select ($\overline{CS}$) input, allowing any number of devices to share the same bus.

The X25021 also features two additional inputs that provide the end user with added flexibility. By asserting the $\overline{HOLD}$ input, the X25021 will ignore transitions on its inputs, thus allowing the host to service higher priority interrupts. The $\overline{WP}$ input can be used as a hardwire input to the X25021 disabling all write attempts, thus providing a mechanism for limiting end user capability of altering the memory.

The X25021 utilizes Xicor's proprietary Direct Write™ cell, providing a minimum endurance of 100,000 cycles per byte and a minimum data retention of 100 years.

FUNCTIONAL DIAGRAM



Direct Write™ and Block Lock™ Protection is a trademark of Xicor, Inc.

6615 FHD F01

6615-1.4 1/12/96 T4/C0/D0 NS

PIN DESCRIPTIONS

Serial Output (SO)

SO is a push/pull serial data output pin. During a read cycle, data is shifted out on this pin. Data is clocked out by the rising edge of the serial clock.

Serial Input (SI)

SI is the serial data input pin. All opcodes, byte addresses, and data to be written to the memory are input on this pin. Data is latched by the falling edge of the serial clock.

Serial Clock (SCK)

The Serial Clock controls the serial bus timing for data input and output. Opcodes, addresses, or data present on the SI pin are latched on the falling edge of the clock input, while data on the SO pin change after the rising edge of the clock input.

Chip Select ($\overline{CS}$)

When $\overline{CS}$ is HIGH, the X25021 is deselected and the SO output pin is at high impedance and unless an internal write operation is underway, the X25021 will be in the standby power mode. $\overline{CS}$ LOW enables the X25021, placing it in the active power mode. It should be noted that after power-up, a HIGH to LOW transition on $\overline{CS}$ is required prior to the start of any operation.

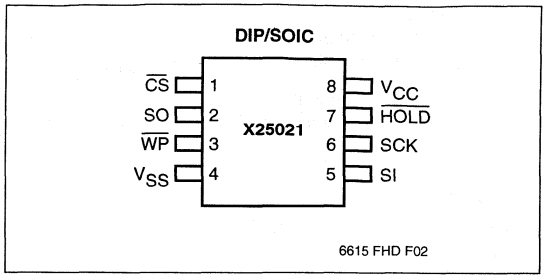
Write Protect ($\overline{WP}$)

When $\overline{WP}$ is LOW, nonvolatile writes to the X25021 are disabled, but the part otherwise functions normally. When $\overline{WP}$ is held HIGH, all functions, including nonvolatile writes operate normally. $\overline{WP}$ going LOW while $\overline{CS}$ is still LOW will interrupt a write to the X25021. If the internal write cycle has already been initiated, $\overline{WP}$ going LOW will have no affect on a write.

Hold ($\overline{HOLD}$)

$\overline{HOLD}$ is used in conjunction with the $\overline{CS}$ pin to select the device. Once the part is selected and a serial sequence is underway, $\overline{HOLD}$ may be used to pause the serial communication with the controller without resetting the serial sequence. To pause, $\overline{HOLD}$ must be brought LOW while SCK is HIGH. To resume communication, $\overline{HOLD}$ is brought HIGH, again while SCK is HIGH. If the pause feature is not used, $\overline{HOLD}$ should be held HIGH at all times.

PIN CONFIGURATION



PIN NAMES

Symbol	Description
$\overline{CS}$	Chip Select Input
SO	Serial Output
SI	Serial Input
SCK	Serial Clock Input
$\overline{WP}$	Write Protect Input
V_{SS}	Ground
V_{CC}	Supply Voltage
$\overline{HOLD}$	Hold Input

6615 PGM T01

PRINCIPLES OF OPERATION

The X25021 is a 256 x 8 E^2PROM designed to interface directly with the synchronous serial peripheral interface (SPI) of many popular microcontroller families.

The X25021 contains an 8-bit instruction register. It is accessed via the SI input, with data being clocked in on the falling SCK. $\overline{CS}$ must be LOW during the entire operation.

Table 1 contains a list of the instructions and their codes. All instructions, addresses and data are transferred MSB first.

Data input is sampled on the first falling edge of SCK after $\overline{CS}$ goes LOW. SCK is static, allowing the user to stop the clock and then resume operations. If the clock line is shared with other peripheral devices on the SPI bus, the user can assert the $\overline{HOLD}$ input to place the X25021 into a "PAUSE" condition. After releasing $\overline{HOLD}$, the X25021 will resume operation from the point when $\overline{HOLD}$ was first asserted.

Write Enable Latch

The X25021 contains a "write enable" latch. This latch must be SET before a write operation will be completed internally. The WREN instruction will set the latch and the WRDI instruction will reset the latch. This latch is automatically reset upon a power-up condition and after the completion of a byte, page, or status register write cycle.

Status Register

The RDSR instruction provides access to the status register. The status register may be read at any time, even during a write cycle. The status register is formatted as follows:

7	6	5	4	3	2	1	0
X	X	X	X	BP1	BP0	WEL	WIP

6615 PGM T02

BP0 and BP1 are set by the WRSR instruction. WEL and WIP are read-only and automatically set by other operations.

The Write-In-Process (WIP) bit indicates whether the X25021 is busy with a write operation. When set to a "1", a write is in progress, when set to a "0", no write is in progress. During a write, all other bits are set to "1".

The Write Enable Latch (WEL) bit indicates the status of the "write enable" latch. When set to a "1", the latch is set, when set to a "0", the latch is reset.

The Block Protect (BP0 and BP1) bits are nonvolatile and allow the user to select one of four levels of protection. The X25021 is divided into four 1024-bit segments. One, two, or all four of the segments may be protected. That is, the user may read the segments but will be unable to alter (write) data within the selected segments. The partitioning is controlled as illustrated below.

Status Register Bits		Array Addresses
BP1	BP0	Protected
0	0	None
0	1	$C0–$FF
1	0	$80–$FF
1	1	$00–$FF

6615 PGM T03

Table 1. Instruction Set

Instruction Name	Instruction Format*	Operation
WREN	0000 0110	Set the Write Enable Latch (Enable Write Operations)
WRDI	0000 0100	Reset the Write Enable Latch (Disable Write Operations)
RDSR	0000 0101	Read Status Register
WRSR	0000 0001	Write Status Register
READ	0000 0011	Read Data from Memory Array beginning at selected address
WRITE	0000 0010	Write Data to Memory Array beginning at Selected Address (1 to 32 Bytes)

6615 PGM T04

*Instructions are shown MSB in leftmost position. Instructions are transferred MSB first.

Clock and Data Timing

Data input on the SI line is latched on the falling edge of SCK. Data is output on the SO line by the rising edge of SCK.

Read Sequence

When reading from the E²PROM memory array, $\overline{CS}$ is first pulled LOW to select the device. The 8-bit READ instruction is transmitted to the X25021, followed by the 8-bit address. After the READ opcode and address are sent, the data stored in the memory at the selected address is shifted out on the SO line. The data stored in memory at the next address can be read sequentially by continuing to provide clock pulses. The address is automatically incremented to the next higher address after each byte of data is shifted out. When the highest address is reached ($FF) the address counter rolls over to address $00 allowing the read cycle to be continued indefinitely. The read operation is terminated by taking $\overline{CS}$ HIGH. Refer to the read E²PROM array operation sequence illustrated in Figure 1.

To read the status register, the $\overline{CS}$ line is first pulled LOW to select the device followed by the 8-bit RDSR instruction. After the read status register opcode is sent, the contents of the status register are shifted out on the SO line. Figure 2 illustrates the read status register sequence.

Write Sequence

Prior to any attempt to write data into the X25021, the "write enable" latch must first be set by issuing the WREN instruction (See Figure 3). $\overline{CS}$ is first taken LOW, then the WREN instruction is clocked into the X25021. After all eight bits of the instruction are transmitted, $\overline{CS}$ must then be taken HIGH. If the user continues the write operation without taking $\overline{CS}$ HIGH after issuing the WREN instruction, the write operation will be ignored.

To write data to the E²PROM memory array, the user issues the WRITE instruction, followed by the address and then the data to be written. This is minimally a twenty-four clock operation. $\overline{CS}$ must go LOW and remain LOW for the duration of the operation. The host may continue to write up to 4 bytes of data to the X25021. The only restriction is the 4 bytes must reside on the same page. If the address counter reaches the end of the page and the clock continues, the counter will "roll over" to the first address of the page and overwrite any data that may have been written.

For the write operation (byte or page write) to be completed, $\overline{CS}$ can only be brought HIGH after bit 0 of data byte N is clocked in. If it is brought HIGH at any other time the write operation will not be completed. Refer to Figures 4 and 5 below for a detailed illustration of the write sequences and time frames in which $\overline{CS}$ going HIGH are valid.

To write to the status register, the WRSR instruction is followed by the data to be written. Data bits 0, 1, 4, 5, 6 and 7 must be "0". Figure 6 illustrates this sequence.

While the write is in progress following a status register or E²PROM write sequence, the status register may be read to check the WIP bit. During this time the WIP bit will be HIGH.

Hold Operation

The $\overline{HOLD}$ input should be HIGH (at V_{IH}) under normal operation. If a data transfer is to be interrupted $\overline{HOLD}$ can be pulled LOW to suspend the transfer until it can be resumed. The only restriction is the SCK input must be HIGH when $\overline{HOLD}$ is first pulled LOW and SCK must also be HIGH when $\overline{HOLD}$ is released.

The HOLD input may be tied HIGH either directly to V_{CC} or tied to V_{CC} through a resistor.

Operational Notes

The X25021 powers-up in the following state:

- The device is in the low power standby state.
- A HIGH to LOW transition on $\overline{CS}$ is required to enter an active state and receive an instruction.
- SO pin is high impedance.
- The "write enable" latch is reset.

Data Protection

The following circuitry has been included to prevent inadvertent writes:

- The "write enable" latch is reset upon power-up.
- A WREN instruction must be issued to set the "write enable" latch.
- $\overline{CS}$ must come HIGH at the proper clock count in order to start a write cycle.

Figure 1. Read E²PROM Array Operation Sequence

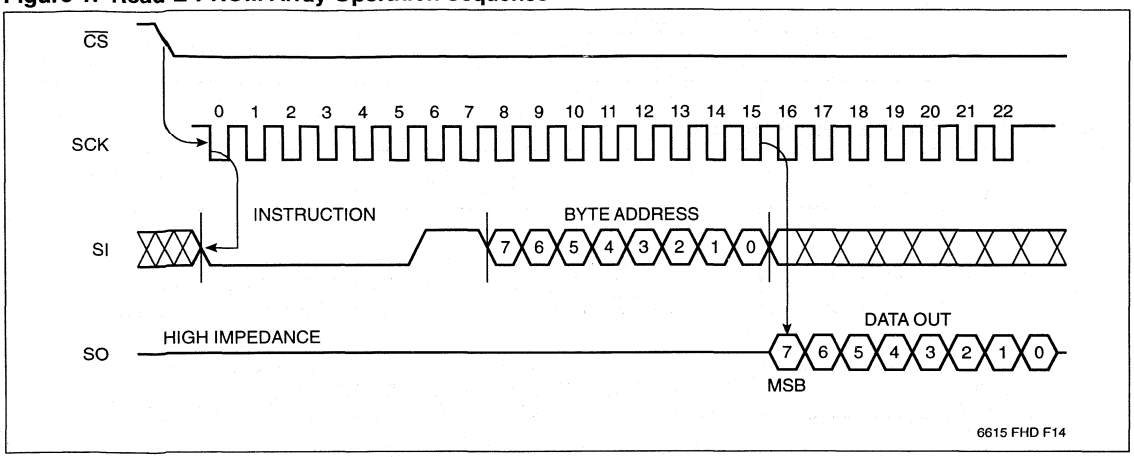


Figure 2. Read Status Register Operation Sequence

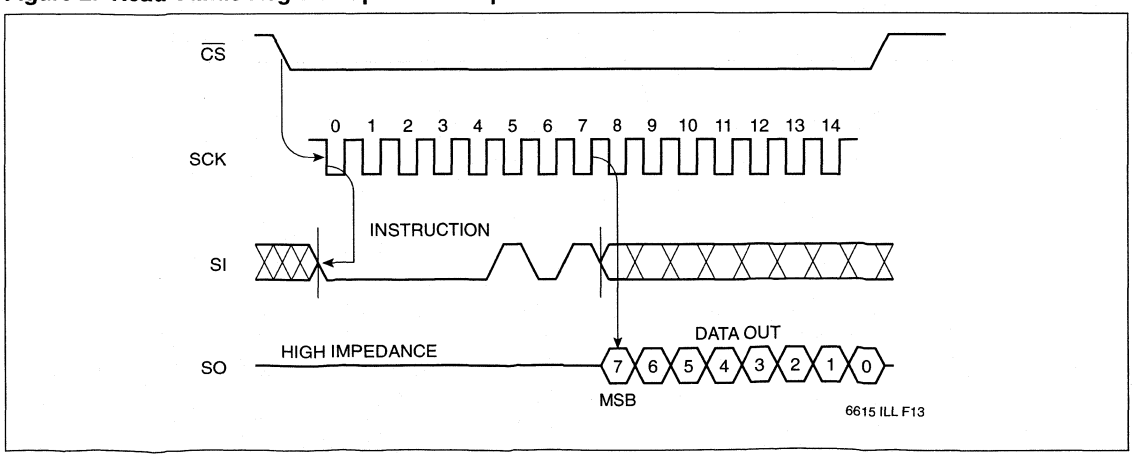


Figure 3. Write Enable Latch Sequence

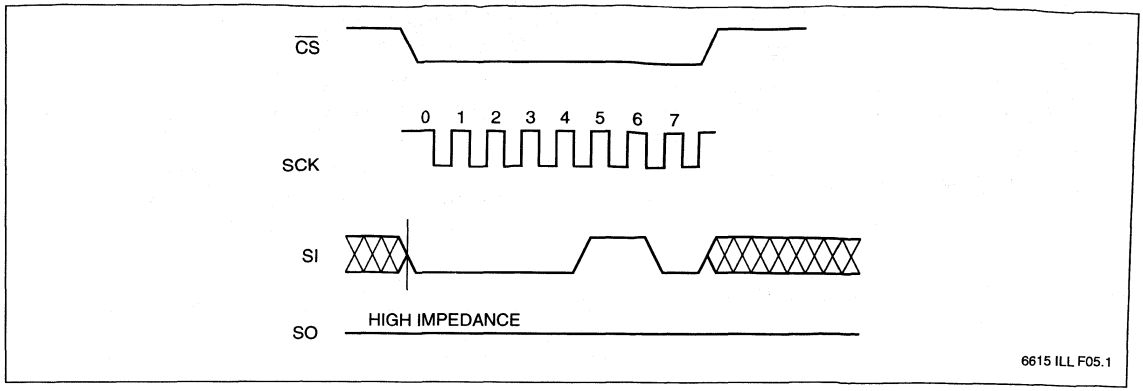


Figure 4. Byte Write Operation Sequence

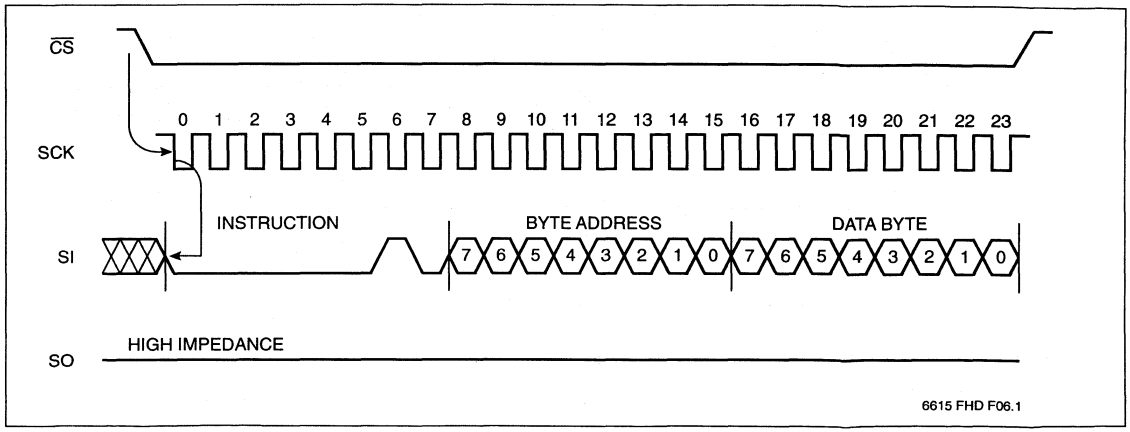


Figure 5. Page Write Operation Sequence

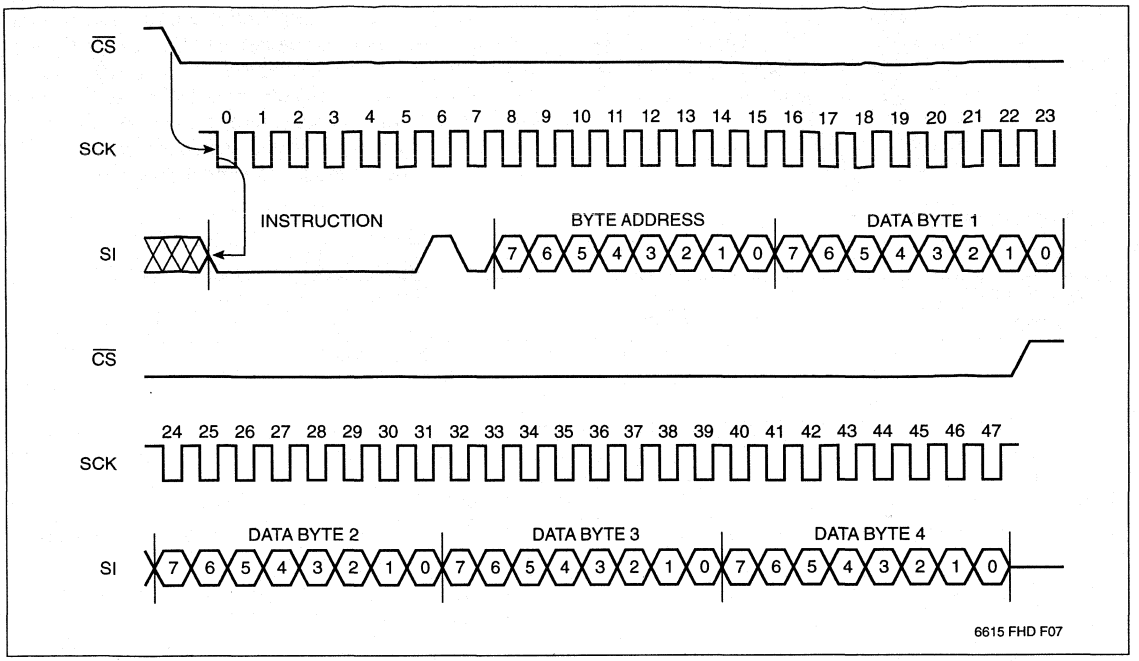
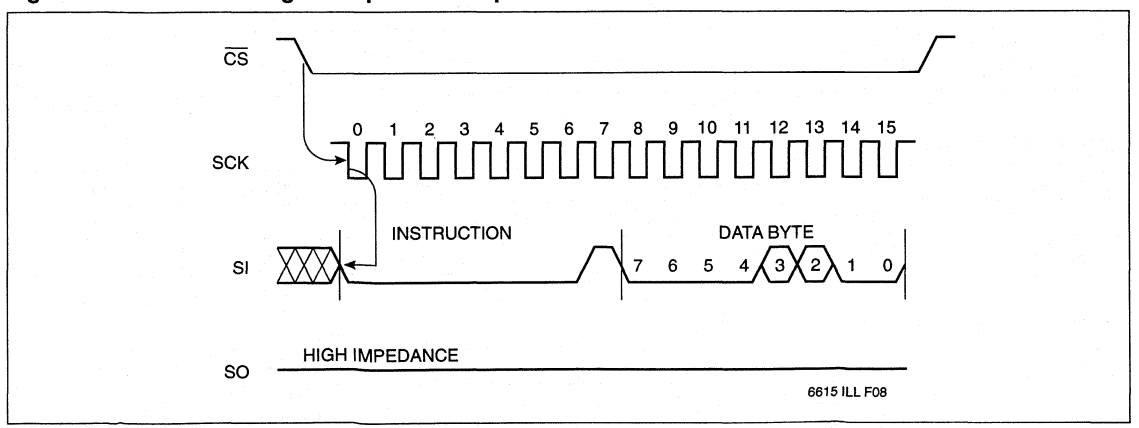


Figure 6. Write Status Register Operation Sequence



ABSOLUTE MAXIMUM RATINGS*

Temperature under Bias ..... –65°C to +135°C
Storage Temperature ..... –65°C to +150°C
Voltage on any Pin with Respect to V_{SS} ..... –1V to +7V
D.C. Output Current 5mA
Lead Temperature
(Soldering, 10 seconds) ..... 300°C

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temp	Min.	Max.
Commercial	0°C	+70°C
Industrial	–40°C	+85°C

6615 PGM T05.1

Supply Voltage	Limits
X25021	5V ±10%
X25021-3	3V to 5.5V
X25021-2.7	2.7 to 5.5V

6615 PGM T06

D.C. OPERATING CHARACTERISTICS (Over the recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
I_{CC}	V_{CC} Supply Current (Active)		3	mA	SCK = V_{CC} x 0.1/V_{CC} x 0.9 @ 1MHz, SO = Open
I_{SB}	V_{CC} Supply Current (Standby)		10	µA	$\overline{CS}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC} – 0.3V
I_{LI}	Input Leakage Current		10	µA	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output Leakage Current		10	µA	V_{OUT} = V_{SS} to V_{CC}
V_{IL}(1)	Input LOW Voltage	–0.5	V_{CC} x 0.3	V	
V_{IH}(1)	Input HIGH Voltage	V_{CC} x 0.7	V_{CC} + 0.5	V	
V_{OL}	Output LOW Voltage		0.4	V	I_{OL} = 2mA
V_{OH}	Output HIGH Voltage	V_{CC} – 0.8		V	I_{OH} = –1mA

6615 PGM T07.2

POWER-UP TIMING

Symbol	Parameter	Min.	Max.	Units
t_{PUR}(2)	Power-up to Read Operation		1	ms
t_{PUW}(2)	Power-up to Write Operation		5	ms

6615 PGM T08

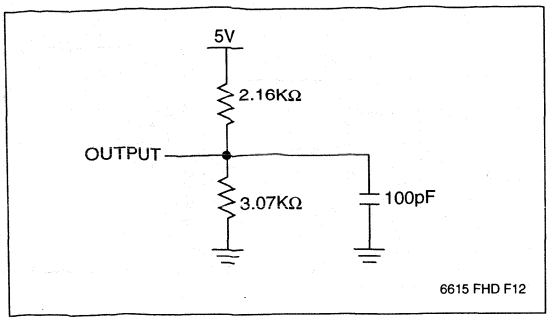
CAPACITANCE T_A = +25°C, f = 1MHz, V_{CC} = 5V.

Symbol	Test	Max.	Units	Conditions
C_{OUT}(2)	Output Capacitance (SO)	8	pF	V_{OUT} = 0V
C_{IN}(2)	Input Capacitance (SCK, SI, $\overline{CS}$, $\overline{WP}$, $\overline{HOLD}$)	6	pF	V_{IN} = 0V

6615 PGM T09

Notes: (1) V_{IL} min. and V_{IH} max. are for reference only and are not tested.
(2) This parameter is periodically sampled and not 100% tested.

EQUIVALENT A.C. LOAD CIRCUIT AT 5V V_{CC}



A.C. TEST CONDITIONS

Input Pulse Levels	V_{CC} x 0.1 to V_{CC} x 0.9
Input Rise and Fall Times	10ns
Input and Output Timing Level	V_{CC} x 0.5

6615 PGM T10

2

A.C. CHARACTERISTICS (Over recommended operating conditions, unless otherwise specified)

Data Input Timing

Symbol	Parameter	Min.	Max.	Units
f_{SCK}	Clock Frequency	0	1	MHz
t_{CYC}	Cycle Time	1000		ns
t_{LEAD}	$\overline{CS}$ Lead Time	500		ns
t_{LAG}	$\overline{CS}$ Lag Time	500		ns
t_{WH}	Clock HIGH Time	400		ns
t_{WL}	Clock LOW Time	400		ns
t_{SU}	Data Setup Time	100		ns
t_H	Data Hold Time	100		ns
t_{RI}	Data In Rise Time		2	µs
t_{FI}	Data In Fall Time		2	µs
t_{HD}	$\overline{HOLD}$ Setup Time	200		ns
t_{CD}	$\overline{HOLD}$ Hold Time	200		ns
t_{CS}	$\overline{CS}$ Deselect Time	500		ns
t_{WC}(4)	Write Cycle Time		10	ms

6615 PGM T11.1

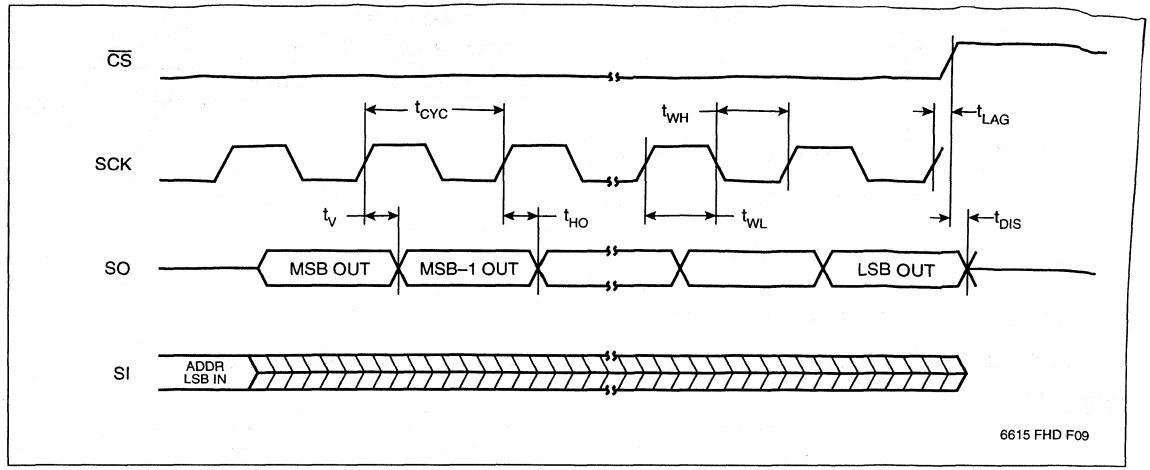
Data Output Timing

Symbol	Parameter	Min.	Max.	Units
f_{SCK}	Clock Frequency	0	1	MHz
t_{DIS}	Output Disable Time		500	ns
t_V	Output Valid from Clock LOW		400	ns
t_{HO}	Output Hold Time	0		ns
t_{RO}(3)	Output Rise Time		300	ns
t_{FO}(3)	Output Fall Time		300	ns
t_{LZ}	$\overline{HOLD}$ HIGH to Output in Low Z	100		ns
t_{HZ}	$\overline{HOLD}$ LOW to Output in High Z	100		ns

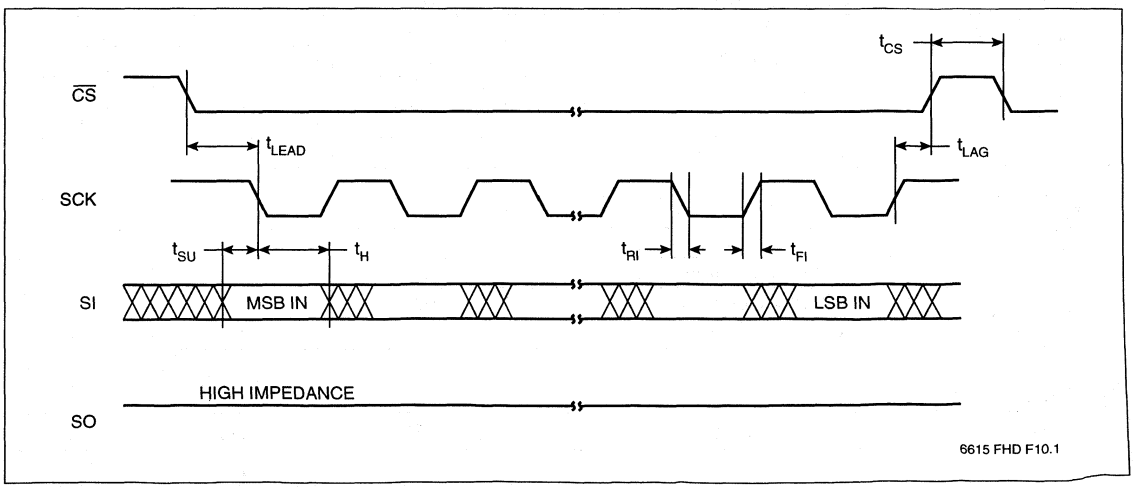
6615 PGM T12.1

Notes: (3) This parameter is periodically sampled and not 100% tested.
(4) t_{WC} is the time from the rising edge of $\overline{CS}$ after a valid write sequence has been sent to the end of the self-timed internal nonvolatile write cycle.

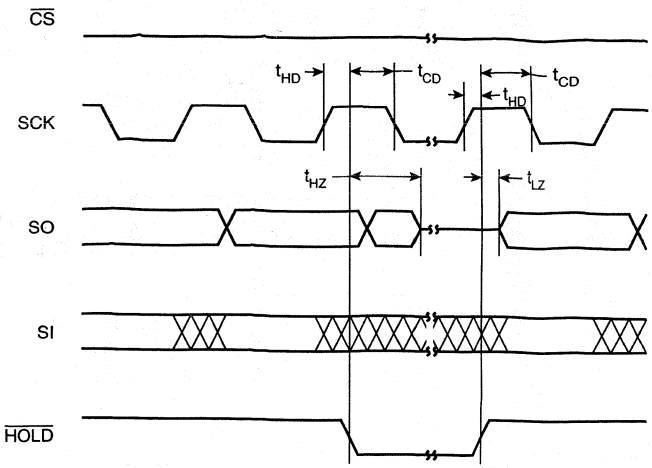
Serial Output Timing



Serial Input Timing



Hold Timing

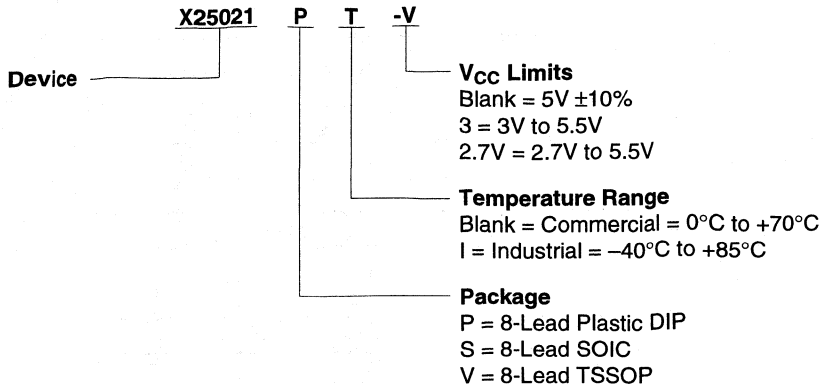


6615 FHD F11

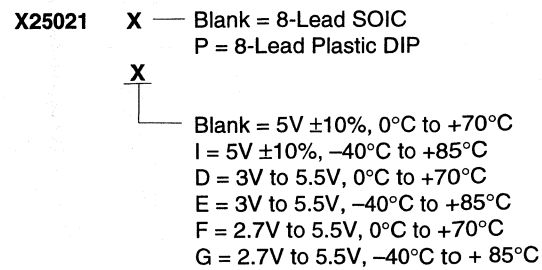
SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

ORDERING INFORMATION



Part Mark Convention



APPLICATION NOTES
AVAILABLE
AN9 • AN18 • AN31 • AN37 • AN40

4K X25040 512 x 8 Bit

SPI Serial E²PROM With BLOCK LOCK™ PROTECTION

FEATURES

- 1MHz Clock Rate
- SPI Modes (0,0 & 1,1)
- 512 X 8 Bits
  - —4 Byte Page Mode
- Low Power CMOS
  - —150µA Standby Current
  - —3mA Active Current
- 2.7V To 5.5V Power Supply
- Block Lock Protection
  - —Protect 1/4, 1/2 or all of E²PROM Array
- Built-in Inadvertent Write Protection
  - —Power-Up/Power-Down protection circuitry
  - —Write Latch
  - —Write Protect Pin
- Self-Timed Write Cycle
  - —5ms Write Cycle Time (Typical)
- High Reliability
  - —Endurance: 100,000 cycles per byte
  - —Data Retention: 100 Years
  - —ESD protection: 2000V on all pins
- 8-Pin Mini-DIP Package
- 8-Lead SOIC Package
- 8-Lead TSSOP

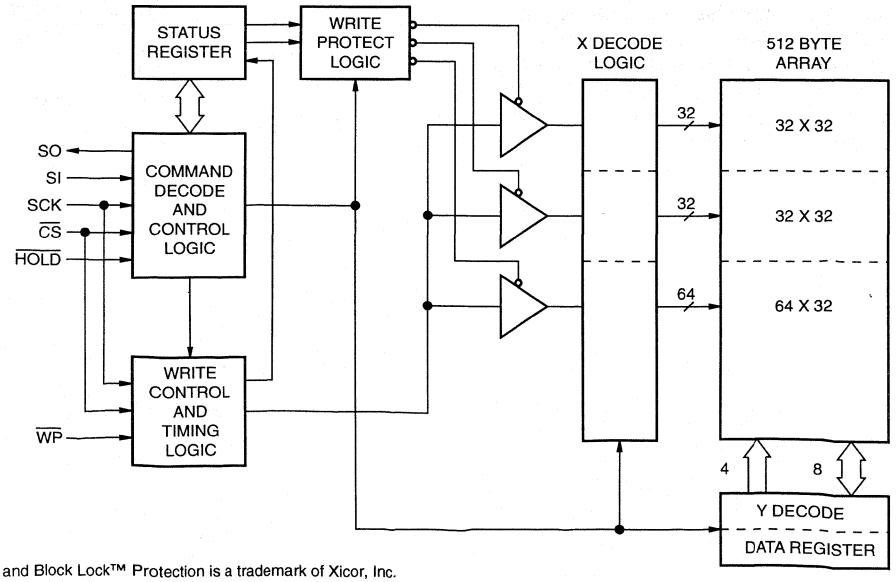
DESCRIPTION

The X25040 is a CMOS 4096-bit serial E²PROM, internally organized as 512 x 8. The X25040 features a Serial Peripheral Interface (SPI) and software protocol allowing operation on a simple three-wire bus. The bus signals are a clock input (SCK) plus separate data in (SI) and data out (SO) lines. Access to the device is controlled through a chip select ($\overline{CS}$) input, allowing any number of devices to share the same bus.

The X25040 also features two additional inputs that provide the end user with added flexibility. By asserting the $\overline{HOLD}$ input, the X25040 will ignore transitions on its inputs, thus allowing the host to service higher priority interrupts. The $\overline{WP}$ input can be used as a hardwire input to the X25040 disabling all write attempts, thus providing a mechanism for limiting end user capability of altering the memory.

The X25040 utilizes Xicor's proprietary Direct Write™ cell, providing a minimum endurance of 100,000 cycles per byte and a minimum data retention of 100 years.

FUNCTIONAL DIAGRAM



Direct Write™ and Block Lock™ Protection is a trademark of Xicor, Inc.

6451 FHD F01

6451-3.5 5/26/95 T16/C6/D0 TD

PIN DESCRIPTIONS

Serial Output (SO)

SO is a push/pull serial data output pin. During a read cycle, data is shifted out on this pin. Data is clocked out by the falling edge of the serial clock.

Serial Input (SI)

SI is the serial data input pin. All opcodes, byte addresses, and data to be written to the memory are input on this pin. Data is latched by the rising edge of the serial clock.

Serial Clock (SCK)

The Serial Clock controls the serial bus timing for data input and output. Opcodes, addresses, or data present on the SI pin are latched on the rising edge of the clock input, while data on the SO pin change after the falling edge of the clock input.

Chip Select ($\overline{CS}$)

When $\overline{CS}$ is HIGH, the X25040 is deselected and the SO output pin is at high impedance and unless an internal write operation is underway, the X25040 will be in the standby power mode. $\overline{CS}$ LOW enables the X25040, placing it in the active power mode. It should be noted that after power-up, a HIGH to LOW transition on $\overline{CS}$ is required prior to the start of any operation.

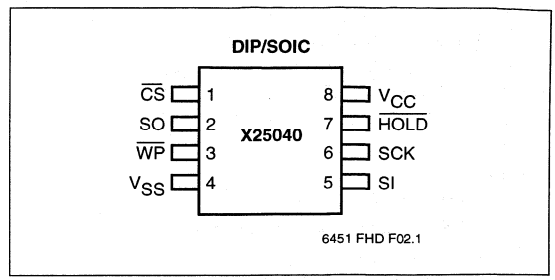
Write Protect ($\overline{WP}$)

When $\overline{WP}$ is LOW, nonvolatile writes to the X25040 are disabled, but the part otherwise functions normally. When $\overline{WP}$ is held HIGH, all functions, including nonvolatile writes operate normally. $\overline{WP}$ going LOW while $\overline{CS}$ is still LOW will interrupt a write to the X25040. If the internal write cycle has already been initiated, $\overline{WP}$ going LOW will have no affect on a write.

Hold ($\overline{HOLD}$)

$\overline{HOLD}$ is used in conjunction with the $\overline{CS}$ pin to select the device. Once the part is selected and a serial sequence is underway, $\overline{HOLD}$ may be used to pause the serial communication with the controller without resetting the serial sequence. To pause, $\overline{HOLD}$ must be brought LOW while SCK is LOW. To resume communication, $\overline{HOLD}$ is brought HIGH, again while SCK is LOW. If the pause feature is not used, $\overline{HOLD}$ should be held HIGH at all times.

PIN CONFIGURATION



PIN NAMES

Symbol	Description
$\overline{CS}$	Chip Select Input
SO	Serial Output
SI	Serial Input
SCK	Serial Clock Input
$\overline{WP}$	Write Protect Input
V_{SS}	Ground
V_{CC}	Supply Voltage
$\overline{HOLD}$	Hold Input

6451 PGM T01

4K X25040 512 x 8 Bit

SPI Serial E²PROM With BLOCK LOCK™ PROTECTION

FEATURES

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  - —3mA Active Current
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  - —Protect 1/4, 1/2 or all of E²PROM Array
- Built-in Inadvertent Write Protection
  - —Power-Up/Power-Down protection circuitry
  - —Write Latch
  - —Write Protect Pin
- Self-Timed Write Cycle
  - —5ms Write Cycle Time (Typical)
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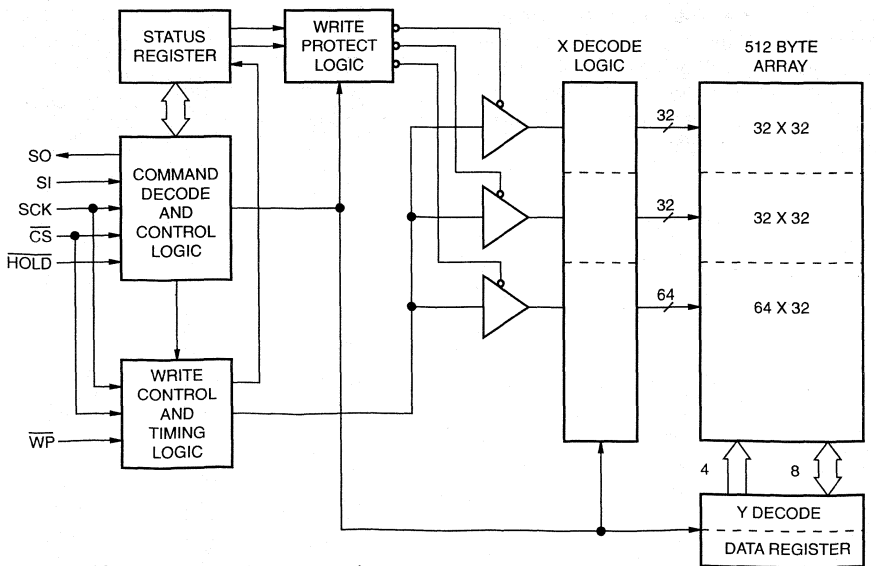
FUNCTIONAL DIAGRAM



6451 FHD F01

Direct Write™ and Block Lock™ Protection is a trademark of Xicor, Inc.

6451-3.5 5/26/95 T16/C6/D0 TD

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When $\overline{WP}$ is LOW, nonvolatile writes to the X25040 are disabled, but the part otherwise functions normally. When $\overline{WP}$ is held HIGH, all functions, including nonvolatile writes operate normally. $\overline{WP}$ going LOW while $\overline{CS}$ is still LOW will interrupt a write to the X25040. If the internal write cycle has already been initiated, $\overline{WP}$ going LOW will have no affect on a write.

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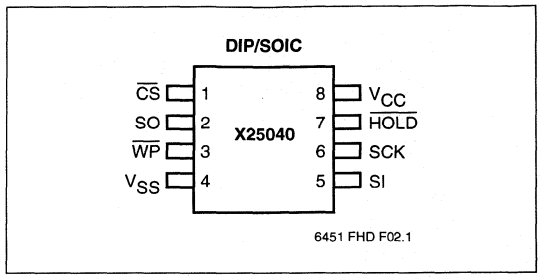
PIN CONFIGURATION



PIN NAMES

Symbol	Description
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SO	Serial Output
SI	Serial Input
SCK	Serial Clock Input
$\overline{WP}$	Write Protect Input
V_{SS}	Ground
V_{CC}	Supply Voltage
$\overline{HOLD}$	Hold Input

6451 PGM T01

PRINCIPLES OF OPERATION

The X25040 is a 512 x 8 E^2PROM designed to interface directly with the synchronous serial peripheral interface (SPI) of many popular microcontroller families.

The X25040 contains an 8-bit instruction register. It is accessed via the SI input, with data being clocked in on the rising SCK. $\overline{CS}$ must be LOW and the $\overline{HOLD}$ and $\overline{WP}$ inputs must be HIGH during the entire operation.

Table 1 contains a list of the instructions and their opcodes. All instructions, addresses and data are transferred MSB first.

Data input is sampled on the first rising edge of SCK after $\overline{CS}$ goes LOW. SCK is static, allowing the user to stop the clock and then resume operations. If the clock line is shared with other peripheral devices on the SPI bus, the user can assert the $\overline{HOLD}$ input to place the X25040 into a "PAUSE" condition. After releasing $\overline{HOLD}$, the X25040 will resume operation from the point when $\overline{HOLD}$ was first asserted.

Write Enable Latch

The X25040 contains a "write enable" latch. This latch must be SET before a write operation will be completed internally. The WREN instruction will set the latch and the WRDI instruction will reset the latch. This latch is automatically reset upon a power-up condition and after the completion of a byte, page, or status register write cycle.

Status Register

The RDSR instruction provides access to the status register. The status register may be read at any time, even during a write cycle. The status register is formatted as follows:

7	6	5	4	3	2	1	0
X	X	X	X	BP1	BP0	WEL	WIP

6451 PGM T02

BP0 and BP1 are set by the WRSR instruction. WEL and WIP are read-only and automatically set by other operations.

The Write-In-Process (WIP) bit indicates whether the X25040 is busy with a write operation. When set to a "1", a write is in progress, when set to a "0", no write is in progress. During a write, all other bits are set to "1".

The Write Enable Latch (WEL) bit indicates the status of the "write enable" latch. When set to a "1", the latch is set, when set to a "0", the latch is reset.

The Block Protect (BP0 and BP1) bits are nonvolatile and allow the user to select one of four levels of protection. The X25040 is divided into four 1024-bit segments. One, two, or all four of the segments may be protected. That is, the user may read the segments but will be unable to alter (write) data within the selected segments. The partitioning is controlled as illustrated below.

Status Register Bits		Array Addresses Protected
BP1	BP0	
0	0	None
0	1	$180–$1FF
1	0	$100–$1FF
1	1	$000–$1FF

6451 PGM T03

Table 1. Instruction Set

Instruction Name	Instruction Format*	Operation
WREN	0000 0110	Set the Write Enable Latch (Enable Write Operations)
WRDI	0000 0100	Reset the Write Enable Latch (Disable Write Operations)
RDSR	0000 0101	Read Status Register
WRSR	0000 0001	Write Status Register
READ	0000 $A_8$011	Read Data from Memory Array beginning at selected address
WRITE	0000 $A_8$010	Write Data to Memory Array beginning at Selected Address (1 to 32 Bytes)

6451 PGM T04.2

*Instructions are shown MSB in leftmost position. Instructions are transferred MSB first.

Clock and Data Timing

Data input on the SI line is latched on the rising edge of SCK. Data is output on the SO line by the falling edge of SCK.

Read Sequence

When reading from the E²PROM memory array, $\overline{CS}$ is first pulled LOW to select the device. The 8-bit READ instruction is transmitted to the X25040, followed by the 8-bit address. Bit 3 of the Read Data instruction contains address A_8. This bit is used to select the upper or lower half of the address. After the READ opcode and address are sent, the data stored in the memory at the selected address is shifted out on the SO line. The data stored in memory at the next address can be read sequentially by continuing to provide clock pulses. The address is automatically incremented to the next higher address after each byte of data is shifted out. When the highest address is reached ($1FF) the address counter rolls over to address $000 allowing the read cycle to be continued indefinitely. The read operation is terminated by taking $\overline{CS}$ HIGH. Refer to the read E²PROM array operation sequence illustrated in Figure 1.

To read the status register, the $\overline{CS}$ line is first pulled LOW to select the device followed by the 8-bit RDSR instruction. After the read status register opcode is sent, the contents of the status register are shifted out on the SO line. Figure 2 illustrates the read status register sequence.

Write Sequence

Prior to any attempt to write data into the X25040, the "write enable" latch must first be set by issuing the WREN instruction (See Figure 3). $\overline{CS}$ is first taken LOW, then the WREN instruction is clocked into the X25040. After all eight bits of the instruction are transmitted, $\overline{CS}$ must then be taken HIGH. If the user continues the write operation without taking $\overline{CS}$ HIGH after issuing the WREN instruction, the write operation will be ignored.

To write data to the E²PROM memory array, the user issues the WRITE instruction, followed by the address and then the data to be written. This is minimally a twenty-four clock operation. $\overline{CS}$ must go LOW and remain LOW for the duration of the operation. The host may continue to write up to 4 bytes of data to the X25040. The only restriction is the 4 bytes must reside on the same page. If the address counter reaches the end of the page and the clock continues, the counter will "roll over" to the first address of the page and overwrite any data that may have been written.

For the write operation (byte or page write) to be completed, $\overline{CS}$ can only be brought HIGH after bit 0 of data byte N is clocked in. If it is brought HIGH at any other time the write operation will not be completed. Refer to Figures 4 and 5 below for a detailed illustration of the write sequences and time frames in which $\overline{CS}$ going HIGH are valid.

To write to the status register, the WRSR instruction is followed by the data to be written. Data bits 0, 1, 4, 5, 6 and 7 must be "0". Figure 6 illustrates this sequence.

While the write is in progress following a status register or E²PROM write sequence, the status register may be read to check the WIP bit. During this time the WIP bit will be HIGH.

Hold Operation

The $\overline{HOLD}$ input should be HIGH (at V_{IH}) under normal operation. If a data transfer is to be interrupted $\overline{HOLD}$ can be pulled LOW to suspend the transfer until it can be resumed. The only restriction is the SCK input must be LOW when $\overline{HOLD}$ is first pulled LOW and SCK must also be LOW when $\overline{HOLD}$ is released.

The HOLD input may be tied HIGH either directly to V_{CC} or tied to V_{CC} through a resistor.

Operational Notes

The X25040 powers-up in the following state:

- The device is in the low power standby state.
- A HIGH to LOW transition on $\overline{CS}$ is required to enter an active state and receive an instruction.
- SO pin is high impedance.
- The "write enable" latch is reset.

Data Protection

The following circuitry has been included to prevent inadvertent writes:

- The "write enable" latch is reset upon power-up.
- A WREN instruction must be issued to set the "write enable" latch.
- $\overline{CS}$ must come HIGH at the proper clock count in order to start a write cycle.

Figure 1. Read E²PROM Array Operation Sequence

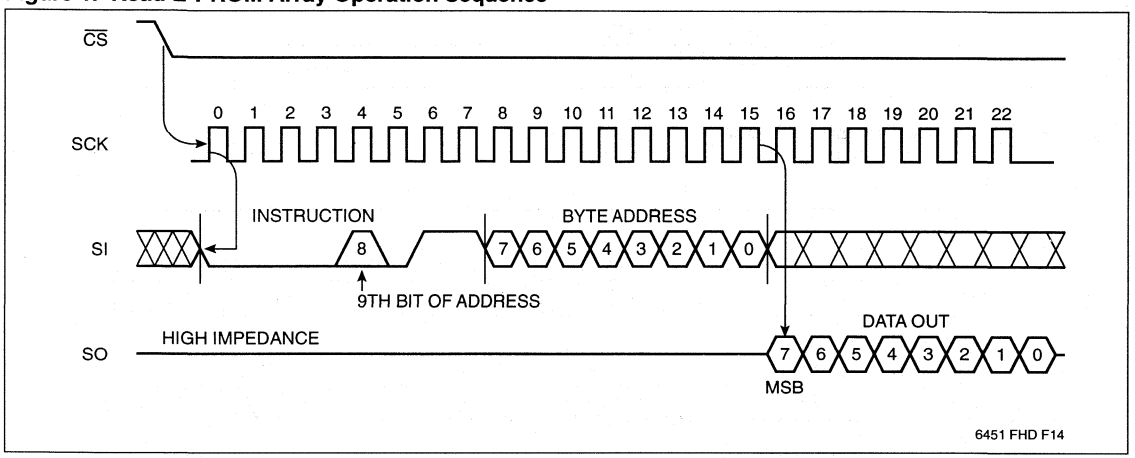


Figure 2. Read Status Register Operation Sequence

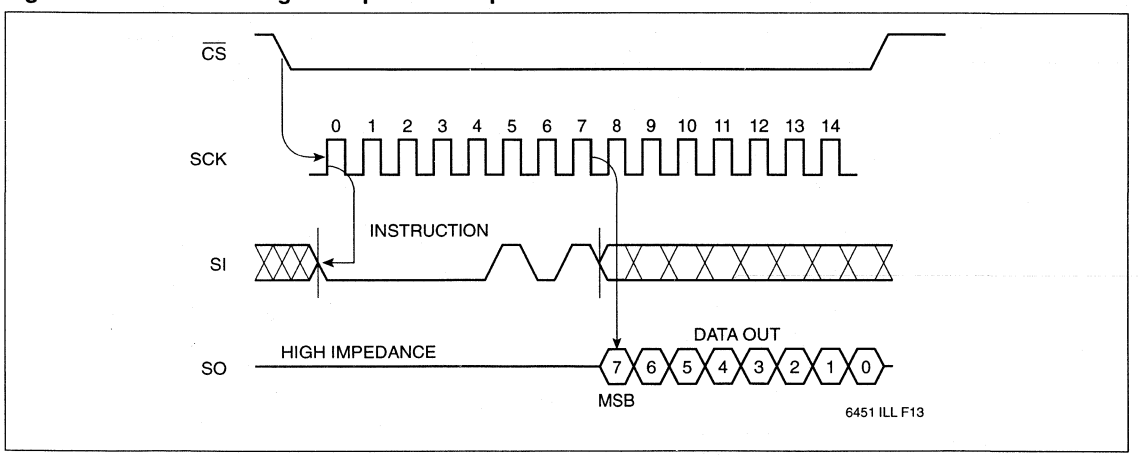


Figure 3. Write Enable Latch Sequence

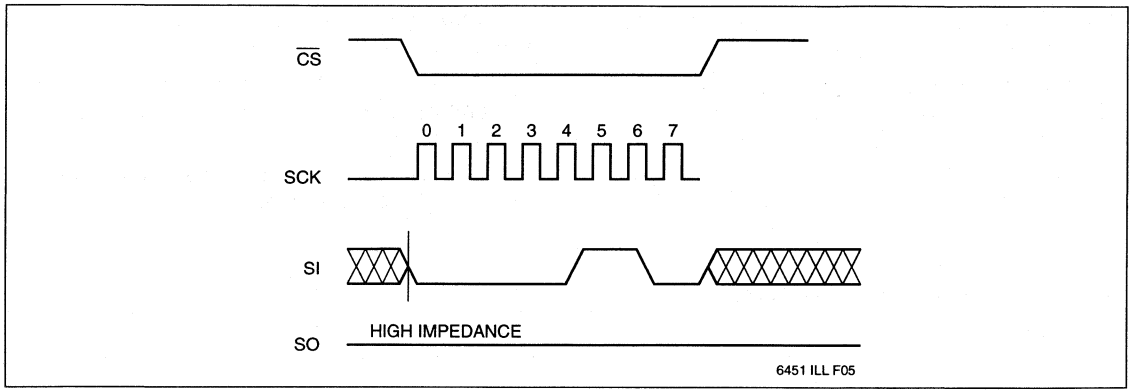


Figure 4. Byte Write Operation Sequence

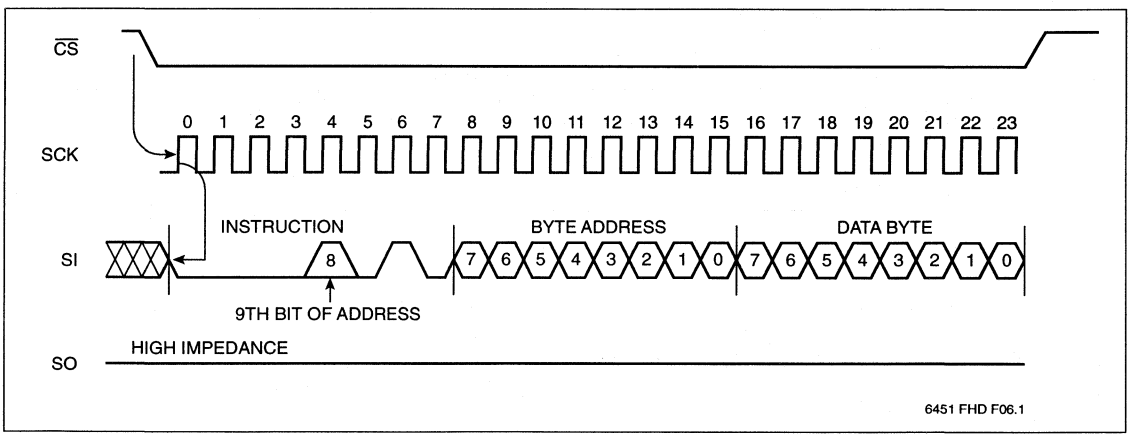


Figure 5. Page Write Operation Sequence

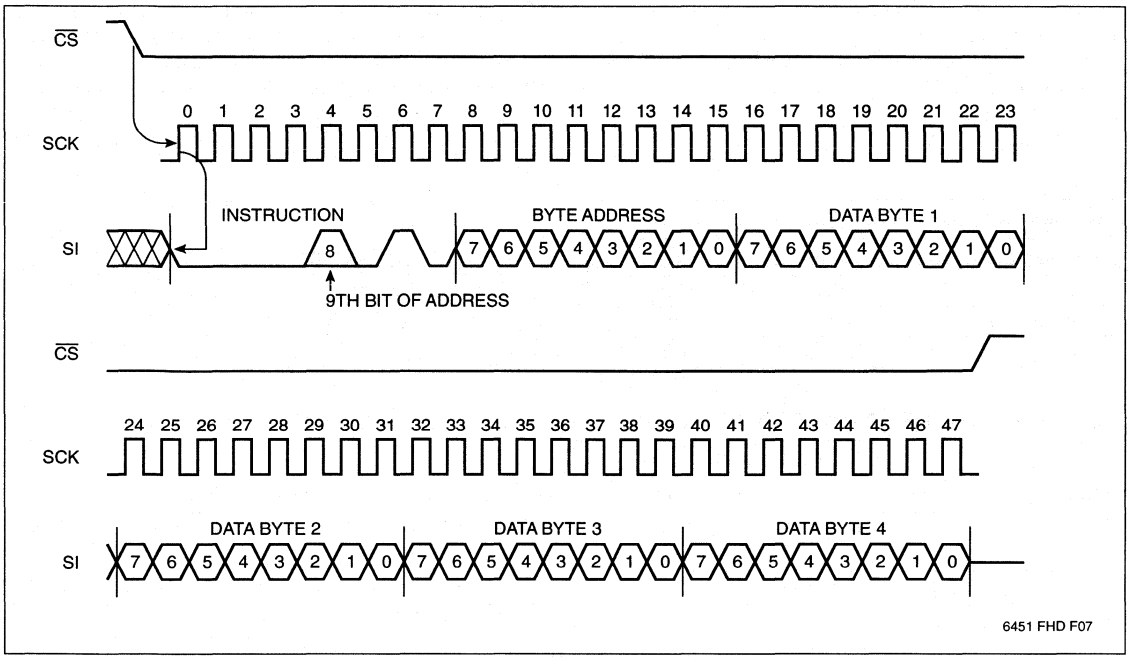
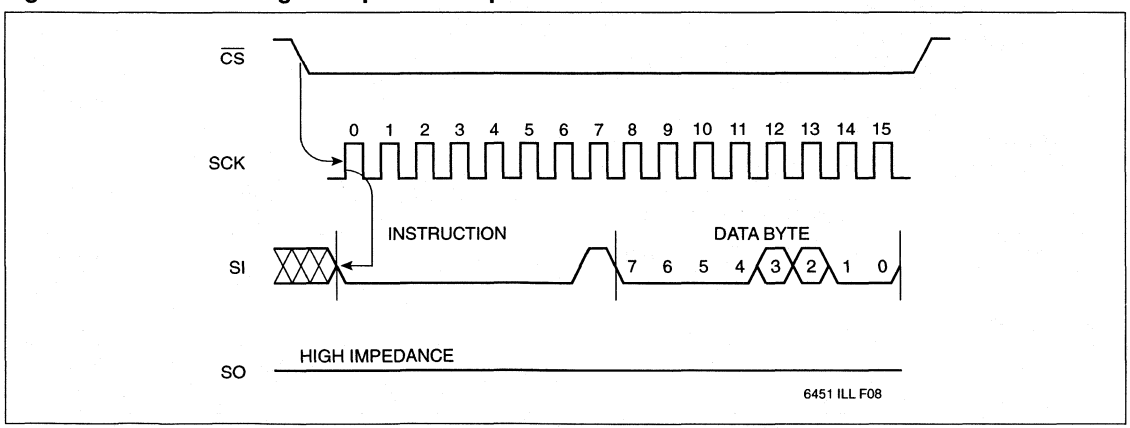


Figure 6. Write Status Register Operation Sequence



ABSOLUTE MAXIMUM RATINGS*

Temperature under Bias ..... –65°C to +135°C
Storage Temperature ..... –65°C to +150°C
Voltage on any Pin with Respect to V_{SS} ..... –1V to +7V
D.C. Output Current 5mA
Lead Temperature
(Soldering, 10 seconds) ..... 300°C

***COMMENT**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temp	Min.	Max.
Commercial	0°C	+70°C
Industrial	–40°C	+85°C
Military	–55°C	+125°C

6451 PGM T05.1

Supply Voltage	Limits
X25040	5V ±10%
X25040-3	3V to 5.5V
X25040-2.7	2.7 to 5.5V

6451 PGM T06.1

D.C. OPERATING CHARACTERISTICS (Over the recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
I_{CC}	V_{CC} Supply Current (Active)		3	mA	SCK = V_{CC} x 0.1/V_{CC} x 0.9 @ 1MHz, SO = Open
I_{SB}	V_{CC} Supply Current (Standby)		150	µA	$\overline{CS}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC} – 0.3V
I_{LI}	Input Leakage Current		10	µA	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output Leakage Current		10	µA	V_{OUT} = V_{SS} to V_{CC}
V_{IL}(1)	Input LOW Voltage	–1	V_{CC} x 0.3	V	
V_{IH}(1)	Input HIGH Voltage	V_{CC} x 0.7	V_{CC} + 0.5	V	
V_{OL}	Output LOW Voltage		0.4	V	I_{OL} = 2mA
V_{OH}	Output HIGH Voltage	V_{CC}–0.8		V	I_{OH} = –1mA

6451 PGM T07.3

POWER-UP TIMING

Symbol	Parameter	Min.	Max.	Units
t_{PUR}(2)	Power-up to Read Operation		1	ms
t_{PUW}(2)	Power-up to Write Operation		5	ms

6451 PGM T08

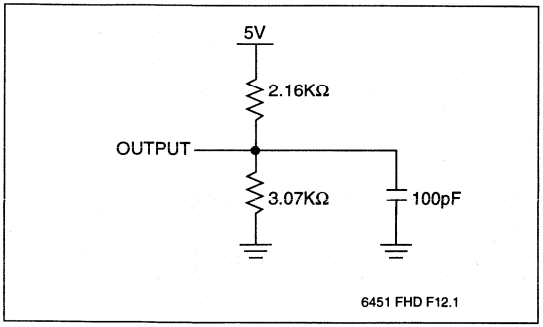
CAPACITANCE T_A = +25°C, f = 1MHz, V_{CC} = 5V.

Symbol	Test	Max.	Units	Conditions
C_{OUT}(2)	Output Capacitance (SO)	8	pF	V_{OUT} = 0V
C_{IN}(2)	Input Capacitance (SCK, SI, $\overline{CS}$, $\overline{WP}$, $\overline{HOLD}$)	6	pF	V_{IN} = 0V

6451 PGM T09.1

Notes: (1) V_{IL} min. and V_{IH} max. are for reference only and are not tested.
(2) This parameter is periodically sampled and not 100% tested.

EQUIVALENT A.C. LOAD CIRCUIT AT 5V V_{CC}



A.C. TEST CONDITIONS

Input Pulse Levels	V_{CC} x 0.1 to V_{CC} x 0.9
Input Rise and Fall Times	10ns
Input and Output Timing Level	V_{CC} x 0.5

6451 PGM T10

2

A.C. CHARACTERISTICS (Over recommended operating conditions, unless otherwise specified)

Data Input Timing

Symbol	Parameter	Min.	Max.	Units
f_{SCK}	Clock Frequency	0	1	MHz
t_{CYC}	Cycle Time	1000		ns
t_{LEAD}	$\overline{CS}$ Lead Time	500		ns
t_{LAG}	$\overline{CS}$ Lag Time	500		ns
t_{WH}	Clock HIGH Time	400		ns
t_{WL}	Clock LOW Time	400		ns
t_{SU}	Data Setup Time	100		ns
t_H	Data Hold Time	100		ns
t_{RI}	Data In Rise Time		2	µs
t_{FI}	Data In Fall Time		2	µs
t_{HD}	$\overline{HOLD}$ Setup Time	200		ns
t_{CD}	$\overline{HOLD}$ Hold Time	200		ns
t_{CS}	$\overline{CS}$ Deselect Time	500		ns
t_{WC}(4)	Write Cycle Time		10	ms

6451 PGM T11.1

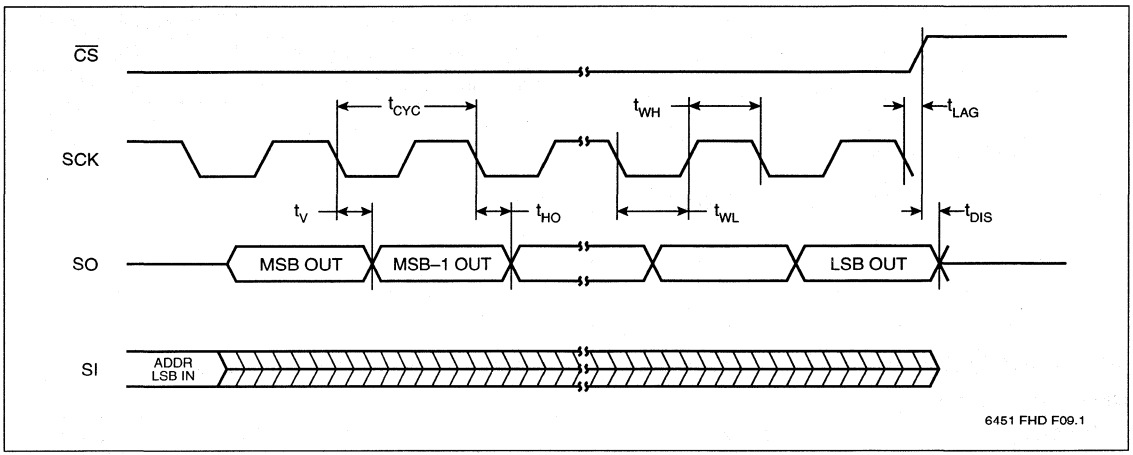
Data Output Timing

Symbol	Parameter	Min.	Max.	Units
f_{SCK}	Clock Frequency	0	1	MHz
t_{DIS}	Output Disable Time		500	ns
t_V	Output Valid from Clock LOW		400	ns
t_{HO}	Output Hold Time	0		ns
t_{RO}(3)	Output Rise Time		300	ns
t_{FO}(3)	Output Fall Time		300	ns
t_{LZ}	$\overline{HOLD}$ HIGH to Output in Low Z	100		ns
t_{HZ}	$\overline{HOLD}$ LOW to Output in High Z	100		ns

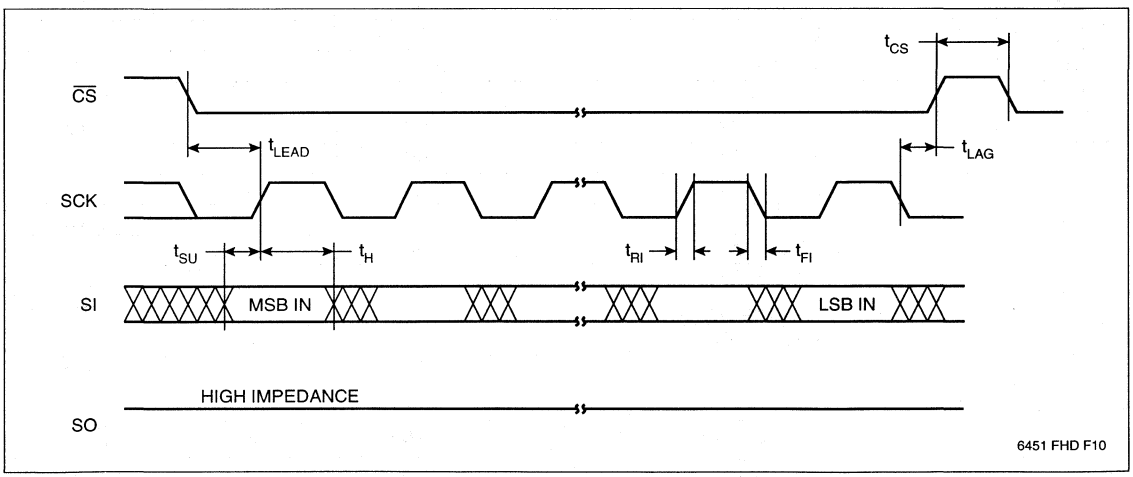
6451 PGM T12.1

Notes: (3) This parameter is periodically sampled and not 100% tested.
(4) t_{WC} is the time from the rising edge of $\overline{CS}$ after a valid write sequence has been sent to the end of the self-timed internal nonvolatile write cycle.

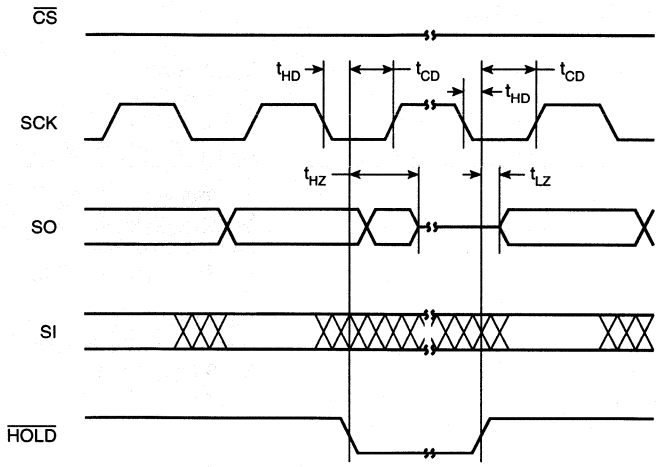
Serial Output Timing



Serial Input Timing

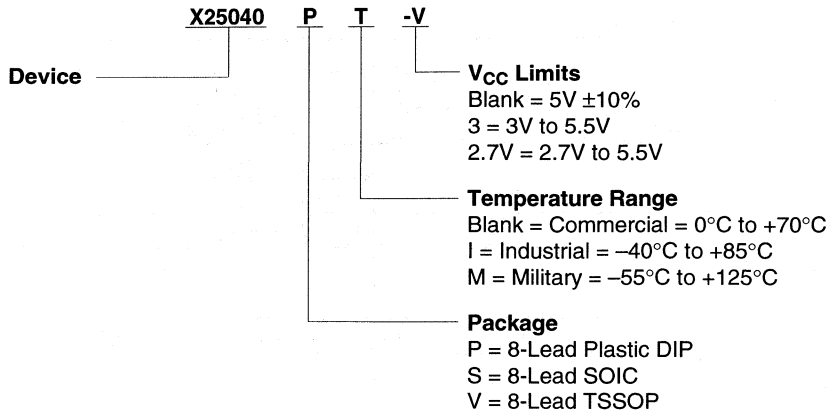


Hold Timing

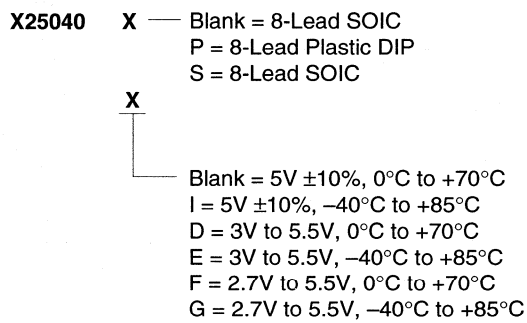


6451 FHD F11

ORDERING INFORMATION



Part Mark Convention



SPI Serial E²PROM With BLOCK LOCK™ PROTECTION

FEATURES

- 1MHz Clock Rate
- SPI Modes (0,1 & 1,0)
- 512 X 8 Bits
  - —4 Byte Page Mode
- Low Power CMOS
  - —150µA Standby Current
  - —3mA Active Current
- 2.7V To 5.5V Power Supply
- Block Lock Protection
  - —Protect 1/4, 1/2 or all of E²PROM Array
- Built-in Inadvertent Write Protection
  - —Power-Up/Power-Down protection circuitry
  - —Write Latch
  - —Write Protect Pin
- Self-Timed Write Cycle
  - —5ms Write Cycle Time (Typical)
- High Reliability
  - —Endurance: 100,000 cycles per byte
  - —Data Retention: 100 Years
  - —ESD protection: 2000V on all pins
- 8-Pin Mini-DIP Package
- 8-Lead SOIC Package
- 8-Lead TSSOP

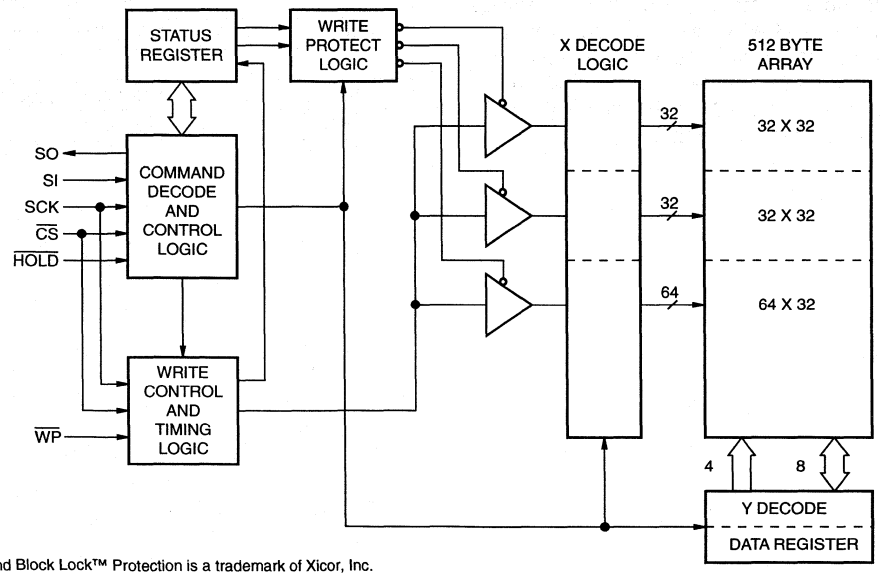
DESCRIPTION

The X25041 is a CMOS 4096-bit serial E²PROM, internally organized as 512 x 8. The X25041 features a Serial Peripheral Interface (SPI) and software protocol allowing operation on a simple three-wire bus. The bus signals are a clock input (SCK) plus separate data in (SI) and data out (SO) lines. Access to the device is controlled through a chip select ($\overline{CS}$) input, allowing any number of devices to share the same bus.

The X25041 also features two additional inputs that provide the end user with added flexibility. By asserting the $\overline{HOLD}$ input, the X25041 will ignore transitions on its inputs, thus allowing the host to service higher priority interrupts. The $\overline{WP}$ input can be used as a hardwire input to the X25041 disabling all write attempts, thus providing a mechanism for limiting end user capability of altering the memory.

The X25041 utilizes Xicor's proprietary Direct Write™ cell, providing a minimum endurance of 100,000 cycles per byte and a minimum data retention of 100 years.

FUNCTIONAL DIAGRAM



6556 FHD F01

Direct Write™ and Block Lock™ Protection is a trademark of Xicor, Inc.

PIN DESCRIPTIONS

Serial Output (SO)

SO is a push/pull serial data output pin. During a read cycle, data is shifted out on this pin. Data is clocked out by the rising edge of the serial clock.

Serial Input (SI)

SI is the serial data input pin. All opcodes, byte addresses, and data to be written to the memory are input on this pin. Data is latched by the falling edge of the serial clock.

Serial Clock (SCK)

The Serial Clock controls the serial bus timing for data input and output. Opcodes, addresses, or data present on the SI pin are latched on the falling edge of the clock input, while data on the SO pin change after the rising edge of the clock input.

Chip Select ($\overline{CS}$)

When $\overline{CS}$ is HIGH, the X25041 is deselected and the SO output pin is at high impedance and unless an internal write operation is underway, the X25041 will be in the standby power mode. $\overline{CS}$ LOW enables the X25041, placing it in the active power mode. It should be noted that after power-up, a HIGH to LOW transition on $\overline{CS}$ is required prior to the start of any operation.

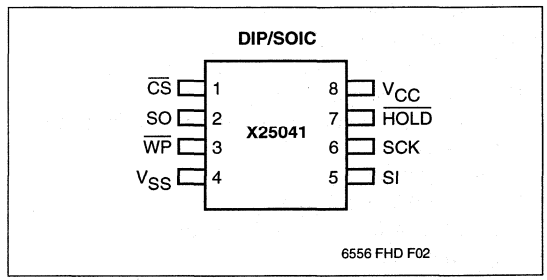
Write Protect ($\overline{WP}$)

When $\overline{WP}$ is LOW, nonvolatile writes to the X25041 are disabled, but the part otherwise functions normally. When $\overline{WP}$ is held HIGH, all functions, including nonvolatile writes operate normally. $\overline{WP}$ going LOW while $\overline{CS}$ is still LOW will interrupt a write to the X25041. If the internal write cycle has already been initiated, $\overline{WP}$ going LOW will have no affect on a write.

Hold ($\overline{HOLD}$)

$\overline{HOLD}$ is used in conjunction with the $\overline{CS}$ pin to select the device. Once the part is selected and a serial sequence is underway, $\overline{HOLD}$ may be used to pause the serial communication with the controller without resetting the serial sequence. To pause, $\overline{HOLD}$ must be brought LOW while SCK is HIGH. To resume communication, $\overline{HOLD}$ is brought HIGH, again while SCK is HIGH. If the pause feature is not used, $\overline{HOLD}$ should be held HIGH at all times.

PIN CONFIGURATION



PIN NAMES

Symbol	Description
$\overline{CS}$	Chip Select Input
SO	Serial Output
SI	Serial Input
SCK	Serial Clock Input
$\overline{WP}$	Write Protect Input
V_{SS}	Ground
V_{CC}	Supply Voltage
$\overline{HOLD}$	Hold Input

6556 PGM T01

PRINCIPLES OF OPERATION

The X25041 is a 512 x 8 E^2PROM designed to interface directly with the synchronous serial peripheral interface (SPI) of many popular microcontroller families.

The X25041 contains an 8-bit instruction register. It is accessed via the SI input, with data being clocked in on the falling SCK. $\overline{CS}$ must be LOW during the entire operation.

Table 1 contains a list of the instructions and their codes. All instructions, addresses and data are transferred MSB first.

Data input is sampled on the first falling edge of SCK after $\overline{CS}$ goes LOW. SCK is static, allowing the user to stop the clock and then resume operations. If the clock line is shared with other peripheral devices on the SPI bus, the user can assert the $\overline{HOLD}$ input to place the X25041 into a "PAUSE" condition. After releasing $\overline{HOLD}$, the X25041 will resume operation from the point when $\overline{HOLD}$ was first asserted.

Write Enable Latch

The X25041 contains a "write enable" latch. This latch must be SET before a write operation will be completed internally. The WREN instruction will set the latch and the WRDI instruction will reset the latch. This latch is automatically reset upon a power-up condition and after the completion of a byte, page, or status register write cycle.

Status Register

The RDSR instruction provides access to the status register. The status register may be read at any time, even during a write cycle. The status register is formatted as follows:

7	6	5	4	3	2	1	0
X	X	X	X	BP1	BP0	WEL	WIP

6556 PGM T02

BP0 and BP1 are set by the WRSR instruction. WEL and WIP are read-only and automatically set by other operations.

The Write-In-Process (WIP) bit indicates whether the X25041 is busy with a write operation. When set to a "1", a write is in progress, when set to a "0", no write is in progress. During a write, all other bits are set to "1".

The Write Enable Latch (WEL) bit indicates the status of the "write enable" latch. When set to a "1", the latch is set, when set to a "0", the latch is reset.

The Block Protect (BP0 and BP1) bits are nonvolatile and allow the user to select one of four levels of protection. The X25041 is divided into four 1024-bit segments. One, two, or all four of the segments may be protected. That is, the user may read the segments but will be unable to alter (write) data within the selected segments. The partitioning is controlled as illustrated below.

Status Register Bits		Array Addresses Protected
BP1	BP0	
0	0	None
0	1	$180–$1FF
1	0	$100–$1FF
1	1	$000–$1FF

6556 PGM T03

Table 1. Instruction Set

Instruction Name	Instruction Format*	Operation
WREN	0000 0110	Set the Write Enable Latch (Enable Write Operations)
WRDI	0000 0100	Reset the Write Enable Latch (Disable Write Operations)
RDSR	0000 0101	Read Status Register
WRSR	0000 0001	Write Status Register
READ	0000 $A_8$011	Read Data from Memory Array beginning at selected address
WRITE	0000 $A_8$010	Write Data to Memory Array beginning at Selected Address (1 to 32 Bytes)

6556 PGM T04

*Instructions are shown MSB in leftmost position. Instructions are transferred MSB first.

Clock and Data Timing

Data input on the SI line is latched on the falling edge of SCK. Data is output on the SO line by the rising edge of SCK.

Read Sequence

When reading from the E²PROM memory array, $\overline{CS}$ is first pulled LOW to select the device. The 8-bit READ instruction is transmitted to the X25041, followed by the 8-bit address. Bit 3 of the Read Data instruction contains address A_8. This bit is used to select the upper or lower half of the address. After the READ opcode and address are sent, the data stored in the memory at the selected address is shifted out on the SO line. The data stored in memory at the next address can be read sequentially by continuing to provide clock pulses. The address is automatically incremented to the next higher address after each byte of data is shifted out. When the highest address is reached ($1FF) the address counter rolls over to address $000 allowing the read cycle to be continued indefinitely. The read operation is terminated by taking $\overline{CS}$ HIGH. Refer to the read E²PROM array operation sequence illustrated in Figure 1.

To read the status register, the $\overline{CS}$ line is first pulled LOW to select the device followed by the 8-bit RDSR instruction. After the read status register opcode is sent, the contents of the status register are shifted out on the SO line. Figure 2 illustrates the read status register sequence.

Write Sequence

Prior to any attempt to write data into the X25041, the "write enable" latch must first be set by issuing the WREN instruction (See Figure 3). $\overline{CS}$ is first taken LOW, then the WREN instruction is clocked into the X25041. After all eight bits of the instruction are transmitted, $\overline{CS}$ must then be taken HIGH. If the user continues the write operation without taking $\overline{CS}$ HIGH after issuing the WREN instruction, the write operation will be ignored.

To write data to the E²PROM memory array, the user issues the WRITE instruction, followed by the address and then the data to be written. This is minimally a twenty-four clock operation. $\overline{CS}$ must go LOW and remain LOW for the duration of the operation. The host may continue to write up to 4 bytes of data to the X25041. The only restriction is the 4 bytes must reside on the same page. If the address counter reaches the end of the page and the clock continues, the counter will "roll over" to the first address of the page and overwrite any data that may have been written.

For the write operation (byte or page write) to be completed, $\overline{CS}$ can only be brought HIGH after bit 0 of data byte N is clocked in. If it is brought HIGH at any other time the write operation will not be completed. Refer to Figures 4 and 5 below for a detailed illustration of the write sequences and time frames in which $\overline{CS}$ going HIGH are valid.

To write to the status register, the WRSR instruction is followed by the data to be written. Data bits 0, 1, 4, 5, 6 and 7 must be "0". Figure 6 illustrates this sequence.

While the write is in progress following a status register or E²PROM write sequence, the status register may be read to check the WIP bit. During this time the WIP bit will be HIGH.

Hold Operation

The $\overline{HOLD}$ input should be HIGH (at V_{IH}) under normal operation. If a data transfer is to be interrupted $\overline{HOLD}$ can be pulled LOW to suspend the transfer until it can be resumed. The only restriction is the SCK input must be HIGH when $\overline{HOLD}$ is first pulled LOW and SCK must also be HIGH when $\overline{HOLD}$ is released.

The HOLD input may be tied HIGH either directly to V_{CC} or tied to V_{CC} through a resistor.

Operational Notes

The X25041 powers-up in the following state:

- The device is in the low power standby state.
- A HIGH to LOW transition on $\overline{CS}$ is required to enter an active state and receive an instruction.
- SO pin is high impedance.
- The "write enable" latch is reset.

Data Protection

The following circuitry has been included to prevent inadvertent writes:

- The "write enable" latch is reset upon power-up.
- A WREN instruction must be issued to set the "write enable" latch.
- $\overline{CS}$ must come HIGH at the proper clock count in order to start a write cycle.

Figure 1. Read E²PROM Array Operation Sequence

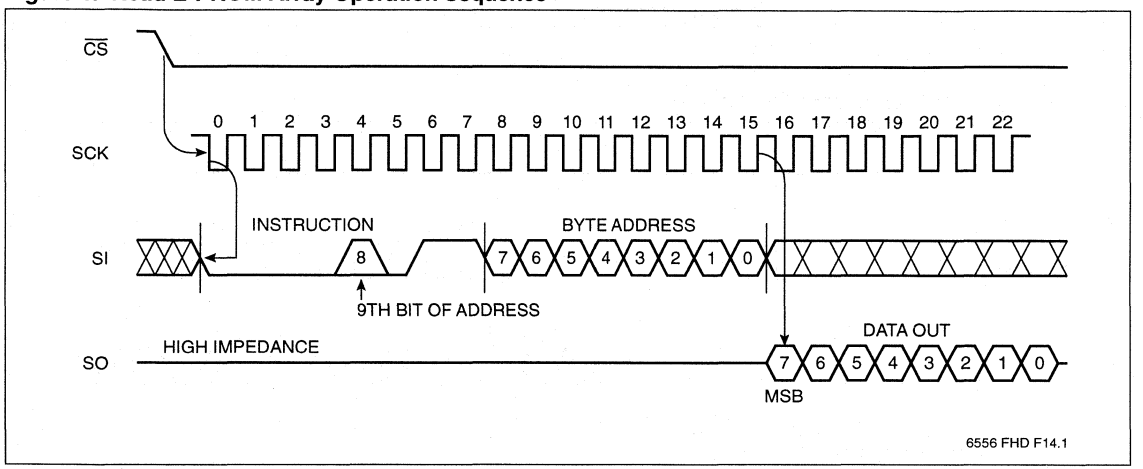


Figure 2. Read Status Register Operation Sequence

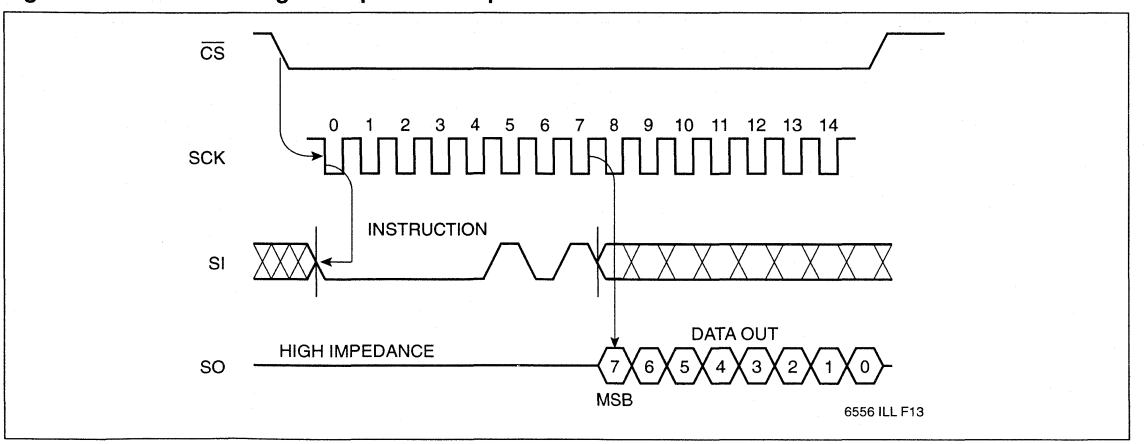


Figure 3. Write Enable Latch Sequence

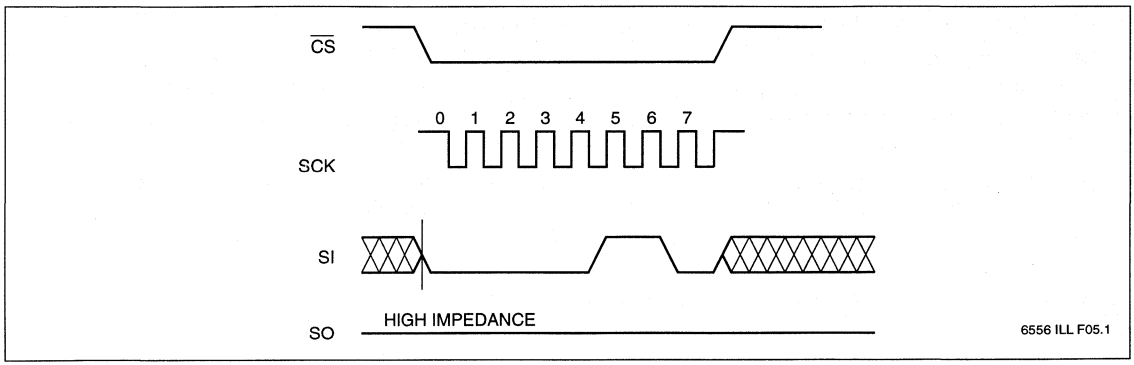


Figure 4. Byte Write Operation Sequence

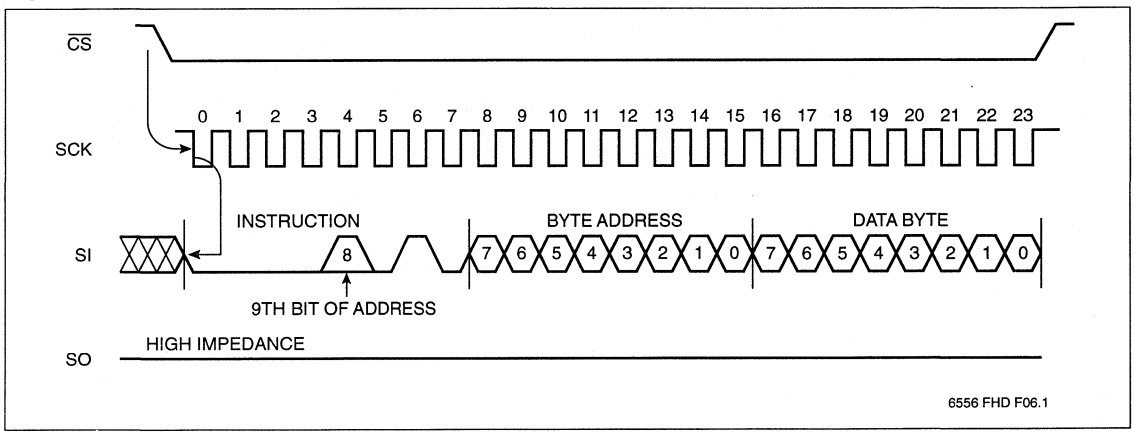


Figure 5. Page Write Operation Sequence

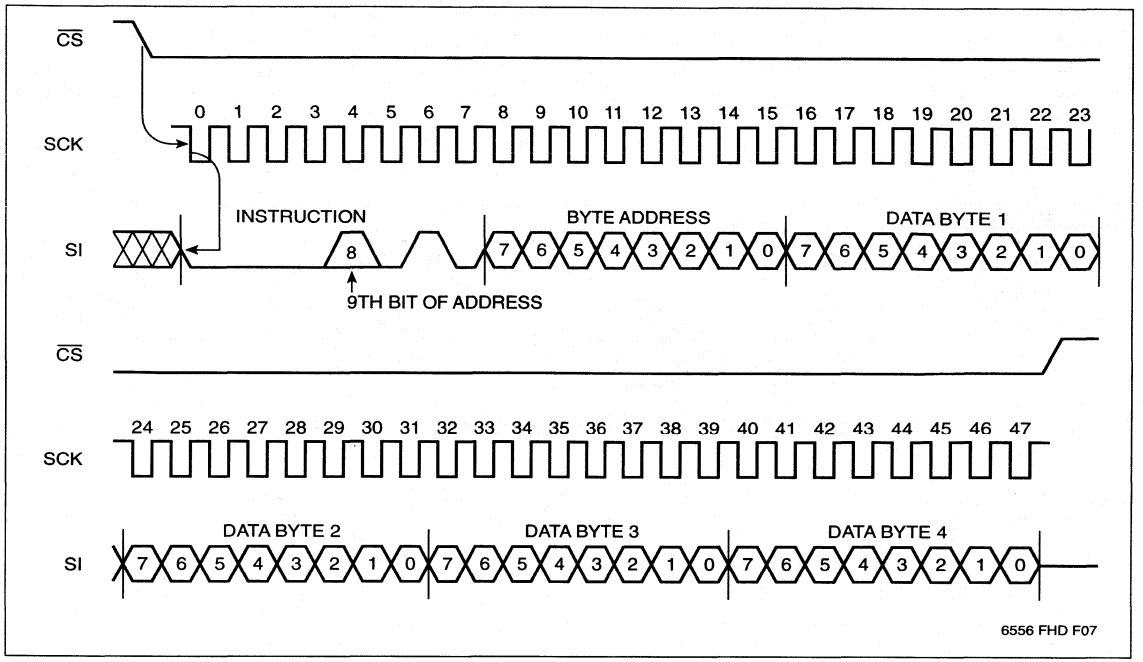
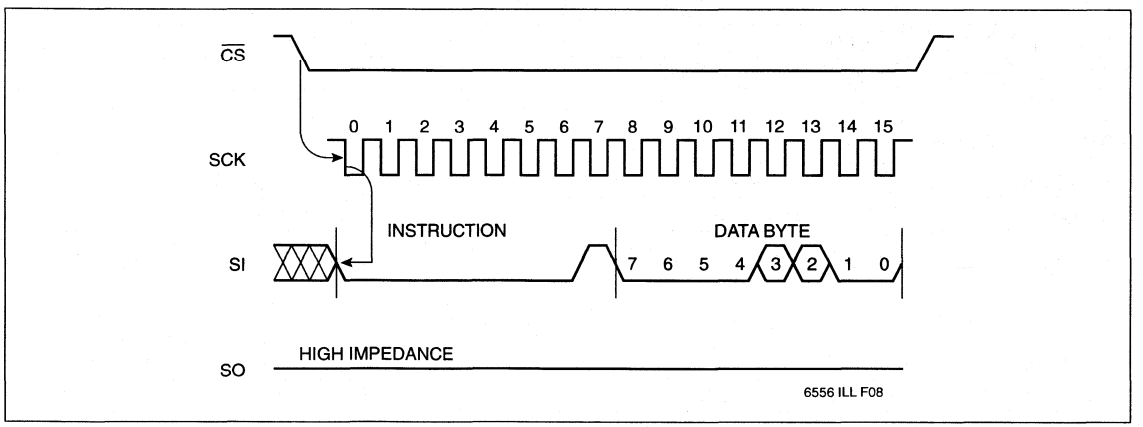


Figure 6. Write Status Register Operation Sequence



ABSOLUTE MAXIMUM RATINGS*

Temperature under Bias ..... –65°C to +135°C
Storage Temperature ..... –65°C to +150°C
Voltage on any Pin with Respect to V_{SS} ..... –1V to +7V
D.C. Output Current 5mA
Lead Temperature
(Soldering, 10 seconds) ..... 300°C

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temp	Min.	Max.
Commercial	0°C	+70°C
Industrial	–40°C	+85°C
Military	–55°C	+125°C

6556 PGM T05

Supply Voltage	Limits
X25041	5V ±10%
X25041-3	3V to 5.5V
X25041-2.7	2.7 to 5.5V

6556 PGM T06

D.C. OPERATING CHARACTERISTICS (Over the recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
I_{CC}	V_{CC} Supply Current (Active)		3	mA	SCK = V_{CC} x 0.1/V_{CC} x 0.9 @ 1MHz, SO = Open
I_{SB}	V_{CC} Supply Current (Standby)		150	µA	$\overline{CS}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC} – 0.3V
I_{LI}	Input Leakage Current		10	µA	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output Leakage Current		10	µA	V_{OUT} = V_{SS} to V_{CC}
V_{IL}(1)	Input LOW Voltage	–1	V_{CC} x 0.3	V	
V_{IH}(1)	Input HIGH Voltage	V_{CC} x 0.7	V_{CC} + 0.5	V	
V_{OL}	Output LOW Voltage		0.4	V	I_{OL} = 2mA
V_{OH}	Output HIGH Voltage	V_{CC}–0.8		V	I_{OH} = –1mA

6556 PGM T07.1

POWER-UP TIMING

Symbol	Parameter	Min.	Max.	Units
t_{PUR}(2)	Power-up to Read Operation		1	ms
t_{PUW}(2)	Power-up to Write Operation		5	ms

6556 PGM T08

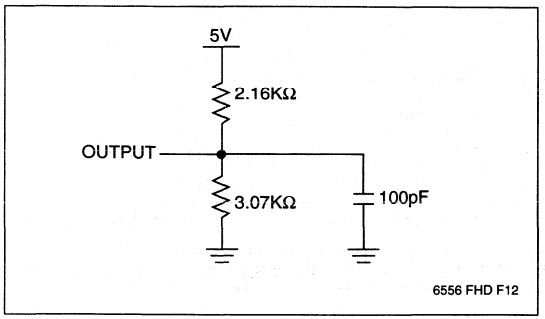
CAPACITANCE T_A = +25°C, f = 1MHz, V_{CC} = 5V.

Symbol	Test	Max.	Units	Conditions
C_{OUT}(2)	Output Capacitance (SO)	8	pF	V_{OUT} = 0V
C_{IN}(2)	Input Capacitance (SCK, SI, $\overline{CS}$, $\overline{WP}$, $\overline{HOLD}$)	6	pF	V_{IN} = 0V

6556 PGM T09

Notes: (1) V_{IL} min. and V_{IH} max. are for reference only and are not tested.
(2) This parameter is periodically sampled and not 100% tested.

EQUIVALENT A.C. LOAD CIRCUIT AT 5V V_{CC}



A.C. TEST CONDITIONS

Input Pulse Levels	V_{CC} x 0.1 to V_{CC} x 0.9
Input Rise and Fall Times	10ns
Input and Output Timing Level	V_{CC} x 0.5

6556 PGM T10

2

A.C. CHARACTERISTICS (Over recommended operating conditions, unless otherwise specified)

Data Input Timing

Symbol	Parameter	Min.	Max.	Units
f_{SCK}	Clock Frequency	0	1	MHz
t_{CYC}	Cycle Time	1000		ns
t_{LEAD}	$\overline{CS}$ Lead Time	500		ns
t_{LAG}	$\overline{CS}$ Lag Time	500		ns
t_{WH}	Clock HIGH Time	400		ns
t_{WL}	Clock LOW Time	400		ns
t_{SU}	Data Setup Time	100		ns
t_H	Data Hold Time	100		ns
t_{RI}	Data In Rise Time		2	µs
t_{FI}	Data In Fall Time		2	µs
t_{HD}	$\overline{HOLD}$ Setup Time	200		ns
t_{CD}	$\overline{HOLD}$ Hold Time	200		ns
t_{CS}	$\overline{CS}$ Deselect Time	500		ns
t_{WC}(4)	Write Cycle Time		10	ms

6556 PGM T11.1

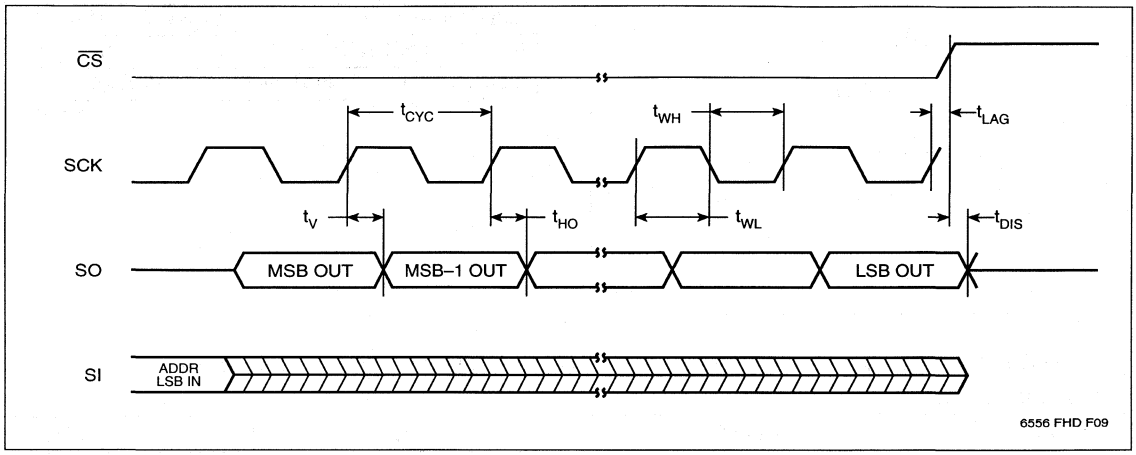
Data Output Timing

Symbol	Parameter	Min.	Max.	Units
f_{SCK}	Clock Frequency	0	1	MHz
t_{DIS}	Output Disable Time		500	ns
t_V	Output Valid from Clock LOW		400	ns
t_{HO}	Output Hold Time	0		ns
t_{RO}(3)	Output Rise Time		300	ns
t_{FO}(3)	Output Fall Time		300	ns
t_{LZ}	$\overline{HOLD}$ HIGH to Output in Low Z	100		ns
t_{HZ}	$\overline{HOLD}$ LOW to Output in High Z	100		ns

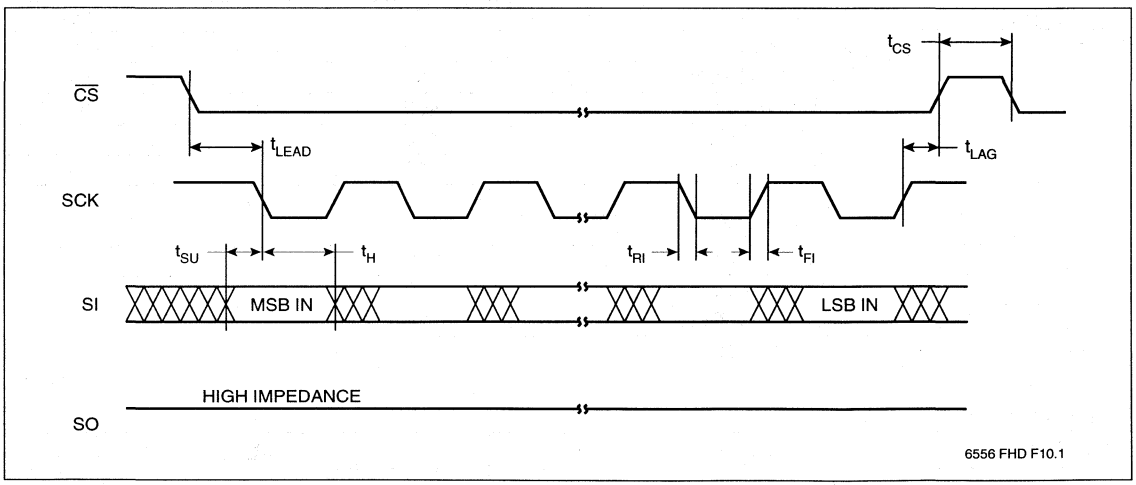
6556 PGM T12.1

Notes: (3) This parameter is periodically sampled and not 100% tested.
(4) t_{WC} is the time from the rising edge of $\overline{CS}$ after a valid write sequence has been sent to the end of the self-timed internal nonvolatile write cycle.

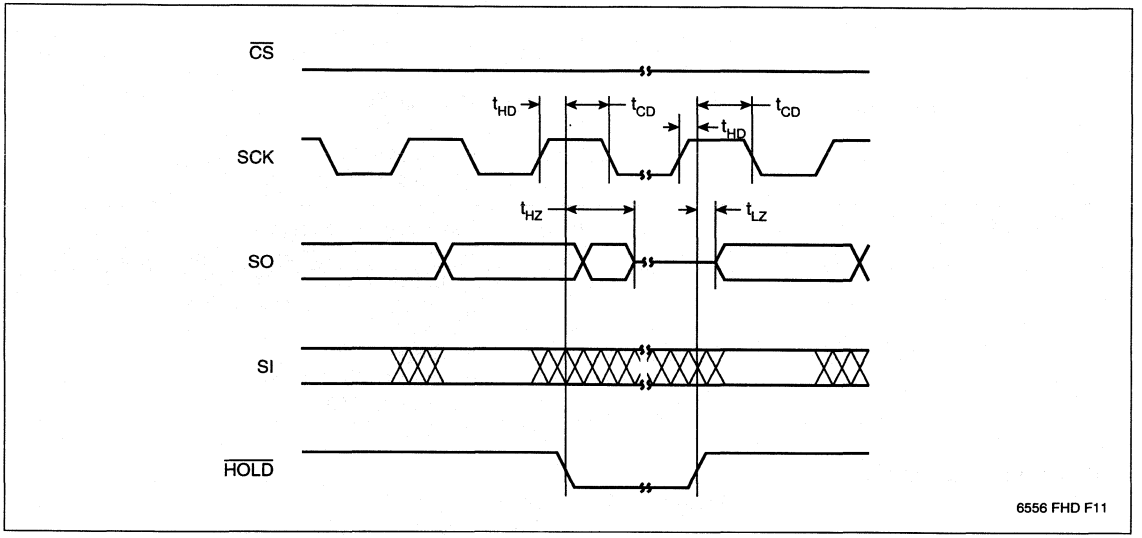
Serial Output Timing



Serial Input Timing



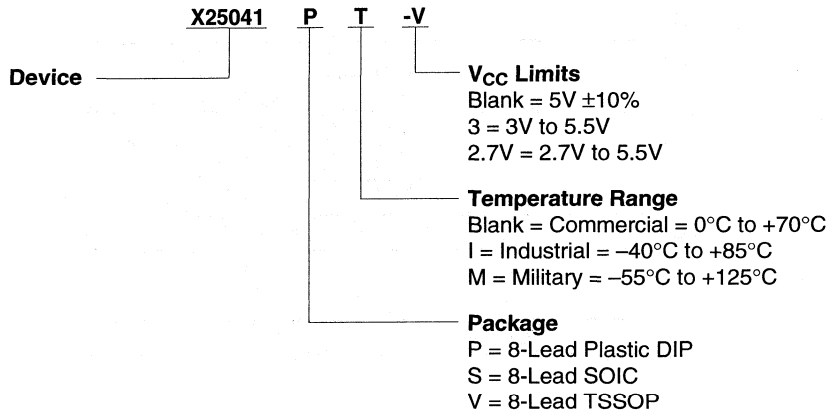
Hold Timing



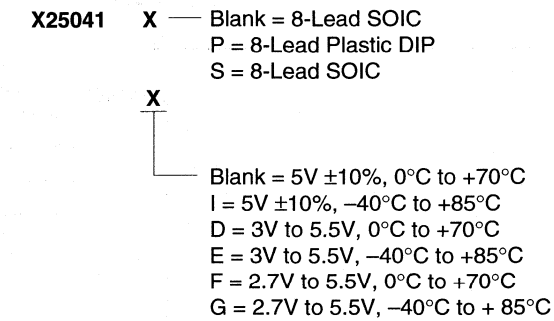
SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

ORDERING INFORMATION



Part Mark Convention



NOTES

Xicor®

#8

Design Engineering Bulletin

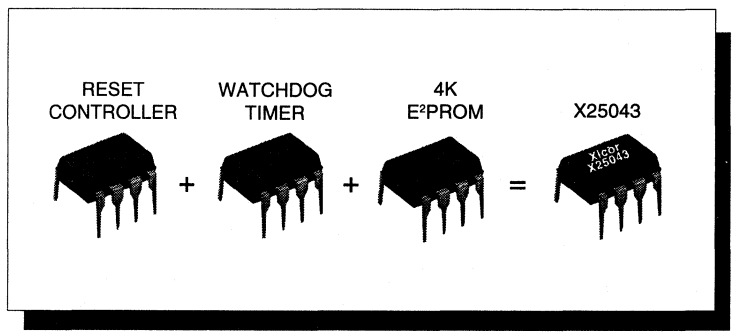
New Product and Applications Information for Design Engineers

Watchdog Timer, Reset Controller and E²PROM Merged Into a Single Chip

The X25043 integrates three of the most common external functional elements in microcontroller based systems into a single low-cost and low power device. The X25043 combines a precision RESET controller, a programmable and flexible Watch Dog Timer and 4K bits of E²PROM memory into a single 8 pin packaged device. The interface to the microcontroller is the advanced SPI (Serial Peripheral Interface) common to most advanced microcontrollers.

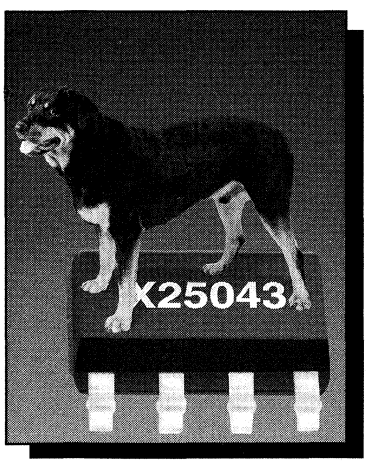
The RESET controller monitors the Vcc level in the system and will generate a RESET pulse to the microcontroller during power-up, power-down and brown out conditions. The Watchdog timer will generate a RESET pulse if the timer is not reset within the configured interval. The E²PROM is organized as 512 Bytes and features advanced data protection features such as Software Data Protection and Block Lock Write Protection.

By combining all of these features onto a single chip, the designer is now able to save board space, power and component cost.



The X25043 reduces component count and system cost dramatically when compared to previous solutions.

X25043 Second Generation Watchdog Timer - Increased Functionality, Flexibility and Dependability



X25043-A better watchdog.

The Watchdog timer of the X25043 represents the ultimate in flexibility, functionality and dependability. Through the utilization of E²PROM technology, the watchdog timer interval is stored in a nonvolatile register. This allows the interval to be valid immediately upon power-on RESET of the microcontroller without the need for initialization as would be required on a volatile configured timer. This insures that the microcontroller will be brought through any initialization problems by the X25043.

The fact that the interval timer on the X25043 is stored in E²PROM allows the system to select the proper interval from 3 choices: 200 msec, 600 msec and 1.2 seconds. The timer may also be disabled through the use of the nonvolatile configuration register. This flexibility allows the interval to be changed in system at various stages of the systems life to allow for software modification, hardware configurations or different algorithm requirements.

4K X25043/45 512 x 8 Bit

Programmable Watchdog Supervisory E²PROM

FEATURES

- Programmable Watchdog Timer
- Low V_{CC} Detection
- Reset Signal Valid to V_{CC} = 1V
- 1MHz Clock Rate
- 512 X 8 Bits Serial E²PROM
  - —4 Byte Page Mode
- Low Power CMOS
  - —50µA Standby Current
  - —3mA Active Current
- 2.7V To 5.5V Power Supply
- Block Lock™
  - —Protect 1/4, 1/2 or all of E²PROM Array
- Built-in Inadvertent Write Protection
  - —Power-Up/Power-Down protection circuitry
  - —Write Latch
  - —Write Protect Pin
- High Reliability
  - —Endurance: 100,000 cycles per byte
  - —Data Retention: 100 Years
  - —ESD protection: 2000V on all pins
- 8-Pin Mini-DIP Package
- 8-Lead SOIC Package
- 14-Lead TSSOP
- X25043 = Active LOW $\overline{\text{RESET}}$
- X25045 = Active HIGH RESET

DESCRIPTION

The X25043/45 combines three popular functions, Watchdog Timer, Voltage Supervision, and E²PROM in a single package. This combination lowers the system cost and reduces the board space requirements.

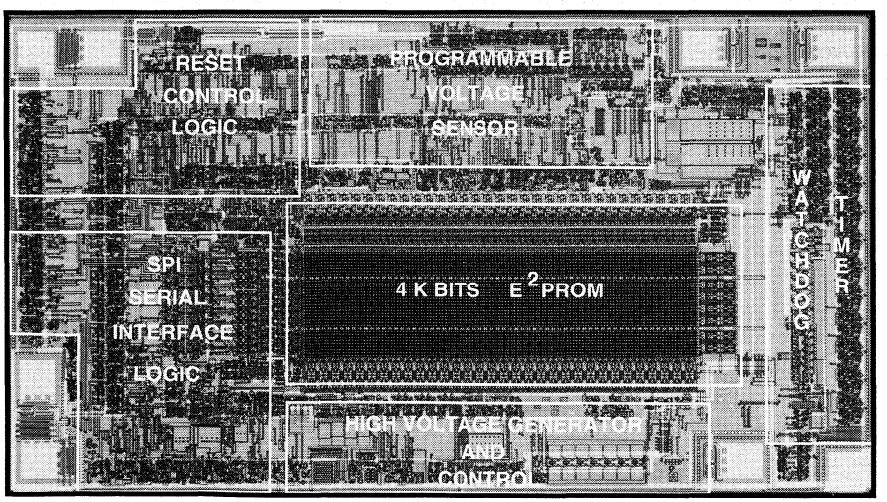
The Watchdog Timer provides an independent protection system for microcontrollers. During a system failure, the X25043/45 watchdog will respond with a $\overline{\text{RESET}}$/RESET signal after a selectable time-out interval. The user selects the interval from three preset values. Once selected, the interval does not change, even after cycling the power.

The system is protected from low voltage conditions by the X25043/45 low V_{CC} detection circuits. When V_{CC} drops below the minimum V_{CC} trip point, the system is reset. Reset is asserted until V_{CC} returns and stabilizes.

The memory portion of the X25043/45 is a CMOS 4096-bit serial E²PROM, internally organized as 512 X 8. The X25043/45 features a Serial Peripheral Interface (SPI) and software protocol allowing operation on a simple three-wire bus.

The X25043/45 utilizes Xicor's proprietary Direct Write™ cell, providing a minimum endurance of 100,000 cycles per byte and a minimum data retention of 100 years.

DIE PHOTOGRAPH



3844 PTO F01

Direct Write™ is a trademark of Xicor, Inc.

PIN DESCRIPTIONS

Serial Output (SO)

SO is a push/pull serial data output pin. During a read cycle, data is shifted out on this pin. Data is clocked out by the falling edge of the serial clock.

Serial Input (SI)

SI is the serial data input pin. All opcodes, byte addresses, and data to be written to the memory are input on this pin. Data is latched by the rising edge of the serial clock.

Serial Clock (SCK)

The Serial Clock controls the serial bus timing for data input and output. Opcodes, addresses, or data present on the SI pin is latched on the rising edge of the clock input, while data on the SO pin changes after the falling edge of the clock input.

Chip Select ($\overline{CS}$)

When $\overline{CS}$ is HIGH, the X25043/45 is deselected and the SO output pin is at high impedance and, unless an internal write operation is underway, the X25043/45 will be in the standby power mode. $\overline{CS}$ LOW enables the X25043/45, placing it in the active power mode. It should be noted that after power-up, a HIGH to LOW transition on $\overline{CS}$ is required prior to the start of any operation.

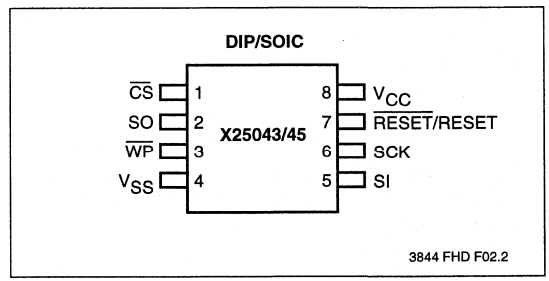
Write Protect ($\overline{WP}$)

When $\overline{WP}$ is LOW, nonvolatile writes to the X25043/45 are disabled, but the part otherwise functions normally. When $\overline{WP}$ is held HIGH, all functions, including nonvolatile writes operate normally. $\overline{WP}$ going LOW while $\overline{CS}$ is still LOW will interrupt a write to the X25043/45. If the internal write cycle has already been initiated, $\overline{WP}$ going LOW will have no affect on a write.

Reset ($\overline{RESET}$, RESET)

X25043/45, $\overline{RESET}$/RESET is an active LOW/HIGH, open drain output which goes active whenever V_{CC} falls below the mimimum V_{CC} sense level. It will remain active until V_{CC} rises above the minimum V_{CC} sense level for 200ms. $\overline{RESET}$/RESET also goes active if the Watchdog timer is enabled and $\overline{CS}$ remains either HIGH or LOW longer than the Watchdog time-out period. A falling edge of $\overline{CS}$ will reset the watchdog timer.

PIN CONFIGURATION



3844 FHD F02.2

PIN NAMES

Symbol	Description
$\overline{CS}$	Chip Select Input
SO	Serial Output
SI	Serial Input
SCK	Serial Clock Input
$\overline{WP}$	Write Protect Input
V_{SS}	Ground
V_{CC}	Supply Voltage
$\overline{RESET}$/RESET	Reset Output

3844 PGM T01.1

PRINCIPLES OF OPERATION

The X25043/45 is a 512 x 8 E^2PROM designed to interface directly with the synchronous serial peripheral interface (SPI) of many popular microcontroller families.

The X25043/45 contains an 8-bit instruction register. It is accessed via the SI input, with data being clocked in on the rising SCK. $\overline{CS}$ must be LOW and $\overline{WP}$ input must be HIGH during the entire operation. The X25043/45 monitors the bus and provides a $\overline{RESET}$/RESET output if there is no bus activity within the preset time period.

Table 1 contains a list of the instructions and their operation codes. All instructions, addresses and data are transferred MSB first. Bit 3 of the Read and Write instructions contain the higher order address bit, A_8.

Data input is sampled on the first rising edge of SCK after $\overline{CS}$ goes LOW. SCK is static, allowing the user to stop the clock and then resume operations.

Write Enable Latch

The X25043/45 contains a "write enable" latch. This latch must be SET before a write operation will be completed internally. The WREN instruction will set the latch and the WRDI instruction will reset the latch. This latch is automatically reset upon a power-up condition and after the completion of a byte, page, or status register write cycle. The latch is also reset if $\overline{WP}$ is brought LOW.

Status Register

The RDSR instruction provides access to the status register. The status register may be read at any time, even during a write cycle. The status register is formatted as follows:

7	6	5	4	3	2	1	0
X	X	WD1	WD0	BL1	BL0	WEL	WIP

3844 PGM T02

When issuing, WREN, WRDI and RDSR commands, it is not necessary to send a byte address or data.

The Write-In-Process (WIP) bit indicates whether the X25043/45 is busy with a write operation. When set to a "1", a write is in progress, when set to a "0", no write is in progress. During a write, all other bits are set to "1". The WIP bit is read-only.

The Write Enable Latch (WEL) bit indicates the status of the "write enable" latch. When set to a "1", the latch is set, when set to a "0", the latch is reset. The WEL bit is read-only and is set by the WREN instruction and reset by WRDI instruction or successful completion of a write cycle.

The Block Protect (BL0 and BL1) bits indicate the extent of protection employed. These nonvolatile bits are set by issuing the WRSR instruction and allows the user to select one of four levels of protection and program the watchdog timer. The X25043/45 is divided into four 1024-bit segments. One, two, or all four of the segments may be locked. That is, the user may read the segments but will be unable to alter (write) data within the selected segments. The partitioning is controlled as illustrated below with the state of BL1 and BL0.

Status Register Bits		Array Addresses Protected
BL1	BL0	
0	0	None
0	1	$180–$1FF
1	0	$100–$1FF
1	1	$000–$1FF

3844 PGM T04

The Watchdog Timer (WD0 and WD1) bits allow setting of the watchdog time-out function as shown in the table below. These nonvolatile bits are set by issuing the WRSR instruction.

Status Register Bits		Watchdog Time-out (Typical)
WD1	WD0	
0	0	1.4 Seconds
0	1	600 Milliseconds
1	0	200 Milliseconds
1	1	Disabled

3844 PGM T03

Clock and Data Timing

Data input on the SI line is latched on the rising edge of SCK. Data is output on the SO line by the falling edge of SCK.

Read Sequence

When reading from the E²PROM memory array, $\overline{CS}$ is first pulled LOW to select the device. The 8-bit READ instruction is transmitted to the X25043/45, followed by the 8-bit byte address. Bit 3 of the Read instruction contains address A_8. This bit is used to select the upper or lower half of the device. After the read opcode and byte address are sent, the data stored in the memory at the selected address is shifted out on the SO line. The data stored in memory at the next address can be read sequentially by continuing to provide clock pulses. The byte address is automatically incremented to the next higher address after each byte of data is shifted out. When the highest address is reached ($1FF) the address counter rolls over to address $000, allowing the read cycle to be continued indefinitely. The read operation is terminated by taking $\overline{CS}$ HIGH. Refer to the read E²PROM Array operation sequence illustrated in Figure 1.

To read the status register the $\overline{CS}$ line is first pulled LOW to select the device followed by the 8-bit RDSR instruction. After the read status register opcode is sent, the contents of the status register is shifted out on the SO line as shown in Figure 2.

Write Sequence

Prior to any attempt to write data into the X25043/45 the "write enable" latch must first be set by issuing the WREN instruction (See Figure 3). $\overline{CS}$ is first taken LOW, then the WREN instruction is clocked into the X25043/45. After all eight bits of the instruction are transmitted, $\overline{CS}$ must then be taken HIGH. If the user continues the write operation without taking $\overline{CS}$ HIGH after issuing the WREN instruction the write operation will be ignored.

To write data to the E²PROM memory array, the user issues the WRITE instruction, followed by the address and then the data to be written. Bit 3 of the Write instruction contains address A_8. This bit is used to select the upper or lower half of the device. This is minimally a twenty-four clock operation. $\overline{CS}$ must go LOW and remain LOW for the duration of the operation. The host may continue to write up to four bytes of data to the X25043/45. The only restriction is the four bytes must reside on the same page. A page address begins with address X XXXX XX00 and ends with X XXXX XX11. If the byte address counter reaches X XXXX XX11 and the clock continues the counter will roll back to the first address of the page and overwrite any data that may have been written.

For the write operation (byte or page write) to be completed, $\overline{CS}$ can only be brought HIGH after the twenty-fourth, thirty-second, fortieth, or forty-eighth clock. If it is brought HIGH at any other time, the write operation will not be completed. Refer to Figure 4 and 5 below for a detailed illustration of the write sequences.

While the write is in progress, following a status register or E²PROM write sequence the status register may be read to check the WIP bit. During this time the WIP bit will be HIGH and all other bits in the status register will be undefined.

$\overline{RESET}$/RESET Operation

The $\overline{RESET}$ (X25043) output is designed to go LOW whenever V_{CC} has dropped below the minimum trip point and/or the Watchdog timer has reached its programmable time-out limit.

Table 1. Instruction Set

Instruction Name	Instruction Format*	Operation
WREN	0000 0110	Set the Write Enable Latch (Enable Write Operations)
WRDI	0000 0100	Reset the Write Enable Latch (Disable Write Operations)
RDSR	0000 0101	Read Status Register
WRSR	0000 0001	Write Status Register (Block Lock Bits)
READ	0000 $A_8$011	Read Data from Memory Array beginning at selected address
WRITE	0000 $A_8$010	Write Data to Memory Array beginning at Selected Address (1 to 4 Bytes)

3844 PGM T05.1

*Instructions are shown MSB in leftmost position. Instructions are transferred MSB first.

The RESET (X25045) output is designed to go HIGH whenever V_{CC} has dropped below the minimum trip point and/or the watchdog timer has reached its programmable time-out limit.

Operational Notes

The X25043/45 powers-up in the following state:

- The device is in the low power standby state.
- A HIGH to LOW transition on $\overline{CS}$ is required to enter an active state and receive an instruction.
- SO pin is high impedance.
- The "write enable" latch is reset.

Data Protection

The following circuitry has been included to prevent inadvertent writes:

- The "write enable" latch is reset upon power-up.
- A WREN instruction must be issued to set the "write enable" latch.
- $\overline{CS}$ must come HIGH at the proper clock count in order to start a write cycle.

The "write enable" latch is reset when $\overline{WP}$ is brought LOW.

Figure 1. Read E²PROM Array Operation Sequence

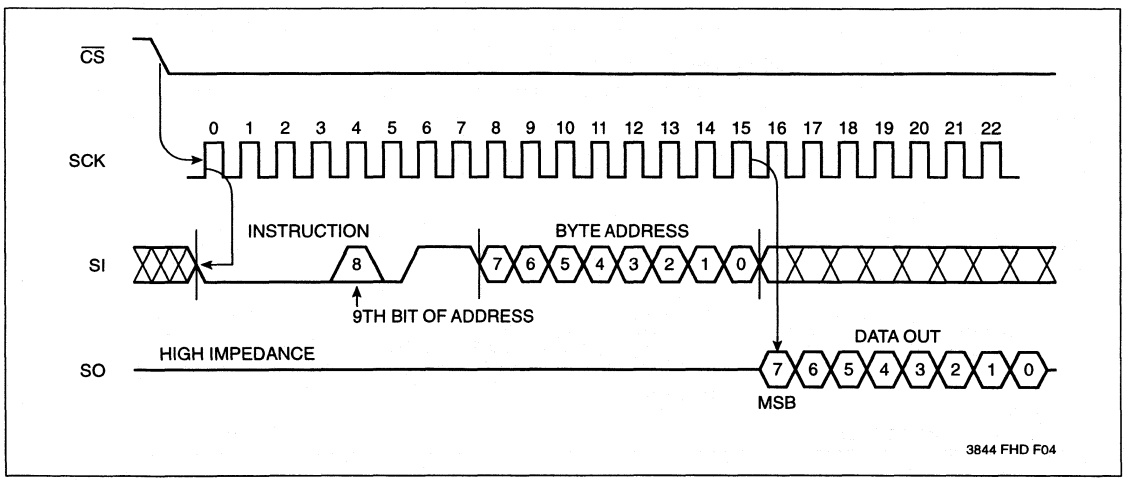


Figure 2. Read Status Register Operation Sequence

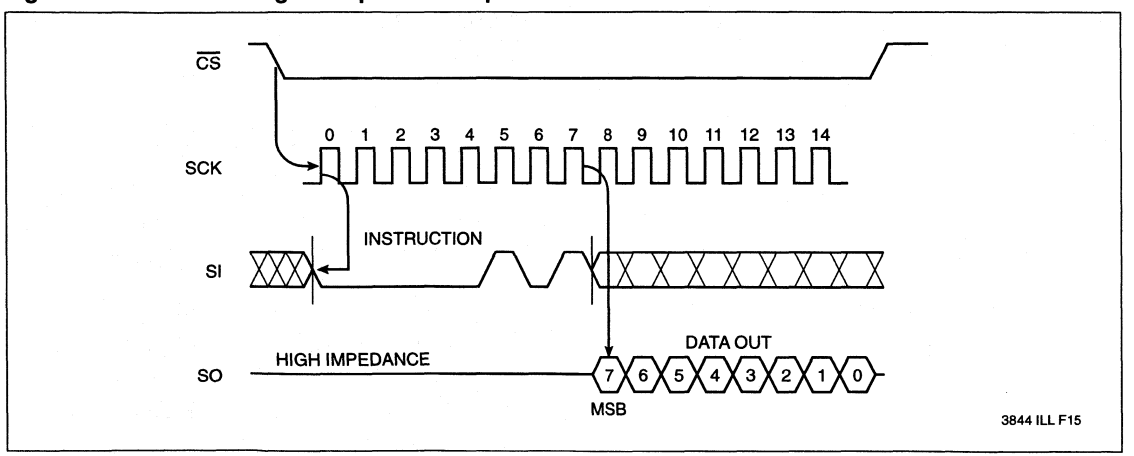


Figure 3. Write Enable Latch Sequence

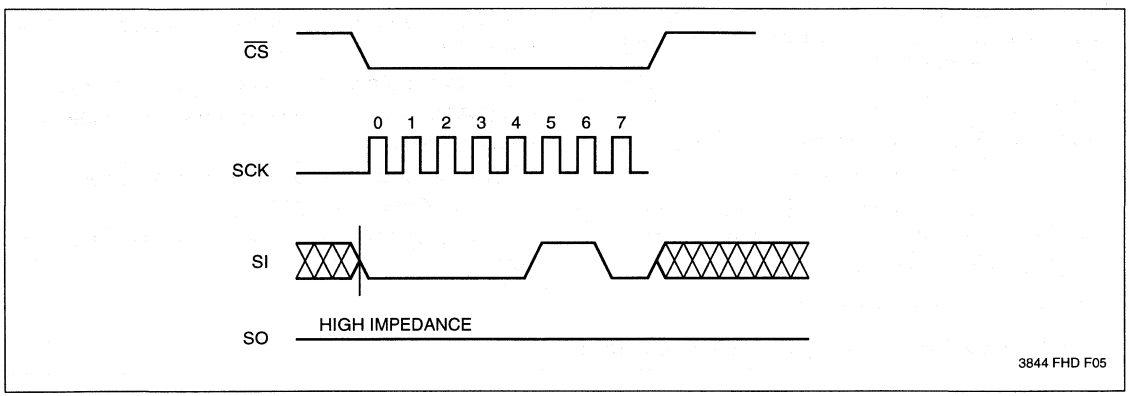
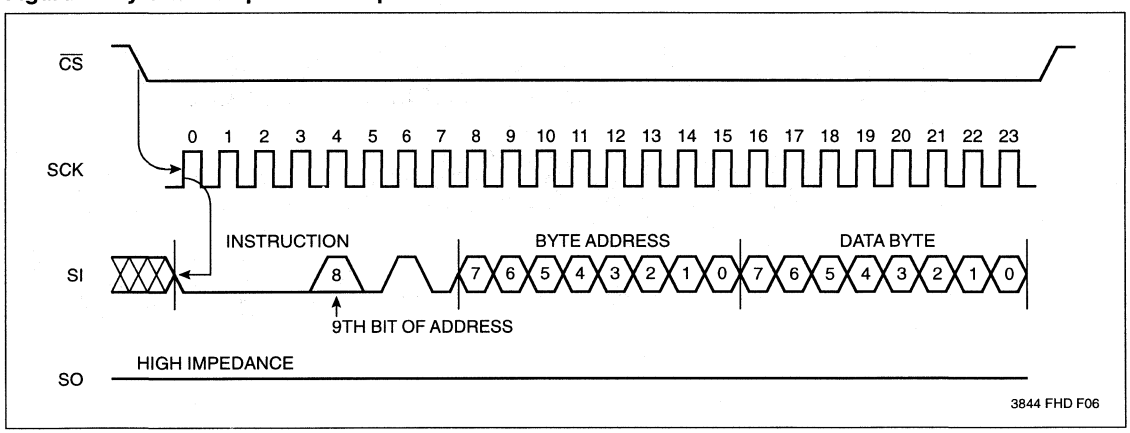


Figure 4. Byte Write Operation Sequence



SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

Figure 5. Page Write Operation Sequence

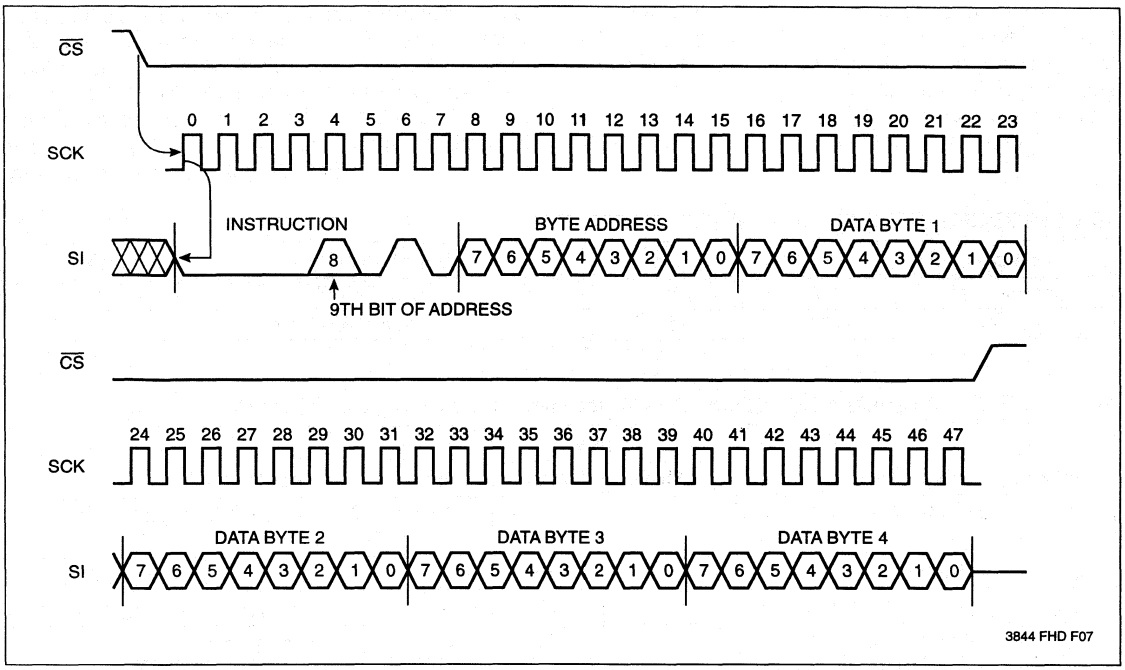
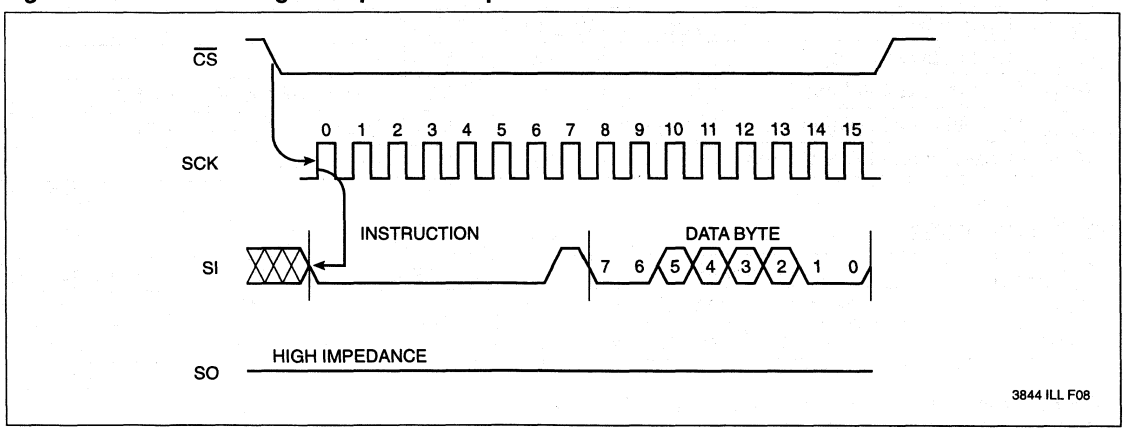


Figure 6. Write Status Register Operation Sequence



ABSOLUTE MAXIMUM RATINGS*

Temperature under Bias ..... –65°C to +135°C
Storage Temperature ..... –65°C to +150°C
Voltage on any Pin with Respect to V_{SS} ..... –1.0V to +7V
D.C. Output Current 5mA
Lead Temperature
(Soldering, 10 seconds) ..... 300°C

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temp	Min.	Max.
Commercial	0°C	70°C
Industrial	–40°C	+85°C

3844 PGM T06.1

Supply Voltage	Limits
X25043/45	5V ±10%
X25043/45-2.7	2.7 to 5.5V

3844 PGM T07.3

D.C. OPERATING CHARACTERISTICS (Over the recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
I_{CC}	V_{CC} Supply Current (Active)		3	mA	SCK = V_{CC} x 0.1/V_{CC} x 0.9 @ 1MHz, SO = Open
I_{SB1}	V_{CC} Standby Current		50	µA	$\overline{CS}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}, V_{CC} = 5.5
I_{SB2}	V_{CC} Standby Current		20	µA	$\overline{CS}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}, V_{CC} = 2.7V
I_{LI}	Input Leakage Current		10	µA	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output Leakage Current		10	µA	V_{OUT} = V_{SS} to V_{CC}
V_{IL}(1)	Input LOW Voltage	–0.5	V_{CC} x 0.3	V	
V_{IH}(1)	Input HIGH Voltage	V_{CC} x 0.7	V_{CC} + 0.5	V	
V_{OL}	Output LOW Voltage		0.4	V	I_{OL} = 2mA
V_{OH1}	Output HIGH Voltage	V_{CC}–0.8		V	I_{OH} = –1.6mA, V_{CC} = 4.5V
V_{OH2}	Output HIGH Voltage	V_{CC}–0.4		V	I_{OH} = –.4mA, V_{CC} = 2.7V
VOLRS	Reset Output LOW Voltage		0.4	V	I_{OL} = 1mA

3844 PGM T08.3

POWER-UP TIMING

Symbol	Parameter	Min.	Max.	Units
t_{PUR}(2)	Power-up to Read Operation		1	ms
t_{PUW}(2)	Power-up to Write Operation		5	ms

3844 PGM T09

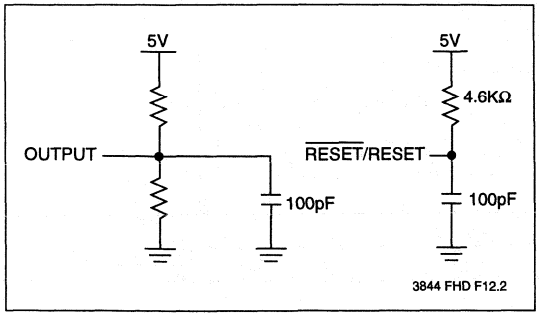
CAPACITANCE T_A = +25°C, f = 1MHz, V_{CC} = 5V.

Symbol	Test	Max.	Units	Conditions
C_{OUT}(2)	Output Capacitance (SO, $\overline{RESET}$, RESET)	8	pF	V_{OUT} = 0V
C_{IN}(2)	Input Capacitance (SCK, SI, $\overline{CS}$, $\overline{WP}$)	6	pF	V_{IN} = 0V

3844 PGM T10.2

Notes: (1) V_{IL} min. and V_{IH} max. are for reference only and are not tested.
(2) This parameter is periodically sampled and not 100% tested.

EQUIVALENT A.C. LOAD CIRCUIT AT 5V VCC



A.C. TEST CONDITIONS

Input Pulse Levels	V_{CC} x 0.1 to V_{CC} x 0.9
Input Rise and Fall Times	10ns
Input and Output Timing Level	V_{CC} x 0.5

3844 PGM T11

2

A.C. CHARACTERISTICS (Over recommended operating conditions, unless otherwise specified)

Data Input Timing

Symbol	Parameter	Min.	Max.	Units
f_{SCK}	Clock Frequency	0	1	MHz
t_{CYC}	Cycle Time	1000		ns
t_{LEAD}	$\overline{CS}$ Lead Time	500		ns
t_{LAG}	$\overline{CS}$ Lag Time	500		ns
t_{WH}	Clock HIGH Time	500		ns
t_{WL}	Clock LOW Time	400		ns
t_{SU}	Data Setup Time	100		ns
t_H	Data Hold Time	100		ns
t_{RI}(3)	Input Rise Time		2	µs
t_{FI}(3)	Input Fall Time		2	µs
t_{CS}	$\overline{CS}$ Deselect Time	500		ns
t_{WC}(4)	Write Cycle Time		10	ms

3844 PGM T12.2

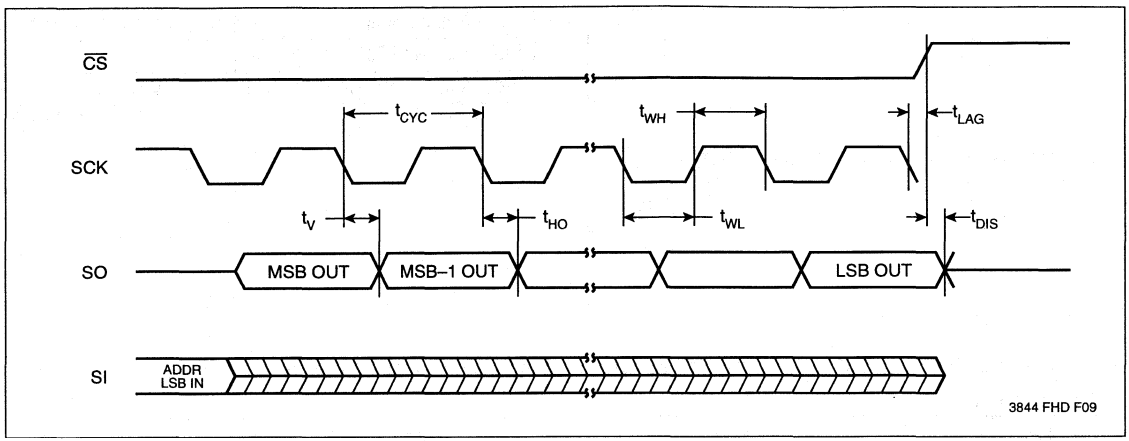
Data Output Timing

Symbol	Parameter	Min.	Max.	Units
f_{SCK}	Clock Frequency	0	1	MHz
t_{DIS}	Output Disable Time		500	ns
t_V	Output Valid from Clock LOW		400	ns
t_{HO}	Output Hold Time	0		ns
t_{RO}(3)	Output Rise Time		300	ns
t_{FO}(3)	Output Fall Time		300	ns

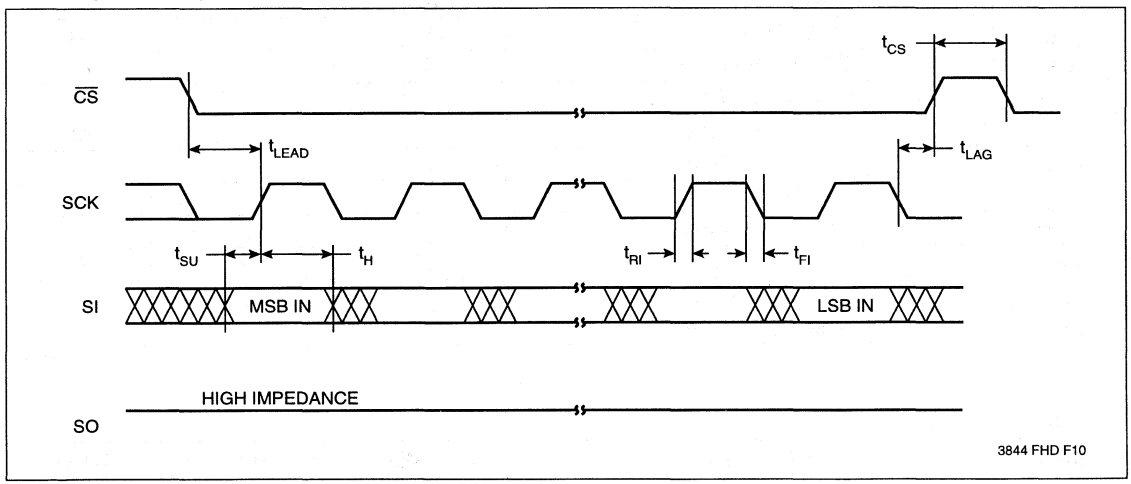
3844 PGM T13.1

Notes: (3) This parameter is periodically sampled and not 100% tested.
(4) t_{WC} is the time from the rising edge of $\overline{CS}$ after a valid write sequence has been sent to the end of the self-timed internal nonvolatile write cycle.

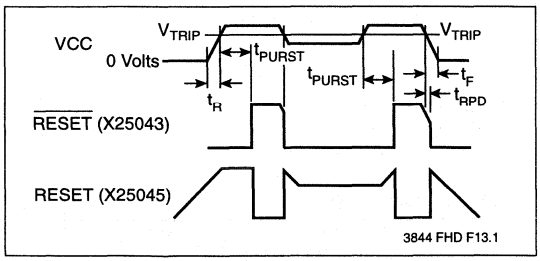
Serial Output Timing



Serial Input Timing



Power-Up and Power-Down Timing



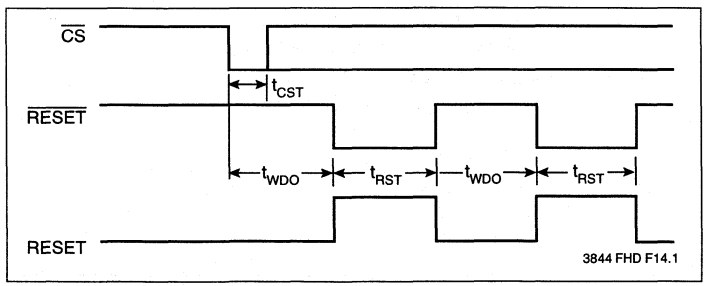
RESET Output Timing

Symbol	Parameter	Min.	Typ.	Max.	Units
V_{TRIP}	Reset Trip Point Voltage, 5V Device Reset Trip Point Voltage, 2.7V Device	4.25 2.55		4.5 2.7	V V
t_{PURST}	Power-up Reset Timeout	100		400	ms
t_{RPD}(5)	V_{CC} Detect to Reset/Output			500	ns
t_F(5)	V_{CC} Fall Time	10			µs
t_R(5)	V_{CC} Rise Time	0			ns
V_{RVALID}	Reset Valid V_{CC}	1			V

3844 PGM T14.3

Notes: (5) This parameter is periodically sampled and not 100% tested.

CS vs RESET/RESET Timing

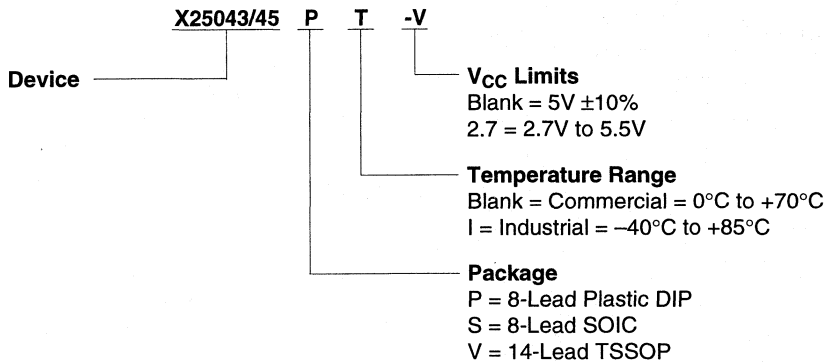


RESET/RESET Output Timing

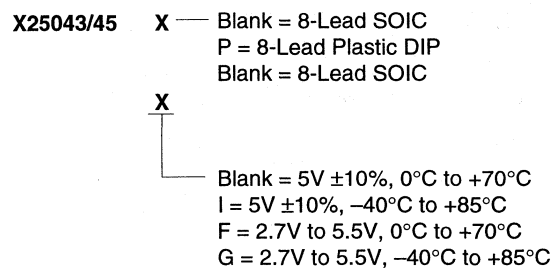
Symbol	Parameter	Min.	Typ.	Max.	Units
t_{WDO}	Watchdog Timeout Period, WD1=1,WD0=0 WD1=0,WD0=1 WD1=0,WD0=0	 100 450 1	 200 600 1.4	 300 800 2	 ms ms sec
t_{CST}	CS Pulse Width to Reset the Watchdog	400			ns
t_{RST}	Reset Timeout	100		400	ms

3844 PGM T15.3

ORDERING INFORMATION



Part Mark Convention



NOTES

XICOR

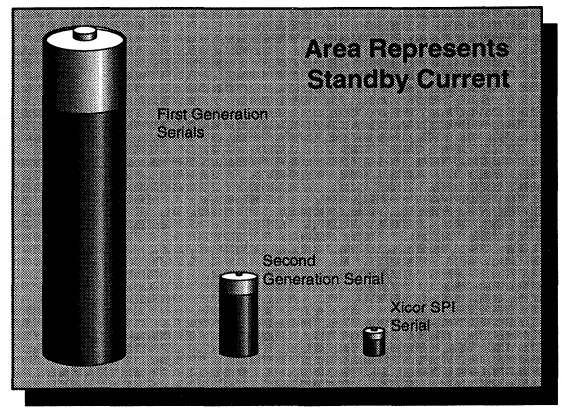
#10

Design Engineering Bulletin

New Product and Applications Information for Design Engineers

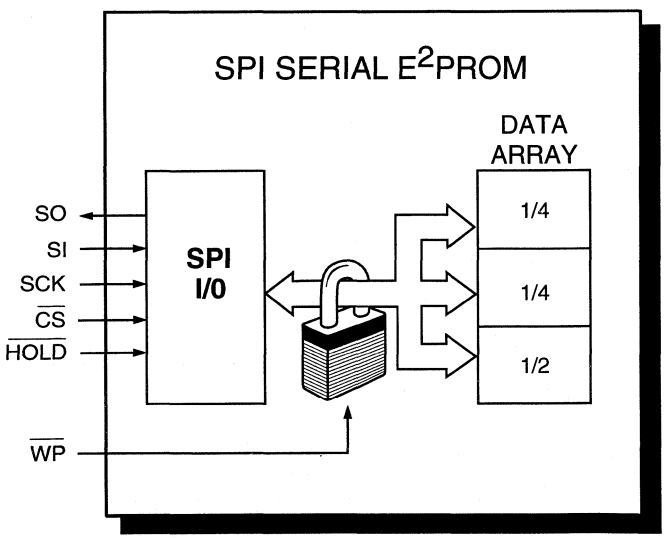
Longer Battery Life, Faster Data Access and High Density!

The New X25080/160/320/642/128 serial E²PROM family from Xicor offers a true low power solution for battery powered systems. Combining low standby current, faster data rates, smaller packages and higher density, this new serial E²PROM family provides the optimum choice for new, portable hand-held equipment designs. In addition the X25080/160/320/642/128 family offers BlockLock which gives you the ability to protect portions of the memory being altered once the device is inserted into the system. BlockLock supports a hierarchical combination of software segmented data protections as well as hardware data protection using a programmable write protection input. This new family of serial E²PROMs continues to pace the industry for innovative nonvolatile devices which addresses the need for low power at the same time as offering optimum density and superior non volatile data protection. The SPI (Serial Peripheral Interface) coupled with an advanced chip architecture makes these devices superior to previous generations of serial E²PROMs.



World's highest density/performance small serial E²PROM.

Programmable Hardware Pin and Data Software Key Locks Down Valuable Data



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The X25080/160/320/642/128 is the first complete family of serial E²PROMs which offer a programmable hardware write protect pin combined with the software ability to protect portions of the memory array from overwriting. Using a configuration register it is possible to define which area of the memory will be write protected. This feature lets you solder the device into a system and then permanently lock down portions of the memory array via a software key after the final system configuration is defined. Once locked, the protected portion of the memory array cannot be overwritten as long as the write protect pin remains soldered to ground. Specific portions of the memory area can be used for storing configuration or serialization data and locked from inadvertent or intrusive data changes once the system is in normal operation. Unlocked portions of the array can be accessed for normal data alteration.

8K X25080 1K x 8 Bit

SPI Serial E²PROM With Block Lock™ Protection

FEATURES

- 2MHz Clock Rate
- SPI Modes (0,0 & 1,1)
- 1K X 8 Bits
  - —32 Byte Page Mode
- Low Power CMOS
  - —<1μA Standby Current
  - —<5mA Active Current
- 2.7V To 5.5V Power Supply
- Block Lock Protection
  - —Protect 1/4, 1/2 or all of E²PROM Array
- Built-in Inadvertent Write Protection
  - —Power-Up/Power-Down protection circuitry
  - —Write Enable Latch
  - —Write Protect Pin
- Self-Timed Write Cycle
  - —5ms Write Cycle Time (Typical)
- High Reliability
  - —Endurance: 100,000 cycles
  - —Data Retention: 100 Years
  - —ESD protection: 2000V on all pins
- 8-Pin Mini-DIP Package
- 8-Lead SOIC Package
- 14-Lead TSSOP Package

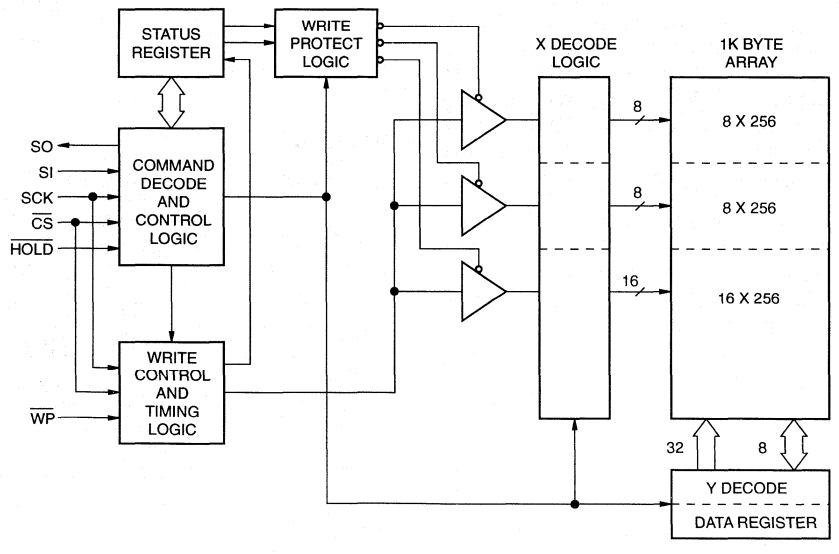
DESCRIPTION

The X25080 is a CMOS 8192-bit serial E²PROM, internally organized as 1K x 8. The X25080 features a Serial Peripheral Interface (SPI) and software protocol allowing operation on a simple three-wire bus. The bus signals are a clock input (SCK) plus separate data in (SI) and data out (SO) lines. Access to the device is controlled through a chip select ($\overline{CS}$) input, allowing any number of devices to share the same bus.

The X25080 also features two additional inputs that provide the end user with added flexibility. By asserting the $\overline{HOLD}$ input, the X25080 will ignore transitions on its inputs, thus allowing the host to service higher priority interrupts. The $\overline{WP}$ input can be used as a hardwire input to the X25080 disabling all write attempts to the status register, thus providing a mechanism for limiting end user capability of altering 0, 1/4, 1/2 or all of the memory.

The X25080 utilizes Xicor's proprietary Direct Write™ cell, providing a minimum endurance of 100,000 cycles and a minimum data retention of 100 years.

FUNCTIONAL DIAGRAM



Direct Write™ and Block Lock™ Protection is a trademark of Xicor, Inc.

PIN DESCRIPTIONS

Serial Output (SO)

SO is a push/pull serial data output pin. During a read cycle, data is shifted out on this pin. Data is clocked out by the falling edge of the serial clock.

Serial Input (SI)

SI is the serial data input pin. All opcodes, byte addresses, and data to be written to the memory are input on this pin. Data is latched by the rising edge of the serial clock.

Serial Clock (SCK)

The Serial Clock controls the serial bus timing for data input and output. Opcodes, addresses, or data present on the SI pin are latched on the rising edge of the clock input, while data on the SO pin change after the falling edge of the clock input.

Chip Select ($\overline{CS}$)

When $\overline{CS}$ is HIGH, the X25080 is deselected and the SO output pin is at high impedance and unless an internal write operation is underway, the X25080 will be in the standby power mode. $\overline{CS}$ LOW enables the X25080, placing it in the active power mode. It should be noted that after power-up, a HIGH to LOW transition on $\overline{CS}$ is required prior to the start of any operation.

Write Protect ($\overline{WP}$)

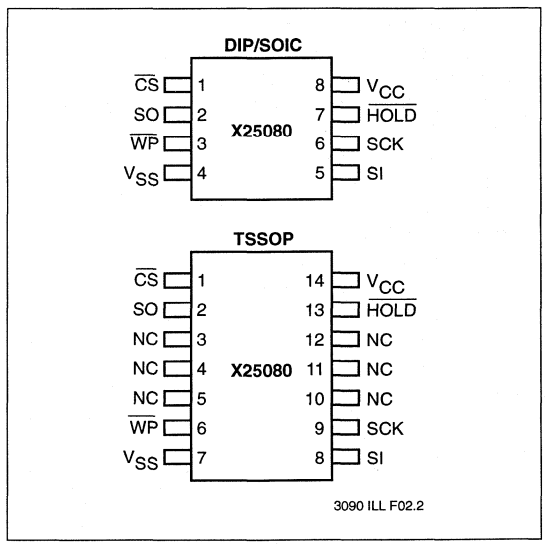
When $\overline{WP}$ is LOW and the nonvolatile bit WPEN is "1", nonvolatile writes to the X25080 status register are disabled, but the part otherwise functions normally. When $\overline{WP}$ is held HIGH, all functions, including nonvolatile writes operate normally. $\overline{WP}$ going LOW while $\overline{CS}$ is still LOW will interrupt a write to the X25080 status register. If the internal write cycle has already been initiated, $\overline{WP}$ going LOW will have no effect on a write.

The $\overline{WP}$ pin function is blocked when the WPEN bit in the status register is "0". This allows the user to install the X25080 in a system with $\overline{WP}$ pin grounded and still be able to write to the status register. The $\overline{WP}$ pin functions will be enabled when the WPEN bit is set "1".

Hold ($\overline{HOLD}$)

$\overline{HOLD}$ is used in conjunction with the $\overline{CS}$ pin to select the device. Once the part is selected and a serial sequence is underway, $\overline{HOLD}$ may be used to pause the serial communication with the controller without resetting the serial sequence. To pause, $\overline{HOLD}$ must be brought LOW while SCK is LOW. To resume communication, $\overline{HOLD}$ is brought HIGH, again while SCK is LOW. If the pause feature is not used, $\overline{HOLD}$ should be held HIGH at all times.

PIN CONFIGURATION



PIN NAMES

SYMBOL	DESCRIPTION
$\overline{CS}$	Chip Select Input
SO	Serial Output
SI	Serial Input
SCK	Serial Clock Input
$\overline{WP}$	Write Protect Input
V_{SS}	Ground
V_{CC}	Supply Voltage
$\overline{HOLD}$	Hold Input
NC	No Connect

3090 PGM T01

PRINCIPLES OF OPERATION

The X25080 is a 1K x 8 E^2PROM designed to interface directly with the synchronous serial peripheral interface (SPI) of many popular microcontroller families.

The X25080 contains an 8-bit instruction register. It is accessed via the SI input, with data being clocked in on the rising SCK. $\overline{CS}$ must be LOW and the $\overline{HOLD}$ and $\overline{WP}$ inputs must be HIGH during the entire operation. The $\overline{WP}$ input is "Don't Care" if WPEN is set "0".

Table 1 contains a list of the instructions and their opcodes. All instructions, addresses and data are transferred MSB first.

Data input is sampled on the first rising edge of SCK after $\overline{CS}$ goes LOW. SCK is static, allowing the user to stop the clock and then resume operations. If the clock line is shared with other peripheral devices on the SPI bus, the user can assert the $\overline{HOLD}$ input to place the X25080 into a "PAUSE" condition. After releasing $\overline{HOLD}$, the X25080 will resume operation from the point when $\overline{HOLD}$ was first asserted.

Write Enable Latch

The X25080 contains a "write enable" latch. This latch must be SET before a write operation will be completed internally. The WREN instruction will set the latch and the WRDI instruction will reset the latch. This latch is automatically reset upon a power-up condition and after the completion of a byte, page, or status register write cycle.

Status Register

The RDSR instruction provides access to the status register. The status register may be read at any time, even during a write cycle. The status register is formatted as follows:

7	6	5	4	3	2	1	0
WPEN	X	X	X	BP1	BP0	WEL	WIP

3090 PGM T02

WPEN, BP0 and BP1 are set by the WRSR instruction. WEL and WIP are read-only and automatically set by other operations.

The Write-In-Process (WIP) bit indicates whether the X25080 is busy with a write operation. When set to a "1", a write is in progress, when set to a "0", no write is in progress. During a write, all other bits are set to "1".

The Write Enable Latch (WEL) bit indicates the status of the "write enable" latch. When set to a "1", the latch is set, when set to a "0", the latch is reset.

The Block Protect (BP0 and BP1) bits are nonvolatile and allow the user to select one of four levels of protection. The X25080 is divided into four 2048-bit segments. One, two, or all four of the segments may be protected. That is, the user may read the segments but will be unable to alter (write) data within the selected segments. The partitioning is controlled as illustrated below.

Status Register Bits		Array Addresses Protected
BP1	BP0	
0	0	None
0	1	$0300–$03FF
1	0	$0200–$03FF
1	1	$0000–$03FF

3090 PGM T03

Table 1. Instruction Set

Instruction Name	Instruction Format*	Operation
WREN	0000 0110	Set the Write Enable Latch (Enable Write Operations)
WRDI	0000 0100	Reset the Write Enable Latch (Disable Write Operations)
RDSR	0000 0101	Read Status Register
WRSR	0000 0001	Write Status Register
READ	0000 0011	Read Data from Memory Array beginning at selected address
WRITE	0000 0010	Write Data to Memory Array beginning at Selected Address (1 to 32 Bytes)

3090 PGM T04

*Instructions are shown MSB in leftmost position. Instructions are transferred MSB first.

Write-Protect Enable

The Write-Protect-Enable (WPEN) is available for the X25080 as a nonvolatile enable bit for the $\overline{WP}$ pin.

WPEN	$\overline{WP}$	WEL	Protected Blocks	Unprotected Blocks	Status Register
0	X	0	Protected	Protected	Protected
0	X	1	Protected	Writable	Writable
1	LOW	0	Protected	Protected	Protected
1	LOW	1	Protected	Writable	Protected
X	HIGH	0	Protected	Protected	Protected
X	HIGH	1	Protected	Writable	Writable

3090 PGM T05.1

The Write Protect ($\overline{WP}$) pin and the nonvolatile Write Protect Enable (WPEN) bit in the Status Register control the programmable hardware write protect feature. Hardware write protection is enabled when $\overline{WP}$ pin is LOW, and the WPEN bit is "1". Hardware write protection is disabled when either the $\overline{WP}$ pin is HIGH or the WPEN bit is "0". When the chip is hardware write protected, nonvolatile writes are disabled to the Status Register, including the Block Protect bits and the WPEN bit itself, as well as the block-protected sections in the memory array. Only the sections of the memory array that are not block-protected can be written.

Note: Since the WPEN bit is write protected, it cannot be changed back to a "0", as long as the $\overline{WP}$ pin is held LOW.

Clock and Data Timing

Data input on the SI line is latched on the rising edge of SCK. Data is output on the SO line by the falling edge of SCK.

Read Sequence

When reading from the E^{2}PROM memory array $\overline{CS}$ is first pulled LOW to select the device. The 8-bit READ instruction is transmitted to the X25080, followed by the 16-bit address of which the last 10 are used. After the READ opcode and address are sent, the data stored in the memory at the selected address is shifted out on the SO line. The data stored in memory at the next address can be read sequentially by continuing to provide clock pulses. The address is automatically incremented to the next higher address after each byte of data is shifted out. When the highest address is reached ($03FF) the address counter rolls over to address $0000 allowing the read cycle to be continued indefinitely. The read operation is terminated by taking $\overline{CS}$ HIGH. Refer to the read E^{2}PROM array operation sequence illustrated in Figure 1.

To read the status register the $\overline{CS}$ line is first pulled LOW to select the device followed by the 8-bit RDSR instruction. After the RDSR opcode is sent, the contents of the status register are shifted out on the SO line. The read status register sequence is illustrated in Figure 2.

Write Sequence

Prior to any attempt to write data into the X25080, the "write enable" latch must first be set by issuing the WREN instruction (See Figure 3). $\overline{CS}$ is first taken LOW, then the WREN instruction is clocked into the X25080. After all eight bits of the instruction are transmitted, $\overline{CS}$ must then be taken HIGH. If the user continues the write operation without taking $\overline{CS}$ HIGH after issuing the WREN instruction, the write operation will be ignored.

To write data to the E^{2}PROM memory array, the user issues the WRITE instruction, followed by the address and then the data to be written. This is minimally a thirty-two clock operation. $\overline{CS}$ must go LOW and remain LOW for the duration of the operation. The host may continue to write up to 32 bytes of data to the X25080. The only restriction is the 32 bytes must reside on the same page. If the address counter reaches the end of the page and the clock continues, the counter will "roll over" to the first address of the page and overwrite any data that may have been written.

For the write operation (byte or page write) to be completed, $\overline{CS}$ can only be brought HIGH after bit 0 of data byte N is clocked in. If it is brought HIGH at any other time the write operation will not be completed. Refer to Figures 4 and 5 below for a detailed illustration of the write sequences and time frames in which $\overline{CS}$ going HIGH are valid.

To write to the status register, the WRSR instruction is followed by the data to be written. Data bits 0, 1, 4, 5 and 6 must be "0". Figure 6 shows this sequence.

While the write is in progress following a status register or E^{2}PROM write sequence, the status register may be read to check the WIP bit. During this time the WIP bit will be "1".

Hold Operation

The $\overline{HOLD}$ input should be HIGH (at V_{IH}) under normal operation. If a data transfer is to be interrupted $\overline{HOLD}$ can be pulled LOW to suspend the transfer until it can be resumed. The only restriction is the SCK input must be LOW when $\overline{HOLD}$ is first pulled LOW and SCK must also be LOW when $\overline{HOLD}$ is released.

The $\overline{HOLD}$ input may be tied HIGH either directly to V_{CC} or tied to V_{CC} through a resistor.

Operational Notes

The X25080 powers-up in the following state:

- The device is in the low power standby state.
- A HIGH to LOW transition on $\overline{CS}$ is required to enter an active state and receive an instruction.
- SO pin is high impedance.
- The "write enable" latch is reset.

Data Protection

The following circuitry has been included to prevent inadvertent writes:

- The "write enable" latch is reset upon power-up.
- A WREN instruction must be issued to set the "write enable" latch.
- $\overline{CS}$ must come HIGH at the proper clock count in order to start a write cycle.

Figure 1. Read E²PROM Array Operation Sequence

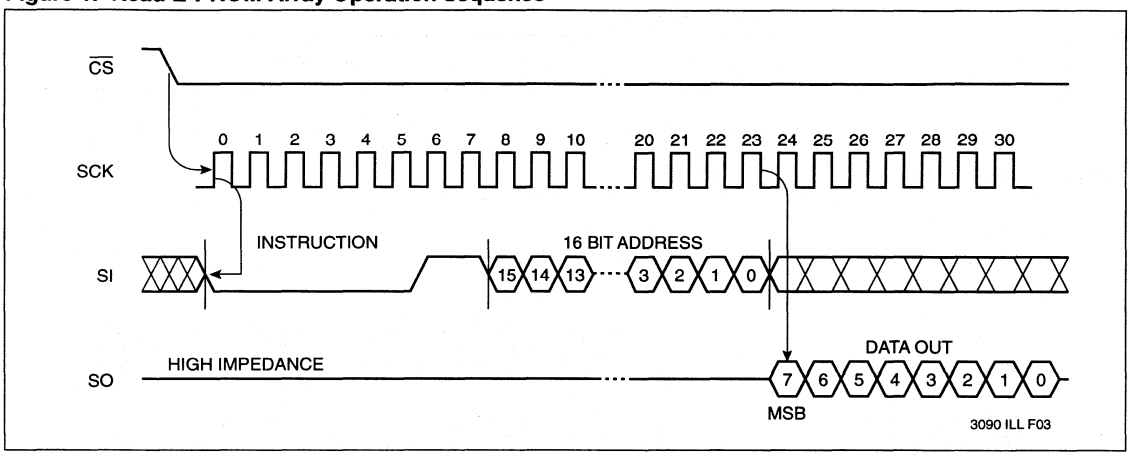


Figure 2. Read Status Register Operation Sequence

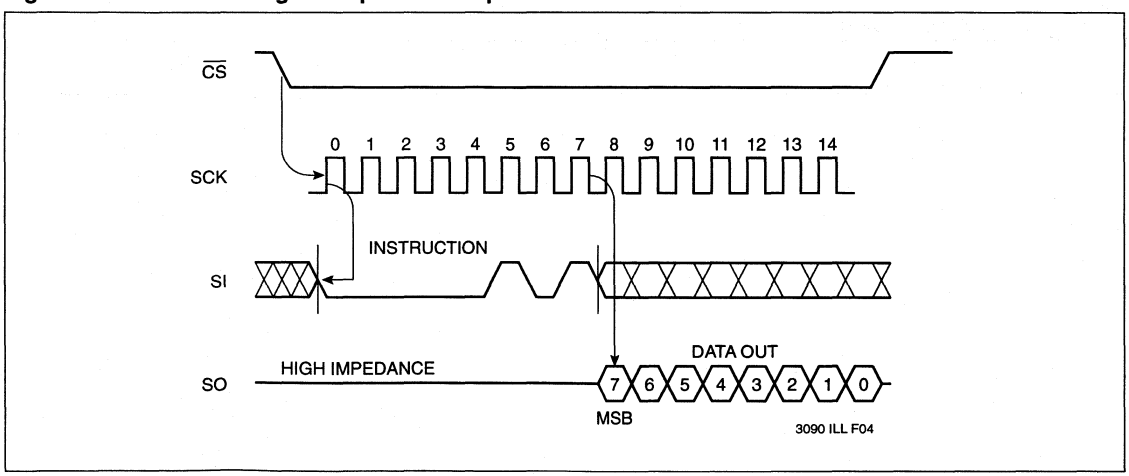


Figure 3. Write Enable Latch Sequence

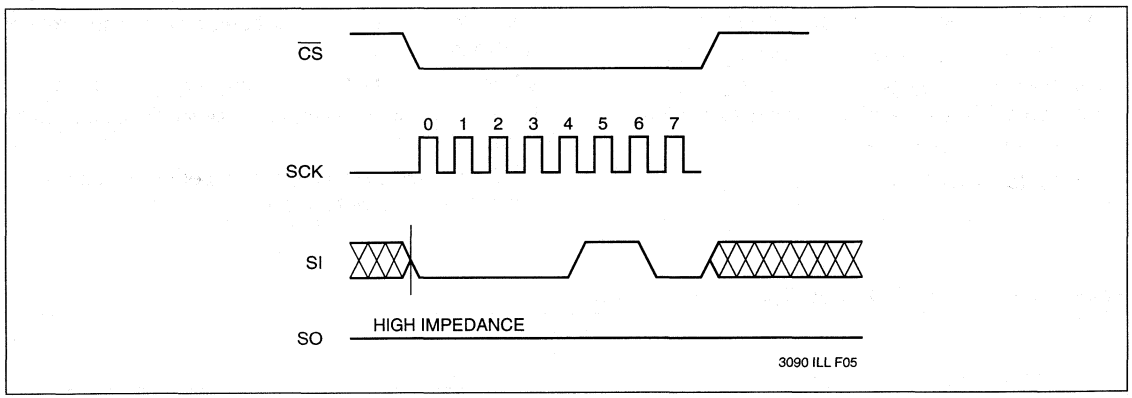


Figure 4. Byte Write Operation Sequence

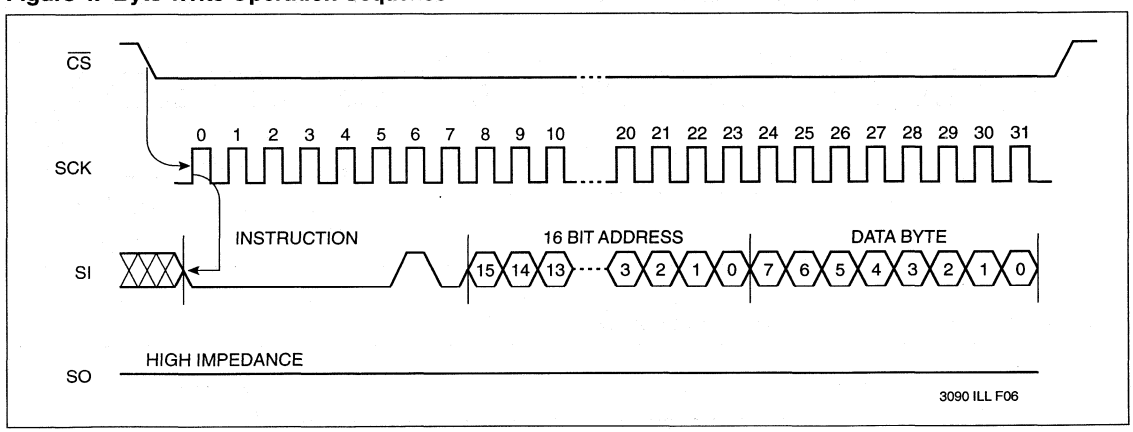


Figure 5. Page Write Operation Sequence

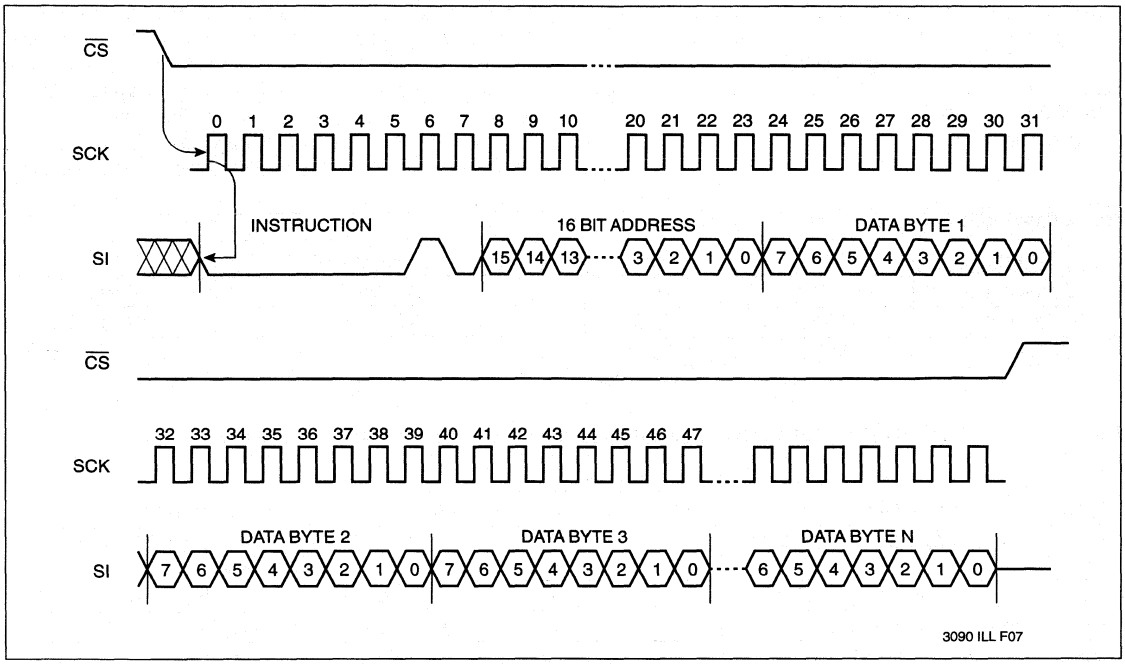
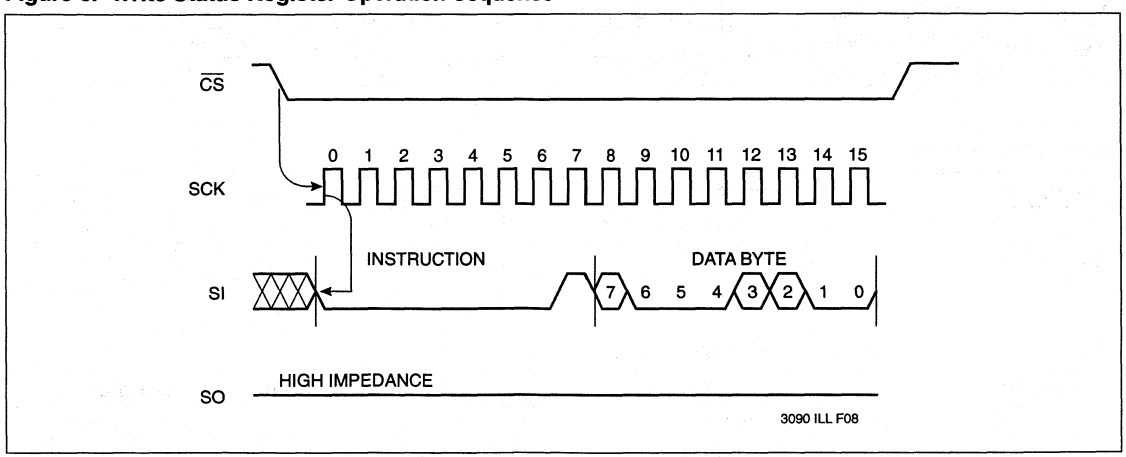


Figure 6. Write Status Register Operation Sequence



ABSOLUTE MAXIMUM RATINGS*

Temperature under Bias ..... –65°C to +135°C
Storage Temperature ..... –65°C to +150°C
Voltage on any Pin with Respect to V_{SS} ..... –1V to +7V
D.C. Output Current 5mA
Lead Temperature
(Soldering, 10 seconds) ..... 300°C

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temp	Min.	Max.
Commercial	0°C	+70°C
Industrial	–40°C	+85°C
Military	–55°C	+125°C

3090 PGM T06.1

Supply Voltage	Limits
X25080	5V ±10%
X25080-2.7	2.7V to 5.5V

3090 PGM T07.1

D.C. OPERATING CHARACTERISTICS (Over the recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
I_{CC}	V_{CC} Supply Current (Active)		5	mA	SCK = V_{CC} x 0.1/V_{CC} x 0.9 @ 2MHz, SO = Open, $\overline{CS}$ = V_{SS}
I_{SB}	V_{CC} Supply Current (Standby)		1	µA	$\overline{CS}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}
I_{LI}	Input Leakage Current		10	µA	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output Leakage Current		10	µA	V_{OUT} = V_{SS} to V_{CC}
V_{IL}(1)	Input LOW Voltage	–1	V_{CC} x 0.3	V	
V_{IH}(1)	Input HIGH Voltage	V_{CC} x 0.7	V_{CC} + 0.5	V	
V_{OL1}	Output LOW Voltage		0.4	V	V_{CC} = 5V, I_{OL} = 3mA
V_{OH1}	Output HIGH Voltage	V_{CC} – 0.8		V	V_{CC} = 5V, I_{OH} = -1.6mA
V_{OL2}	Output LOW Voltage		0.4	V	V_{CC} = 3V, I_{OL} = 1.5mA
V_{OH2}	Output HIGH Voltage	V_{CC} – 0.3		V	V_{CC} = 3V, I_{OH} = -0.4mA

3090 PGM T08.3

POWER-UP TIMING

Symbol	Parameter	Min.	Max.	Units
t_{PUR}(3)	Power-up to Read Operation		1	ms
t_{PUW}(3)	Power-up to Write Operation		5	ms

3090 PGM T09

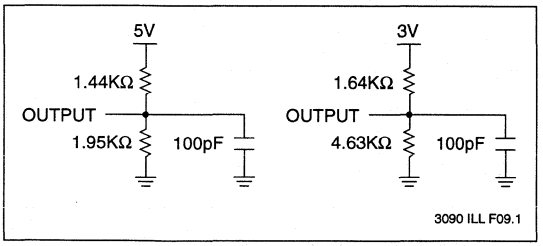
CAPACITANCE T_A = +25°C, f = 1MHz, V_{CC} = 5V.

Symbol	Test	Max.	Units	Conditions
C_{OUT}(2)	Output Capacitance (SO)	8	pF	V_{OUT} = 0V
C_{IN}(2)	Input Capacitance (SCK, SI, $\overline{CS}$, $\overline{WP}$, $\overline{HOLD}$)	6	pF	V_{IN} = 0V

3090 PGM T10.1

Notes: (1) V_{IL} min. and V_{IH} max. are for reference only and are not tested.
(2) This parameter is periodically sampled and not 100% tested.
(3) t_{PUR} and t_{PUW} are the delays required from the time V_{CC} is stable until the specified operation can be initiated. These parameters are periodically sampled and not 100% tested.

EQUIVALENT A.C. LOAD CIRCUIT



A.C. TEST CONDITIONS

Input Pulse Levels	V_{CC} x 0.1 to V_{CC} x 0.9
Input Rise and Fall Times	10ns
Input and Output Timing Level	V_{CC} x 0.5

3090 PGM T11

2

A.C. CHARACTERISTICS (Over recommended operating conditions, unless otherwise specified)

Data Input Timing

Symbol	Parameter	Min.	Max.	Units
f_{SCK}	Clock Frequency	0	2	MHz
t_{CYC}	Cycle Time	500		ns
t_{LEAD}	$\overline{CS}$ Lead Time	250		ns
t_{LAG}	$\overline{CS}$ Lag Time	250		ns
t_{WH}	Clock HIGH Time	200		ns
t_{WL}	Clock LOW Time	200		ns
t_{SU}	Data Setup Time	50		ns
t_H	Data Hold Time	50		ns
t_{RI}(4)	Data In Rise Time		2	µs
t_{FI}(4)	Data In Fall Time		2	µs
t_{HD}	$\overline{HOLD}$ Setup Time	100		ns
t_{CD}	$\overline{HOLD}$ Hold Time	100		ns
t_{CS}	$\overline{CS}$ Deselect Time	2.0		µs
t_{WC}(5)	Write Cycle Time		10	ms

3090 PGM T12.2

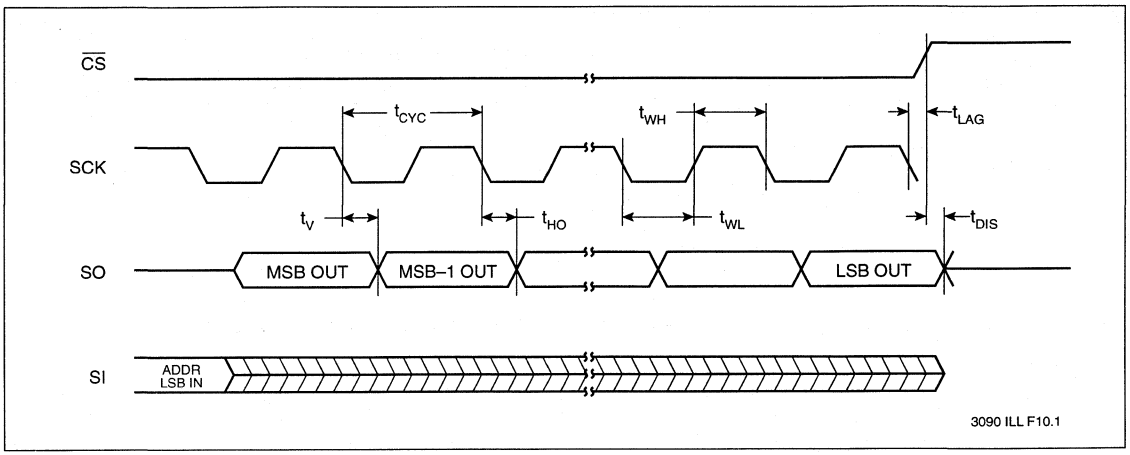
Data Output Timing

Symbol	Parameter	Min.	Max.	Units
f_{SCK}	Clock Frequency	0	2	MHz
t_{DIS}	Output Disable Time		250	ns
t_V	Output Valid from Clock LOW		200	ns
t_{HO}	Output Hold Time	0		ns
t_{RO}(4)	Output Rise Time		100	ns
t_{FO}(4)	Output Fall Time		100	ns
t_{LZ}(4)	$\overline{HOLD}$ HIGH to Output in Low Z	100		ns
t_{HZ}(4)	$\overline{HOLD}$ LOW to Output in High Z	100		ns

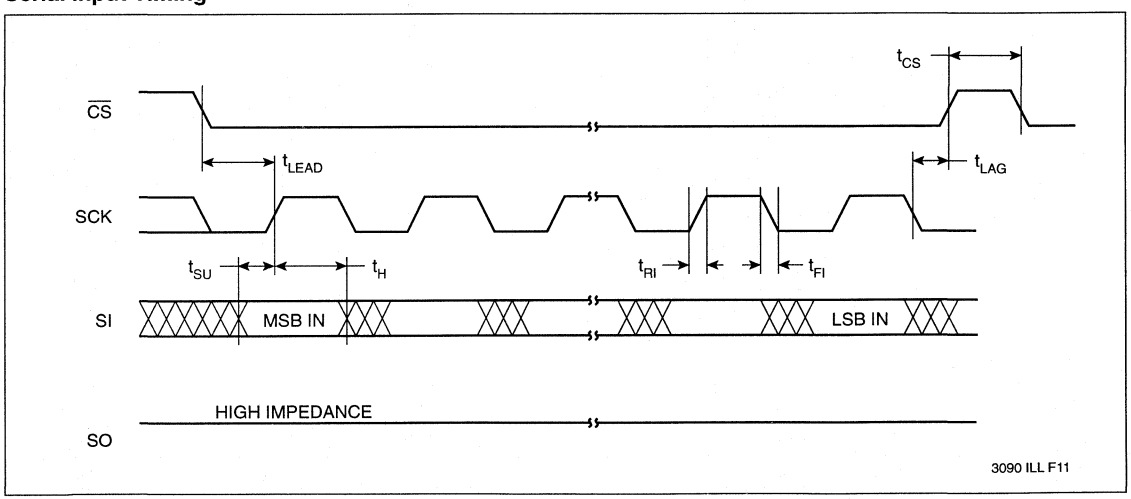
3090 PGM T13.2

Notes: (4) This parameter is periodically sampled and not 100% tested.
(5) t_{WC} is the time from the rising edge of $\overline{CS}$ after a valid write sequence has been sent to the end of the self-timed internal nonvolatile write cycle.

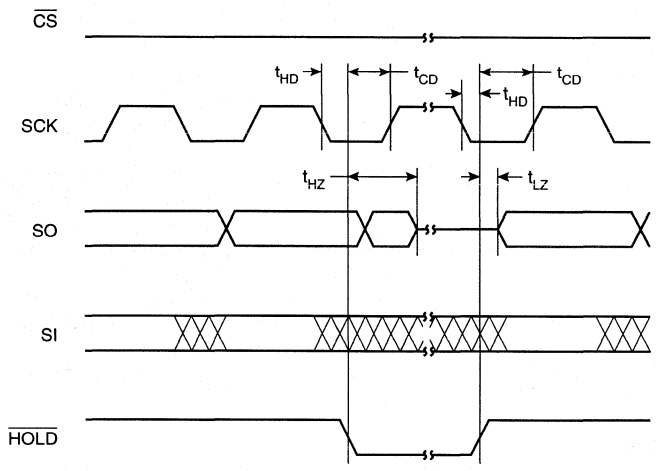
Serial Output Timing



Serial Input Timing



Hold Timing

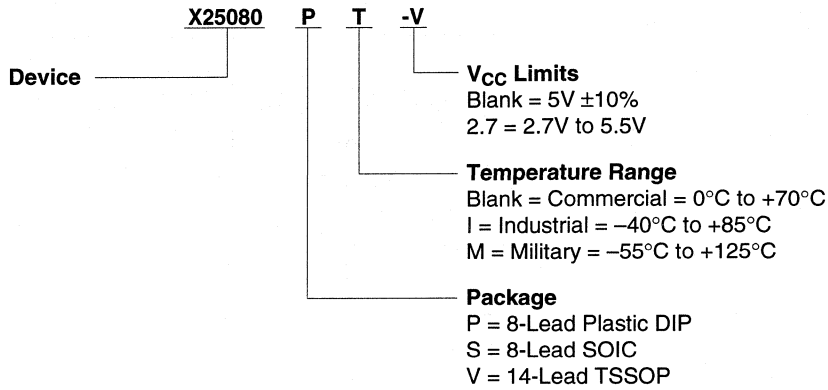


3090 ILL F12.1

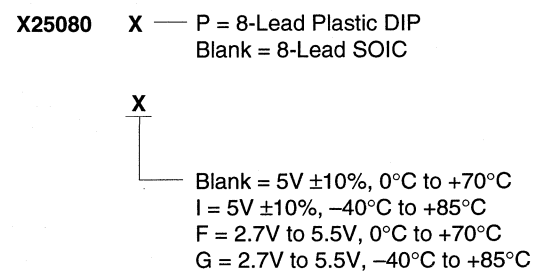
SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

ORDERING INFORMATION



Part Mark Convention



16K X25160 2K x 8 Bit

SPI Serial E²PROM With Block Lock™ Protection

FEATURES

- 2MHz Clock Rate
- SPI Modes (0,0 & 1,1)
- 2K X 8 Bits
  - —32 Byte Page Mode
- Low Power CMOS
  - —<1μA Standby Current
  - —<5mA Active Current
- 2.7V To 5.5V Power Supply
- Block Lock Protection
  - —Protect 1/4, 1/2 or all of E²PROM Array
- Built-in Inadvertent Write Protection
  - —Power-Up/Power-Down protection circuitry
  - —Write Enable Latch
  - —Write Protect Pin
- Self-Timed Write Cycle
  - —5ms Write Cycle Time (Typical)
- High Reliability
  - —Endurance: 100,000 cycles
  - —Data Retention: 100 Years
  - —ESD protection: 2000V on all pins
- 8-Pin Mini-DIP Package
- 8-Lead SOIC Package
- 14-Lead TSSOP Package

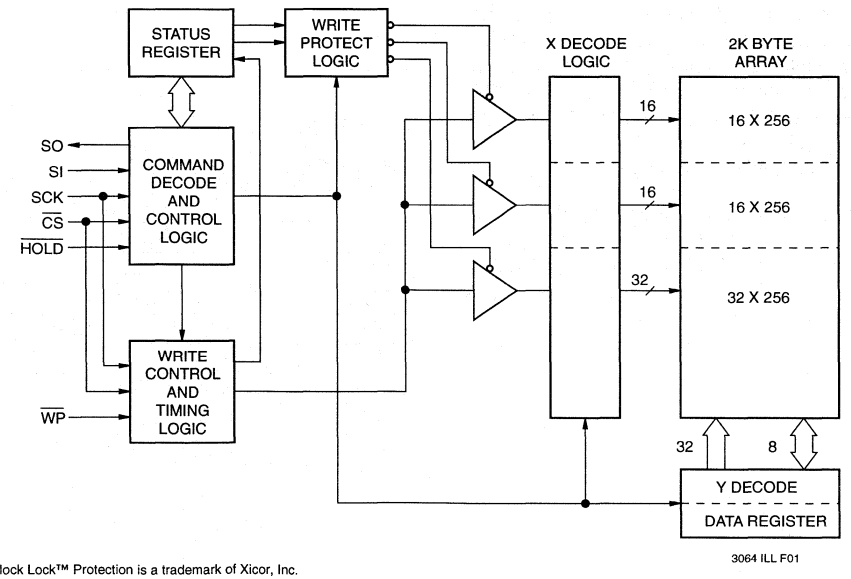
DESCRIPTION

The X25160 is a CMOS 16384-bit serial E²PROM, internally organized as 2K x 8. The X25160 features a Serial Peripheral Interface (SPI) and software protocol allowing operation on a simple three-wire bus. The bus signals are a clock input (SCK) plus separate data in (SI) and data out (SO) lines. Access to the device is controlled through a chip select ($\overline{CS}$) input, allowing any number of devices to share the same bus.

The X25160 also features two additional inputs that provide the end user with added flexibility. By asserting the $\overline{HOLD}$ input, the X25160 will ignore transitions on its inputs, thus allowing the host to service higher priority interrupts. The $\overline{WP}$ input can be used as a hardwire input to the X25160 disabling all write attempts to the status register, thus providing a mechanism for limiting end user capability of altering 0, 1/4, 1/2 or all of the memory.

The X25160 utilizes Xicor's proprietary Direct Write™ cell, providing a minimum endurance of 100,000 cycles and a minimum data retention of 100 years.

FUNCTIONAL DIAGRAM



3064 ILL F01

Direct Write™ and Block Lock™ Protection is a trademark of Xicor, Inc.

PIN DESCRIPTIONS

Serial Output (SO)

SO is a push/pull serial data output pin. During a read cycle, data is shifted out on this pin. Data is clocked out by the falling edge of the serial clock.

Serial Input (SI)

SI is the serial data input pin. All opcodes, byte addresses, and data to be written to the memory are input on this pin. Data is latched by the rising edge of the serial clock.

Serial Clock (SCK)

The Serial Clock controls the serial bus timing for data input and output. Opcodes, addresses, or data present on the SI pin are latched on the rising edge of the clock input, while data on the SO pin change after the falling edge of the clock input.

Chip Select ($\overline{CS}$)

When $\overline{CS}$ is HIGH, the X25160 is deselected and the SO output pin is at high impedance and unless an internal write operation is underway, the X25160 will be in the standby power mode. $\overline{CS}$ LOW enables the X25160, placing it in the active power mode. It should be noted that after power-up, a HIGH to LOW transition on $\overline{CS}$ is required prior to the start of any operation.

Write Protect ($\overline{WP}$)

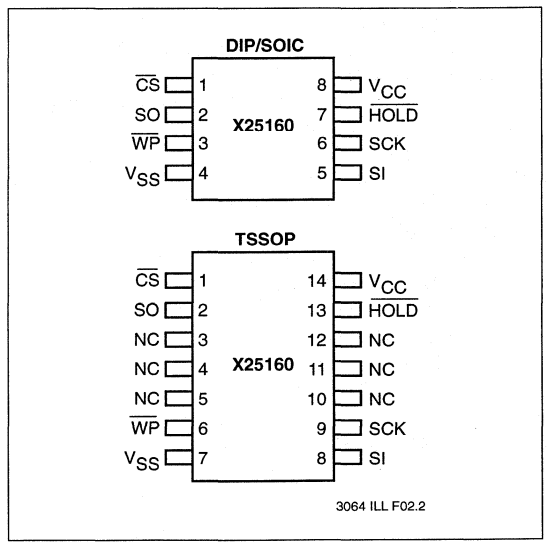
When $\overline{WP}$ is LOW and the nonvolatile bit WPEN is "1", nonvolatile writes to the X25160 status register are disabled, but the part otherwise functions normally. When $\overline{WP}$ is held HIGH, all functions, including nonvolatile writes operate normally. $\overline{WP}$ going LOW while $\overline{CS}$ is still LOW will interrupt a write to the X25160 status register. If the internal write cycle has already been initiated, $\overline{WP}$ going LOW will have no effect on a write.

The $\overline{WP}$ pin function is blocked when the WPEN bit in the status register is "0". This allows the user to install the X25160 in a system with $\overline{WP}$ pin grounded and still be able to write to the status register. The $\overline{WP}$ pin functions will be enabled when the WPEN bit is set "1".

Hold ($\overline{HOLD}$)

$\overline{HOLD}$ is used in conjunction with the $\overline{CS}$ pin to select the device. Once the part is selected and a serial sequence is underway, $\overline{HOLD}$ may be used to pause the serial communication with the controller without resetting the serial sequence. To pause, $\overline{HOLD}$ must be brought LOW while SCK is LOW. To resume communication, $\overline{HOLD}$ is brought HIGH, again while SCK is LOW. If the pause feature is not used, $\overline{HOLD}$ should be held HIGH at all times.

PIN CONFIGURATION



PIN NAMES

SYMBOL	DESCRIPTION
$\overline{CS}$	Chip Select Input
SO	Serial Output
SI	Serial Input
SCK	Serial Clock Input
$\overline{WP}$	Write Protect Input
V_{SS}	Ground
V_{CC}	Supply Voltage
$\overline{HOLD}$	Hold Input
NC	No Connect

3064 PGM T01

PRINCIPLES OF OPERATION

The X25160 is a 2K x 8 E^2PROM designed to interface directly with the synchronous serial peripheral interface (SPI) of many popular microcontroller families.

The X25160 contains an 8-bit instruction register. It is accessed via the SI input, with data being clocked in on the rising SCK. $\overline{CS}$ must be LOW and the $\overline{HOLD}$ and $\overline{WP}$ inputs must be HIGH during the entire operation. The $\overline{WP}$ input is "Don't Care" if WPEN is set "0".

Table 1 contains a list of the instructions and their opcodes. All instructions, addresses and data are transferred MSB first.

Data input is sampled on the first rising edge of SCK after $\overline{CS}$ goes LOW. SCK is static, allowing the user to stop the clock and then resume operations. If the clock line is shared with other peripheral devices on the SPI bus, the user can assert the $\overline{HOLD}$ input to place the X25160 into a "PAUSE" condition. After releasing $\overline{HOLD}$, the X25160 will resume operation from the point when $\overline{HOLD}$ was first asserted.

Write Enable Latch

The X25160 contains a "write enable" latch. This latch must be SET before a write operation will be completed internally. The WREN instruction will set the latch and the WRDI instruction will reset the latch. This latch is automatically reset upon a power-up condition and after the completion of a byte, page, or status register write cycle.

Status Register

The RDSR instruction provides access to the status register. The status register may be read at any time, even during a write cycle. The status register is formatted as follows:

7	6	5	4	3	2	1	0
WPEN	X	X	X	BP1	BP0	WEL	WIP

3064 PGM T02

WPEN, BP0 and BP1 are set by the WRSR instruction. WEL and WIP are read-only and automatically set by other operations.

The Write-In-Process (WIP) bit indicates whether the X25160 is busy with a write operation. When set to a "1", a write is in progress, when set to a "0", no write is in progress. During a write, all other bits are set to "1".

The Write Enable Latch (WEL) bit indicates the status of the "write enable" latch. When set to a "1", the latch is set, when set to a "0", the latch is reset.

The Block Protect (BP0 and BP1) bits are nonvolatile and allow the user to select one of four levels of protection. The X25160 is divided into four 4096-bit segments. One, two, or all four of the segments may be protected. That is, the user may read the segments but will be unable to alter (write) data within the selected segments. The partitioning is controlled as illustrated below.

Status Register Bits		Array Addresses Protected
BP1	BP0	
0	0	None
0	1	$0600–$07FF
1	0	$0400–$07FF
1	1	$0000–$07FF

3064 PGM T03

Table 1. Instruction Set

Instruction Name	Instruction Format*	Operation
WREN	0000 0110	Set the Write Enable Latch (Enable Write Operations)
WRDI	0000 0100	Reset the Write Enable Latch (Disable Write Operations)
RDSR	0000 0101	Read Status Register
WRSR	0000 0001	Write Status Register
READ	0000 0011	Read Data from Memory Array beginning at selected address
WRITE	0000 0010	Write Data to Memory Array beginning at Selected Address (1 to 32 Bytes)

3064 PGM T04

*Instructions are shown MSB in leftmost position. Instructions are transferred MSB first.

Write-Protect Enable

The Write-Protect-Enable (WPEN) is available for the X25160 as a nonvolatile enable bit for the $\overline{WP}$ pin.

WPEN	$\overline{WP}$	WEL	Protected Blocks	Unprotected Blocks	Status Register
0	X	0	Protected	Protected	Protected
0	X	1	Protected	Writable	Writable
1	LOW	0	Protected	Protected	Protected
1	LOW	1	Protected	Writable	Protected
X	HIGH	0	Protected	Protected	Protected
X	HIGH	1	Protected	Writable	Writable

3064 PGM T05.1

The Write Protect ($\overline{WP}$) pin and the nonvolatile Write Protect Enable (WPEN) bit in the Status Register control the programmable hardware write protect feature. Hardware write protection is enabled when $\overline{WP}$ pin is LOW, and the WPEN bit is "1". Hardware write protection is disabled when either the $\overline{WP}$ pin is HIGH or the WPEN bit is "0". When the chip is hardware write protected, nonvolatile writes are disabled to the Status Register, including the Block Protect bits and the WPEN bit itself, as well as the block-protected sections in the memory array. Only the sections of the memory array that are not block-protected can be written.

Note: Since the WPEN bit is write protected, it cannot be changed back to a "0", as long as the $\overline{WP}$ pin is held LOW.

Clock and Data Timing

Data input on the SI line is latched on the rising edge of SCK. Data is output on the SO line by the falling edge of SCK.

Read Sequence

When reading from the E²PROM memory array, $\overline{CS}$ is first pulled LOW to select the device. The 8-bit READ instruction is transmitted to the X25160, followed by the 16-bit address of which the last 11 are used. After the READ opcode and address are sent, the data stored in the memory at the selected address is shifted out on the SO line. The data stored in memory at the next address can be read sequentially by continuing to provide clock pulses. The address is automatically incremented to the next higher address after each byte of data is shifted out. When the highest address is reached ($07FF) the address counter rolls over to address $0000 allowing the read cycle to be continued indefinitely. The read operation is terminated by taking $\overline{CS}$ HIGH. Refer to the read E²PROM array operation sequence illustrated in Figure 1.

To read the status register the $\overline{CS}$ line is first pulled LOW to select the device followed by the 8-bit RDSR instruction. After the RDSR opcode is sent, the contents of the status register are shifted out on the SO line. The read status register sequence is illustrated in Figure 2.

Write Sequence

Prior to any attempt to write data into the X25160, the "write enable" latch must first be set by issuing the WREN instruction (See Figure 3). $\overline{CS}$ is first taken LOW, then the WREN instruction is clocked into the X25160. After all eight bits of the instruction are transmitted, $\overline{CS}$ must then be taken HIGH. If the user continues the write operation without taking $\overline{CS}$ HIGH after issuing the WREN instruction, the write operation will be ignored.

To write data to the E²PROM memory array, the user issues the WRITE instruction, followed by the address and then the data to be written. This is minimally a thirty-two clock operation. $\overline{CS}$ must go LOW and remain LOW for the duration of the operation. The host may continue to write up to 32 bytes of data to the X25160. The only restriction is the 32 bytes must reside on the same page. If the address counter reaches the end of the page and the clock continues, the counter will "roll over" to the first address of the page and overwrite any data that may have been written.

For the write operation (byte or page write) to be completed, $\overline{CS}$ can only be brought HIGH after bit 0 of data byte N is clocked in. If it is brought HIGH at any other time the write operation will not be completed. Refer to Figures 4 and 5 below for a detailed illustration of the write sequences and time frames in which $\overline{CS}$ going HIGH are valid.

To write to the status register, the WRSR instruction is followed by the data to be written. Data bits 0, 1, 4, 5 and 6 must be "0". This sequence is shown in Figure 6.

While the write is in progress following a status register or E²PROM write sequence, the status register may be read to check the WIP bit. During this time the WIP bit will be HIGH.

Hold Operation

The $\overline{HOLD}$ input should be HIGH (at V_{IH}) under normal operation. If a data transfer is to be interrupted $\overline{HOLD}$ can be pulled LOW to suspend the transfer until it can be resumed. The only restriction is the SCK input must be LOW when $\overline{HOLD}$ is first pulled LOW and SCK must also be LOW when $\overline{HOLD}$ is released.

The $\overline{HOLD}$ input may be tied HIGH either directly to V_{CC} or tied to V_{CC} through a resistor.

Operational Notes

The X25160 powers-up in the following state:

- The device is in the low power standby state.
- A HIGH to LOW transition on $\overline{CS}$ is required to enter an active state and receive an instruction.
- SO pin is high impedance.
- The "write enable" latch is reset.

Data Protection

The following circuitry has been included to prevent inadvertent writes:

- The "write enable" latch is reset upon power-up.
- A WREN instruction must be issued to set the "write enable" latch.
- $\overline{CS}$ must come HIGH at the proper clock count in order to start a write cycle.

Figure 1. Read E²PROM Array Operation Sequence

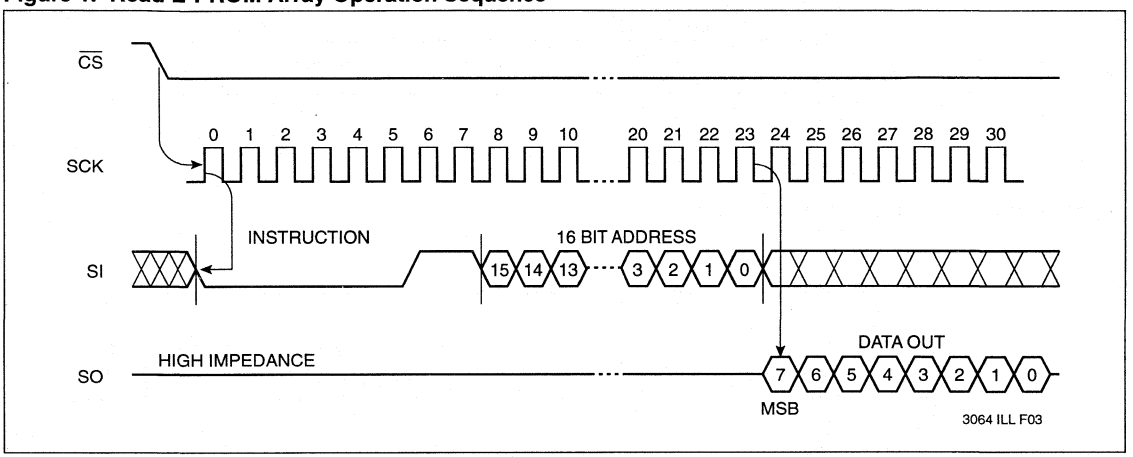


Figure 2. Read Status Register Operation Sequence

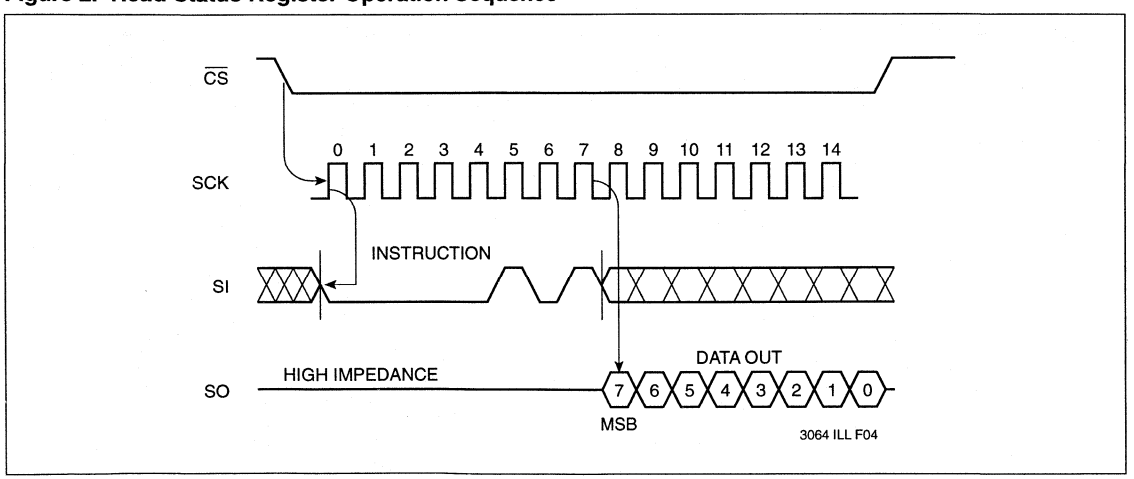


Figure 3. Write Enable Latch Sequence

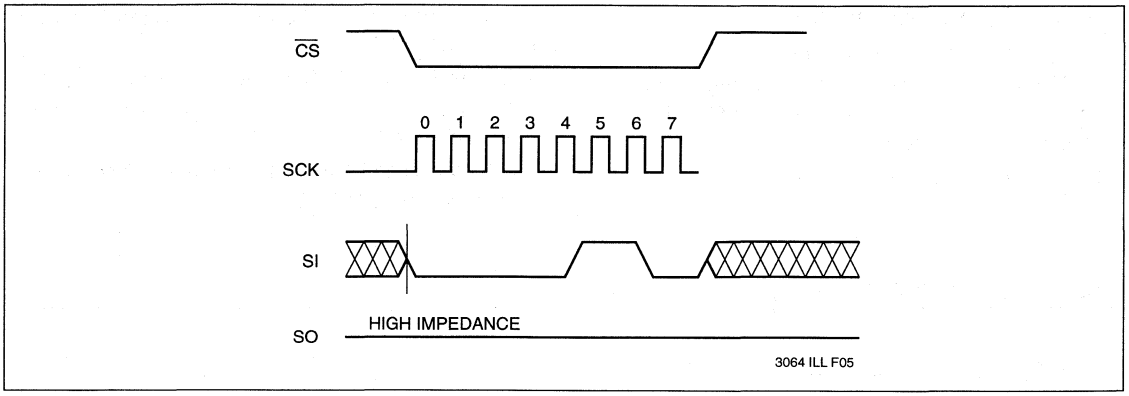


Figure 4. Byte Write Operation Sequence

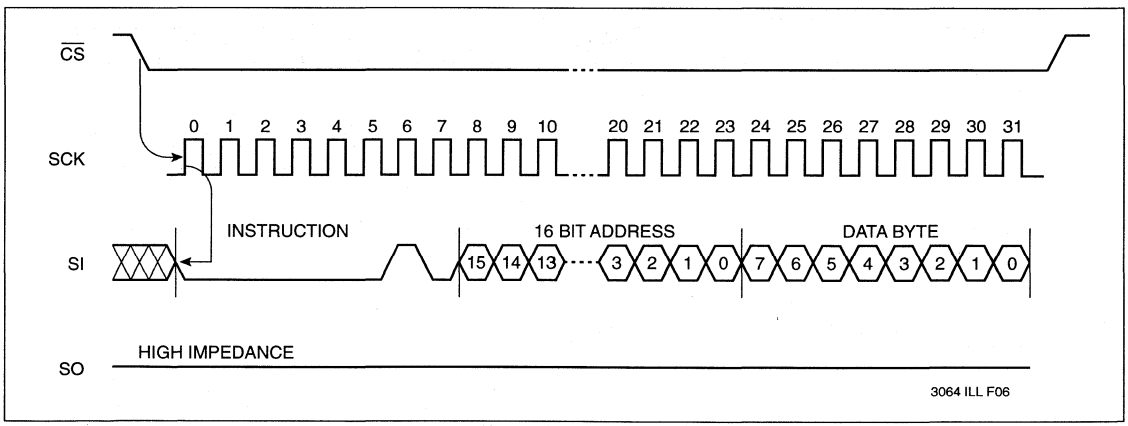


Figure 5. Page Write Operation Sequence

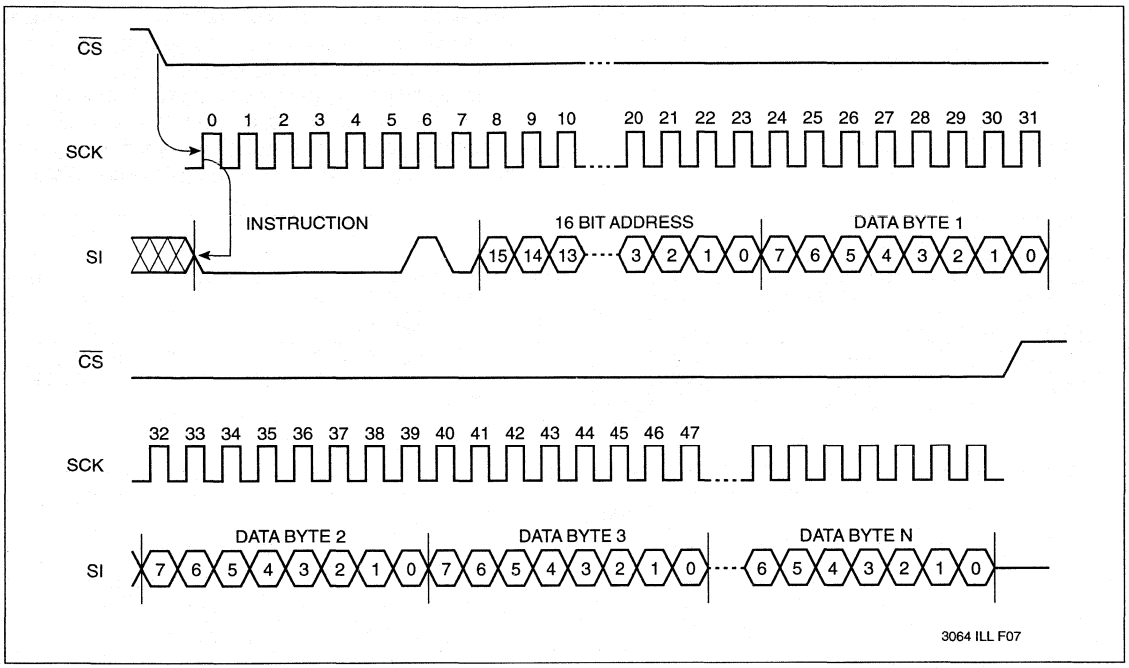
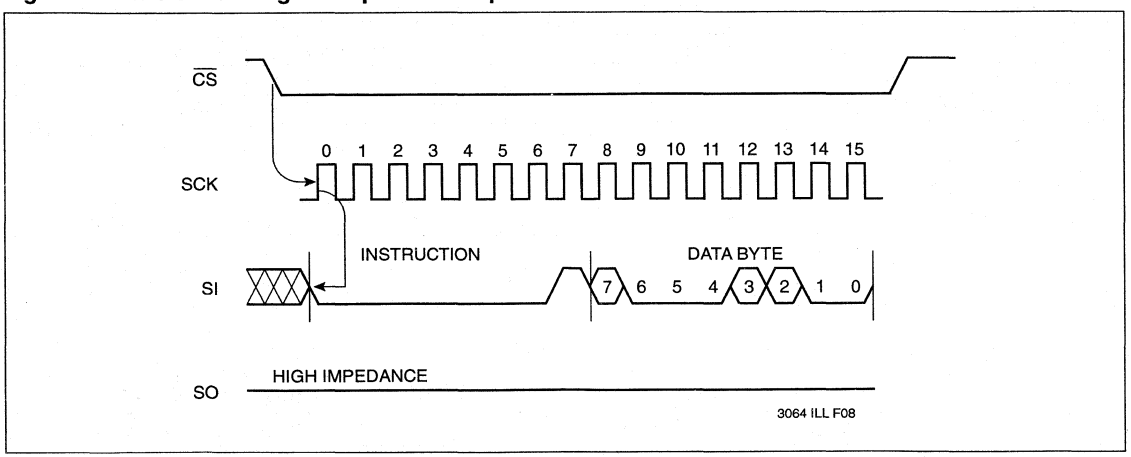


Figure 6. Write Status Register Operation Sequence



ABSOLUTE MAXIMUM RATINGS*

Temperature under Bias ..... –65°C to +135°C
Storage Temperature ..... –65°C to +150°C
Voltage on any Pin with Respect to V_{SS} ..... –1V to +7V
D.C. Output Current 5mA
Lead Temperature
(Soldering, 10 seconds) ..... 300°C

***COMMENT**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temp	Min.	Max.
Commercial	0°C	+70°C
Industrial	–40°C	+85°C
Military	–55°C	+125°C

3064 PGM T06.1

Supply Voltage	Limits
X25160	5V ±10%
X25160-2.7	2.7V to 5.5V

3064 PGM T07.1

D.C. OPERATING CHARACTERISTICS (Over the recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
I_{CC}	V_{CC} Supply Current (Active)		5	mA	SCK = V_{CC} x 0.1/V_{CC} x 0.9 @ 2MHz, SO = Open, $\overline{CS}$ = V_{SS}
I_{SB}	V_{CC} Supply Current (Standby)		1	µA	$\overline{CS}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}
I_{LI}	Input Leakage Current		10	µA	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output Leakage Current		10	µA	V_{OUT} = V_{SS} to V_{CC}
V_{IL}(1)	Input LOW Voltage	–1	V_{CC} x 0.3	V	
V_{IH}(1)	Input HIGH Voltage	V_{CC} x 0.7	V_{CC} + 0.5	V	
V_{OL1}	Output LOW Voltage		0.4	V	V_{CC} = 5V, I_{OL} = 3mA
V_{OH1}	Output HIGH Voltage	V_{CC} – 0.8		V	V_{CC} = 5V, I_{OH} = -1.6mA
V_{OL2}	Output LOW Voltage		0.4	V	V_{CC} = 3V, I_{OL} = 1.5mA
V_{OH2}	Output HIGH Voltage	V_{CC} – 0.3		V	V_{CC} = 3V, I_{OH} = -0.4mA

3064 PGM T08.3

POWER-UP TIMING

Symbol	Parameter	Min.	Max.	Units
t_{PUR}(3)	Power-up to Read Operation		1	ms
t_{PUW}(3)	Power-up to Write Operation		5	ms

3064 PGM T09

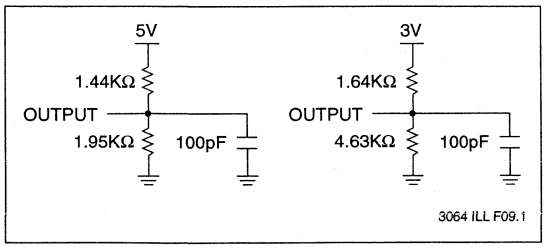
CAPACITANCE T_A = +25°C, f = 1MHz, V_{CC} = 5V.

Symbol	Test	Max.	Units	Conditions
C_{OUT}(2)	Output Capacitance (SO)	8	pF	V_{OUT} = 0V
C_{IN}(2)	Input Capacitance (SCK, SI, $\overline{CS}$, $\overline{WP}$, $\overline{HOLD}$)	6	pF	V_{IN} = 0V

3064 PGM T10.1

Notes: (1) V_{IL} min. and V_{IH} max. are for reference only and are not tested.
(2) This parameter is periodically sampled and not 100% tested.
(3) t_{PUR} and t_{PUW} are the delays required from the time V_{CC} is stable until the specified operation can be initiated. These parameters are periodically sampled and not 100% tested.

EQUIVALENT A.C. LOAD CIRCUIT



A.C. TEST CONDITIONS

Input Pulse Levels	V_{CC} x 0.1 to V_{CC} x 0.9
Input Rise and Fall Times	10ns
Input and Output Timing Level	V_{CC} x 0.5

3064 PGM T11

2

A.C. CHARACTERISTICS (Over recommended operating conditions, unless otherwise specified)

Data Input Timing

Symbol	Parameter	Min.	Max.	Units
f_{SCK}	Clock Frequency	0	2	MHz
t_{CYC}	Cycle Time	500		ns
t_{LEAD}	$\overline{CS}$ Lead Time	250		ns
t_{LAG}	$\overline{CS}$ Lag Time	250		ns
t_{WH}	Clock HIGH Time	200		ns
t_{WL}	Clock LOW Time	200		ns
t_{SU}	Data Setup Time	50		ns
t_H	Data Hold Time	50		ns
t_{RI}(4)	Data In Rise Time		2	µs
t_{FI}(4)	Data In Fall Time		2	µs
t_{HD}	$\overline{HOLD}$ Setup Time	100		ns
t_{CD}	$\overline{HOLD}$ Hold Time	100		ns
t_{CS}	$\overline{CS}$ Deselect Time	2.0		µs
t_{WC}(5)	Write Cycle Time		10	ms

3064 PGM T12.2

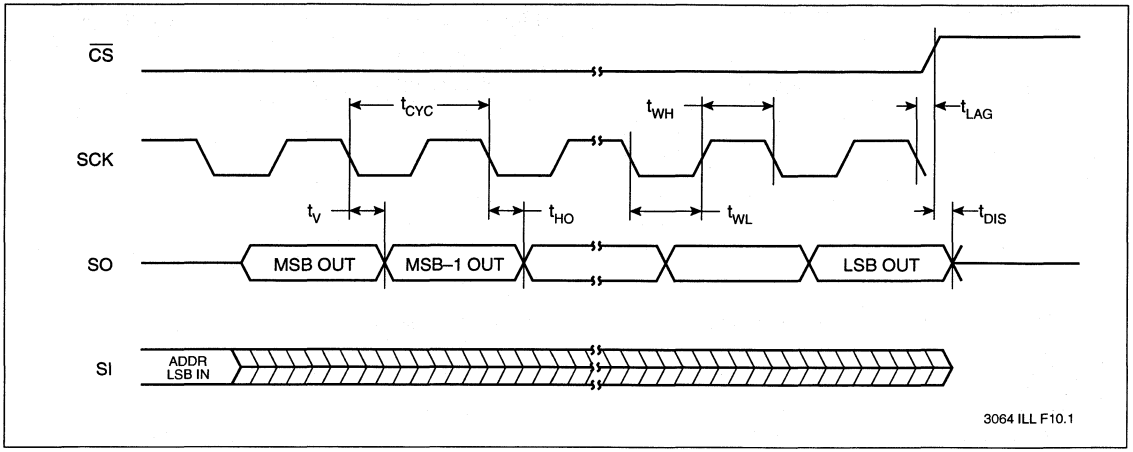
Data Output Timing

Symbol	Parameter	Min.	Max.	Units
f_{SCK}	Clock Frequency	0	2	MHz
t_{DIS}	Output Disable Time		250	ns
t_V	Output Valid from Clock LOW		200	ns
t_{HO}	Output Hold Time	0		ns
t_{RO}(4)	Output Rise Time		100	ns
t_{FO}(4)	Output Fall Time		100	ns
t_{LZ}(4)	$\overline{HOLD}$ HIGH to Output in Low Z	100		ns
t_{HZ}(4)	$\overline{HOLD}$ LOW to Output in High Z	100		ns

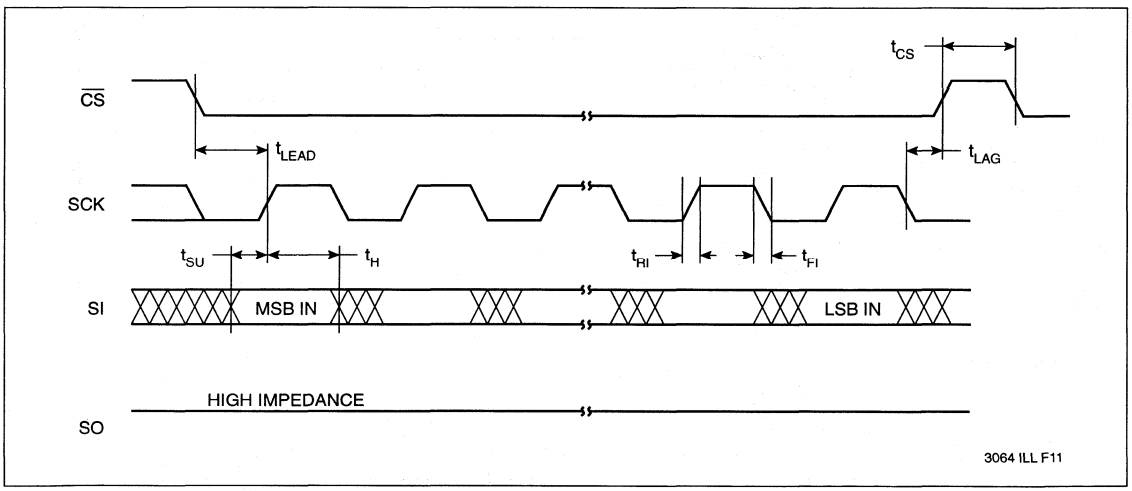
3064 PGM T13.2

2Notes: (4) This parameter is periodically sampled and not 100% tested.
(5) t_{WC} is the time from the rising edge of $\overline{CS}$ after a valid write sequence has been sent to the end of the self-timed internal nonvolatile write cycle.

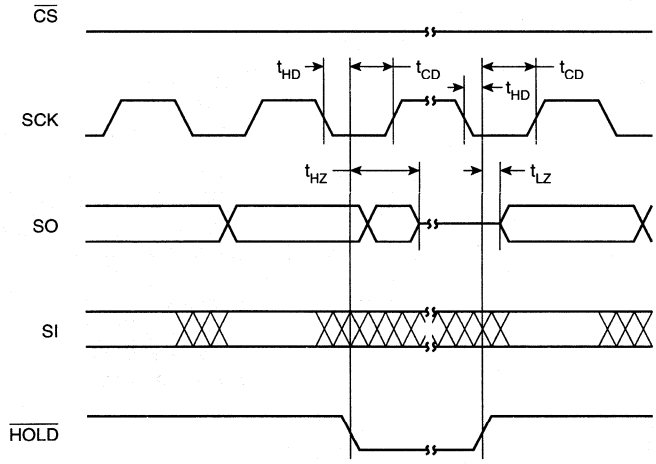
Serial Output Timing



Serial Input Timing



Hold Timing

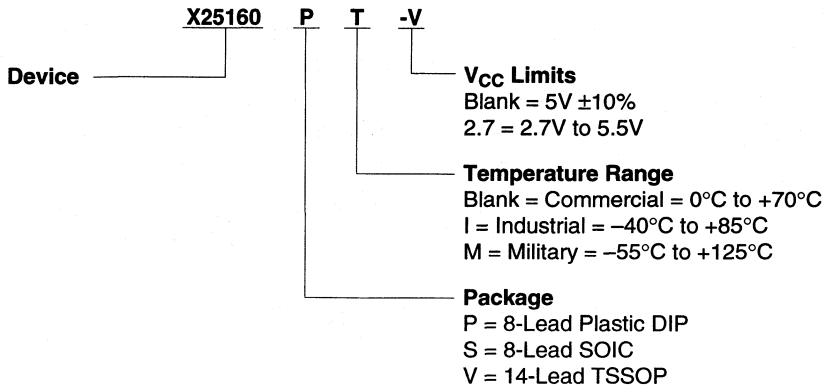


3064 ILL F12.1

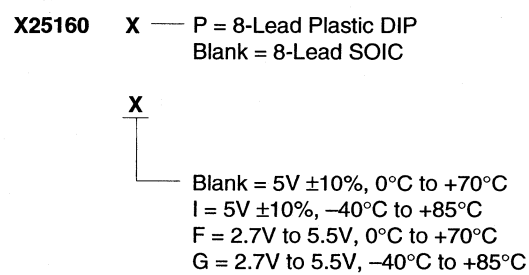
SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

ORDERING INFORMATION



Part Mark Convention



32K X25320 4K x 8 Bit

SPI Serial E²PROM With Block Lock™ Protection

FEATURES

- 2MHz Clock Rate
- SPI Modes (0,0 & 1,1)
- 4K X 8 Bits
  - —32 Byte Page Mode
- Low Power CMOS
  - —<1μA Standby Current
  - —<5mA Active Current During Write
- 2.7V To 5.5V Power Supply
- Block Lock Protection
  - —Protect 1/4, 1/2 or all of E²PROM Array
- Built-in Inadvertent Write Protection
  - —Power-Up/Power-Down protection circuitry
  - —Write Enable Latch
  - —Write Protect Pin
- Self-Timed Write Cycle
  - —5ms Write Cycle Time (Typical)
- High Reliability
  - —Endurance: 100,000 cycles
  - —Data Retention: 100 Years
  - —ESD protection: 2000V on all pins
- 8-Pin Mini-DIP Package
- 8-Lead SOIC Package
- 14-Lead TSSOP Package

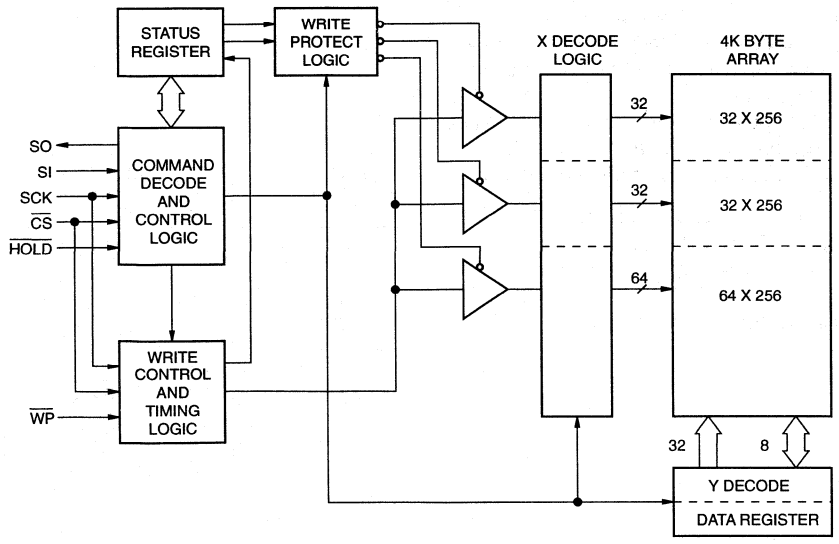
DESCRIPTION

The X25320 is a CMOS 32768-bit serial E²PROM, internally organized as 4K x 8. The X25320 features a Serial Peripheral Interface (SPI) and software protocol allowing operation on a simple three-wire bus. The bus signals are a clock input (SCK) plus separate data in (SI) and data out (SO) lines. Access to the device is controlled through a chip select ($\overline{CS}$) input, allowing any number of devices to share the same bus.

The X25320 also features two additional inputs that provide the end user with added flexibility. By asserting the $\overline{HOLD}$ input, the X25320 will ignore transitions on its inputs, thus allowing the host to service higher priority interrupts. The $\overline{WP}$ input can be used as a hardwire input to the X25320 disabling all write attempts to the status register, thus providing a mechanism for limiting end user capability of altering 0, 1/4, 1/2 or all of the memory.

The X25320 utilizes Xicor's proprietary Direct Write™ cell, providing a minimum endurance of 100,000 cycles and a minimum data retention of 100 years.

FUNCTIONAL DIAGRAM



Direct Write™ and Block Lock™ Protection is a trademark of Xicor, Inc.

PIN DESCRIPTIONS

Serial Output (SO)

SO is a push/pull serial data output pin. During a read cycle, data is shifted out on this pin. Data is clocked out by the falling edge of the serial clock.

Serial Input (SI)

SI is the serial data input pin. All opcodes, byte addresses, and data to be written to the memory are input on this pin. Data is latched by the rising edge of the serial clock.

Serial Clock (SCK)

The Serial Clock controls the serial bus timing for data input and output. Opcodes, addresses, or data present on the SI pin are latched on the rising edge of the clock input, while data on the SO pin change after the falling edge of the clock input.

Chip Select ($\overline{CS}$)

When $\overline{CS}$ is HIGH, the X25320 is deselected and the SO output pin is at high impedance and unless an internal write operation is underway, the X25320 will be in the standby power mode. $\overline{CS}$ LOW enables the X25320, placing it in the active power mode. It should be noted that after power-on, a HIGH to LOW transition on $\overline{CS}$ is required prior to the start of any operation.

Write Protect ($\overline{WP}$)

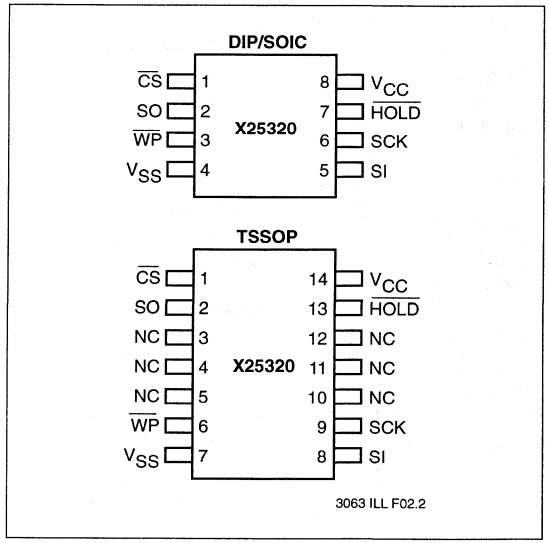
When $\overline{WP}$ is LOW and the nonvolatile bit WPEN is "1", nonvolatile writes to the X25320 status register are disabled, but the part otherwise functions normally. When $\overline{WP}$ is held HIGH, all functions, including nonvolatile writes operate normally. $\overline{WP}$ going LOW while $\overline{CS}$ is still LOW will interrupt a write to the X25320 status register. If the internal write cycle has already been initiated, $\overline{WP}$ going LOW will have no effect on a write.

The $\overline{WP}$ pin function is blocked when the WPEN bit in the status register is "0". This allows the user to install the X25320 in a system with $\overline{WP}$ pin grounded and still be able to write to the status register. The $\overline{WP}$ pin functions will be enabled when the WPEN bit is set "1".

Hold ($\overline{HOLD}$)

$\overline{HOLD}$ is used in conjunction with the $\overline{CS}$ pin to select the device. Once the part is selected and a serial sequence is underway, $\overline{HOLD}$ may be used to pause the serial communication with the controller without resetting the serial sequence. To pause, $\overline{HOLD}$ must be brought LOW while SCK is LOW. To resume communication, $\overline{HOLD}$ is brought HIGH, again while SCK is LOW. If the pause feature is not used, $\overline{HOLD}$ should be held HIGH at all times.

PIN CONFIGURATION



PIN NAMES

SYMBOL	DESCRIPTION
$\overline{CS}$	Chip Select Input
SO	Serial Output
SI	Serial Input
SCK	Serial Clock Input
$\overline{WP}$	Write Protect Input
V_{SS}	Ground
V_{CC}	Supply Voltage
$\overline{HOLD}$	Hold Input
NC	No Connect

3063 PGM T01

PRINCIPLES OF OPERATION

The X25320 is a 4K x 8 E^2PROM designed to interface directly with the synchronous serial peripheral interface (SPI) of many popular microcontroller families.

The X25320 contains an 8-bit instruction register. It is accessed via the SI input, with data being clocked in on the rising SCK. $\overline{CS}$ must be LOW and the $\overline{HOLD}$ and $\overline{WP}$ inputs must be HIGH during the entire operation. The $\overline{WP}$ input is "Don't Care" if WPEN is set "0".

Table 1 contains a list of the instructions and their opcodes. All instructions, addresses and data are transferred MSB first.

Data input is sampled on the first rising edge of SCK after $\overline{CS}$ goes LOW. SCK is static, allowing the user to stop the clock and then resume operations. If the clock line is shared with other peripheral devices on the SPI bus, the user can assert the $\overline{HOLD}$ input to place the X25320 into a "PAUSE" condition. After releasing $\overline{HOLD}$, the X25320 will resume operation from the point when $\overline{HOLD}$ was first asserted.

Write Enable Latch

The X25320 contains a "write enable" latch. This latch must be SET before a write operation will be completed internally. The WREN instruction will set the latch and the WRDI instruction will reset the latch. This latch is automatically reset upon a power-up condition and after the completion of a byte, page, or status register write cycle.

Status Register

The RDSR instruction provides access to the status register. The status register may be read at any time, even during a write cycle. The status register is formatted as follows:

7	6	5	4	3	2	1	0
WPEN	X	X	X	BP1	BP0	WEL	WIP

3063 PGM T02

WPEN, BP0 and BP1 are set by the WRSR instruction. WEL and WIP are read-only and automatically set by other operations.

The Write-In-Process (WIP) bit indicates whether the X25320 is busy with a write operation. When set to a "1", a write is in progress, when set to a "0", no write is in progress. During a write, all other bits are set to "1".

The Write Enable Latch (WEL) bit indicates the status of the "write enable" latch. When set to a "1", the latch is set, when set to a "0", the latch is reset.

The Block Protect (BP0 and BP1) bits are nonvolatile and allow the user to select one of four levels of protection. The X25320 is divided into four 8192-bit segments. One, two, or all four of the segments may be protected. That is, the user may read the segments but will be unable to alter (write) data within the selected segments. The partitioning is controlled as illustrated below.

Status Register Bits		Array Addresses Protected
BP1	BP0	
0	0	None
0	1	$0C00–$0FFF
1	0	$0800–$0FFF
1	1	$0000–$0FFF

3063 PGM T03

Table 1. Instruction Set

Instruction Name	Instruction Format*	Operation
WREN	0000 0110	Set the Write Enable Latch (Enable Write Operations)
WRDI	0000 0100	Reset the Write Enable Latch (Disable Write Operations)
RDSR	0000 0101	Read Status Register
WRSR	0000 0001	Write Status Register
READ	0000 0011	Read Data from Memory Array beginning at selected address
WRITE	0000 0010	Write Data to Memory Array beginning at Selected Address (1 to 32 Bytes)

3063 PGM T04

*Instructions are shown MSB in leftmost position. Instructions are transferred MSB first.

Write-Protect Enable

The Write-Protect-Enable (WPEN) is available for the X25320 as a nonvolatile enable bit for the $\overline{WP}$ pin.

WPEN	$\overline{WP}$	WEL	Blocks	Blocks	Register
0	X	0	Protected	Protected	Protected
0	X	1	Protected	Writable	Writable
1	LOW	0	Protected	Protected	Protected
1	LOW	1	Protected	Writable	Protected
X	HIGH	0	Protected	Protected	Protected
X	HIGH	1	Protected	Writable	Writable

3063 PGM T05.1

The Write Protect ($\overline{WP}$) pin and the nonvolatile Write Protect Enable (WPEN) bit in the Status Register control the programmable hardware write protect feature. Hardware write protection is enabled when $\overline{WP}$ pin is LOW, and the WPEN bit is "1". Hardware write protection is disabled when either the $\overline{WP}$ pin is HIGH or the WPEN bit is "0". When the chip is hardware write protected, nonvolatile writes are disabled to the Status Register, including the Block Protect bits and the WPEN bit itself, as well as the block-protected sections in the memory array. Only the sections of the memory array that are not block-protected can be written.

Note: Since the WPEN bit is write protected, it cannot be changed back to a "0", as long as the $\overline{WP}$ pin is held LOW.

Clock and Data Timing

Data input on the SI line is latched on the rising edge of SCK. Data is output on the SO line by the falling edge of SCK.

Read Sequence

When reading from the E^{2}PROM memory array, $\overline{CS}$ is first pulled LOW to select the device. The 8-bit READ instruction is transmitted to the X25320, followed by the 16-bit address of which the last 12 are used. After the READ opcode and address are sent, the data stored in the memory at the selected address is shifted out on the SO line. The data stored in memory at the next address can be read sequentially by continuing to provide clock pulses. The address is automatically incremented to the next higher address after each byte of data is shifted out. When the highest address is reached ($0FFF) the address counter rolls over to address $0000 allowing the read cycle to be continued indefinitely. The read operation is terminated by taking $\overline{CS}$ HIGH. Refer to the read E^{2}PROM array operation sequence illustrated in Figure 1.

To read the status register the $\overline{CS}$ line is first pulled LOW to select the device followed by the 8-bit RDSR instruction. After the RDSR opcode is sent, the contents of the status register are shifted out on the SO line. The read status register sequence is illustrated in Figure 2.

Write Sequence

Prior to any attempt to write data into the X25320, the "write enable" latch must first be set by issuing the WREN instruction (See Figure 3). $\overline{CS}$ is first taken LOW, then the WREN instruction is clocked into the X25320. After all eight bits of the instruction are transmitted, $\overline{CS}$ must then be taken HIGH. If the user continues the write operation without taking $\overline{CS}$ HIGH after issuing the WREN instruction, the write operation will be ignored.

To write data to the E^{2}PROM memory array, the user issues the WRITE instruction, followed by the address and then the data to be written. This is minimally a thirty-two clock operation. $\overline{CS}$ must go LOW and remain LOW for the duration of the operation. The host may continue to write up to 32 bytes of data to the X25320. The only restriction is the 32 bytes must reside on the same page. If the address counter reaches the end of the page and the clock continues, the counter will "roll over" to the first address of the page and overwrite any data that may have been written.

For the write operation (byte or page write) to be completed, $\overline{CS}$ can only be brought HIGH after bit 0 of data byte N is clocked in. If it is brought HIGH at any other time the write operation will not be completed. Refer to Figures 4 and 5 below for a detailed illustration of the write sequences and time frames in which $\overline{CS}$ going HIGH are valid.

To write to the status register, the WRSR instruction is followed by the data to be written. Data bits 0, 1, 4, 5 and 6 must be "0". This sequence is shown in Figure 6.

While the write is in progress following a status register or E^{2}PROM write sequence, the status register may be read to check the WIP bit. During this time the WIP bit will be HIGH.

Hold Operation

The $\overline{HOLD}$ input should be HIGH (at V_{IH}) under normal operation. If a data transfer is to be interrupted $\overline{HOLD}$ can be pulled LOW to suspend the transfer until it can be resumed. The only restriction is the SCK input must be LOW when $\overline{HOLD}$ is first pulled LOW and SCK must also be LOW when $\overline{HOLD}$ is released.

The $\overline{HOLD}$ input may be tied HIGH either directly to V_{CC} or tied to V_{CC} through a resistor.

Operational Notes

The X25320 powers-up in the following state:

- The device is in the low power standby state.
- A HIGH to LOW transition on $\overline{CS}$ is required to enter an active state and receive an instruction.
- SO pin is high impedance.
- The "write enable" latch is reset.

Data Protection

The following circuitry has been included to prevent inadvertent writes:

- The "write enable" latch is reset upon power-up.
- A WREN instruction must be issued to set the "write enable" latch.
- $\overline{CS}$ must come HIGH at the proper clock count in order to start a write cycle.

Figure 1. Read E²PROM Array Operation Sequence

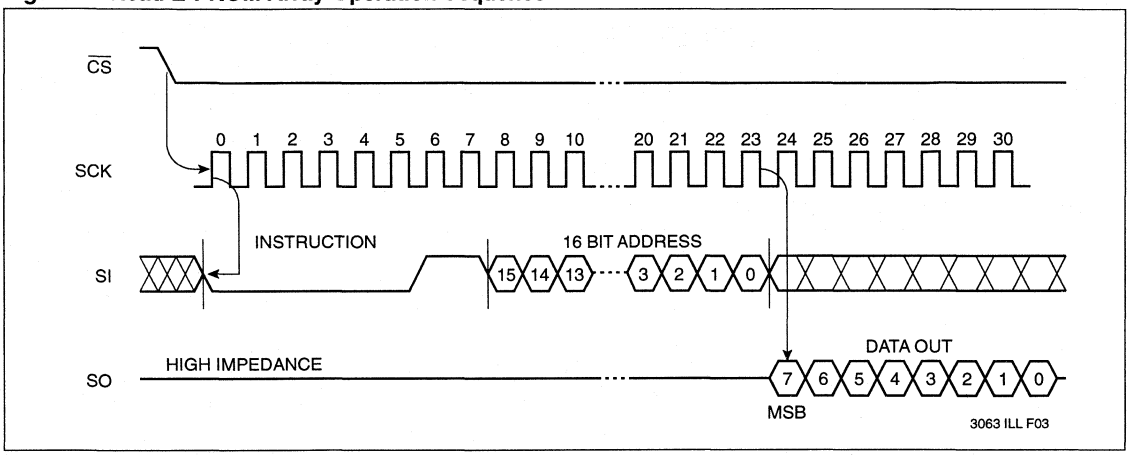


Figure 2. Read Status Register Operation Sequence

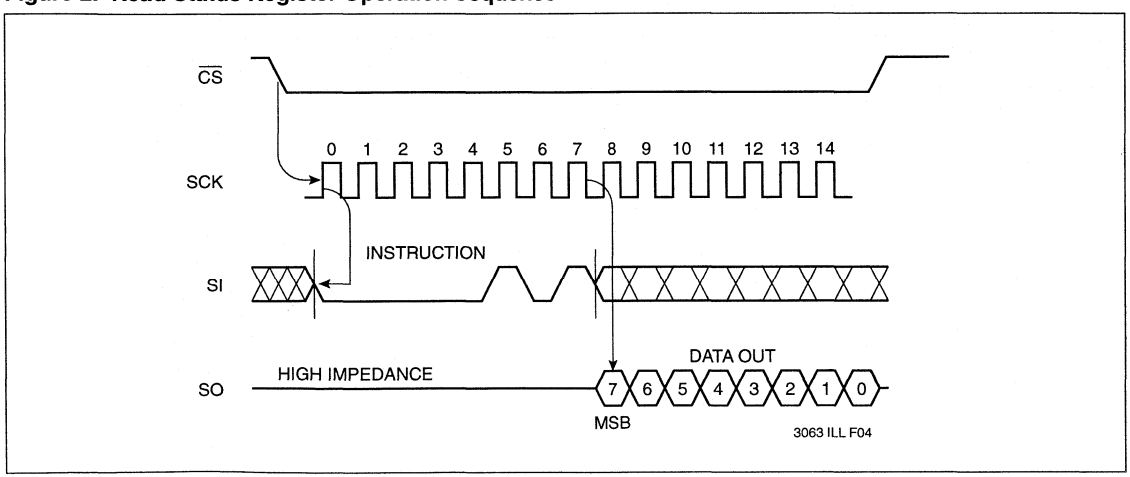


Figure 3. Write Enable Latch Sequence

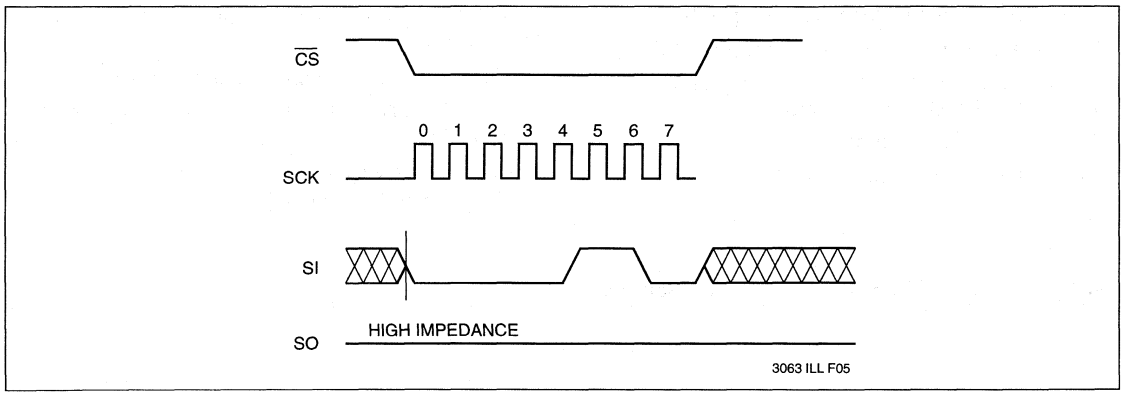


Figure 4. Byte Write Operation Sequence

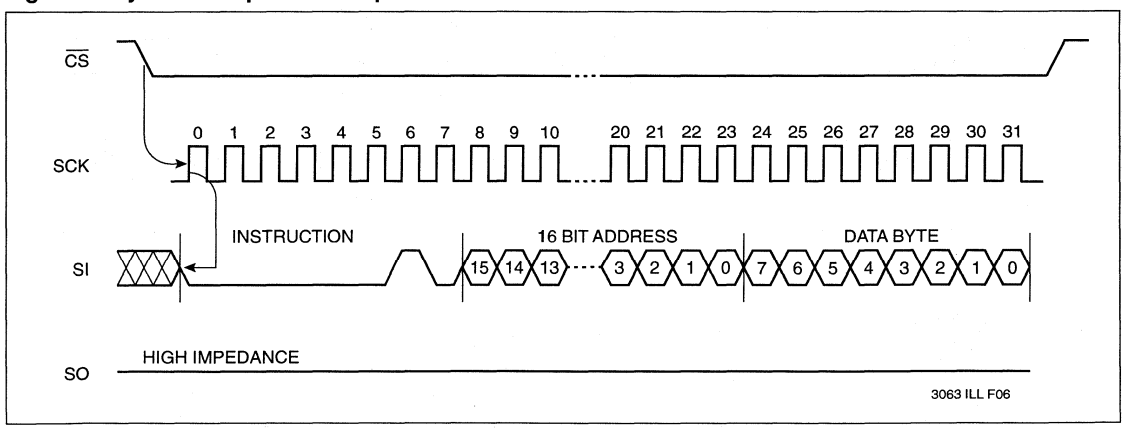


Figure 5. Page Write Operation Sequence

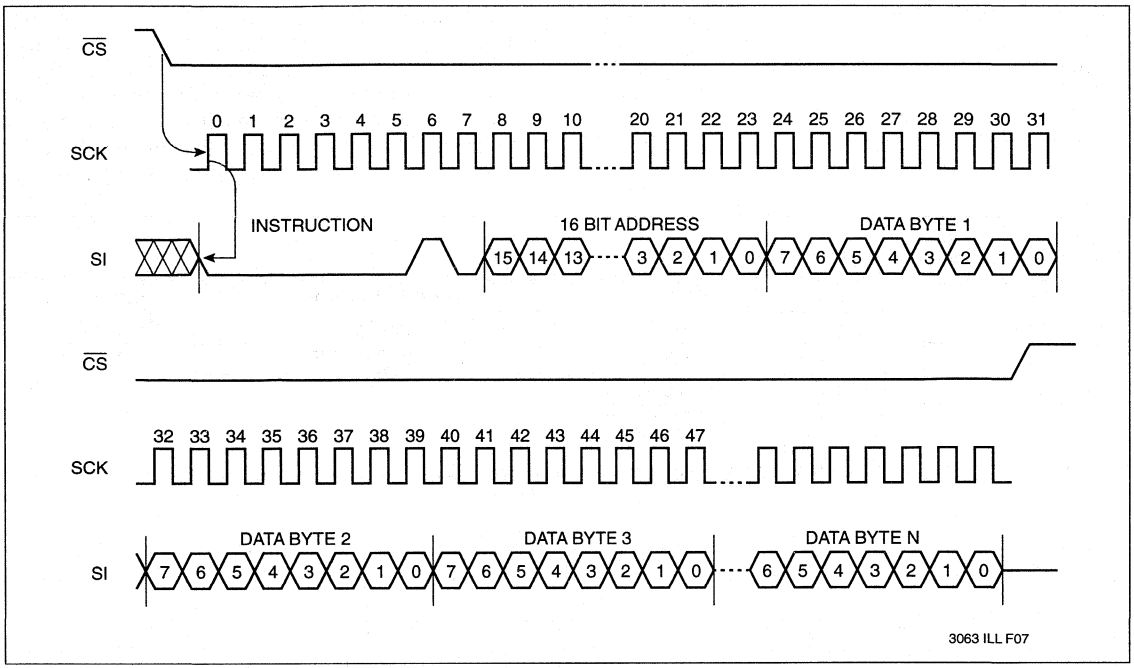
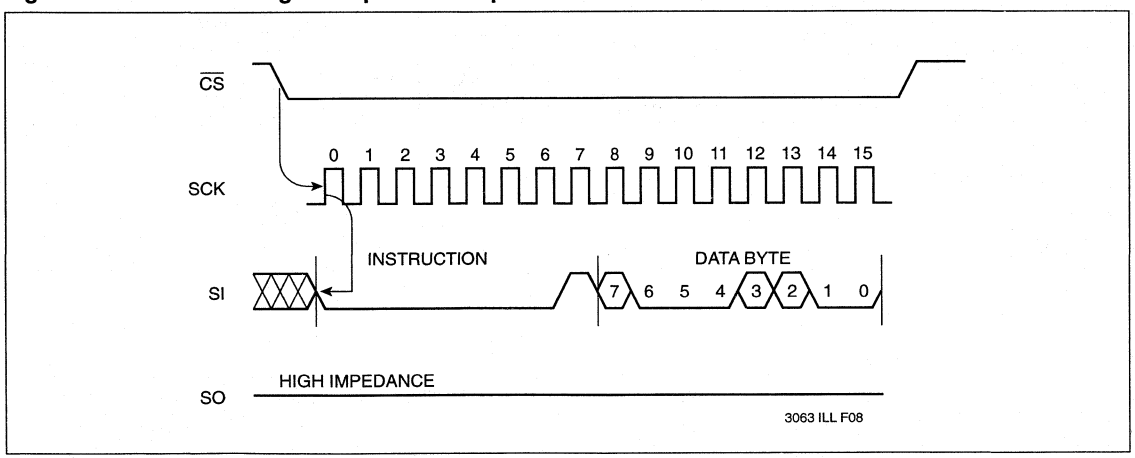


Figure 6. Write Status Register Operation Sequence



ABSOLUTE MAXIMUM RATINGS*

Temperature under Bias ..... –65°C to +135°C
Storage Temperature ..... –65°C to +150°C
Voltage on any Pin with Respect to V_{SS} ..... –1V to +7V
D.C. Output Current 5mA
Lead Temperature
(Soldering, 10 seconds) ..... 300°C

***COMMENT**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temp	Min.	Max.
Commercial	0°C	+70°C
Industrial	–40°C	+85°C
Military	–55°C	+125°C

3063 PGM T06.1

Supply Voltage	Limits
X25320	5V ±10%
X25320-2.7	2.7V to 5.5V

3063 PGM T07.1

D.C. OPERATING CHARACTERISTICS (Over the recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
I_{CC}	V_{CC} Supply Current (Active)		5	mA	SCK = V_{CC} x 0.1/V_{CC} x 0.9 @ 2MHz, SO = Open, $\overline{CS}$ = V_{SS}
I_{SB}	V_{CC} Supply Current (Standby)		1	µA	$\overline{CS}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}
I_{LI}	Input Leakage Current		10	µA	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output Leakage Current		10	µA	V_{OUT} = V_{SS} to V_{CC}
V_{IL}(1)	Input LOW Voltage	–1	V_{CC} x 0.3	V	
V_{IH}(1)	Input HIGH Voltage	V_{CC} x 0.7	V_{CC} + 0.5	V	
V_{OL1}	Output LOW Voltage		0.4	V	V_{CC} = 5V, I_{OL} = 3mA
V_{OH1}	Output HIGH Voltage	V_{CC} – 0.8		V	V_{CC} = 5V, I_{OH} = -1.6mA
V_{OL2}	Output LOW Voltage		0.4	V	V_{CC} = 3V, I_{OL} = 1.5mA
V_{OH2}	Output HIGH Voltage	V_{CC} – 0.3		V	V_{CC} = 3V, I_{OH} = -0.4mA

3063 PGM T08.3

POWER-UP TIMING

Symbol	Parameter	Min.	Max.	Units
t_{PUR}(3)	Power-up to Read Operation		1	ms
t_{PUW}(3)	Power-up to Write Operation		5	ms

3063 PGM T09

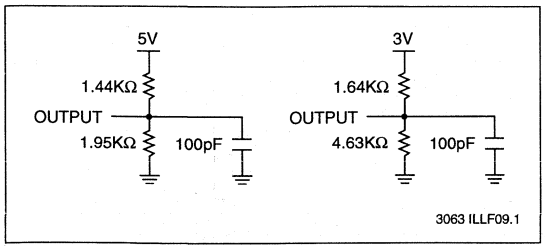
CAPACITANCE T_A = +25°C, f = 1MHz, V_{CC} = 5V.

Symbol	Test	Max.	Units	Conditions
C_{OUT}(2)	Output Capacitance (SO)	8	pF	V_{OUT} = 0V
C_{IN}(2)	Input Capacitance (SCK, SI, $\overline{CS}$, $\overline{WP}$, $\overline{HOLD}$)	6	pF	V_{IN} = 0V

3063 PGM T10.1

Notes: (1) V_{IL} min. and V_{IH} max. are for reference only and are not tested.
(2) This parameter is periodically sampled and not 100% tested.
(3) t_{PUR} and t_{PUW} are the delays required from the time V_{CC} is stable until the specified operation can be initiated. These parameters are periodically sampled and not 100% tested.

EQUIVALENT A.C. LOAD CIRCUIT



A.C. TEST CONDITIONS

Input Pulse Levels	V_{CC} x 0.1 to V_{CC} x 0.9
Input Rise and Fall Times	10ns
Input and Output Timing Level	V_{CC} x 0.5

3063 PGM T11

2

A.C. CHARACTERISTICS (Over recommended operating conditions, unless otherwise specified)

Data Input Timing

Symbol	Parameter	Min.	Max.	Units
f_{SCK}	Clock Frequency	0	2	MHz
t_{CYC}	Cycle Time	500		ns
t_{LEAD}	$\overline{CS}$ Lead Time	250		ns
t_{LAG}	$\overline{CS}$ Lag Time	250		ns
t_{WH}	Clock HIGH Time	200		ns
t_{WL}	Clock LOW Time	200		ns
t_{SU}	Data Setup Time	50		ns
t_H	Data Hold Time	50		ns
t_{RI}(4)	Data In Rise Time		2	µs
t_{FI}(4)	Data In Fall Time		2	µs
t_{HD}	$\overline{HOLD}$ Setup Time	100		ns
t_{CD}	$\overline{HOLD}$ Hold Time	100		ns
t_{CS}	$\overline{CS}$ Deselect Time	2.0		µs
t_{WC}(5)	Write Cycle Time		10	ms

3063 PGM T12.2

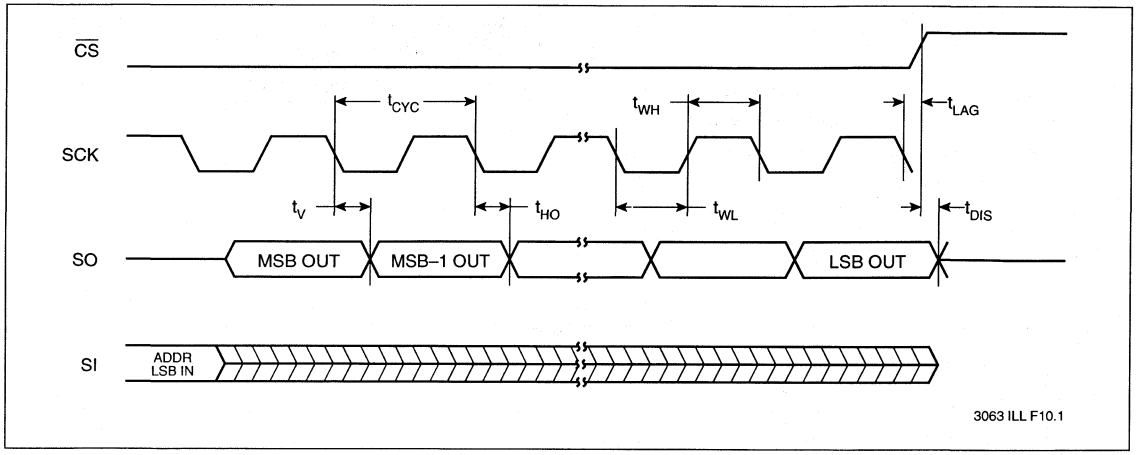
Data Output Timing

Symbol	Parameter	Min.	Max.	Units
f_{SCK}	Clock Frequency	0	2	MHz
t_{DIS}	Output Disable Time		250	ns
t_V	Output Valid from Clock LOW		200	ns
t_{HO}	Output Hold Time	0		ns
t_{RO}(4)	Output Rise Time		100	ns
t_{FO}(4)	Output Fall Time		100	ns
t_{LZ}(4)	$\overline{HOLD}$ HIGH to Output in Low Z	100		ns
t_{HZ}(4)	$\overline{HOLD}$ LOW to Output in High Z	100		ns

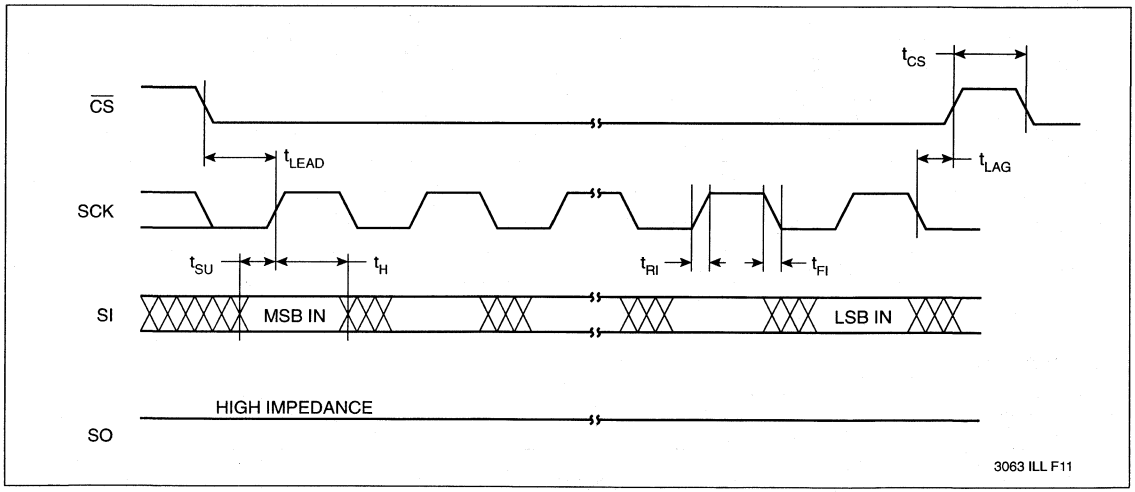
3063 PGM T13.2

Notes: (4) This parameter is periodically sampled and not 100% tested.
(5) t_{WC} is the time from the rising edge of $\overline{CS}$ after a valid write sequence has been sent to the end of the self-timed internal nonvolatile write cycle.

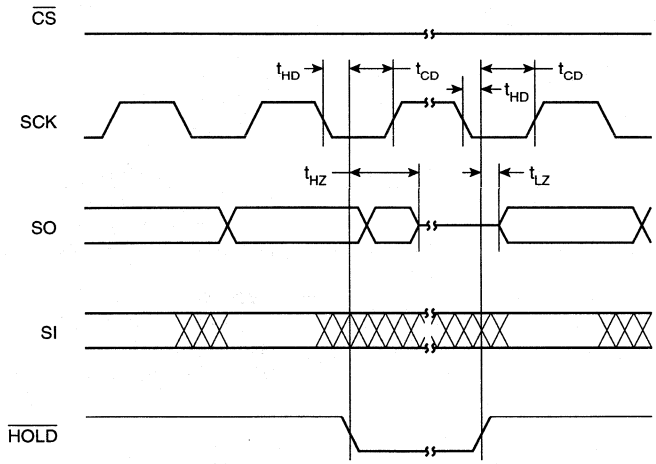
Serial Output Timing



Serial Input Timing



Hold Timing

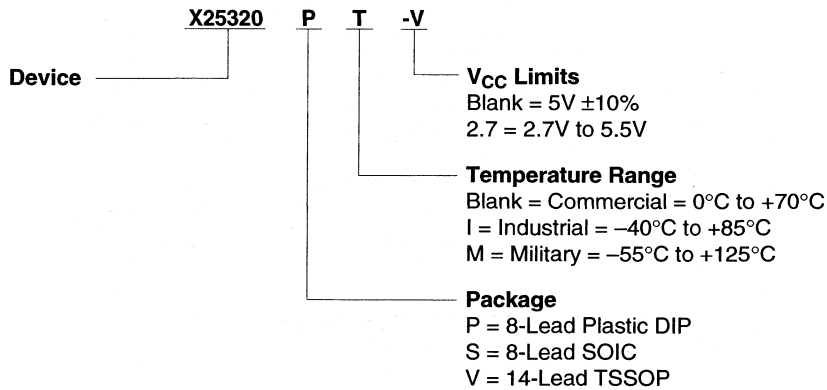


3063 ILL F12.1

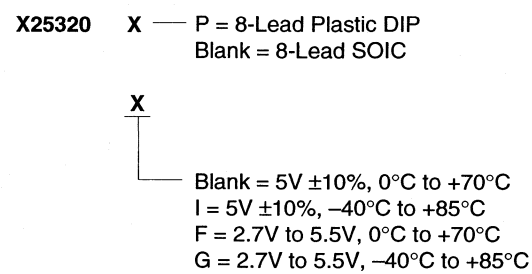
SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

ORDERING INFORMATION



Part Mark Convention



NOTES

Xicor®

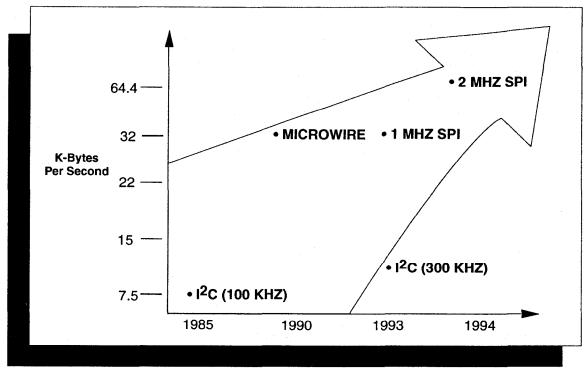
#7

Design Engineering Bulletin

New Product and Applications Information for Design Engineers

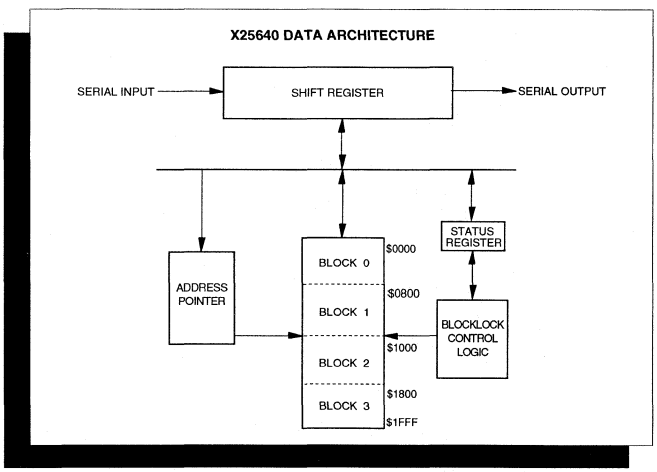
The X25640 Breaks The Speed Record For 64K Serial E²PROM Device Data Transfer

Until the introduction of the **X25640** 64K serial E²PROM from Xicor, microcontroller program execution had to be slowed down by inserting No Op instructions into the interface software to match the low speed of previously available serial interface E²PROMs. The X25640 alleviates this problem by providing a random byte read transfer rate of 64.4K Bytes/sec which represents an order of magnitude increase in performance over previously available serial devices. This new breed of serial E²PROM devices address the "need for speed" and at the same time offer higher density and superior non volatile data protection. The SPI (Serial Peripheral Interface) coupled with an advanced chip architecture makes this device stand out above the previous generation of serial E²PROM devices.



High density serial data transmission keeps pace with advanced µC speeds.

Superior Hardware and Software Data Protection Is Made Possible With the X25640 SPI E²PROM



"Lockdown" system configuration of manufacturing data to prevent accidental or intentional user alteration.

The **X25640** is the first of a new advanced family of serial E²PROMS which offer a Programmable hardware Write Protect pin combined with the software ability to "lock down" portions of the memory array. This feature provides the ability to combine user alterable data with manufacturer secured data. The system designer can define specific portions of the memory area for storing configuration or serialization data and protecting it from inadvertent or intrusive data changes once the system is in user control while allowing the user the ability to access other parts of the memory for normal data alteration. The configuration for memory array protection is defined by programming two nonvolatile bits in the device status register. With these two bits, one quarter, one half or all of the memory array maybe configured for write protection.

Xicor®

64K X25640 8K x 8 Bit

Advanced SPI Serial E²PROM With Block Lock™ Protection

FEATURES

- 1MHz Clock Rate
- Low Power CMOS
  - —200µA Standby Current
  - —5mA Active Current
- 5 Volt Power Supply
- 8-Pin Mini-DIP Package
- 150 Mil, Narrow SOIC Package
- SPI Modes (0,0 & 1,1)
- 8K X 8 Bits
  - —32 Byte Page Mode
- Block Lock Protection
  - —Protect 1/4, 1/2 or all of E²PROM Array
- Built-in Inadvertent Write Protection
  - —Power-Up/Power-Down protection circuitry
  - —Write Enable Latch
  - —Write Protect Pin
- Self-Timed Write Cycle
  - —5ms Write Cycle Time (Typical)
- High Reliability
  - —Endurance: 100,000 cycles
  - —Data Retention: 100 Years
  - —ESD protection: 2000V on all pins

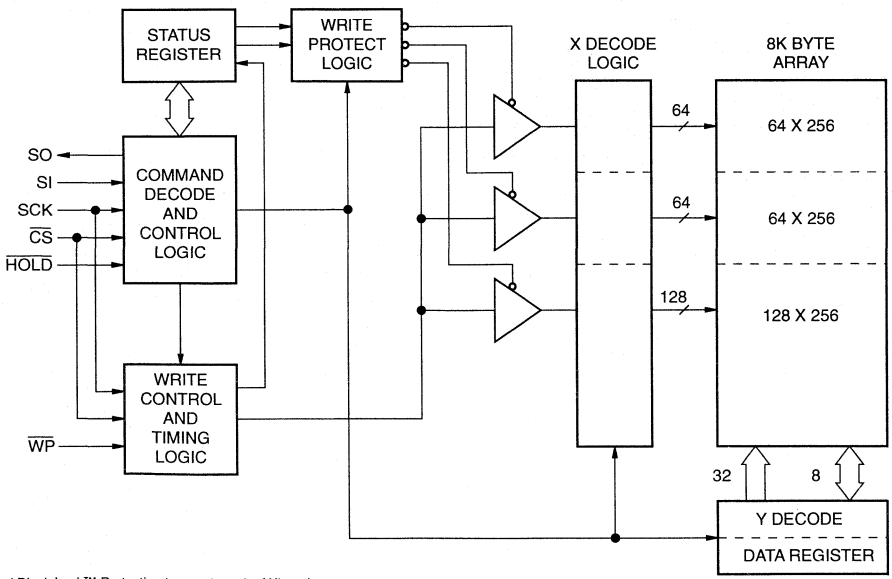
DESCRIPTION

The X25640 is a CMOS 65,536-bit serial E²PROM, internally organized as 8K x 8. The X25640 features a Serial Peripheral Interface (SPI) and software protocol allowing operation on a simple three-wire bus. The bus signals are a clock input (SCK) plus separate data in (SI) and data out (SO) lines. Access to the device is controlled through a chip select ($\overline{CS}$) input, allowing any number of devices to share the same bus.

The X25640 also features two additional inputs that provide the end user with added flexibility. By asserting the $\overline{HOLD}$ input, the X25640 will ignore transitions on its inputs, thus allowing the host to service higher priority interrupts. The $\overline{WP}$ input can be used as a hardwire input to the X25640 disabling all write attempts to the status register, thus providing a mechanism for limiting end user capability of altering 0, 1/4, 1/2 or all of the memory.

The X25640 utilizes Xicor's proprietary Direct Write™ cell, providing a minimum endurance of 100,000 cycles and a minimum data retention of 100 years.

FUNCTIONAL DIAGRAM



3089 ILL F01

Direct Write™ and Block Lock™ Protection is a trademark of Xicor, Inc.

PIN DESCRIPTIONS

Serial Output (SO)

SO is a push/pull serial data output pin. During a read cycle, data is shifted out on this pin. Data is clocked out by the falling edge of the serial clock.

Serial Input (SI)

SI is the serial data input pin. All opcodes, byte addresses, and data to be written to the memory are input on this pin. Data is latched by the rising edge of the serial clock.

Serial Clock (SCK)

The Serial Clock controls the serial bus timing for data input and output. Opcodes, addresses, or data present on the SI pin are latched on the rising edge of the clock input, while data on the SO pin change after the falling edge of the clock input.

Chip Select ($\overline{CS}$)

When $\overline{CS}$ is HIGH, the X25640 is deselected and the SO output pin is at high impedance and unless an internal write operation is underway, the X25640 will be in the standby power mode. $\overline{CS}$ LOW enables the X25640, placing it in the active power mode. It should be noted that after power-up, a HIGH to LOW transition on $\overline{CS}$ is required prior to the start of any operation.

Write Protect ($\overline{WP}$)

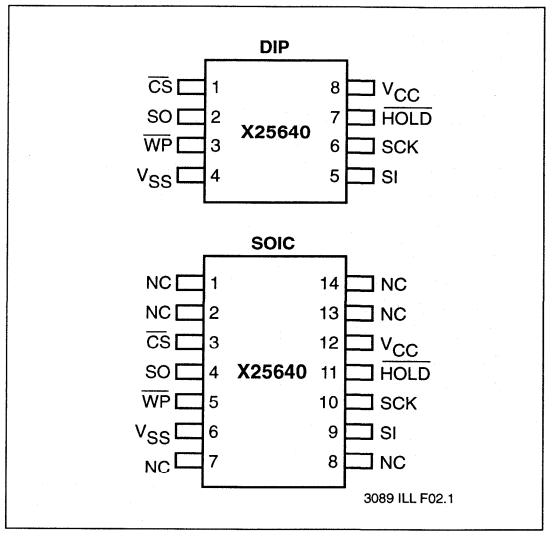
When $\overline{WP}$ is LOW and the nonvolatile bit WPEN is high, nonvolatile writes to the X25640 status register are disabled, but the part otherwise functions normally. When $\overline{WP}$ is held HIGH, all functions, including nonvolatile writes operate normally. $\overline{WP}$ going LOW while $\overline{CS}$ is still LOW will interrupt a write to the X25640 status register. If the internal write cycle has already been initiated, $\overline{WP}$ going LOW will have no affect on a write.

The $\overline{WP}$ pin function is blocked when the WPEN bit in the status register is LOW. This allows the user to install the X25640 in a system with $\overline{WP}$ pin grounded and still be able to write to the status register. The $\overline{WP}$ pin functions will be enabled when the WPEN bit is set "1".

Hold ($\overline{HOLD}$)

$\overline{HOLD}$ is used in conjunction with the $\overline{CS}$ pin to select the device. Once the part is selected and a serial sequence is underway, $\overline{HOLD}$ may be used to pause the serial communication with the controller without resetting the serial sequence. To pause, $\overline{HOLD}$ must be brought LOW while SCK is LOW. To resume communication, $\overline{HOLD}$ is brought HIGH, again while SCK is LOW. If the pause feature is not used, $\overline{HOLD}$ should be held HIGH at all times.

PIN CONFIGURATION



PIN NAMES

Symbol	Description
$\overline{CS}$	Chip Select Input
SO	Serial Output
SI	Serial Input
SCK	Serial Clock Input
$\overline{WP}$	Write Protect Input
V_{SS}	Ground
V_{CC}	Supply Voltage
$\overline{HOLD}$	Hold Input
NC	No Connect

3089 PGM T01

PRINCIPLES OF OPERATION

The X25640 is a 8K x 8 E^2PROM designed to interface directly with the synchronous serial peripheral interface (SPI) of many popular microcontroller families.

The X25640 contains an 8-bit instruction register. It is accessed via the SI input, with data being clocked in on the rising SCK. $\overline{CS}$ must be LOW and the $\overline{HOLD}$ and $\overline{WP}$ inputs must be HIGH during the entire operation.

Table 1 contains a list of the instructions and their opcodes. All instructions, addresses and data are transferred MSB first.

Data input is sampled on the first rising edge of SCK after $\overline{CS}$ goes LOW. SCK is static, allowing the user to stop the clock and then resume operations. If the clock line is shared with other peripheral devices on the SPI bus, the user can assert the $\overline{HOLD}$ input to place the X25640 into a "PAUSE" condition. After releasing $\overline{HOLD}$, the X25640 will resume operation from the point when $\overline{HOLD}$ was first asserted.

Write Enable Latch

The X25640 contains a "write enable" latch. This latch must be SET before a write operation will be completed internally. The WREN instruction will set the latch and the WRDI instruction will reset the latch. This latch is automatically reset upon a power-up condition and after the completion of a byte, page, or status register write cycle.

Status Register

The RDSR instruction provides access to the status register. The status register may be read at any time, even during a write cycle. The status register is formatted as follows:

7	6	5	4	3	2	1	0
WPEN	X	X	X	BP1	BP0	WEL	WIP

3089 PGM T02

WPEN, BP0 and BP1 are set by the WRSR instruction. WEL and WIP are read-only and automatically set by other operations.

The Write-In-Process (WIP) bit indicates whether the X25640 is busy with a write operation. When set to a "1", a write is in progress, when set to a "0", no write is in progress. During a write, all other bits are set to "1".

The Write Enable Latch (WEL) bit indicates the status of the "write enable" latch. When set to a "1", the latch is set, when set to a "0", the latch is reset.

The Block Protect (BP0 and BP1) bits are nonvolatile and allow the user to select one of four levels of protection. The X25640 is divided into four 16384-bit segments. One, two, or all four of the segments may be protected. That is, the user may read the segments but will be unable to alter (write) data within the selected segments. The partitioning is controlled as illustrated below.

Status Register Bits		Array Addresses Protected
BP1	BP0	
0	0	None
0	1	$1800–$1FFF
1	0	$1000–$1FFF
1	1	$0000–$1FFF

3834 PGM T03

Table 1. Instruction Set

Instruction Name	Instruction Format*	Operation
WREN	0000 0110	Set the Write Enable Latch (Enable Write Operations)
WRDI	0000 0100	Reset the Write Enable Latch (Disable Write Operations)
RDSR	0000 0101	Read Status Register
WRSR	0000 0001	Write Status Register
READ	0000 0011	Read Data from Memory Array beginning at selected address
WRITE	0000 0010	Write Data to Memory Array beginning at Selected Address (1 to 32 Bytes)

3089 PGM T04

*Instructions are shown MSB in leftmost position. Instructions are transferred MSB first.

Write-Protect Enable

The Write-Protect-Enable (WPEN) is available for the X25640 as a nonvolatile enable bit for the $\overline{WP}$ pin.

WPEN	$\overline{WP}$	WEL	Protected Blocks	Unprotected Blocks	Status Register
0	X	0	Protected	Protected	Protected
0	X	1	Protected	Writable	Writable
1	LOW	0	Protected	Protected	Protected
1	LOW	1	Protected	Writable	Protected
X	HIGH	0	Protected	Protected	Protected
X	HIGH	1	Protected	Writable	Writable

3089 PGM T03

The Write Protect ($\overline{WP}$) pin and the nonvolatile Write Protect Enable (WPEN) bit in the Status Register control the programmable hardware write protect feature. Hardware write protection is enabled when $\overline{WP}$ pin is LOW, and the WPEN bit is "1". Hardware write protection is disabled when either the $\overline{WP}$ pin is HIGH or the WPEN bit is "0". When the chip is hardware write protected, nonvolatile writes are disabled to the Status Register, including the Block Protect bits and the WPEN bit itself, as well as the block-protected sections in the memory array. Only the sections of the memory array that are not block-protected can be written.

Note: Since the WPEN bit is write protected, it cannot be changed back to a "0", as long as the $\overline{WP}$ pin is held LOW.

Clock and Data Timing

Data input on the SI line is latched on the rising edge of SCK. Data is output on the SO line by the falling edge of SCK.

Read Sequence

When reading from the E²PROM memory array, $\overline{CS}$ is first pulled LOW to select the device. The 8-bit READ instruction is transmitted to the X25640, followed by the 16-bit address of which the last 13 are used. After the READ opcode and address are sent, the data stored in the memory at the selected address is shifted out on the SO line. The data stored in memory at the next address can be read sequentially by continuing to provide clock pulses. The address is automatically incremented to the next higher address after each byte of data is shifted out. When the highest address is reached ($1FFF) the address counter rolls over to address $0000 allowing the read cycle to be continued indefinitely. The read operation is terminated by taking $\overline{CS}$ HIGH. Refer to the read E²PROM array operation sequence illustrated in Figure 1.

To read the status register the $\overline{CS}$ line is first pulled LOW to select the device followed by the 8-bit RDSR instruction. After the RDSR opcode is sent, the contents of the status register are shifted out on the SO line. Figure 2 illustrates the read status register sequence.

Write Sequence

Prior to any attempt to write data into the X25640, the "write enable" latch must first be set by issuing the WREN instruction (See Figure 3). $\overline{CS}$ is first taken LOW, then the WREN instruction is clocked into the X25640. After all eight bits of the instruction are transmitted, $\overline{CS}$ must then be taken HIGH. If the user continues the write operation without taking $\overline{CS}$ HIGH after issuing the WREN instruction, the write operation will be ignored.

To write data to the E²PROM memory array, the user issues the WRITE instruction, followed by the address and then the data to be written. This is minimally a thirty-two clock operation. $\overline{CS}$ must go LOW and remain LOW for the duration of the operation. The host may continue to write up to 32 bytes of data to the X25640. The only restriction is the 32 bytes must reside on the same page. If the address counter reaches the end of the page and the clock continues, the counter will "roll over" to the first address of the page and overwrite any data that may have been written.

For the write operation (byte or page write) to be completed, $\overline{CS}$ can only be brought HIGH after bit 0 of data byte N is clocked in. If it is brought HIGH at any other time the write operation will not be completed. Refer to Figures 4 and 5 below for a detailed illustration of the write sequences and time frames in which $\overline{CS}$ going HIGH are valid.

To write to the status register, the WRSR instruction is followed by the data to be written. Data bits 0, 1, 4, 5 and 6 must be "0". Figure 6 illustrates this sequence.

While the write is in progress following a status register or E²PROM write sequence, the status register may be read to check the WIP bit. During this time the WIP bit will be HIGH.

Hold Operation

The $\overline{HOLD}$ input should be HIGH (at V_{IH}) under normal operation. If a data transfer is to be interrupted $\overline{HOLD}$ can be pulled LOW to suspend the transfer until it can be resumed. The only restriction is the SCK input must be LOW when $\overline{HOLD}$ is first pulled LOW and SCK must also be LOW when $\overline{HOLD}$ is released.

The HOLD input may be tied HIGH either directly to V_{CC} or tied to V_{CC} through a resistor.

Operational Notes

The X25640 powers-up in the following state:

- The device is in the low power standby state.
- A HIGH to LOW transition on $\overline{CS}$ is required to enter an active state and receive an instruction.
- SO pin is high impedance.
- The "write enable" latch is reset.

Data Protection

The following circuitry has been included to prevent inadvertent writes:

- The "write enable" latch is reset upon power-up.
- A WREN instruction must be issued to set the "write enable" latch.
- $\overline{CS}$ must come HIGH at the proper clock count in order to start a write cycle.

Figure 1. Read E²PROM Array Operation Sequence

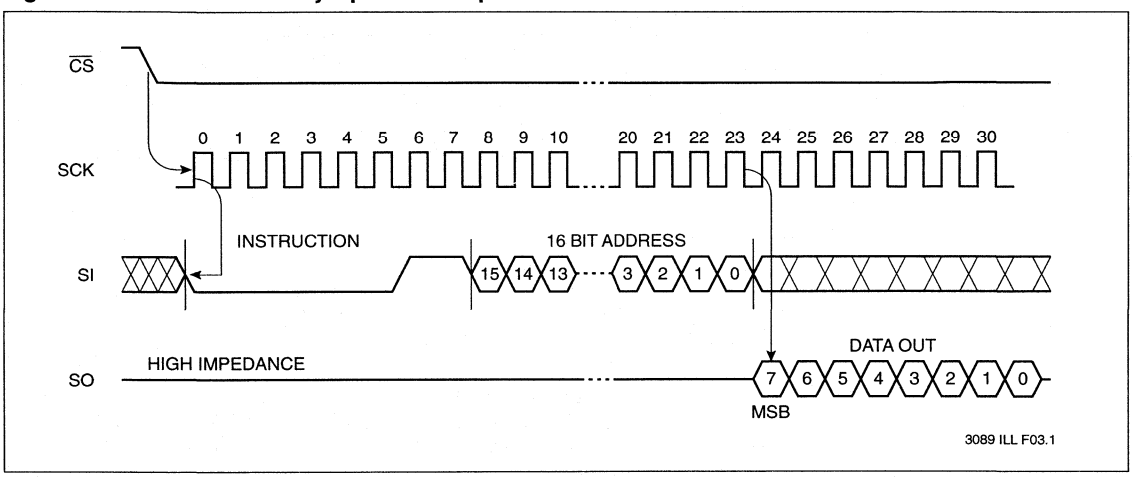


Figure 2. Read Status Register Operation Sequence

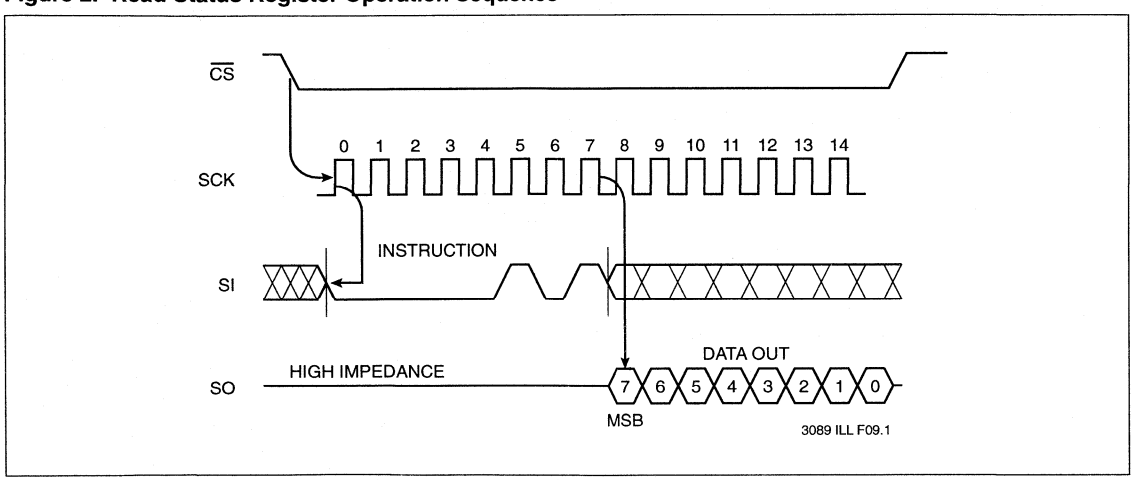


Figure 3. Write Enable Latch Sequence

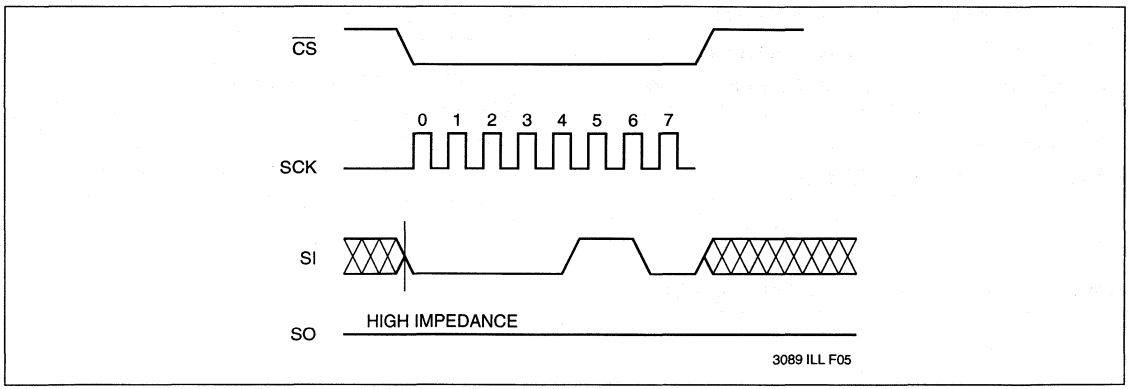


Figure 4. Byte Write Operation Sequence

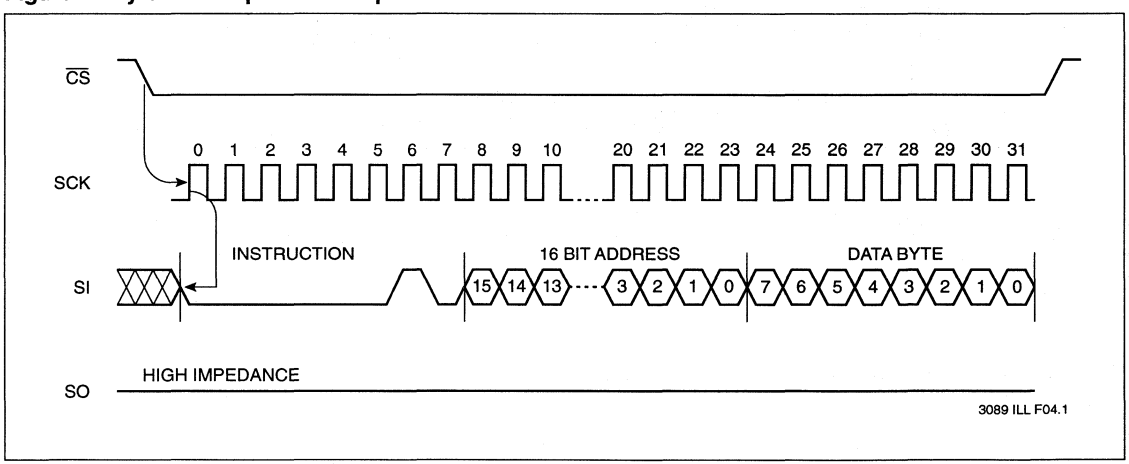


Figure 5. Page Write Operation Sequence

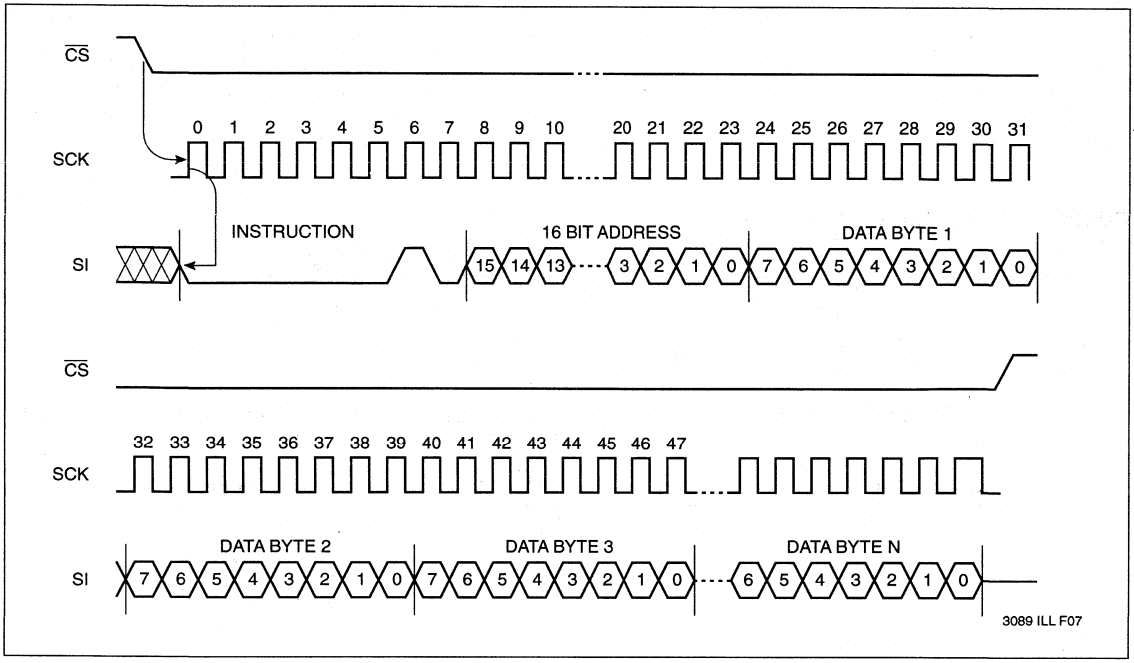
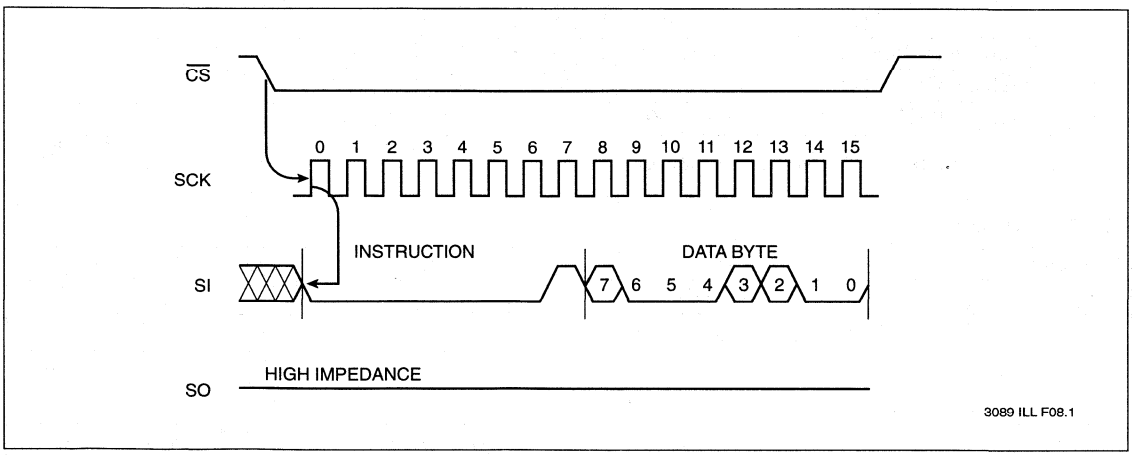


Figure 6. Write Status Register Operation Sequence



ABSOLUTE MAXIMUM RATINGS*

Temperature under Bias ..... –65°C to +135°C
Storage Temperature ..... –65°C to +150°C
Voltage on any Pin with Respect to V_{SS} ..... –1V to +7V
D.C. Output Current 5mA
Lead Temperature
(Soldering, 10 seconds) ..... 300°C

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temp	Min.	Max.
Commercial	0°C	+70°C
Industrial	–40°C	+85°C
Military	–55°C	+125°C

3089 PGM T06.1

Supply Voltage	Limits
X25640	5V ±10%

3089 PGM T07.1

D.C. OPERATING CHARACTERISTICS (Over the recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
I_{CC}	V_{CC} Supply Current (Active)		5	mA	SCK = V_{CC} x 0.1/V_{CC} x 0.9 @ 1MHz, SO = Open, $\overline{CS}$ = V_{SS}
I_{SB}*	V_{CC} Supply Current (Standby)		200	µA	$\overline{CS}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC} – 0.3V V_{CC} = 5.5V
V_{OH2}	Output High Voltage	V_{CC} – 0.4		V	I_{OH} = –0.4mA
I_{LI}	Input Leakage Current		10	µA	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output Leakage Current		10	µA	V_{OUT} = V_{SS} to V_{CC}
V_{IL}(1)	Input LOW Voltage	–1	V_{CC} x 0.3	V	
V_{IH}(1)	Input HIGH Voltage	V_{CC} x 0.7	V_{CC} + 0.5	V	
V_{OL}	Output LOW Voltage		0.4	V	I_{OL} = 2mA
V_{OH1}	Output HIGH Voltage	V_{CC}–0.8		V	I_{OH} = –1mA

3089 PGM T08.3

*I_{SB} is measured after a 2 second settling time upon initial power up.

POWER-UP TIMING

Symbol	Parameter	Min.	Max.	Units
t_{PUR}(3)	Power-up to Read Operation		1	ms
t_{PUW}(3)	Power-up to Write Operation		5	ms

3089 PGM T09

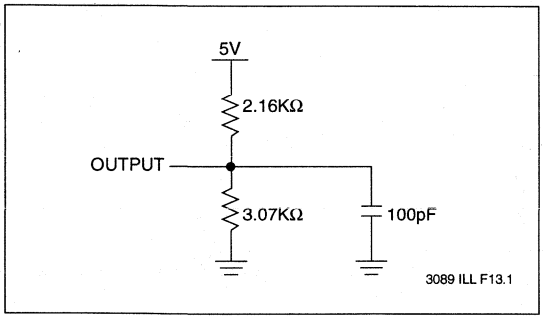
CAPACITANCE T_A = +25°C, f = 1MHz, V_{CC} = 5V.

Symbol	Test	Max.	Units	Conditions
C_{OUT}(2)	Output Capacitance (SO)	8	pF	V_{OUT} = 0V
C_{IN}(2)	Input Capacitance (SCK, SI, $\overline{CS}$, $\overline{WP}$, $\overline{HOLD}$)	6	pF	V_{IN} = 0V

3089 PGM T10.1

Notes: (1) V_{IL} min. and V_{IH} max. are for reference only and are not tested.
(2) This parameter is periodically sampled and not 100% tested.
(3) t_{PUR} and t_{PUW} are the delays required from the time V_{CC} is stable until the specified operation can be initiated. These parameters are periodically sampled and not 100% tested.

EQUIVALENT A.C. LOAD CIRCUIT, V_{CC} = 5V



A.C. TEST CONDITIONS

Input Pulse Levels	V_{CC} x 0.1 to V_{CC} x 0.9
Input Rise and Fall Times	10ns
Input and Output Timing Level	V_{CC} x 0.5

3089 PGM T11

2

A.C. CHARACTERISTICS (Over recommended operating conditions, unless otherwise specified)

Data Input Timing

Symbol	Parameter	Min.	Max.	Units
f_{SCK}	Clock Frequency	0	1	MHz
t_{CYC}	Cycle Time	1000		ns
t_{LEAD}	$\overline{CS}$ Lead Time	500		ns
t_{LAG}	$\overline{CS}$ Lag Time	500		ns
t_{WH}	Clock HIGH Time	400		ns
t_{WL}	Clock LOW Time	400		ns
t_{SU}	Data Setup Time	100		ns
t_H	Data Hold Time	100		ns
t_{RI}(3)	Data In Rise Time		2	µs
t_{FI}(3)	Data In Fall Time		2	µs
t_{HD}	$\overline{HOLD}$ Setup Time	200		ns
t_{CD}	$\overline{HOLD}$ Hold Time	200		ns
t_{CS}(5)	$\overline{CS}$ Deselect Time	500		ns
t_{WC}(4)	Write Cycle Time		10	ms

3089 PGM T12.2

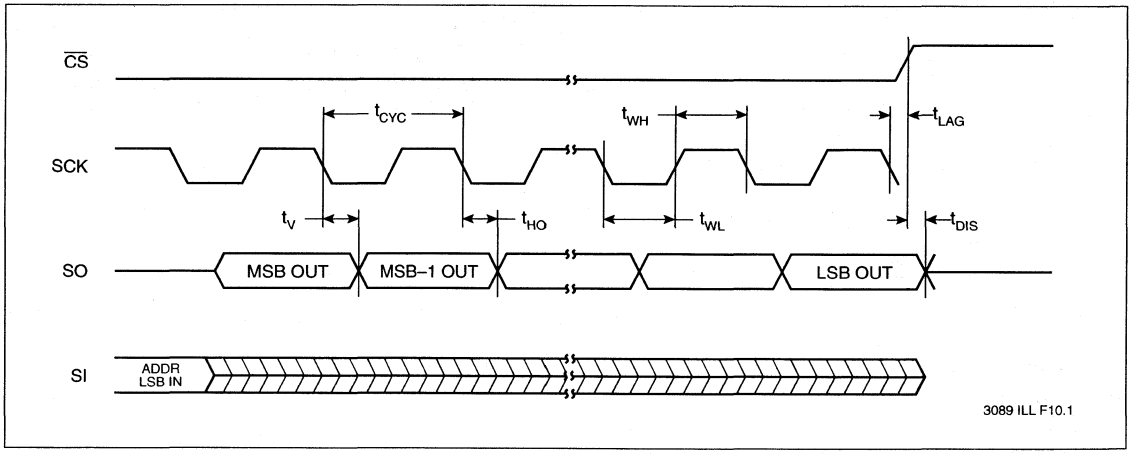
Data Output Timing

Symbol	Parameter	Min.	Max.	Units
f_{SCK}	Clock Frequency	0	1	MHz
t_{DIS}	Output Disable Time		500	ns
t_V	Output Valid from Clock LOW		400	ns
t_{HO}	Output Hold Time	0		ns
t_{RO}(3)	Output Rise Time		300	ns
t_{FO}(3)	Output Fall Time		300	ns
t_{LZ}(3)	$\overline{HOLD}$ HIGH to Output in Low Z	100		ns
t_{HZ}(3)	$\overline{HOLD}$ LOW to Output in High Z	100		ns

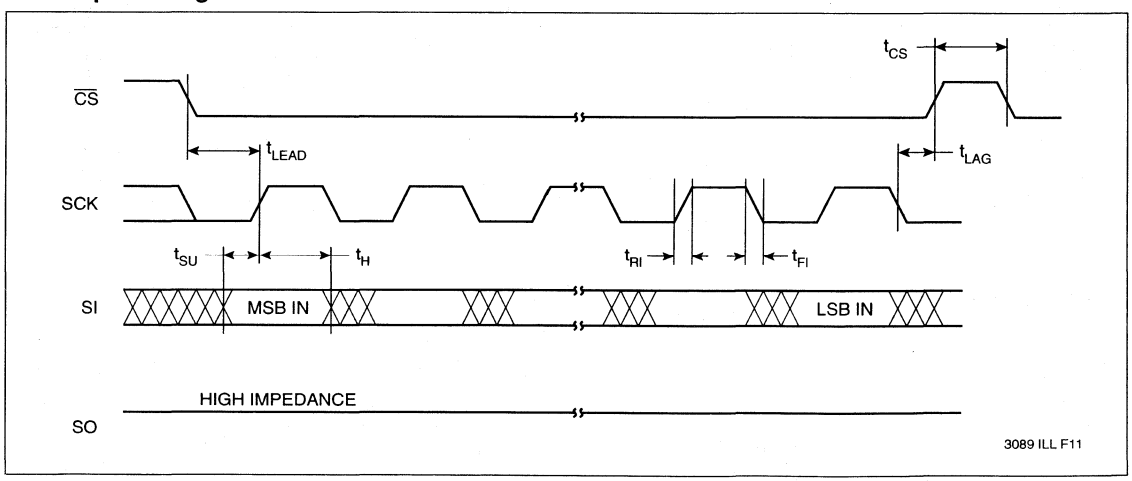
3089 PGM T13.1

Notes: (3) This parameter is periodically sampled and not 100% tested.
(4) t_{WC} is the time from the rising edge of $\overline{CS}$ after a valid write sequence has been sent to the end of the self-timed internal nonvolatile write cycle.
(5) After a read status register operation for WIP bit LOW, t_{CS} min. is 500µs.

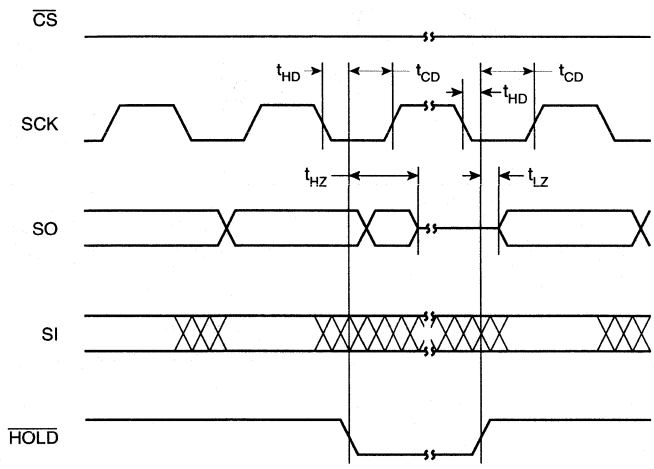
Serial Output Timing



Serial Input Timing

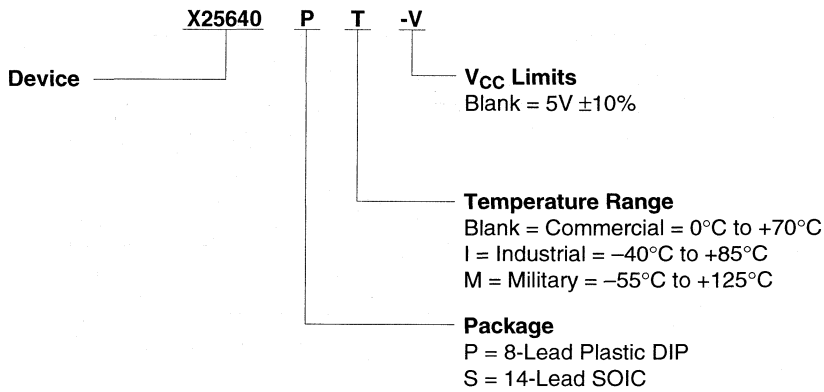


Hold Timing

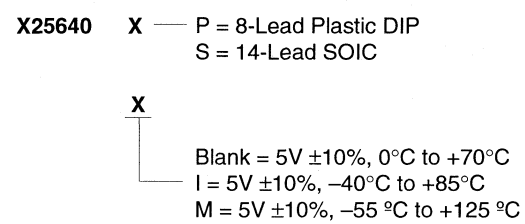


3089 ILL F12.1

ORDERING INFORMATION



Part Mark Convention



APPLICATION NOTES
A V A I L A B L E
AN19 • AN38 • AN41 • AN61

64K X25642 8K x 8 Bit

Advanced SPI Serial E²PROM with Block Lock™ Protection

FEATURES

- 2MHz Clock Rate
- Low Power CMOS
  - —<1μA Standby Current
  - —<5mA Active Current
- 2.7V To 5.5V Power Supply
- Packages
  - —8-Pin Mini-DIP
  - —8-Lead SOIC
  - —14-Lead SOIC
  - —20-Lead TSSOP
- SPI Modes (0,0 & 1,1)
- 8K X 8 Bits
  - —32 Byte Page Mode
- Block Lock Protection
  - —Protect 1/4, 1/2 or all of E²PROM Array
- Built-in Inadvertent Write Protection
  - —Power-Up/Down protection circuitry
  - —Write Enable Latch
  - —Write Protect Pin
- Self-Timed Write Cycle
  - —5ms Write Cycle Time (Typical)
- High Reliability
  - —Endurance: 100,000 cycles
  - —Data Retention: 100 Years
  - —ESD protection: 2000V on all pins

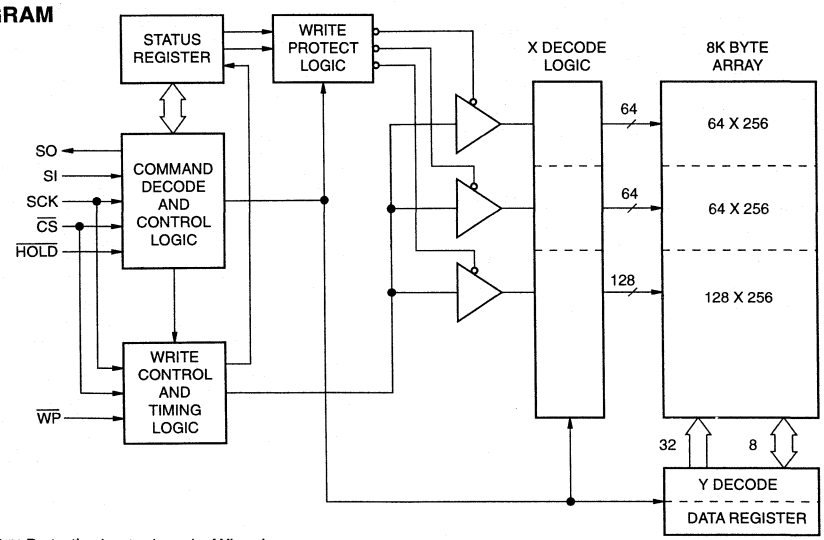
DESCRIPTION

The X25642 is a CMOS 65,536-bit serial E²PROM, internally organized as 8K x 8. The X25642 features a Serial Peripheral Interface (SPI) and software protocol allowing operation on a simple three-wire bus. The bus signals are a clock input (SCK) plus separate data in (SI) and data out (SO) lines. Access to the device is controlled through a chip select ($\overline{CS}$) input, allowing any number of devices to share the same bus.

The X25642 also features two additional inputs that provide the end user with added flexibility. By asserting the $\overline{HOLD}$ input, the X25642 will ignore transitions on its inputs, thus allowing the host to service higher priority interrupts. The $\overline{WP}$ input can be used as a hardwire input to the X25642 disabling all write attempts to the status register, thus providing a mechanism for limiting end user capability of altering 0, 1/4, 1/2 or all of the memory.

The X25642 utilizes Xicor's proprietary Direct Write™ cell, providing a minimum endurance of 100,000 cycles and a minimum data retention of 100 years.

FUNCTIONAL DIAGRAM



Direct Write™ and Block Lock™ Protection is a trademark of Xicor, Inc.

PIN DESCRIPTIONS

Serial Output (SO)

SO is a push/pull serial data output pin. During a read cycle, data is shifted out on this pin. Data is clocked out by the falling edge of the serial clock.

Serial Input (SI)

SI is the serial data input pin. All opcodes, byte addresses, and data to be written to the memory are input on this pin. Data is latched by the rising edge of the serial clock.

Serial Clock (SCK)

The Serial Clock controls the serial bus timing for data input and output. Opcodes, addresses, or data present on the SI pin are latched on the rising edge of the clock input, while data on the SO pin change after the falling edge of the clock input.

Chip Select ($\overline{CS}$)

When $\overline{CS}$ is HIGH, the X25642 is deselected and the SO output pin is at high impedance and unless an internal write operation is underway, the X25642 will be in the standby power mode. $\overline{CS}$ LOW enables the X25642, placing it in the active power mode. It should be noted that after power-up, a HIGH to LOW transition on $\overline{CS}$ is required prior to the start of any operation.

Write Protect ($\overline{WP}$)

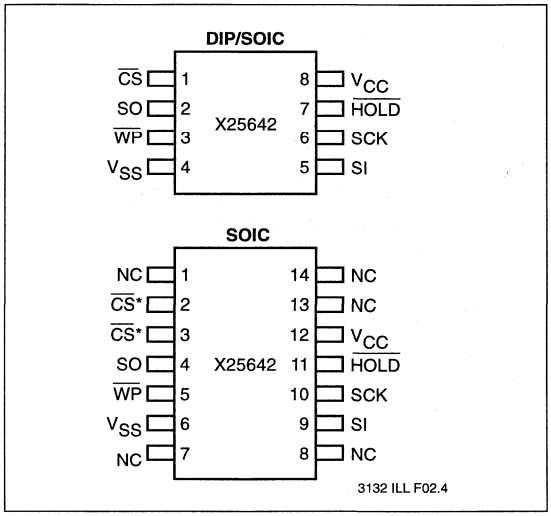
When $\overline{WP}$ is LOW and the nonvolatile bit WPEN is "1", nonvolatile writes to the X25642 status register are disabled, but the part otherwise functions normally. When $\overline{WP}$ is held HIGH, all functions, including nonvolatile writes operate normally. $\overline{WP}$ going LOW while $\overline{CS}$ is still LOW will interrupt a write to the X25642 status register. If the internal write cycle has already been initiated, $\overline{WP}$ going LOW will have no affect on a write.

The $\overline{WP}$ pin function is blocked when the WPEN bit in the status register is "0". This allows the user to install the X25642 in a system with $\overline{WP}$ pin grounded and still be able to write to the status register. The $\overline{WP}$ pin functions will be enabled when the WPEN bit is set "1".

Hold ($\overline{HOLD}$)

$\overline{HOLD}$ is used in conjunction with the $\overline{CS}$ pin to select the device. Once the part is selected and a serial sequence is underway, $\overline{HOLD}$ may be used to pause the serial communication with the controller without resetting the serial sequence. To pause, $\overline{HOLD}$ must be brought LOW while SCK is LOW. To resume communication, $\overline{HOLD}$ is brought HIGH, again while SCK is LOW. If the pause feature is not used, $\overline{HOLD}$ should be held HIGH at all times.

PIN CONFIGURATION



* Pin 2 and Pin 3 are internally connected. Only one $\overline{CS}$ needs to be connected externally.

PIN NAMES

Symbol	Description
$\overline{CS}$	Chip Select Input
SO	Serial Output
SI	Serial Input
SCK	Serial Clock Input
$\overline{WP}$	Write Protect Input
V_{SS}	Ground
V_{CC}	Supply Voltage
$\overline{HOLD}$	Hold Input
NC	No Connect

3132 FRM T01

PRINCIPLES OF OPERATION

The X25642 is a 8K x 8 E^2PROM designed to interface directly with the synchronous serial peripheral interface (SPI) of many popular microcontroller families.

The X25642 contains an 8-bit instruction register. It is accessed via the SI input, with data being clocked in on the rising SCK. $\overline{CS}$ must be LOW and the $\overline{HOLD}$ and $\overline{WP}$ inputs must be HIGH during the entire operation.

Table 1 contains a list of the instructions and their opcodes. All instructions, addresses and data are transferred MSB first.

Data input is sampled on the first rising edge of SCK after $\overline{CS}$ goes LOW. SCK is static, allowing the user to stop the clock and then resume operations. If the clock line is shared with other peripheral devices on the SPI bus, the user can assert the $\overline{HOLD}$ input to place the X25642 into a "PAUSE" condition. After releasing $\overline{HOLD}$, the X25642 will resume operation from the point when $\overline{HOLD}$ was first asserted.

Write Enable Latch

The X25642 contains a "write enable" latch. This latch must be SET before a write operation will be completed internally. The WREN instruction will set the latch and the WRDI instruction will reset the latch. This latch is automatically reset upon a power-up condition and after the completion of a byte, page, or status register write cycle.

Status Register

The RDSR instruction provides access to the status register. The status register may be read at any time, even during a write cycle. The status register is formatted as follows:

7	6	5	4	3	2	1	0
WPEN	X	X	X	BP1	BP0	WEL	WIP

3132 FRM T02

WPEN, BP0 and BP1 are set by the WRSR instruction. WEL and WIP are read-only and automatically set by other operations.

The Write-In-Process (WIP) bit indicates whether the X25642 is busy with a write operation. When set to a "1", a write is in progress, when set to a "0", no write is in progress. During a write, all other bits are set to "1".

The Write Enable Latch (WEL) bit indicates the status of the "write enable" latch. When set to a "1", the latch is set, when set to a "0", the latch is reset.

The Block Protect (BP0 and BP1) bits are nonvolatile and allow the user to select one of four levels of protection. The X25642 is divided into four 16384-bit segments. One, two, or all four of the segments may be protected. That is, the user may read the segments but will be unable to alter (write) data within the selected segments. The partitioning is controlled as illustrated below.

Status Register Bits		Array Addresses Protected
BP1	BP0	
0	0	None
0	1	$1800–$1FFF
1	0	$1000–$1FFF
1	1	$0000–$1FFF

3132 FRM T03

Table 1. Instruction Set

Instruction Name	Instruction Format*	Operation
WREN	0000 0110	Set the Write Enable Latch (Enable Write Operations)
WRDI	0000 0100	Reset the Write Enable Latch (Disable Write Operations)
RDSR	0000 0101	Read Status Register
WRSR	0000 0001	Write Status Register
READ	0000 0011	Read Data from Memory Array beginning at selected address
WRITE	0000 0010	Write Data to Memory Array beginning at Selected Address (1 to 32 Bytes)

3132 FRM T04

*Instructions are shown MSB in leftmost position. Instructions are transferred MSB first.

Write-Protect Enable

The Write-Protect-Enable (WPEN) is available for the X25642 as a nonvolatile enable bit for the $\overline{WP}$ pin.

WPEN	$\overline{WP}$	WEL	Protected Blocks	Unprotected Blocks	Status Register
0	X	0	Protected	Protected	Protected
0	X	1	Protected	Writable	Writable
1	LOW	0	Protected	Protected	Protected
1	LOW	1	Protected	Writable	Protected
X	HIGH	0	Protected	Protected	Protected
X	HIGH	1	Protected	Writable	Writable

3132 FRM T05

The Write Protect ($\overline{WP}$) pin and the nonvolatile Write Protect Enable (WPEN) bit in the Status Register control the programmable hardware write protect feature. Hardware write protection is enabled when $\overline{WP}$ pin is LOW, and the WPEN bit is "1". Hardware write protection is disabled when either the $\overline{WP}$ pin is HIGH or the WPEN bit is "0". When the chip is hardware write protected, nonvolatile writes are disabled to the Status Register, including the Block Protect bits and the WPEN bit itself, as well as the block-protected sections in the memory array. Only the sections of the memory array that are not block-protected can be written.

Note: Since the WPEN bit is write protected, it cannot be changed back to a "0", as long as the $\overline{WP}$ pin is held LOW.

Clock and Data Timing

Data input on the SI line is latched on the rising edge of SCK. Data is output on the SO line by the falling edge of SCK.

Read Sequence

When reading from the E^2PROM memory array, $\overline{CS}$ is first pulled LOW to select the device. The 8-bit READ instruction is transmitted to the X25642, followed by the 16-bit address of which the last 13 are used. After the READ opcode and address are sent, the data stored in the memory at the selected address is shifted out on the SO line. The data stored in memory at the next address can be read sequentially by continuing to provide clock pulses. The address is automatically incremented to the next higher address after each byte of data is shifted out. When the highest address is reached ($1FFF) the address counter rolls over to address $0000 allowing the read cycle to be continued indefinitely. The read operation is terminated by taking $\overline{CS}$ HIGH. Refer to the read E^2PROM array operation sequence illustrated in Figure 1.

To read the status register the $\overline{CS}$ line is first pulled LOW to select the device followed by the 8-bit RDSR instruction. After the RDSR opcode is sent, the contents of the status register are shifted out on the SO line. Figure 2 illustrates the read status register sequence.

Write Sequence

Prior to any attempt to write data into the X25642, the "write enable" latch must first be set by issuing the WREN instruction (See Figure 3). $\overline{CS}$ is first taken LOW, then the WREN instruction is clocked into the X25642. After all eight bits of the instruction are transmitted, $\overline{CS}$ must then be taken HIGH. If the user continues the write operation without taking $\overline{CS}$ HIGH after issuing the WREN instruction, the write operation will be ignored.

To write data to the E^2PROM memory array, the user issues the WRITE instruction, followed by the address and then the data to be written. This is minimally a thirty-two clock operation. $\overline{CS}$ must go LOW and remain LOW for the duration of the operation. The host may continue to write up to 32 bytes of data to the X25642. The only restriction is the 32 bytes must reside on the same page. If the address counter reaches the end of the page and the clock continues, the counter will "roll over" to the first address of the page and overwrite any data that may have been written.

For the write operation (byte or page write) to be completed, $\overline{CS}$ can only be brought HIGH after bit 0 of data byte N is clocked in. If it is brought HIGH at any other time the write operation will not be completed. Refer to Figures 4 and 5 below for a detailed illustration of the write sequences and time frames in which $\overline{CS}$ going HIGH are valid.

To write to the status register, the WRSR instruction is followed by the data to be written. Data bits 0, 1, 4, 5 and 6 must be "0". Figure 6 illustrates this sequence.

While the write is in progress following a status register or E^2PROM write sequence, the status register may be read to check the WIP bit. During this time the WIP bit will be HIGH.

Hold Operation

The $\overline{HOLD}$ input should be HIGH (at V_{IH}) under normal operation. If a data transfer is to be interrupted $\overline{HOLD}$ can be pulled LOW to suspend the transfer until it can be resumed. The only restriction is the SCK input must be LOW when $\overline{HOLD}$ is first pulled LOW and SCK must also be LOW when $\overline{HOLD}$ is released.

The $\overline{HOLD}$ input may be tied HIGH either directly to V_{CC} or tied to V_{CC} through a resistor.

Operational Notes

The X25642 powers-up in the following state:

- The device is in the low power standby state.
- A HIGH to LOW transition on $\overline{CS}$ is required to enter an active state and receive an instruction.
- SO pin is high impedance.
- The "write enable" latch is reset.

Data Protection

The following circuitry has been included to prevent inadvertent writes:

- The "write enable" latch is reset upon power-up.
- A WREN instruction must be issued to set the "write enable" latch.
- $\overline{CS}$ must come HIGH at the proper clock count in order to start a write cycle.

Figure 1. Read E²PROM Array Operation Sequence

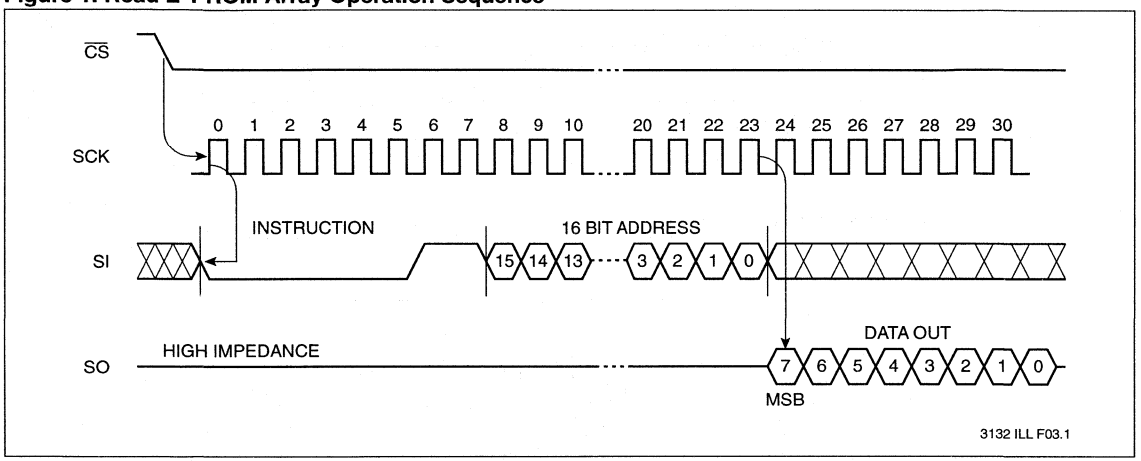


Figure 2. Read Status Register Operation Sequence

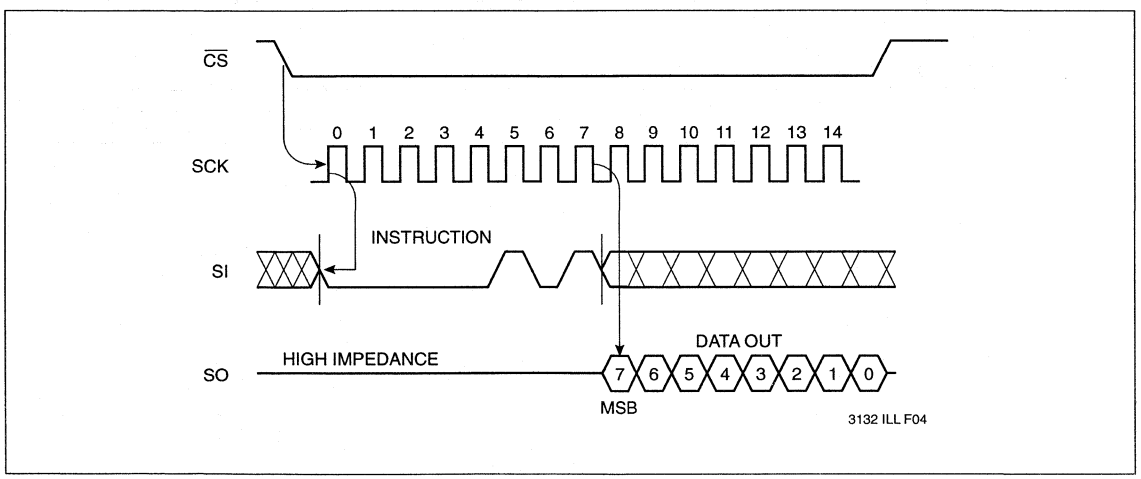


Figure 3. Write Enable Latch Sequence

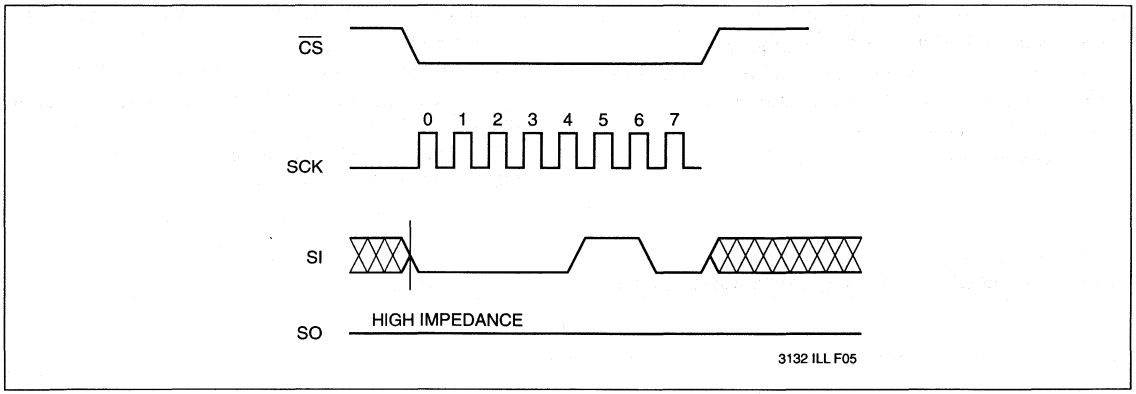


Figure 4. Byte Write Operation Sequence

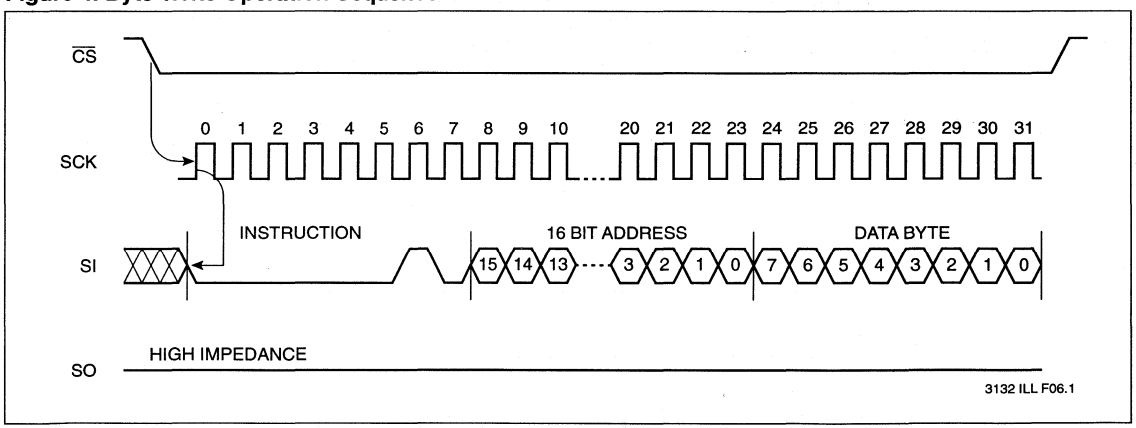


Figure 5. Page Write Operation Sequence

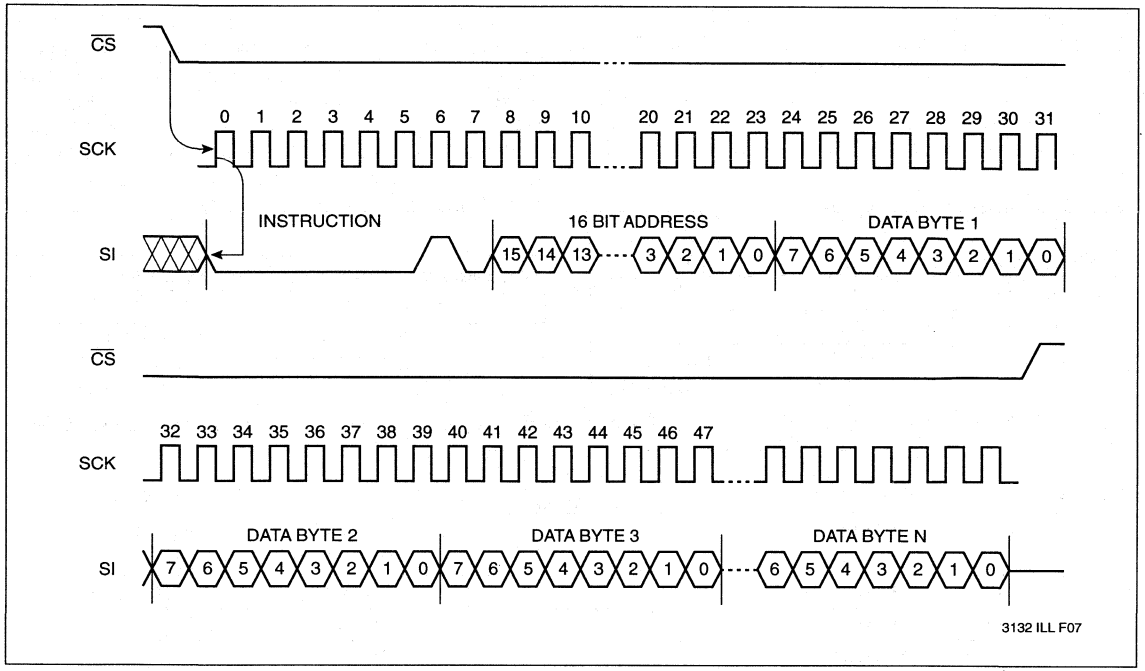
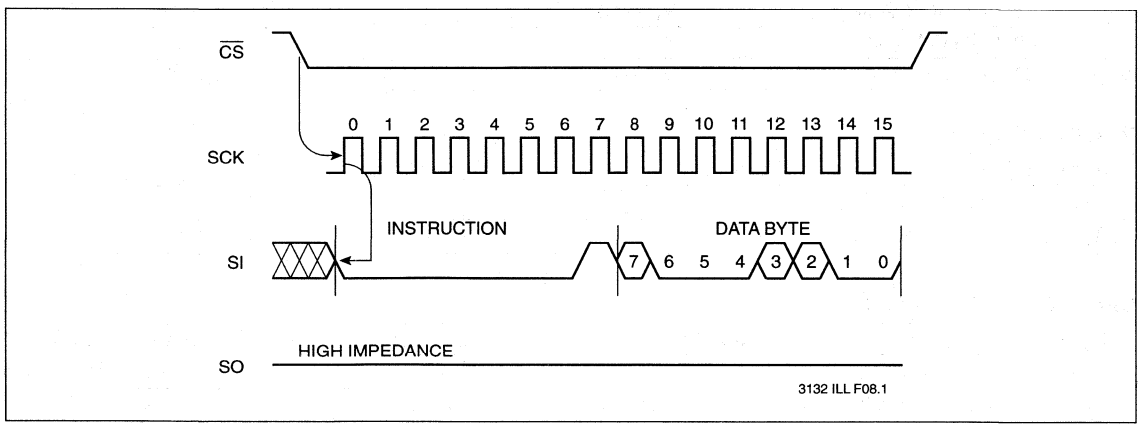


Figure 6. Write Status Register Operation Sequence



ABSOLUTE MAXIMUM RATINGS*

Temperature under Bias .....–65°C to +135°C
Storage Temperature .....–65°C to +150°C
Voltage on any Pin with Respect to V_{SS} .....–1V to +7V
D.C. Output Current 5mA
(Soldering, 10 seconds) .....300°C

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	+70°C
Industrial	–40°C	+85°C
Military	–55°C	+125°C

3132 FRM T06.1

Supply Voltage	Limits
X25642	5V ±10%
X25642-2.7	2.7V to 5.5V

3132 FRM T07

D.C. OPERATING CHARACTERISTICS (Over the recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
I_{CC}	V_{CC} Supply Current (Active)		5	mA	SCK = V_{CC} x 0.1/V_{CC} x 0.9 @ 2MHz, SO = Open, $\overline{CS}$ = V_{SS}
I_{SB}	V_{CC} Supply Current (Standby)		1	µA	$\overline{CS}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC} – 0.3V
I_{LI}	Input Leakage Current		10	µA	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output Leakage Current		10	µA	V_{OUT} = V_{SS} to V_{CC}
V_{IL}(1)	Input LOW Voltage	–1	V_{CC} x 0.3	V	
V_{IH}(1)	Input HIGH Voltage	V_{CC} x 0.7	V_{CC} + 0.5	V	
V_{OL1}	Output LOW Voltage		0.4	V	I_{OL} = 3mA, V_{CC} = 5V
V_{OH1}	Output HIGH Voltage	V_{CC}–0.8		V	I_{OH} = –1.6mA, V_{CC} = 5V
V_{OL2}	Output LOW Voltage		0.4	V	I_{OL} = 1.5mA, V_{CC} = 3V
V_{OH2}	Output HIGH Voltage	V_{CC}–0.3		V	I_{OH} = –0.4mA, V_{CC} = 3V

3132 FRM T08.3

POWER-UP TIMING

Symbol	Parameter	Min.	Max.	Units
T_{PUR}(3)	Power-up to Read Operation		1	ms
T_{PUW}(3)	Power-up to Write Operation		1	ms

3132 FRM T09

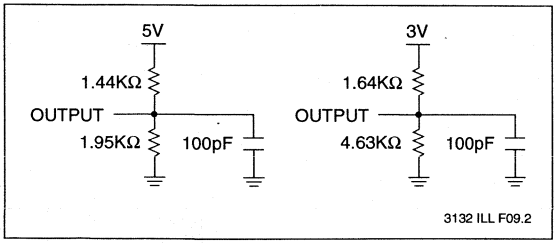
CAPACITANCE T_A = +25°C, f = 1MHz, V_{CC} = 5V

Symbol	Parameter	Max.	Units	Test Conditions
$C_{I/O}$(3)	Output Capacitance (SO)	8	pF	$V_{I/O}$ = 0V
C_{IN}(3)	Input Capacitance (SCK, SI, $\overline{CS}$, $\overline{WP}$, $\overline{HOLD}$)	6	pF	V_{IN} = 0V

3132 FRM T10.1

Notes: (1) V_{IL} min. and V_{IH} max. are for reference only and are not tested.
(2) This parameter is periodically sampled and not 100% tested.
(3) t_{PUR} and t_{PUW} are the delays required from the time V_{CC} is stable until the specified operation can be initiated. These parameters are periodically sampled and not 100% tested.

EQUIVALENT A.C. LOAD CIRCUIT



A.C. CONDITIONS OF TEST

Input Pulse Levels	V_{CC} x 0.1 to V_{CC} x 0.9
Input Rise and Fall Times	10ns
Input and OutputTiming Levels	V_{CC} X 0.5

3132 FRM T11.

2

A.C. OPERATING CHARACTERISTICS

Data Input Timing

Symbol	Parameter	Min.	Max.	Units
f_{SCK}	Clock Frequency	0	2	MHz
t_{CYC}	Cycle Time	500		ns
t_{LEAD}	$\overline{CS}$ Lead Time	250		ns
t_{LAG}	$\overline{CS}$ Lag Time	250		ns
t_{WH}	Clock HIGH Time	200		ns
t_{WL}	Clock LOW Time	200		ns
t_{SU}	Data Setup Time	50		ns
t_H	Data Hold Time	50		ns
t_{RI}(4)	Data In Rise Time		2	µs
t_{FI}(4)	Data In Fall Time		2	µs
t_{HD}	$\overline{HOLD}$ Setup Time	100		ns
t_{CD}	$\overline{HOLD}$ Hold Time	100		ns
t_{CS}	$\overline{CS}$ Deselect Time	2.0		µs
t_{WC}(5)	Write Cycle Time		10	ms

3132 FRM T12.1

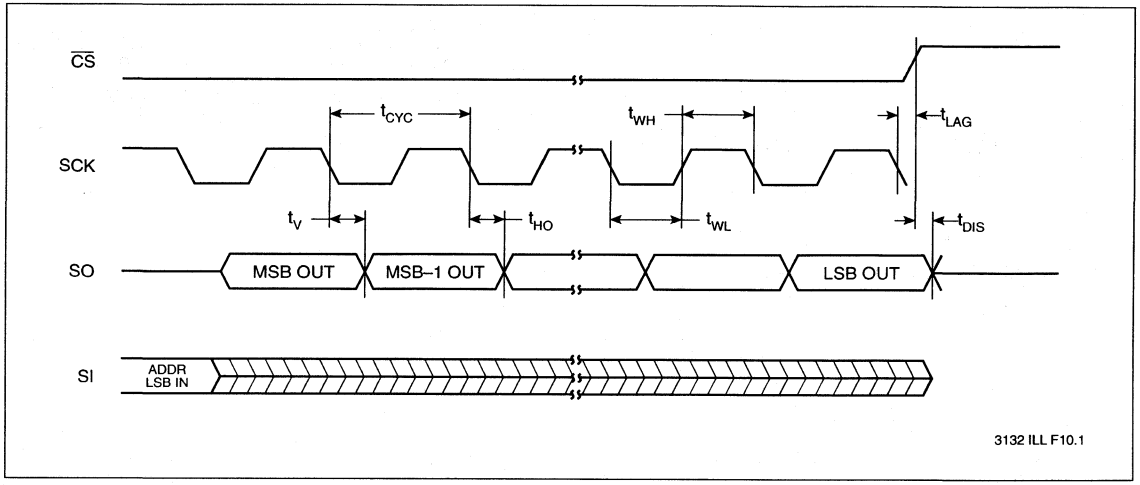
Data Output Timing

Symbol	Parameter	Min.	Max.	Units
f_{SCK}	Clock Frequency	0	2	MHz
t_{DIS}	Output Disable Time		250	ns
t_V	Output Valid from Clock LOW		200	ns
t_{HO}	Output Hold Time	0		ns
t_{RO}(4)	Output Rise Time		100	ns
t_{FO}(4)	Output Fall Time		100	ns
t_{LZ}(4)	$\overline{HOLD}$ HIGH to Output in Low Z	100		ns
t_{HZ}(4)	$\overline{HOLD}$ LOW to Output in High Z	100		ns

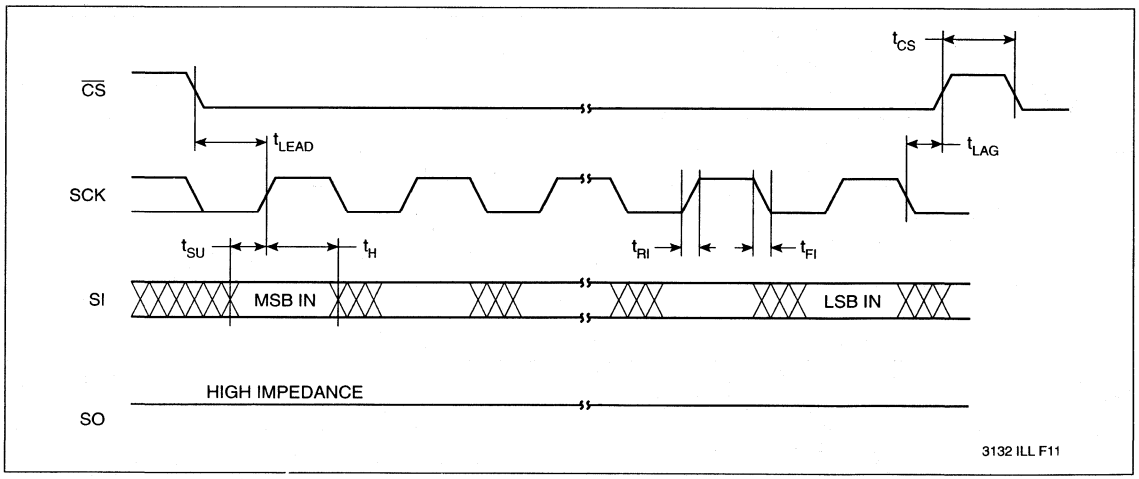
3132 FRM T13.1

Notes: (4) This parameter is periodically sampled and not 100% tested.
(5) t_{WC} is the time from the rising edge of $\overline{CS}$ after a valid write sequence has been sent to the end of the self-timed internal nonvolatile write cycle.

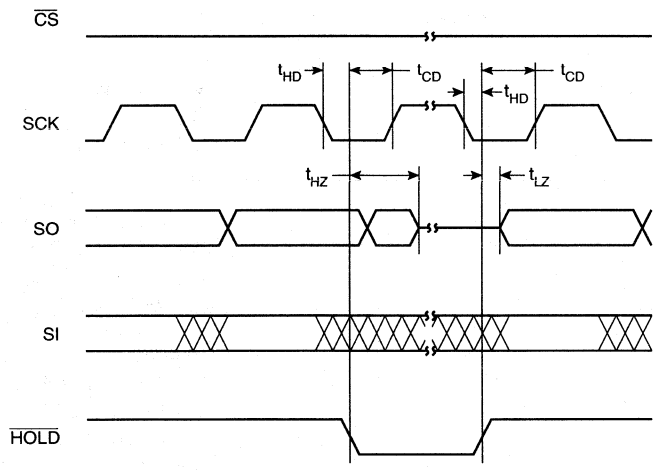
Serial Output Timing



Serial Input Timing

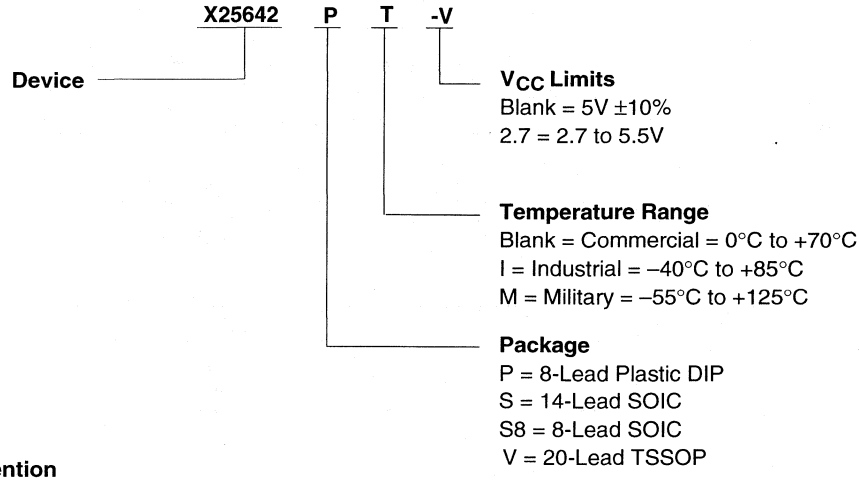


Hold Timing

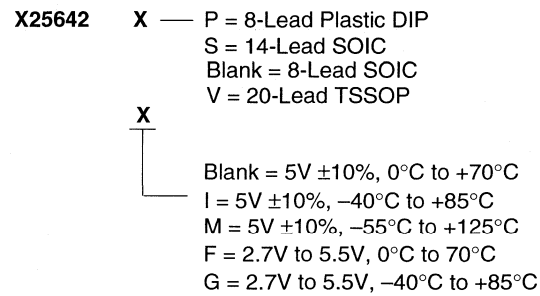


3132 ILL F12.1

ORDERING INFORMATION



Part Mark Convention



APPLICATION NOTE
AVAILABLE
AN61

128K X25128 16K x 8 Bit

SPI Serial E²PROM With Block Lock™ Protection

FEATURES

- 2MHz Clock Rate
- SPI Modes (0,0 & 1,1)
- 16K X 8 Bits
  - —32 Byte Page Mode
- Low Power CMOS
  - —<1μA Standby Current
  - —<5mA Active Current
- 2.7V To 5.5V Power Supply
- Block Lock Protection
  - —Protect 1/4, 1/2 or all of E²PROM Array
- Built-in Inadvertent Write Protection
  - —Power-Up/Power-Down protection circuitry
  - —Write Enable Latch
  - —Write Protect Pin
- Self-Timed Write Cycle
  - —5ms Write Cycle Time (Typical)
- High Reliability
  - —Endurance: 100,000 cycles
  - —Data Retention: 100 Years
  - —ESD protection: 2000V on all pins
- 8-Pin Mini-DIP Package
- 16-Lead 150 mil SOIC Package

DESCRIPTION

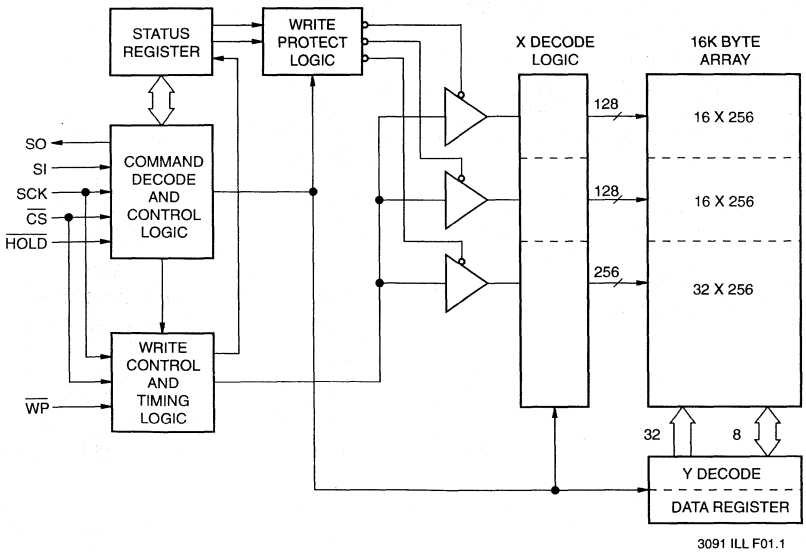
The X25128 is a CMOS 131,072-bit serial E²PROM, internally organized as 16K x 8. The X25128 features a Serial Peripheral Interface (SPI) and software protocol allowing operation on a simple three-wire bus. The bus signals are a clock input (SCK) plus separate data in (SI) and data out (SO) lines. Access to the device is controlled through a chip select ($\overline{CS}$) input, allowing any number of devices to share the same bus.

The X25128 also features two additional inputs that provide the end user with added flexibility. By asserting the $\overline{HOLD}$ input, the X25128 will ignore transitions on its inputs, thus allowing the host to service higher priority interrupts. The $\overline{WP}$ input can be used as a hardwire input to the X25128 disabling all write attempts to the status register, thus providing a mechanism for limiting end user capability of altering 0, 1/4, 1/2 or all of the memory.

The X25128 utilizes Xicor's proprietary Direct Write™ cell, providing a minimum endurance of 100,000 cycles and a minimum data retention of 100 years.

2

FUNCTIONAL DIAGRAM



3091 ILL F01.1

Direct Write™ and Block Lock™ Protection is a trademark of Xicor, Inc.

PIN DESCRIPTIONS

Serial Output (SO)

SO is a push/pull serial data output pin. During a read cycle, data is shifted out on this pin. Data is clocked out by the falling edge of the serial clock.

Serial Input (SI)

SI is the serial data input pin. All opcodes, byte addresses, and data to be written to the memory are input on this pin. Data is latched by the rising edge of the serial clock.

Serial Clock (SCK)

The Serial Clock controls the serial bus timing for data input and output. Opcodes, addresses, or data present on the SI pin are latched on the rising edge of the clock input, while data on the SO pin change after the falling edge of the clock input.

Chip Select ($\overline{CS}$)

When $\overline{CS}$ is HIGH, the X25128 is deselected and the SO output pin is at high impedance and unless an internal write operation is underway, the X25128 will be in the standby power mode. $\overline{CS}$ LOW enables the X25128, placing it in the active power mode. It should be noted that after power-up, a HIGH to LOW transition on $\overline{CS}$ is required prior to the start of any operation.

Write Protect ($\overline{WP}$)

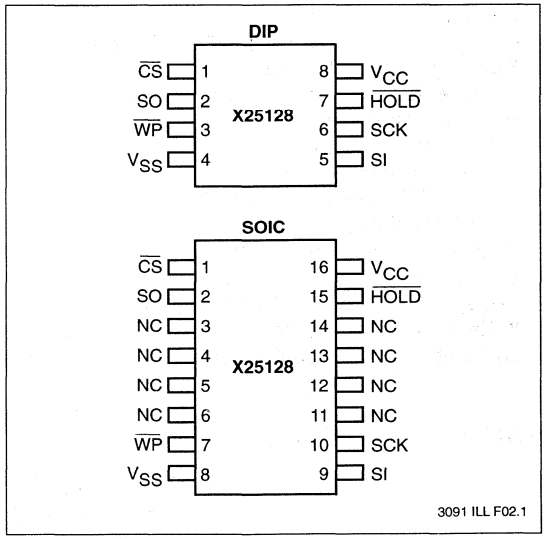
When $\overline{WP}$ is LOW and the nonvolatile bit WPEN is "1", nonvolatile writes to the X25128 status register are disabled, but the part otherwise functions normally. When $\overline{WP}$ is held HIGH, all functions, including nonvolatile writes operate normally. $\overline{WP}$ going LOW while $\overline{CS}$ is still LOW will interrupt a write to the X25128 status register. If the internal write cycle has already been initiated, $\overline{WP}$ going LOW will have no effect on a write.

The $\overline{WP}$ pin function is blocked when the WPEN bit in the status register is "0". This allows the user to install the X25128 in a system with $\overline{WP}$ pin grounded and still be able to write to the status register. The $\overline{WP}$ pin functions will be enabled when the WPEN bit is set "0".

Hold ($\overline{HOLD}$)

$\overline{HOLD}$ is used in conjunction with the $\overline{CS}$ pin to select the device. Once the part is selected and a serial sequence is underway, $\overline{HOLD}$ may be used to pause the serial communication with the controller without resetting the serial sequence. To pause, $\overline{HOLD}$ must be brought low while SCK is Low. To resume communication, $\overline{HOLD}$ is brought high, again while SCK is low. If the pause feature is not used, $\overline{HOLD}$ should be held high at all times.

PIN CONFIGURATION



PIN NAMES

SYMBOL	DESCRIPTION
$\overline{CS}$	Chip Select Input
SO	Serial Output
SI	Serial Input
SCK	Serial Clock Input
$\overline{WP}$	Write Protect Input
V_{SS}	Ground
V_{CC}	Supply Voltage
$\overline{HOLD}$	Hold Input
NC	No Connect

3091 PGM T01

PRINCIPLES OF OPERATION

The X25128 is a 8K x 8 E^2PROM designed to interface directly with the synchronous serial peripheral interface (SPI) of many popular microcontroller families.

The X25128 contains an 16-bit instruction register. It is accessed via the SI input, with data being clocked in on the rising SCK. $\overline{CS}$ must be LOW and the $\overline{HOLD}$ and $\overline{WP}$ inputs must be HIGH during the entire operation. The $\overline{WP}$ input is "Don't Care" if WPEN is set "0".

Table 1 contains a list of the instructions and their opcodes. All instructions, addresses and data are transferred MSB first.

Data input is sampled on the first rising edge of SCK after $\overline{CS}$ goes LOW. SCK is static, allowing the user to stop the clock and then resume operations. If the clock line is shared with other peripheral devices on the SPI bus, the user can assert the $\overline{HOLD}$ input to place the X25128 into a "PAUSE" condition. After releasing $\overline{HOLD}$, the X25128 will resume operation from the point when $\overline{HOLD}$ was first asserted.

Write Enable Latch

The X25128 contains a "write enable" latch. This latch must be SET before a write operation will be completed internally. The WREN instruction will set the latch and the WRDI instruction will reset the latch. This latch is automatically reset upon a power-on condition and after the completion of a byte, page, or status register write cycle.

Status Register

The RDSR instruction provides access to the status register. The status register may be read at any time, even during a write cycle. The status register is formatted as follows:

7	6	5	4	3	2	1	0
WPEN	X	X	X	BP1	BP0	WEL	WIP

3091 PGM T02

WPEN, BP0 and BP1 are set by the WRSR instruction. WEL and WIP are read-only and automatically set by other operations.

The Write-In-Process (WIP) bit indicates whether the X25128 is busy with a write operation. When set to a "1", a write is in progress, when set to a "0", no write is in progress. During a write, all other bits are set to "1".

The Write Enable Latch (WEL) bit indicates the status of the "write enable" latch. When set to a "1", the latch is set, when set to a "0", the latch is reset.

The Block Protect (BP0 and BP1) bits are nonvolatile and allows the user to select one of four levels of protection. The X25128 is divided into four 32,768-bit segments. One, two, or all four of the segments may be protected. That is, the user may read the segments but will be unable to alter (write) data within the selected segments. The partitioning is controlled as illustrated below.

Status Register Bits		Array Addresses Protected
BP1	BP0	
0	0	None
0	1	$3000–$3FFF
1	0	$2000–$3FFF
1	1	$0000–$3FFF

3091 PGM T03

Table 1. Instruction Set

Instruction Name	Instruction Format*	Operation
WREN	0000 0110	Set the Write Enable Latch (Enable Write Operations)
WRDI	0000 0100	Reset the Write Enable Latch (Disable Write Operations)
RDSR	0000 0101	Read Status Register
WRSR	0000 0001	Write Status Register
READ	0000 0011	Read Data from Memory Array beginning at selected address
WRITE	0000 0010	Write Data to Memory Array beginning at Selected Address (1 to 32 Bytes)

3091 PGM T04

*Instructions are shown MSB in leftmost position. Instructions are transferred MSB first.

Write-Protect Enable

The Write-Protect-Enable (WPEN) is available for the X25128 as a nonvolatile enable bit for the $\overline{WP}$ pin.

WPEN	$\overline{WP}$	WEL	Protected Blocks	Unprotected Blocks	Status Register
0	X	0	Protected	Protected	Protected
0	X	1	Protected	Writable	Writable
1	LOW	0	Protected	Protected	Protected
1	LOW	1	Protected	Writable	Protected
X	HIGH	0	Protected	Protected	Protected
X	HIGH	1	Protected	Writable	Writable

3091 PGM T05.1

The Write Protect ($\overline{WP}$) pin and the nonvolatile Write Protect Enable (WPEN) bit in the Status Register control the programmable hardware write protect feature. Hardware write protection is enabled when $\overline{WP}$ pin is LOW, and the WPEN bit is "1". Hardware write protection is disabled when either the $\overline{WP}$ pin is HIGH or the WPEN bit is "0". When the chip is hardware write protected, nonvolatile writes are disabled to the Status Register, including the Block Protect bits and the WPEN bit itself, as well as the block-protected sections in the memory array. Only the sections of the memory array that are not block-protected can be written.

Note: Since the WPEN bit is write protected, it cannot be changed back to a "0", as long as the $\overline{WP}$ pin is held LOW.

Clock and Data Timing

Data input on the SI line is latched on the rising edge of SCK. Data is output on the SO line by the falling edge of SCK.

Read Sequence

When reading from the E^{2}PROM array, $\overline{CS}$ is first pulled LOW to select the device. The 8-bit READ instruction is transmitted to the X25128, followed by the 16-bit address of which the last 14 are used. After the READ opcode and address are sent, the data stored in the memory at the selected address is shifted out on the SO line. The data stored in memory at the next address can be read sequentially by continuing to provide clock pulses. The address is automatically incremented to the next higher address after each byte of data is shifted out. When the highest address is reached ($3FFF) the address counter rolls over to address $0000 allowing the read cycle to be continued indefinitely. The read operation is terminated by taking $\overline{CS}$ HIGH. Refer to the read E^{2}PROM array operation sequence illustrated in Figure 1.

To read the status register the $\overline{CS}$ line is first pulled LOW to select the device followed by the 8-bit instruction. After the RDSR opcode is sent, the contents of the status register are shifted out on the SO line. The read status register sequence is illustrated in Figure 2.

Write Sequence

Prior to any attempt to write data into the X25128, the "write enable" latch must first be set by issuing the WREN instruction (See Figure 3). $\overline{CS}$ is first taken LOW, then the WREN instruction is clocked into the X25128. After all eight bits of the instruction are transmitted, $\overline{CS}$ must then be taken HIGH. If the user continues the write operation without taking $\overline{CS}$ HIGH after issuing the WREN instruction, the write operation will be ignored.

To write data to the E^{2}PROM memory array, the user issues the WRITE instruction, followed by the address and then the data to be written. This is minimally a thirty-two clock operation. $\overline{CS}$ must go LOW and remain LOW for the duration of the operation. The host may continue to write up to 32 bytes of data to the X25128. The only restriction is the 32 bytes must reside on the same page. If the address counter reaches the end of the page and the clock continues, the counter will "roll over" to the first address of the page and overwrite any data that may have been written.

For the write operation (byte or page write) to be completed, $\overline{CS}$ can only be brought HIGH after bit 0 of data byte N is clocked in. If it is brought HIGH at any other time the write operation will not be completed. Refer to Figures 4 and 5 below for a detailed illustration of the write sequences and time frames in which $\overline{CS}$ going HIGH are valid.

To write to the status register, the WRSR instruction is followed by the data to be written. Data bits 0, 1, 4, 5 and 6 must be "0". This sequence is shown in Figure 6.

While the write is in progress, following a status register or E^{2}PROM write sequence, the status register may be read to check the WIP bit. During this time the WIP bit will be HIGH.

Hold Operation

The $\overline{HOLD}$ input should be HIGH (at V_{IH}) under normal operation. If a data transfer is to be interrupted $\overline{HOLD}$ can be pulled LOW to suspend the transfer until it can be resumed. The only restriction is the SCK input must be LOW when $\overline{HOLD}$ is first pulled LOW and SCK must also be LOW when $\overline{HOLD}$ is released.

The $\overline{HOLD}$ input may be tied HIGH either directly to V_{CC} or tied to V_{CC} through a resistor.

Operational Notes

The X25128 powers-up in the following state:

- The device is in the low power standby state.
- A HIGH to LOW transition on $\overline{CS}$ is required to enter an active state and receive an instruction.
- SO pin is high impedance.
- The "write enable" latch is reset.

Data Protection

The following circuitry has been included to prevent inadvertent writes:

- The "write enable" latch is reset upon power-up.
- A WREN instruction must be issued to set the "write enable" latch.
- $\overline{CS}$ must come HIGH at the proper clock count in order to start a write cycle.

Figure 1. Read E²PROM Array Operation Sequence

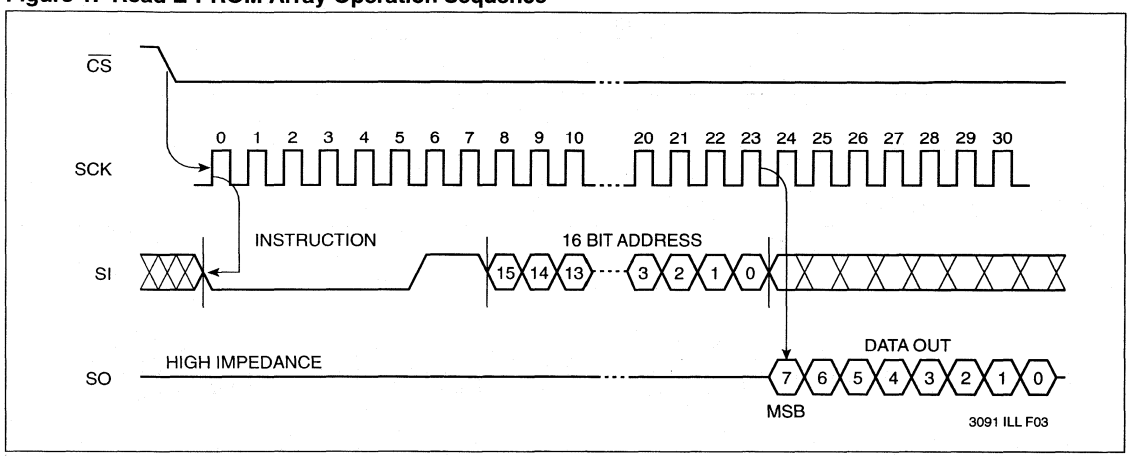


Figure 2. Read Status Register Operation Sequence

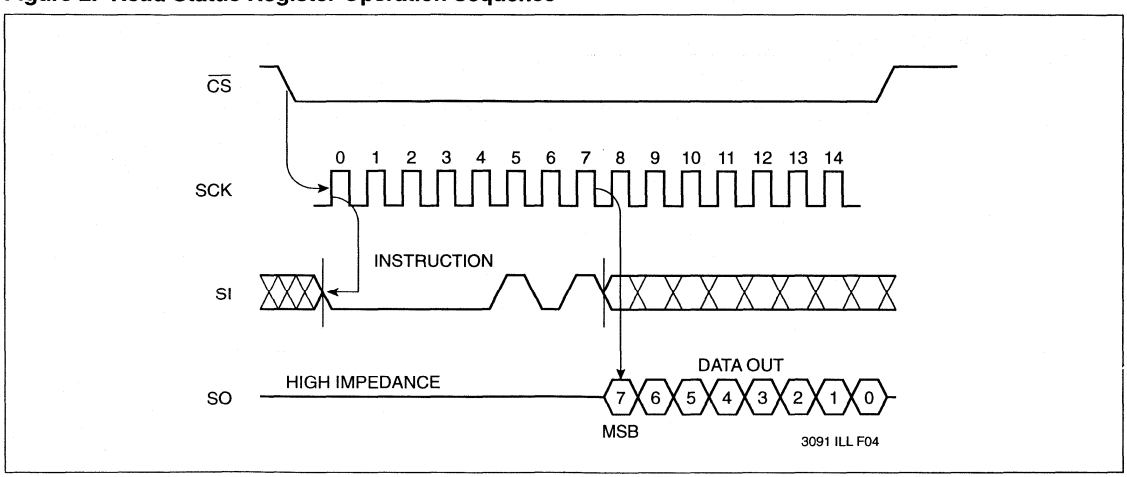


Figure 3. Write Enable Latch Sequence

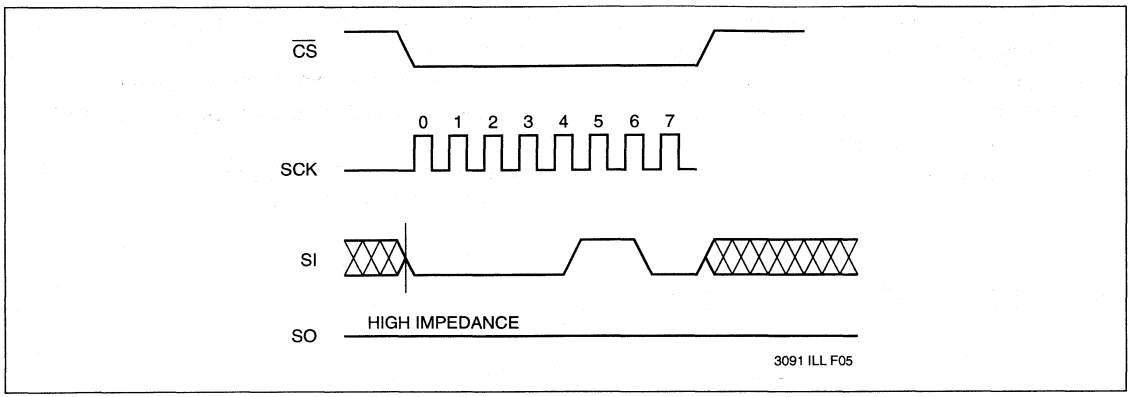


Figure 4. Byte Write Operation Sequence

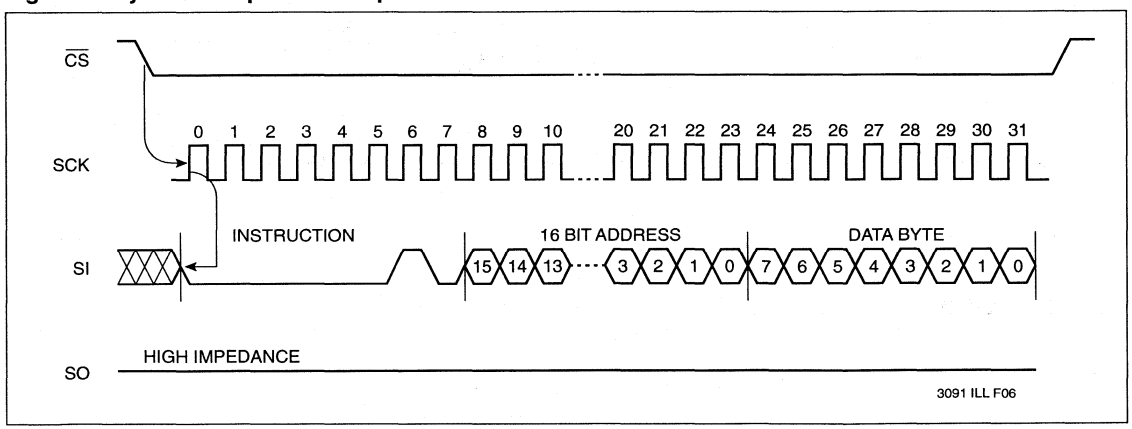


Figure 5. Page Write Operation Sequence

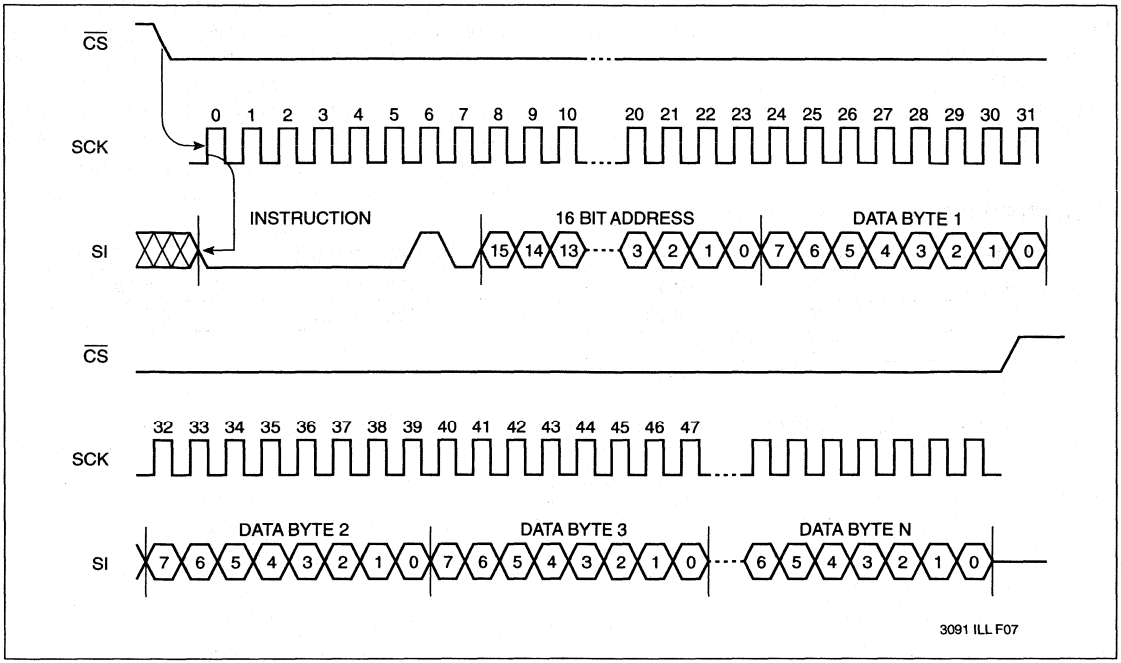
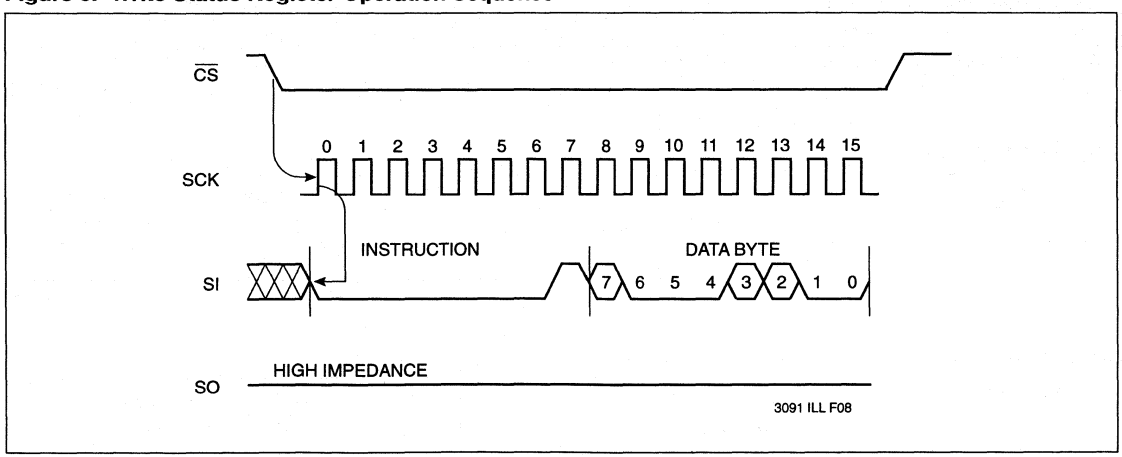


Figure 6. Write Status Register Operation Sequence



ABSOLUTE MAXIMUM RATINGS*

Temperature under Bias ..... –65°C to +135°C
Storage Temperature ..... –65°C to +150°C
Voltage on any Pin with Respect to V_{SS} ..... –1V to +7V
D.C. Output Current 5mA
Lead Temperature
(Soldering, 10 seconds) ..... 300°C

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temp	Min.	Max.
Commercial	0°C	+70°C
Industrial	–40°C	+85°C
Military	–55°C	+125°C

3091 PGM T06.1

Supply Voltage	Limits
X25128	5V ±10%
X25128-2.7	2.7V to 5.5V

3091 PGM T07.2

D.C. OPERATING CHARACTERISTICS (Over the recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
I_{CC}	V_{CC} Supply Current (Active)		5	mA	SCK = V_{CC} x 0.1/V_{CC} x 0.9 @ 2MHz, SO = Open, $\overline{CS}$ = V_{SS}
I_{SB}	V_{CC} Supply Current (Standby)		1	µA	$\overline{CS}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}
I_{LI}	Input Leakage Current		10	µA	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output Leakage Current		10	µA	V_{OUT} = V_{SS} to V_{CC}
V_{IL}(1)	Input LOW Voltage	–1	V_{CC} x 0.3	V	
V_{IH}(1)	Input HIGH Voltage	V_{CC} x 0.7	V_{CC} + 0.5	V	
V_{OL1}	Output LOW Voltage		0.4	V	V_{CC} = 5V, I_{OL} = 3mA
V_{OH1}	Output HIGH Voltage	V_{CC} – 0.8		V	V_{CC} = 5V, I_{OH} = -1.6mA
V_{OL2}	Output LOW Voltage		0.4	V	V_{CC} = 3V, I_{OL} = 1.5mA
V_{OH2}	Output HIGH Voltage	V_{CC} – 0.3		V	V_{CC} = 3V, I_{OH} = -0.4mA

3091 PGM T08.3

POWER-UP TIMING

Symbol	Parameter	Min.	Max.	Units
t_{PUR}(3)	Power-up to Read Operation		1	ms
t_{PUW}(3)	Power-up to Write Operation		5	ms

3091 PGM T09

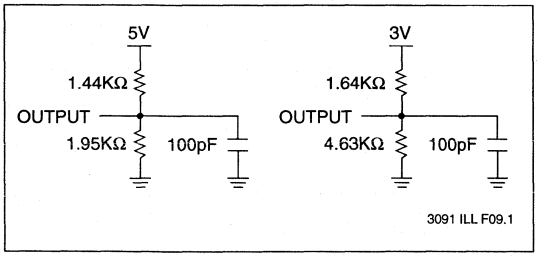
CAPACITANCE T_A = +25°C, f = 1MHz, V_{CC} = 5V.

Symbol	Test	Max.	Units	Conditions
C_{OUT}(2)	Output Capacitance (SO)	8	pF	V_{OUT} = 0V
C_{IN}(2)	Input Capacitance (SCK, SI, $\overline{CS}$, $\overline{WP}$, $\overline{HOLD}$)	6	pF	V_{IN} = 0V

3091 PGM T10.1

Notes: (1) V_{IL} min. and V_{IH} max. are for reference only and are not tested.
(2) This parameter is periodically sampled and not 100% tested.
(3) t_{PUR} and t_{PUW} are the delays required from the time V_{CC} is stable until the specified operation can be initiated. These parameters are periodically sampled and not 100% tested.

EQUIVALENT A.C. LOAD CIRCUIT



A.C. TEST CONDITIONS

Input Pulse Levels	V_{CC} x 0.1 to V_{CC} x 0.9
Input Rise and Fall Times	10ns
Input and Output Timing Level	V_{CC} x 0.5

3091 PGM T11

2

A.C. CHARACTERISTICS (Over recommended operating conditions, unless otherwise specified)

Data Input Timing

Symbol	Parameter	Min.	Max.	Units
f_{SCK}	Clock Frequency	0	2	MHz
t_{CYC}	Cycle Time	500		ns
t_{LEAD}	$\overline{CS}$ Lead Time	250		ns
t_{LAG}	$\overline{CS}$ Lag Time	250		ns
t_{WH}	Clock HIGH Time	200		ns
t_{WL}	Clock LOW Time	200		ns
t_{SU}	Data Setup Time	50		ns
t_H	Data Hold Time	50		ns
t_{RI}(4)	Data In Rise Time		2	µs
t_{FI}(4)	Data In Fall Time		2	µs
t_{HD}	$\overline{HOLD}$ Setup Time	100		ns
t_{CD}	$\overline{HOLD}$ Hold Time	100		ns
t_{CS}	$\overline{CS}$ Deselect Time	2.0		µs
t_{WC}(5)	Write Cycle Time		10	ms

3091 PGM T12.2

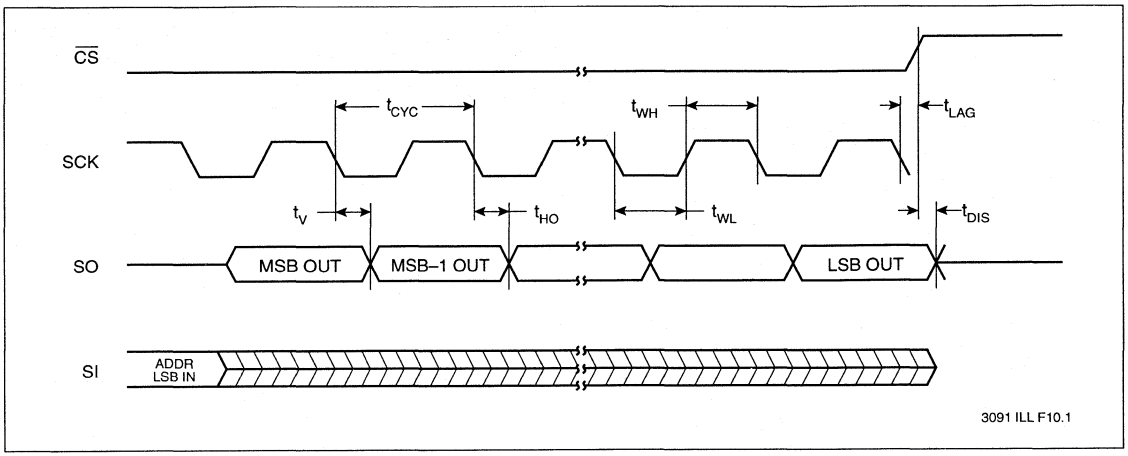
Data Output Timing

Symbol	Parameter	Min.	Max.	Units
f_{SCK}	Clock Frequency	0	2	MHz
t_{DIS}	Output Disable Time		250	ns
t_V	Output Valid from Clock LOW		200	ns
t_{HO}	Output Hold Time	0		ns
t_{RO}(4)	Output Rise Time		100	ns
t_{FO}(4)	Output Fall Time		100	ns
t_{LZ}(4)	$\overline{HOLD}$ HIGH to Output in Low Z	100		ns
t_{HZ}(4)	$\overline{HOLD}$ LOW to Output in High Z	100		ns

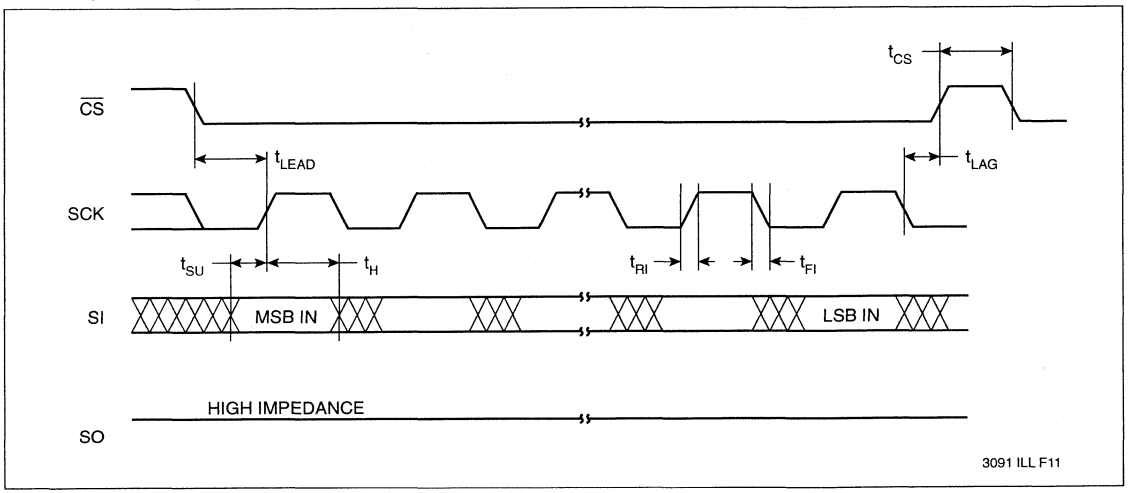
3091 PGM T13.2

Notes: (4) This parameter is periodically sampled and not 100% tested.
(5) t_{WC} is the time from the rising edge of $\overline{CS}$ after a valid write sequence has been sent to the end of the self-timed internal nonvolatile write cycle.

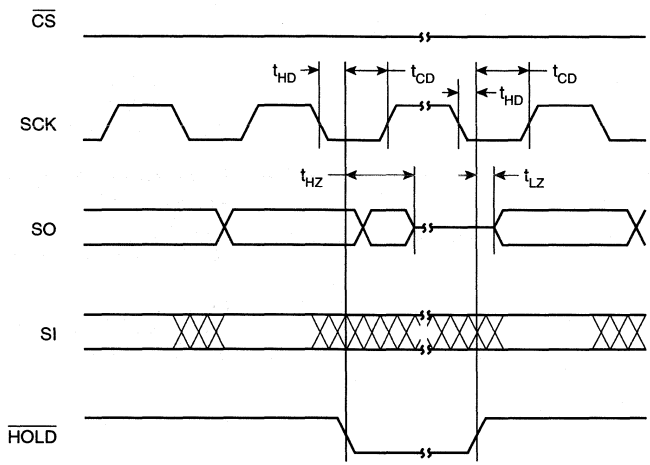
Serial Output Timing



Serial Input Timing



Hold Timing

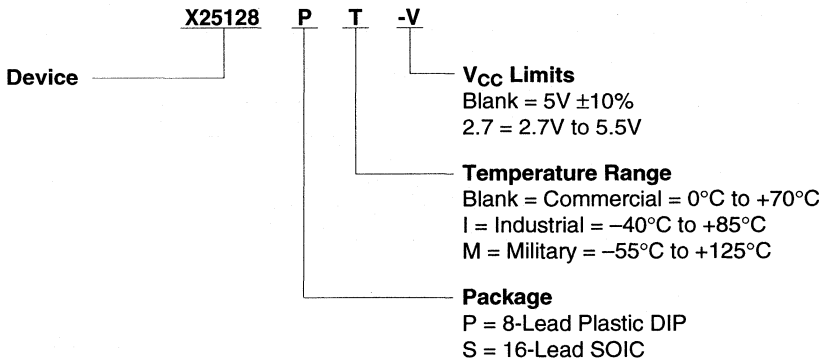


3091 ILL F12.1

SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

ORDERING INFORMATION



NOTES

Xicor

#9

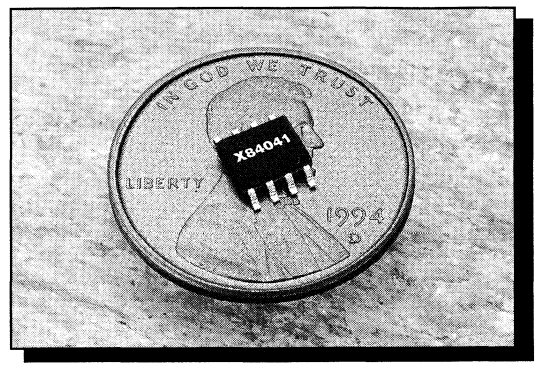
Design Engineering Bulletin

New Product and Applications Information for Design Engineers

New Memory Architecture Eliminates I/O Port Requirements X84041 MPS™ E² Directly Connects to Parallel Bus

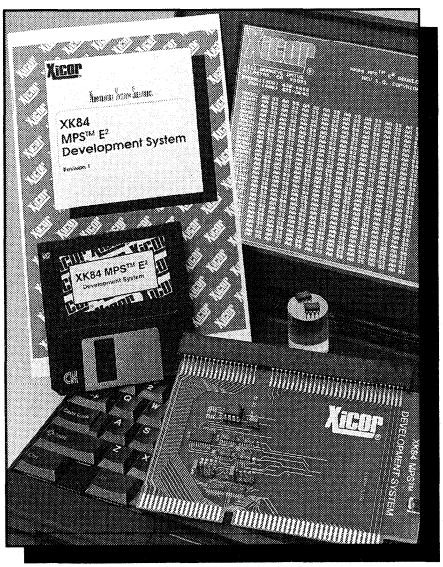
Glue logic for microprocessor or system bus interface is eliminated by the X84041's new architecture. The X84041 utilizes the typical microprocessor control signals ($\overline{OE}$, $\overline{WE}$, $\overline{CE}$) and a simple read/write sequence to directly interface with most common families of microprocessors. It's small size, low cost and low power is designed to replace more expensive and bulky bytewide E²PROMs.

The X84041 offers advanced features such as Low Voltage operation (2.5V), Write Protect ($\overline{WP}$), Page Mode operation, and a 45ns read access time. It is available in 8 pin DIP, SOIC and 14 pin TSSOP packages. The low cost and small footprint of this unique product line makes it attractive for applications such as cellular telephones, SIM module identification, PCMCIA cards boot configuration storage, and network node ID storage.



Direct microprocessor bus compatible serial E² in 8 pin SOIC saves board space.

The XK84 Development System Simplifies the Task of Prototyping with MPS™ E² Devices and Reduces Software Development Time



For ordering information on the XK84 Development System please use the ordering information located on the back cover of this bulletin.

The XK84 Development System enables designers to easily evaluate and prototype with the X84041 and future MPS™ E² devices. Using the system is as simple as inserting the XK84 into any unused expansion slot of a PC and executing the associated XK84 programming software. This software allows a designer to alter the E²PROM data by writing to (and reading from) any address in the X84041 in a similar manner as with any PC based EPROM programmer.

The XK84 can also be used in conjunction with another prototype card. The designer controls the I/O addresses used to control the $\overline{CE}$ and $\overline{WP}$ inputs to the X84041 and allows the other card to physically "piggyback" on top of the XK84. Xicor also provides ANSI C code that is used to interface with MPS™ E² devices. With this development system, any number of devices can be easily programmed prior to use in a prototype system and their contents can be just as easily examined during system debug. This will allow a designer to proceed quickly and efficiently when designing in an MPS™ E² device.

4K X84041 MPS™ E²PROM

Micro Port Saver E²PROM

FEATURES

- **Direct Interface to Micros**
  - **—Eliminates I/O port requirements**
  - **—No interface glue logic required**
  - **—Eliminates need for parallel to serial converters**
- **3.3Mbps data transfer rate**
- **Low Power CMOS**
  - **—2.7V to 5.5V Operation**
  - **—Standby Current Less than 50µA**
  - **—Active Current Less than 1mA**
- **45ns Read Access Time**
- **8-Byte Page Write Mode**
- **Typical Nonvolatile Write Cycle Time: 5ms**
- **High Reliability**
  - **—100,000 Endurance Cycles**
  - **—Guaranteed Data Retention: 100 Years**
- **8-Pin Mini-DIP, SOIC, and 14-Lead TSSOP Packages**

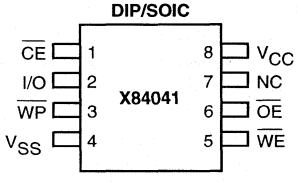
DESCRIPTION

The X84041 Micro Port Saver is a 4096-bit CMOS E²PROM designed for a direct interface to port limited microcontroller or I/O limited microprocessor designs. The X84041 provides all of the benefits of serial memories, such as low cost, low power, low voltage operation, and small package size, while featuring higher data transfer rates and reduced interface code requirements—without the need for a dedicated serial bus. The X84041 is organized as a 512 x 8, but is also suitable in 16-bit or 32-bit environments, due to the bit serial nature of the interface.

The X84041 directly connects to the processor bus and communicates over a single data line using a sequence of standard bus read and write operations. This eliminates the need for dedicated port pins, parallel to serial converters, complicated ASIC implementations, or other glue logic, lowering system cost.

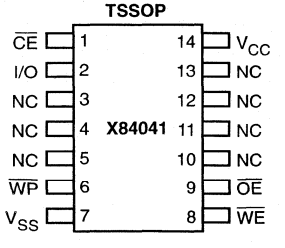
PIN CONFIGURATION

DIP/SOIC



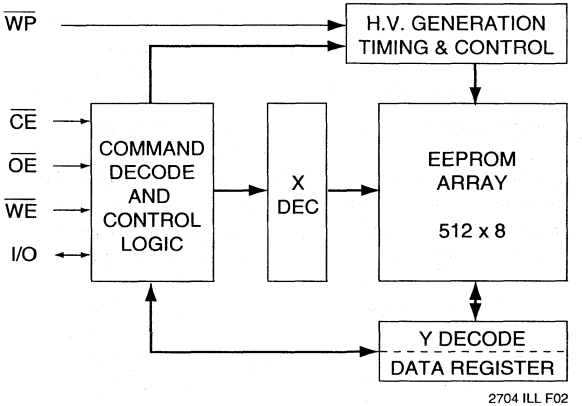
2704 ILL F01.2

TSSOP



2704 ILL F02a.1

BLOCK DIAGRAM



2704 ILL F02

PIN NAMES

I/O	Data Input/Output
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
$\overline{WP}$	Write Protect Input
V_{CC}	Supply Voltage
V_{SS}	Ground
NC	No Connect

2704 PGM T01

A Write Protect ($\overline{WP}$) pin provides hardware protection against inadvertent writes to the memory.

Xicor E^{2}PROMs are designed and tested for applications requiring extended endurance. Inherent data retention is greater than 100 years.

PIN DESCRIPTIONS

Chip Enable ($\overline{CE}$)

The Chip Enable input must be LOW to enable all read/write operations. When $\overline{CE}$ is HIGH, the chip is deselected, the I/O pin is in the high impedance state, and unless a nonvolatile write operation is underway, the X84041 is in the standby power mode.

Output Enable ($\overline{OE}$)

The Output Enable input must be LOW to enable the output buffer and to read data from the X84041 on the I/O line.

Write Enable ($\overline{WE}$)

The Write Enable input must be LOW to write either data or command sequences to the X84041.

Data In/Data Out (I/O)

Data and command sequences are serially written to or serially read from the X84041 through the I/O pin.

Write Protect ($\overline{WP}$)

When the Write Protect input is LOW, nonvolatile writes to the X84041 are disabled. When $\overline{WP}$ is HIGH, all functions, including nonvolatile writes, operate normally. If a nonvolatile write cycle is in progress, $\overline{WP}$ going LOW will have no effect on the cycle already underway, but will inhibit any additional nonvolatile write cycles.

DEVICE OPERATION

The X84041 is a serial 512 x 8 bit E^{2}PROM designed to interface directly with most microprocessor buses. Standard $\overline{CE}$, $\overline{OE}$, and $\overline{WE}$ signals control the read and write operations, and a single I/O line is used to send and receive data and commands serially.

Data Timing

Data input on the I/O line is latched on the rising edge of either $\overline{WE}$ or $\overline{CE}$, whichever occurs first. Data output on the I/O line is active whenever both $\overline{OE}$ and $\overline{CE}$ are LOW. Care should be taken to ensure that $\overline{WE}$ and $\overline{OE}$ are never both LOW while $\overline{CE}$ is LOW.

Read Sequence

A read sequence consists of sending a 16-bit address followed by the reading of data serially. The address is written by issuing 16 separate write cycles ($\overline{WE}$ and $\overline{CE}$ LOW, $\overline{OE}$ HIGH) to the part without a read cycle between the write cycles. The address is sent serially, most significant bit first, over the I/O line. Note that this sequence is fully static, with no special timing restrictions, and the processor is free to perform other tasks on the bus whenever the X84041 $\overline{CE}$ pin is HIGH. Once the 16 address bits are sent, a byte of data can be read on the I/O line by issuing 8 separate read cycles ($\overline{OE}$ and $\overline{CE}$ LOW, $\overline{WE}$ HIGH). At this point, issuing a reset sequence will terminate the read sequence, otherwise the X84041 will await further reads in the sequential read mode.

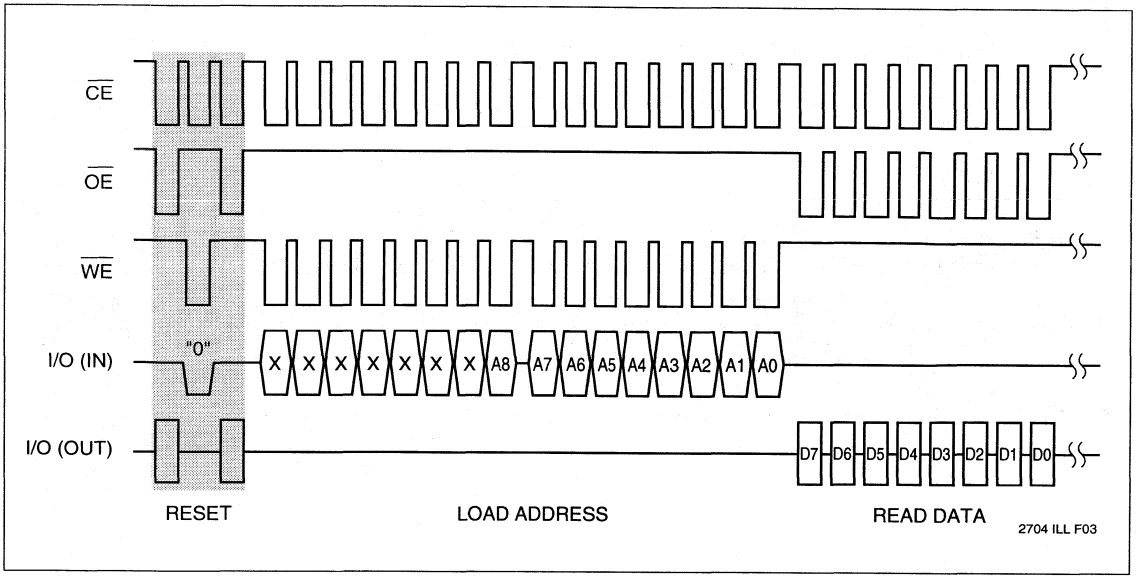
Sequential Read

The byte address is automatically incremented to the next higher address after each byte of data is read. The data stored in the memory at the next address can be read sequentially by continuing to issue read cycles. When the highest address is reached ($1FF), the address counter rolls over to address $000 and reading may be continued indefinitely.

Reset Sequence

The reset sequence resets the X84041 and sets an internal write enable latch. A reset sequence can be sent at any time by performing a read/write "0"/read sequence (see Figs. 1 and 2). This sequence breaks the multiple read or write cycle sequences that are normally used when reading from or writing to the part. This sequence can be used at any time to interrupt or end a sequential read or page load. As soon as the write "0" cycle is complete, the part is reset (unless a nonvolatile write cycle is in progress). The second read cycle in this sequence, and any further read cycles, will read a HIGH on the I/O pin until a valid read sequence is issued. The reset sequence must be issued at the beginning of both read and write sequences to be sure the X84041 initiates these operations properly.

Figure 1. Read Sequence



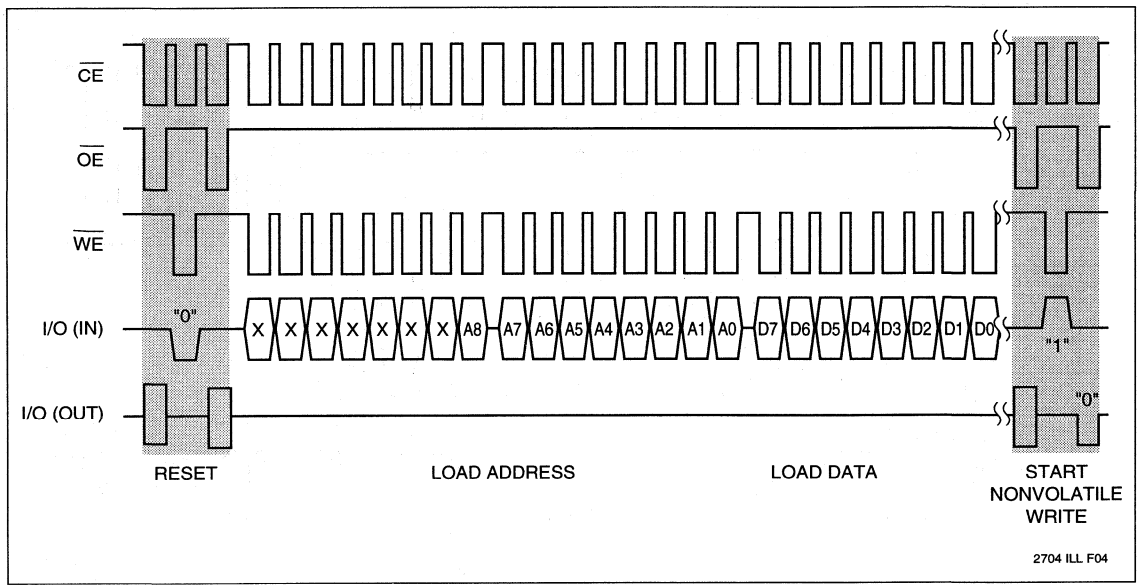
Write Sequence

A nonvolatile write sequence consists of sending a reset sequence, a 16-bit address (the first 7 of which are don't cares), up to 8 bytes of data, and then a special "start nonvolatile write cycle" command sequence. The reset sequence is issued first (as described in the Reset Sequence section) to set the internal write enable latch. The address is written serially by issuing 16 separate write cycles ($\overline{WE}$ and $\overline{CE}$ LOW, $\overline{OE}$ HIGH) to the part without any read cycles between the writes. The address is sent serially, most significant bit first, on the I/O pin. Up to eight bytes of data are written by issuing either 8, 16, 24, 32, 40, 48, 56, or 64 separate write cycles. Again, no read cycles are allowed between writes. The nonvolatile write cycle is initiated by issuing a special read/write "1"/read sequence. The first read cycle ends the page load, then the write "1" followed by a read starts the nonvolatile write cycle. The X84041 recognizes 8-byte pages beginning at addresses XXXXXX000. When sending data to the part, attempts to exceed the upper address of the page will result in the address counter "wrapping-around" to the first address on the page, where data loading can continue. For this reason, sending more than 64 consecutive data bits will result in overwriting previous data. A nonvolatile write cycle will not start if a partial or incomplete write sequence is issued. The internal write enable latch is reset when the nonvolatile write cycle is completed to prevent inadvertent writes. Note that this sequence is fully static, with no special timing restrictions. The processor is free to perform other tasks on the bus whenever the chip enable pin ($\overline{CE}$) is HIGH.

Nonvolatile Write Status

The status of a nonvolatile write cycle can be determined at any time by simply reading the state of the I/O pin on the X84041. This pin is read when $\overline{OE}$ and $\overline{CE}$ are LOW and $\overline{WE}$ is HIGH. During a nonvolatile write cycle the I/O pin is LOW. When the nonvolatile write cycle is complete, the I/O pin goes HIGH. A reset sequence can also be issued during a nonvolatile write cycle with the same result: I/O is LOW as long as a nonvolatile write cycle is in progress, and I/O is HIGH when the nonvolatile write cycle is done.

Figure 2. Write Sequence



Write Protection

The following circuitry has been included to prevent inadvertent nonvolatile writes:

— The internal Write Enable latch is reset upon power-up.

— A reset sequence must be issued to set the internal write enable latch before starting a write sequence.

— A special "start nonvolatile write" command sequence is required to start a nonvolatile write cycle.

— The internal Write Enable latch is reset automatically at the end of a nonvolatile write cycle.

— The internal Write Enable latch is reset and remains reset as long as the $\overline{WP}$ pin is LOW, which blocks all nonvolatile write cycles.

SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

ABSOLUTE MAXIMUM RATINGS*

Temperature under Bias ..... –65°C to +135°C
Storage Temperature ..... –65°C to +150°C
Terminal Voltage with
Respect to V_{SS} ..... –1V to +7V
DC Output Current 5mA
Lead Temperature (Soldering, 10 seconds) ..... 300°C

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	+70°C
Industrial	–40°C	+85°C

2704 PGM T02.2

Supply Voltage	Limits
X84041	5V ±10%
X84041 – 3	3V ±10%
X84041 – 2.7†	2.7V to 5.5V

† Contact factory for availability.

2704 PGM T03.2

D.C. OPERATING CHARACTERISTICS (V_{CC} = 5V ±10%)

(Over the recommended operating conditions, unless otherwise specified.)

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
I_{CC1}	V_{CC} Supply Current (Read)		1	mA	$\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}, I/O = Open, $\overline{CE}$ clocking @ 2MHz
I_{CC2}	V_{CC} Supply Current (Write)		3	mA	I_{CC} During Nonvolatile Write Cycle All Inputs at CMOS Levels
I_{SB}	V_{CC} Standby Current		50	µA	$\overline{CE}$ = V_{CC}, Other Inputs = V_{CC} or V_{SS} V_{CC} = 5V ±10%
I_{LI}	Input Leakage Current		10	µA	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output Leakage Current		10	µA	V_{OUT} = V_{SS} to V_{CC}
V_{IL} (1)	Input LOW Voltage	–1	V_{CC} x 0.3	V	
V_{IH} (1)	Input HIGH Voltage	V_{CC} x 0.7	V_{CC} + 0.5	V	
V_{OL}	Output LOW Voltage		0.4	V	I_{OL} = 2.1mA, V_{CC} = 5V ±10%
V_{OH}	Output HIGH Voltage	V_{CC} – 0.8		V	I_{OH} = –1mA, V_{CC} = 5V ±10%

Notes: (1) V_{IL} min. and V_{IH} max. are for reference only and are not tested.

2704 PGM T04.3

D.C. OPERATING CHARACTERISTICS (V_{CC} = 3V ±10%)

(Over the recommended operating conditions, unless otherwise specified.)

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
I_{CC1}	V_{CC} Supply Current (Read)		250	µA	$\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}, I/O = Open, $\overline{CE}$ clocking @ 2MHz
I_{CC2}	V_{CC} Supply Current (Write)		1	mA	I_{CC} During Nonvolatile Write Cycle All Inputs at CMOS Levels
I_{SB1}	V_{CC} Standby Current		10	µA	$\overline{CE}$ = V_{CC}, Other Inputs = V_{CC} or V_{SS} V_{CC} = 3V ±10%
I_{LI}	Input Leakage Current		10	µA	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output Leakage Current		10	µA	V_{OUT} = V_{SS} to V_{CC}
V_{IL}(1)	Input LOW Voltage	–1	V_{CC} x 0.3	V	
V_{IH}(1)	Input HIGH Voltage	V_{CC} x 0.7	V_{CC} + 0.5	V	
V_{OL}	Output LOW Voltage		0.4	V	I_{OL} = 1mA, V_{CC} = 3V ±10%
V_{OH}	Output HIGH Voltage	V_{CC} – 0.4		V	I_{OH} = –400µA, V_{CC} = 3V ±10%

Notes: (1) V_{IL} min. and V_{IH} max. are for reference only and are not tested.

2704 PGM T05.2

CAPACITANCE

T_A = +25°C, f = 1MHz, V_{CC} = 5V

Symbol	Parameter	Max.	Units	Test Conditions
$C_{I/O}$(2)	Input/Output Capacitance	8	pF	$V_{I/O}$ = 0V
C_{IN}(2)	Input Capacitance	6	pF	V_{IN} = 0V

Notes: (2) Periodically sampled, but not 100% tested.

2704 PGM T06.2

POWER-UP TIMING

Symbol	Parameter	Max.	Units
t_{PUR}(3)	Power-up to Read Operation	2	ms
t_{PUW}(3)	Power-up to Write Operation	5	ms

Notes: (3) Time delays required from the time the V_{CC} is stable until the specific operation can be initiated. Periodically sampled, but not 100% tested.

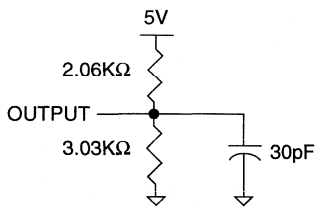
2704 PGM T07

A.C. CONDITIONS OF TEST

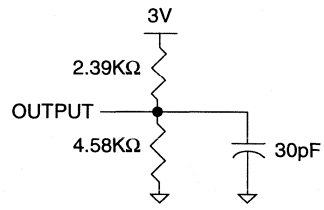
Input Pulse Levels	V_{CC} x 0.1 to V_{CC} x 0.9
Input Rise and Fall Times	5ns
Input and Output Timing Levels	V_{CC} x 0.5

2704 PGM T08.1

EQUIVALENT A.C. LOAD CIRCUITS



2704 ILL F05.2



2704 ILL F05a.3

A.C. CHARACTERISTICS

(Over the recommended operating conditions, unless otherwise specified.)

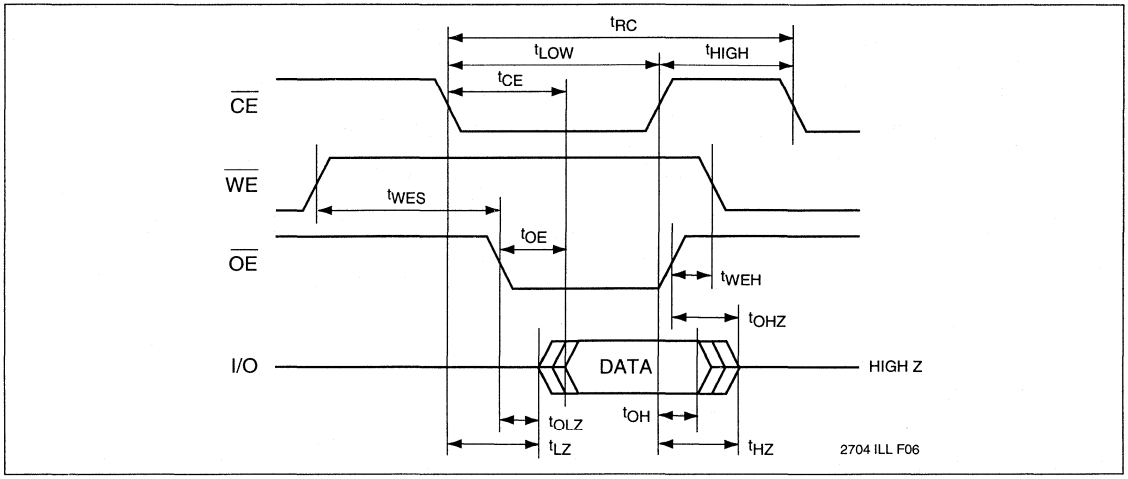
Read Cycle Limits – X84041

Symbol	Parameter	V_{CC} = 5V ±10%		V_{CC} = 3V ±10%		Units
		Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	300		300		ns
t_{CE}	$\overline{CE}$ Access Time		45		65	ns
t_{OE}	$\overline{OE}$ Access Time		45		65	ns
t_{LOW}	$\overline{CE}$ LOW Time	70		70		ns
t_{HIGH}	$\overline{CE}$ HIGH Time	70		70		ns
t_{LZ}(4)	$\overline{CE}$ LOW to Output In Low Z	0		0		ns
t_{HZ}(4)	$\overline{CE}$ HIGH to Output In High Z	0	30	0	35	ns
t_{OLZ}(4)	$\overline{OE}$ LOW to Output In Low Z	0		0		ns
t_{OHZ}(4)	$\overline{OE}$ HIGH to Output In High Z	0	30	0	35	ns
t_{OH}	Output Hold from $\overline{CE}$ or $\overline{OE}$ HIGH	0		0		ns
t_{WES}	$\overline{WE}$ HIGH Setup Time	25		25		ns
t_{WEH}	$\overline{WE}$ HIGH Hold Time	25		25		ns

Notes: (4) Periodically sampled, but not 100% tested. t_{HZ} and t_{OHZ} are measured from the point where $\overline{CE}$ or $\overline{OE}$ goes HIGH (whichever occurs first) to the time when I/O is no longer being driven into a 5pF load.

2704 PGM T09.3

Read Cycle



Write Cycle Limits – X84041

Symbol	Parameter	V_{CC} = 5V ±10%		V_{CC} = 3V ±10%		Units
		Min.	Max.	Min.	Max.	
t_{NVWC}(5)	Nonvolatile Write Cycle Time		10		10	ms
t_{WC}	Write Cycle Time	300		300		ns
t_{WP}	$\overline{WE}$ Pulse Width	30		30		ns
t_{WPH}	$\overline{WE}$ HIGH Recovery Time	200		200		ns
t_{CS}	Write Setup Time	0		0		ns
t_{CH}	Write Hold Time	0		0		ns
t_{CP}	$\overline{CE}$ Pulse Width	30		30		ns
t_{CPH}	$\overline{CE}$ HIGH Recovery Time	200		200		ns
t_{OES}	$\overline{OE}$ HIGH Setup Time	50		50		ns
t_{OEH}	$\overline{OE}$ HIGH Hold Time	50		50		ns
t_{DS}(6)	Data Setup Time	30		30		ns
t_{DH}(6)	Data Hold Time	5		5		ns
t_{WPCS}(7)	$\overline{WP}$ HIGH Before $\overline{CE}$	500		500		ns
t_{WPCH}(7)	$\overline{WP}$ HIGH After $\overline{CE}$	500		500		ns
t_{WPWS}(7)	$\overline{WP}$ HIGH Before $\overline{WE}$	500		500		ns
t_{WPWH}(7)	$\overline{WP}$ HIGH After $\overline{WE}$	500		500		ns

Notes: (5) t_{NVWC} is the time from the falling edge of $\overline{OE}$ or $\overline{CE}$ (whichever occurs last) of the second read cycle in the "start nonvolatile write cycle" sequence until the self-timed, internal nonvolatile write cycle is completed.
(6) Data is latched into the X84041 on the rising edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs first.
(7) Periodically sampled, but not 100% tested.

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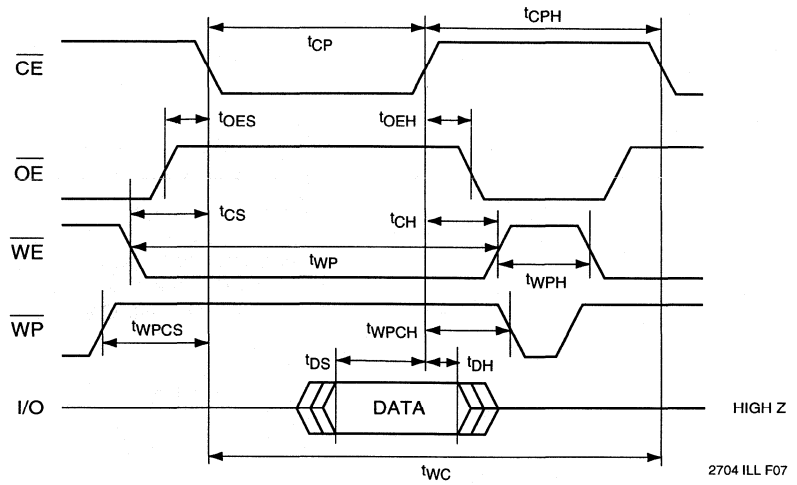
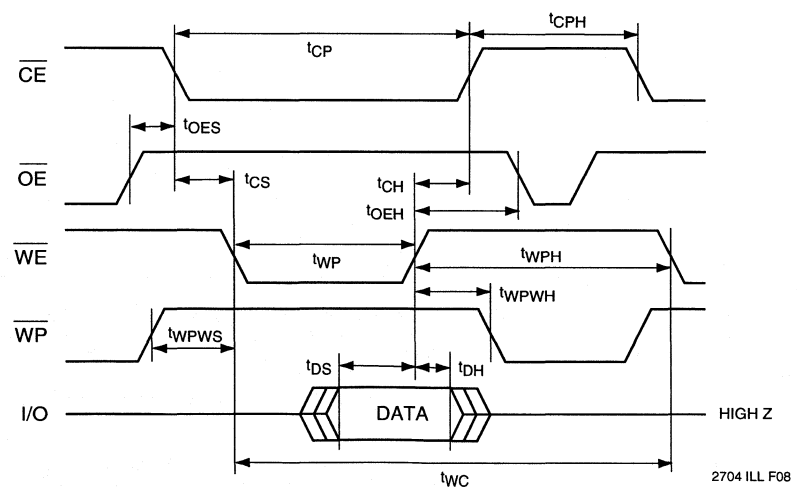
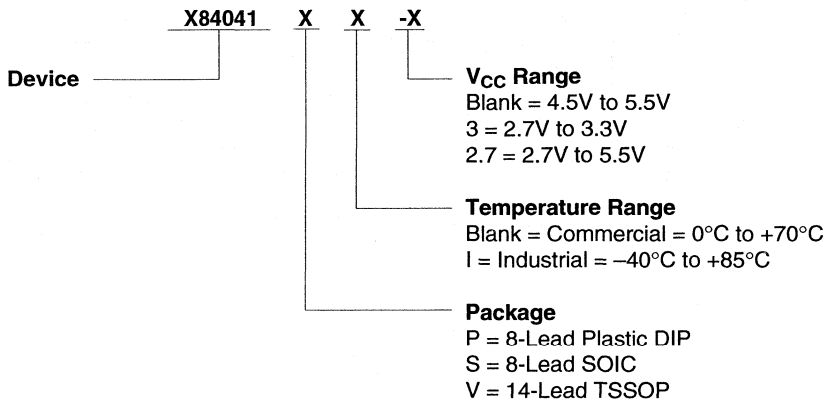
$\overline{CE}$ Controlled Write Cycle



$\overline{WE}$ Controlled Write Cycle



ORDERING INFORMATION



SerialFlash™ Memory with Block Lock™ Protection

FEATURES

- 1.8V to 3.6V and 5V "Univolt" Read and Program Power Supply
- Low Power CMOS
  - —Active Read Current Less Than 1mA
  - —Active Program Current Less Than 3mA
  - —Standby Current Less Than 1μA
- Internally Organized 1K/2K/4K/8K x 8
- New Programmable Block Lock Protection
  - —Software Write Protection
  - —Programmable hardware Write Protect
- Block Lock (0, 1/4, 1/2, or all of the Flash Memory array)
- 2 Wire Serial Interface
- Bidirectional Data Transfer Protocol
- 32 Byte Sector Programming
- Self Timed Program Cycle
  - —Typical Programming Time of 5ms Per Sector
- High Reliability
  - —Endurance: 100,000 cycles per byte
  - —Data Retention: 100 Years
- Available Packages
  - —8-Lead Mini-DIP
  - —8-Lead SOIC (JEDEC)
  - —14-Lead TSSOP (X24F008/016/032)
  - —20-Lead TSSOP (X24F064)

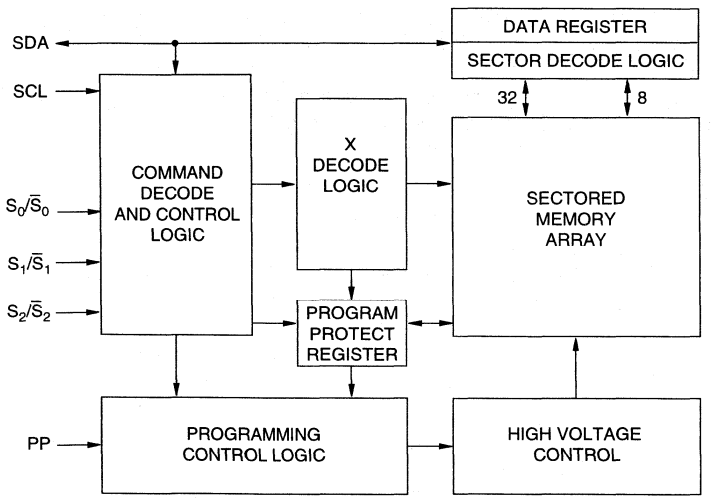
DESCRIPTION

The X24F008/016/032/064 is a CMOS SerialFlash Memory Family, internally organized 1K/2K/4K/8K x 8. The family features a serial interface and software protocol allowing operation on a simple two wire bus.

Device select inputs (S_0, S_1, S_2) allow up to eight devices to share a common two wire bus.

A Program Protect Register at the highest address location, provides three new programming protection features: Software Programming Protection, Block Lock Protection, and Hardware Programming Protection. The Software Programming Protection feature prevents any nonvolatile writes to the device until the WEL bit in the program protect register is set. The Block Lock™ Protection feature allows the user to individually protect four blocks of the array by programming two bits in the programming protect register. The Programmable Hardware Program Protect feature allows the user to install each device with PP tied to V_{CC}, program the entire memory array in place, and then enable the hardware programming protection by programming a PPEN bit in the program protect register. After this, selected blocks of the array, including the program protect register itself, are permanently protected from being programmed.

FUNCTIONAL DIAGRAM



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Xicor SerialFlash Memories are designed and tested for applications requiring extended endurance. Inherent data retention is greater than 100 years.

PIN DESCRIPTIONS

Serial Clock (SCL)

The SCL input is used to clock all data into and out of the device.

Serial Data (SDA)

SDA is a bidirectional pin used to transfer data into and out of the device. It is an open drain output and may be wire-ORed with any number of open drain or open collector outputs.

An open drain output requires the use of a pull-up resistor. For selecting typical values, refer to the pull-up resistor selection graph at the end of this data sheet.

Device Select (S_0, $\overline{S}_0$, S_1, $\overline{S}_1$, S_2, $\overline{S}_2$)

The device select inputs are used to set the device select bits of the 8-bit slave address. This allows multiple devices to share a common bus. These inputs can be static or actively driven. If used statically they must be tied to V_{SS} or V_{CC} as appropriate. If actively driven, they must be driven with CMOS levels (driven to V_{CC} or V_{SS}).

Program Protect (PP)

The program protect input controls the hardware program protect feature. When held LOW, hardware program protection is disabled and the X24F008/016/032/064 can be programmed normally. When this input is held HIGH, and the PPEN bit in the program protect register is set HIGH, program protection is enabled, and nonvolatile writes are disabled to the selected blocks as well as the program protect register itself.

PIN NAMES

Symbol	Description
S_0, $\overline{S}_0$, S_1, $\overline{S}_1$, S_2, $\overline{S}_2$	Device Select Inputs
SDA	Serial Data
SCL	Serial Clock
PP	Program Protect
V_{SS}	Ground
V_{CC}	Supply Voltage
NC	No Connect

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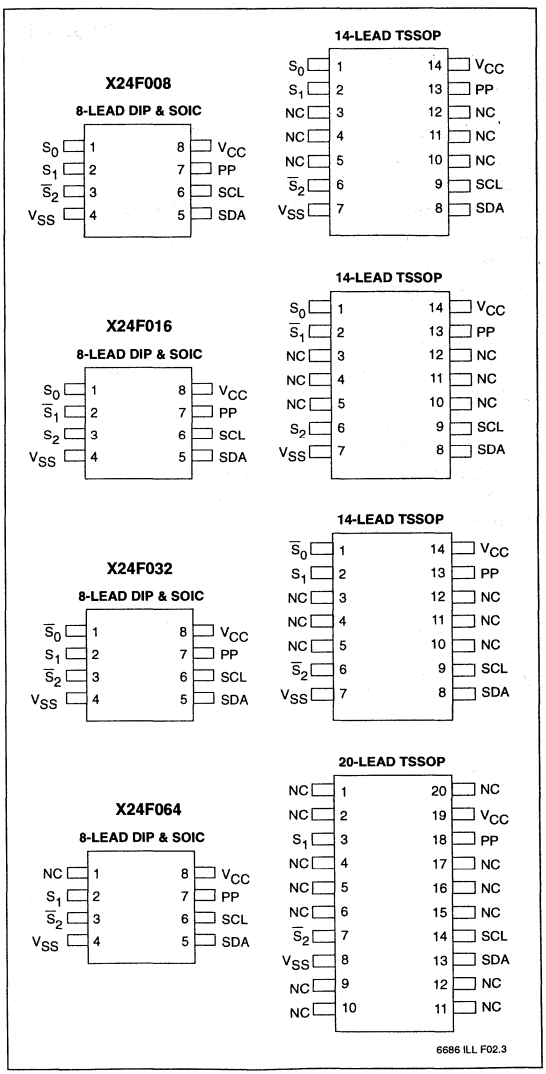
PIN CONFIGURATION



DEVICE OPERATION

The X24F008/016/032/064 supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter, and the receiving device as the receiver. The device controlling the transfer is a master and the device being controlled is the slave. The master will always initiate data transfers, and provide the clock for both transmit and receive operations. Therefore, the X24F008/016/032/064 will be considered a slave in all applications.

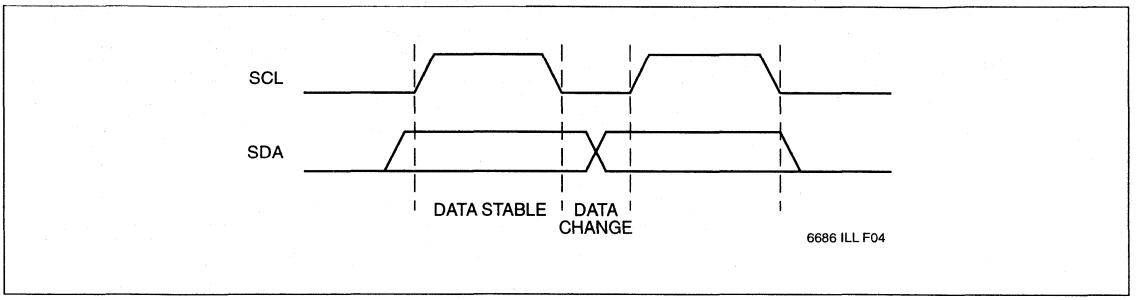
Clock and Data Conventions

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions. Refer to Figures 1 and 2.

Start Condition

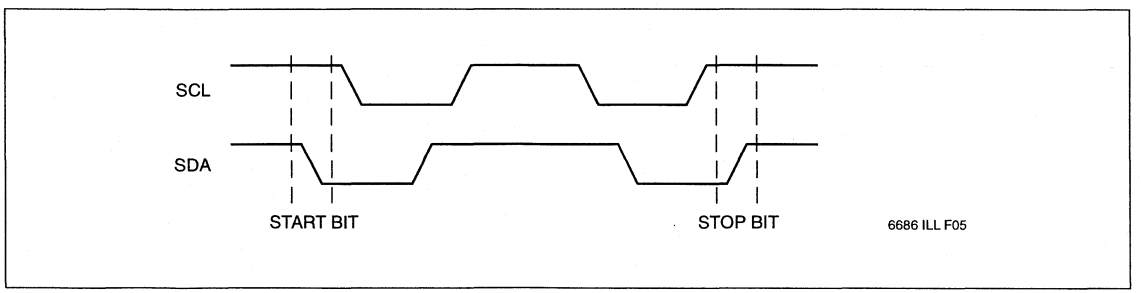
All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The X24F008/016/032/064 continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

Figure 1. Data Validity



Notes: (5) Typical values are for $T_A = 25°C$ and nominal supply voltage (2.7V)
(6) t_{PR} is the minimum cycle time from the system perspective when polling techniques are not used. It is the maximum time the device requires to perform the internal program operation.

Figure 2. Definition of Start and Stop



Stop Condition

All communications must be terminated by a stop condition, which is a LOW to HIGH transition of SDA when SCL is HIGH. The stop condition is also used to place the device into the standby power mode after a read sequence. A stop condition can only be issued after the transmitting device has released the bus.

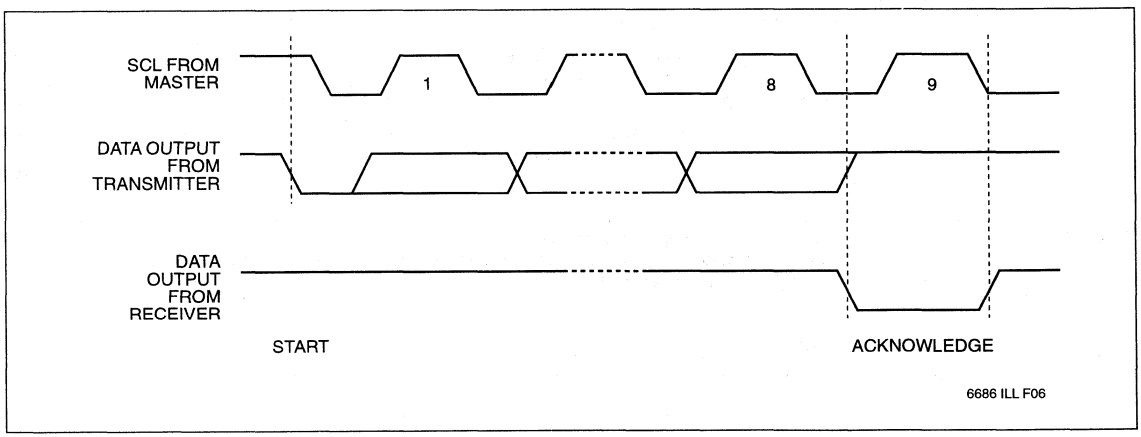
Acknowledge

Acknowledge is a software convention used to indicate successful data transfer. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data. Refer to Figure 3.

The X24F008/016/032/064 will respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a write operation have been selected, the X24F008/016/032/064 will respond with an acknowledge after the receipt of each subsequent eight-bit word.

In the read mode the X24F008/016/032/064 will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the X24F008/016/032/064 will continue to transmit data. If an acknowledge is not detected, the device will terminate further data transmissions. The master must then issue a stop condition to return the X24F008/016/032/064 to the standby power mode and place the device into a known state.

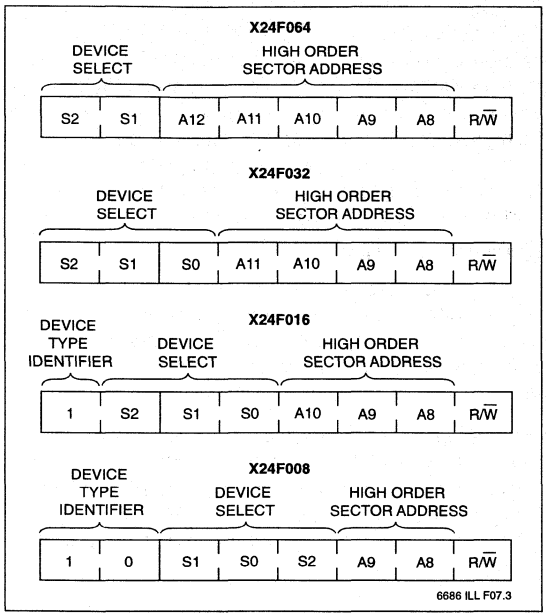
Figure 3. Acknowledge Response From Receiver



DEVICE ADDRESSING

Following a start condition the master must output the address of the slave it is accessing (see Figure 4). The next two bits are the device select bits. A system could have up to eight X24F008/016/032's on the bus or up to four 24F064's on the bus. The device addresses are defined by the state of the S_0, S_1, and S_2 inputs. Note some of the slave addresses must be the inverse of the corresponding input pin.

Figure 4. Slave Address



Also included in the slave address is an extension of the array's address which is concatenated with the eight bits of address in the sector address field, providing direct access to the entire SerialFlash Memory array.

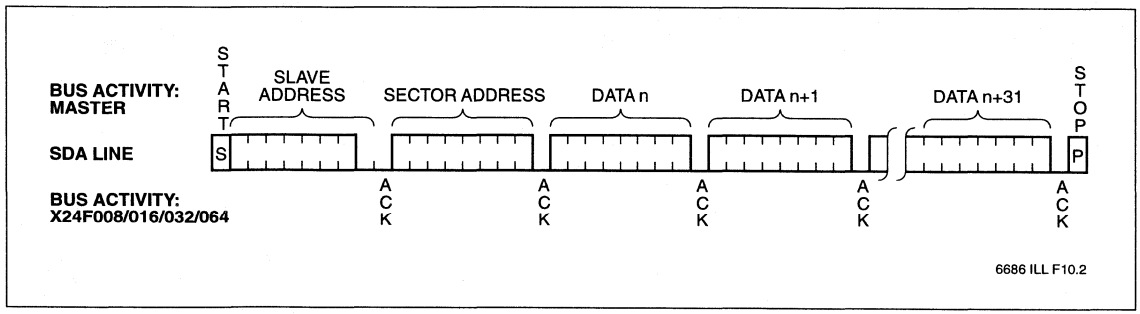
The last bit of the slave address defines the operation to be performed. When set HIGH a read operation is selected, when set LOW a program operation is selected.

Following the start condition, the X24F008/016/032/064 monitors the SDA bus comparing the slave address being transmitted with its slave address device type identifier. Upon a correct comparison of the device select inputs, the X24F008/016/032/064 outputs an acknowledge on the SDA line. Depending on the state of the R/$\overline{W}$ bit, the X24F008/016/032/064 will execute a read or program operation.

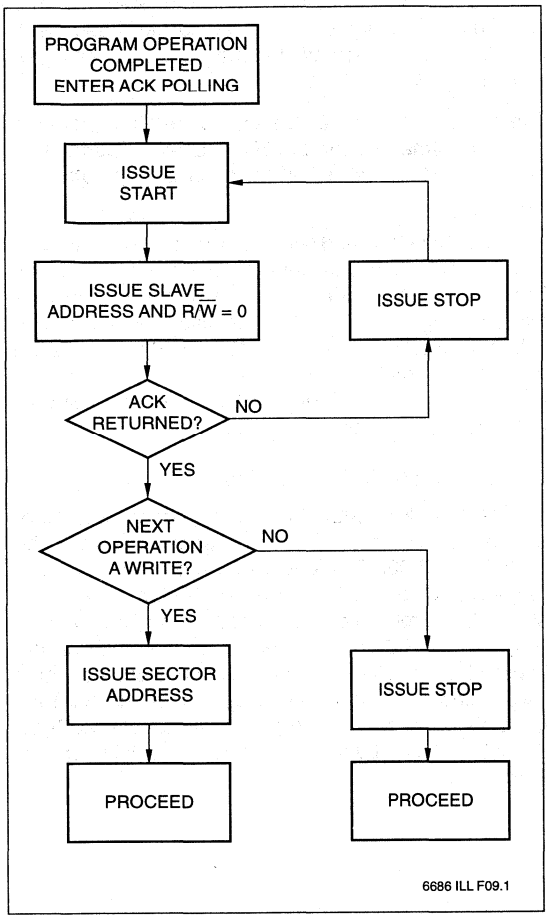
PROGRAMMING OPERATIONS

The X24F008/016/032/064 offers a 32-byte sector programming operation. For a program operation, the X24F008/016/032/064 requires a second address field. This field contains the address of the first byte in the sector. Upon receipt of the address, comprised of eight bits, the X24F008/016/032/064 responds with an acknowledge and awaits the next eight bits of data, again responding with an acknowledge. The master then transmits 31 more bytes. After the receipt of each byte, the X24F008/016/032/064 will respond with an acknowledge.

Figure 5. Sector Programming



Flow 1. ACK Polling Sequence



After the receipt of each byte, the five low order address bits are internally incremented by one. The high order bits of the sector address remain constant. If the master should transmit more or less than 32 bytes prior to generating the stop condition, the contents of the sector cannot be guaranteed. All inputs are disabled until completion of the internal program cycle. Refer to Figure 5 for the address, acknowledge and data transfer sequence.

Acknowledge Polling

The 10ms Max Write Cycle Time (5ms Typical) can be significantly reduced using Acknowledge Polling. To initiate Acknowledge Polling, the master issues a start condition followed by the Slave Address Byte for a write or read operation. If the device is still busy with the high voltage cycle, then no ACK will be returned. If the device has completed the write operation, an ACK will be returned and the host can then proceed with the read or write operation. Refer to Flow 1.

READ OPERATIONS

Read operations are initiated in the same manner as program operations with the exception that the R/$\overline{W}$ bit of the slave address is set HIGH. There are three basic read operations: current address read, random read and sequential read.

It should be noted that the ninth clock cycle of the read operation is not a "don't care." To terminate a read operation, the master must either issue a stop condition during the ninth cycle or hold SDA HIGH during the ninth clock cycle and then issue a stop condition.

Current Address Read

Internally, the X24F008/016/032/064 contains an address counter that maintains the address of the last byte read, incremented by one byte. Therefore, if the last read was from address n, the next read operation accesses data from address n + 1. Upon receipt of the slave address with the R/$\overline{W}$ set HIGH, the X24F008/016/032/064 issues an acknowledge and transmits the eight-bit word. The read operation is terminated by the master; by not responding with an acknowledge and by issuing a stop condition. Refer to Figure 6 for the sequence of address, acknowledge and data transfer.

Random Read

Random read operations allow the master to access any memory location in a random manner. Prior to issuing the slave address with the R/$\overline{W}$ bit set HIGH, the master must first perform a "dummy" write operation. The master issues the start condition, and the slave address with the R/$\overline{W}$ bit set LOW, followed by the byte address it is to read. After the byte address acknowledge, the master immediately reissues the start condition and the slave address with the R/$\overline{W}$ bit set HIGH. This will be followed by an acknowledge from the X24F008/016/032/064 and then by the eight-bit byte. The read operation is terminated by the master; by not responding with an acknowledge and by issuing a stop condition. Refer to Figure 7 for the address, acknowledge and data transfer sequence.

Figure 6. Current Address Read

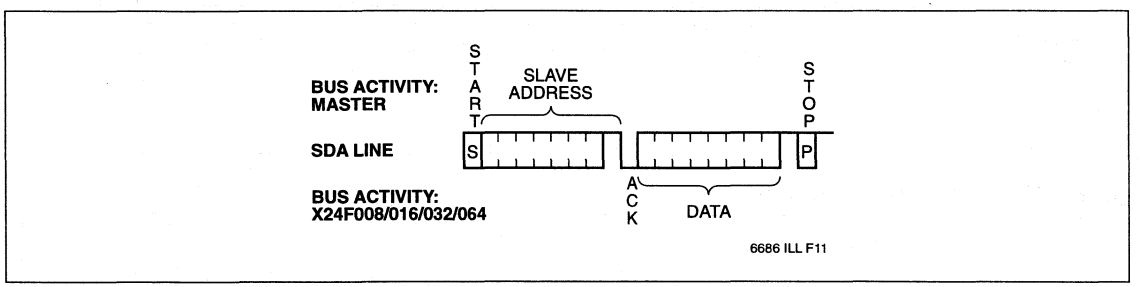
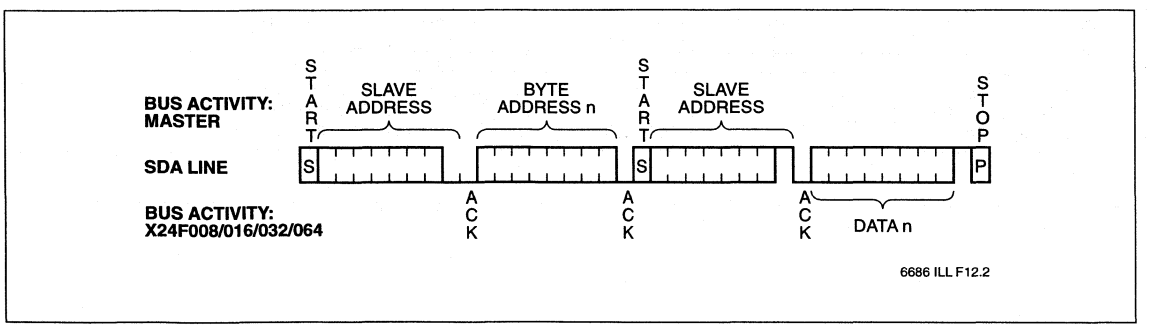


Figure 7. Random Read



Sequential Read

Sequential reads can be initiated as either a current address read or random access read. The first byte is transmitted as with the other modes, however, the master now responds with an acknowledge, indicating it requires additional data. The X24F008/016/032/064 continues to output data for each acknowledge received. The read operation is terminated by the master; by not responding with an acknowledge and then issuing a stop condition.

The data output is sequential, with the data from address n followed by the data from n + 1. The address counter for read operations increments all address bits, allowing the entire memory contents to be serially read during one operation. At the end of the address space, the counter "rolls over" to 0 and the X24F008/016/032/064 continues to output data for each acknowledge received. Refer to Figure 8 for the address, acknowledge and data transfer sequence.

Figure 8. Sequential Read

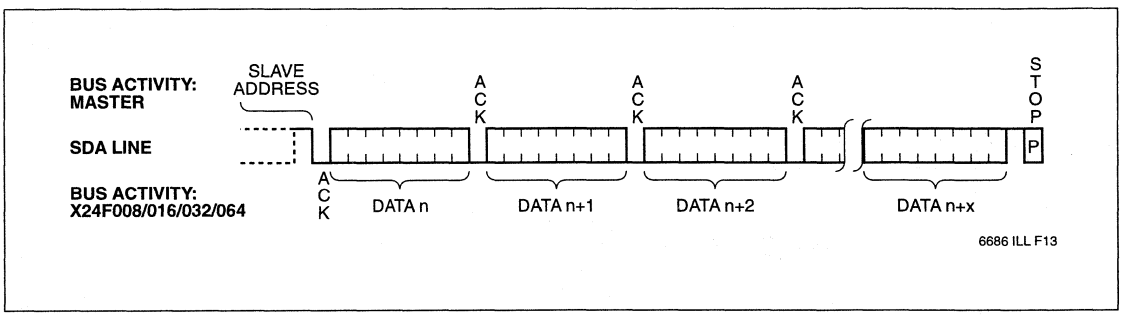
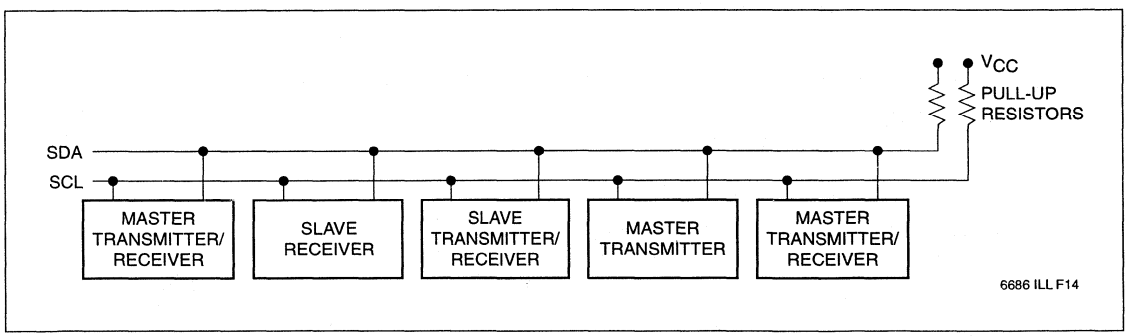


Figure 9. Typical System Configuration



PROGRAM PROTECT REGISTER

The Program Protect Register (PPR) is located at the highest address of each device:

X24F008 = 03FF
X24F016 = 07FF
X24F032 = 0FFF
X24F064 = 1FFF

Figure 10. Program Protect Register

7	6	5	4	3	2	1	0
PPEN	0	0	BL1	BL0	RWEL	WEL	0

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PPR.1 = WEL

– Write Enable Latch (Volatile)
0 = Write enable latch reset, programming disabled
1 = Write enable latch set, programming enabled

If WEL = 0 then "no ACK" after first byte of input data.

PPR.2 = RWEL
– Register Write Enable Latch (Volatile)
0 = Register write enable latch reset, programming disabled
1 = Register write enable latch set, programming enabled

PPR.3, PPR.4 = BL0, BL1
– Block Lock Bits (Nonvolatile)
(See Block Lock Bits section for definition)

PPR.7 = PPEN
– Programming Protect Enable Bit (Nonvolatile)
(See Programmable Hardware Program Protect section for definition)

Writing to the Program Protect Register

The Program Protect Register is written by performing a write of one byte directly to the highest address location. During normal Sector Programming, the byte in the array at the highest address will be written instead of the Program Protect Register (assuming programming is not disabled by the Block Lock register).

The state of the Program Protect Register can be read by performing a random read at the highest address location at any time. If a sequential read starting at any other address than the highest address location is performed, the contents of the byte in the array at the highest address location is read out instead of the Program Protect Register.

WEL and RWEL are volatile latches that power-up in the LOW (disabled) state. A write to any address other than the highest address location, where the Program Protect Register is located, will be ignored (no ACK) until the WEL bit is set HIGH. The WEL bit is set by writing 0000001x to the highest address location. Once set, WEL remains HIGH until either reset (by writing 00000000 to the highest address location) or until the part powers-up again. The RWEL bit controls writes to the Block Lock bits. RWEL is set by first setting WEL = 1 and then writing 0000011x to the highest address location. RWEL must be set in order to change the Block Lock bits (BL0 and BL1) or the PPEN bit. RWEL is reset when the Block Lock or PPEN bits are changed, or when the part powers-up again.

Programming the BL or PPEN Bits

A three step sequence is required to change the nonvolatile Block Lock or Program Protect Enable:

1) Set WEL = 1 (write 00000010 to the highest address location, volatile write cycle)

(Start)

2) Set RWEL = 1 (write 00000110 to the highest address location, volatile write cycle)

(Start)

3) Set BL1, BL0, and/or PPEN bits (Write w00yz010 to the highest address location)

w = PPEN, y = BL1, Z = BL0,

(Stop)

Step 3 is a nonvolatile program cycle, requiring 10ms to complete. RWEL is reset (0) by this program cycle, requiring another program cycle to set RWEL again before the Block Lock bits can be changed. RWEL must be 0 in step 3; if w00yz110 is written to the highest address location, RWEL is set but PPEN, BL1 and BL0 are not changed (the device remains at step 2).

Block Lock Bits

The Block Lock Bits BL0 and BL1 determine which blocks of the memory are write-protected:

Table 1. Block Lock Bits

BL1	BL0	Array Locked
0	0	None
0	1	Upper 1/4
1	0	Upper 1/2
1	1	Full Array (WPR not included)

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Programmable Hardware Program Protect

The Program Protect (PP) pin and the Program Protect Enable (PPEN) bit in the Program Protect Register control the programmable hardware program protect feature. Hardware program protection is enabled when the PP pin and the PPEN bit are both HIGH, and disabled when either the PP pin is LOW or the PPEN bit is LOW. When the chip is hardware program-protected, nonvolatile programming is disabled, including the Program Protect Register, the BL bits and the PPEN bit itself, as well as to Block Locked sections in the memory array. Only the sections of the memory array that are not Block Locked can be written. Note that since the PPEN bit is program-protected, it cannot be changed back to a LOW state, and program protection is disabled as long as the PP pin is held HIGH. Table 2 defines the program protection status for each state of PPEN and PP.

Table 2. Program Protect Status Table

PP	PPEN	Memory Array (Not Block Locked)	Memory Array (Block Locked)	BL Bits	PPEN Bit
0	X	Programmable	Locked	Programmable	Programmable
X	0	Programmable	Locked	Programmable	Programmable
1	1	Programmable	Locked	Locked	Locked

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ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias
X24F008/016/032/064 ..... –65°C to +135°C
Storage Temperature..... –65°C to +150°C
Voltage on any Pin with
Respect to V_{SS}..... –1V to +7V
D.C. Output Current..... 5mA
Lead Temperature (Soldering, 10 Seconds)..... 300°C

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	+70°C
Industrial	–40°C	+85°C

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Supply Voltage	Limits
X24F008/016/032/064	1.8V to 3.6V
X24F008/016/032/064–5	4.5V to 5.5V

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D.C. OPERATING CHARACTERISTICS (Over the recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
I_{CC1}	V_{CC} Supply Current (Read)		1	mA	SCL = V_{CC} X 0.1/V_{CC} X 0.9 Levels @ 100KHz, SDA = Open, All Other Inputs = V_{SS} or V_{CC} – 0.3V
I_{CC2}	V_{CC} Supply Current (Write)		3	mA	
I_{SB1}(1)	V_{CC} Standby Current		1	µA	SCL = SDA = V_{CC}, All Other Inputs = V_{SS} or V_{CC} – 0.3V, V_{CC} = 3.6V
I_{SB2}(1)	V_{CC} Standby Current		10	µA	SCL = SDA = V_{CC}, All Other Inputs = V_{SS} or V_{CC} – 0.3V, V_{CC} = 5V ±10%
I_{LI}	Input Leakage Current		10	µA	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output Leakage Current		10	µA	V_{OUT} = V_{SS} to V_{CC}
V_{IL}(2)	Input LOW Voltage	–1	V_{CC} x 0.3	V	
V_{IH}(2)	Input HIGH Voltage	V_{CC} x 0.7	V_{CC} + 0.5	V	
V_{OL}	Output LOW Voltage		0.4	V	I_{OL} = 3mA

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CAPACITANCE T_A = +25°C, f = 1MHz, V_{CC} = 2.7V

Symbol	Parameter	Max.	Units	Test Conditions
$C_{I/O}$(3)	Input/Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}(3)	Input Capacitance (S_1, $\overline{S_2}$, SCL)	6	pF	V_{IN} = 0V

6686 FRM T07

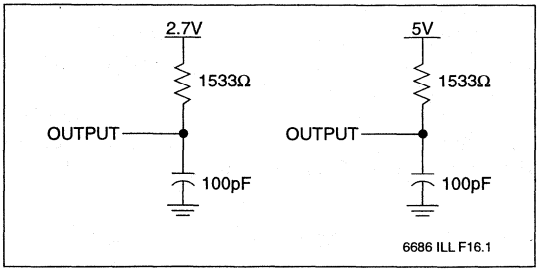
Notes: (1) Must perform a stop command prior to measurement.
(2) V_{IL} min. and V_{IH} max. are for reference only and are not 100% tested.
(3) This parameter is periodically sampled and not 100% tested.

A.C. CONDITIONS OF TEST

Input Pulse Levels	V_{CC} x 0.1 to V_{CC} x 0.9
Input Rise and Fall Times	10ns
Input and Output Timing Levels	V_{CC} X 0.5

6686 FRM T08

EQUIVALENT A.C. LOAD CIRCUIT



6686 ILL F16.1

A.C. OPERATING CHARACTERISTICS (Over the recommended operating conditions, unless otherwise specified.)

Read & Write Cycle Limits

Symbol	Parameter	Min.	Max.	Units
f_{SCL}	SCL Clock Frequency	0	100	KHz
T_I	Noise Suppression Time Constant at SCL, SDA Inputs		100	ns
t_{AA}	SCL LOW to SDA Data Out Valid	0.3	3.5	µs
t_{BUF}	Time the Bus Must Be Free Before a New Transmission Can Start	4.7		µs
$t_{HD:STA}$	Start Condition Hold Time	4		µs
t_{LOW}	Clock LOW Period	4.7		µs
t_{HIGH}	Clock HIGH Period	4		µs
$t_{SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	4.7		µs
$t_{HD:DAT}$	Data In Hold Time	0		µs
$t_{SU:DAT}$	Data In Setup Time	250		ns
t_R	SDA and SCL Rise Time		1	µs
t_F	SDA and SCL Fall Time		300	ns
$t_{SU:STO}$	Stop Condition Setup Time	4.7		µs
t_{DH}	Data Out Hold Time	300		ns

6686 FRM T09.1

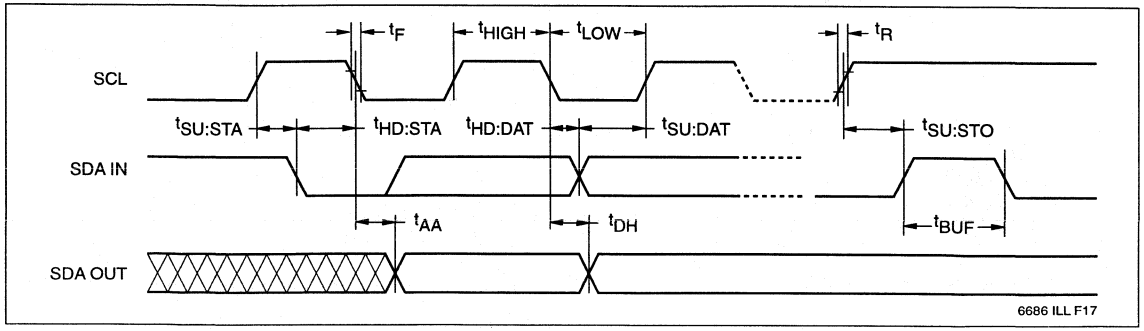
POWER-UP TIMING(4)

Symbol	Parameter	Max.	Units
t_{PUR}	Power-up to Read Operation	1	ms
t_{PUW}	Power-up to Write Operation	5	ms

6686 FRM T10

Notes: (4) t_{PUR} and t_{PUW} are the delays required from the time V_{CC} is stable until the specified operation can be initiated. These parameters are periodically sampled and not 100% tested.

Bus Timing



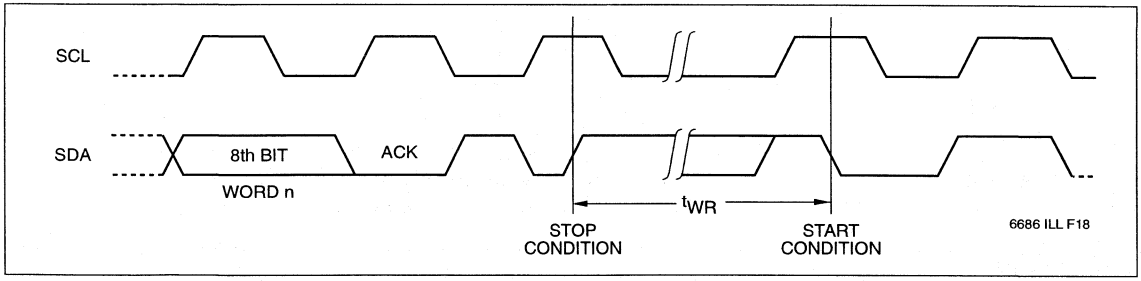
Program Cycle Limits

Symbol	Parameter	Min.	Typ.(5)	Max.	Units
t_{PR}(6)	Program Cycle Time		5	10	ms

6686 FRM T11.1

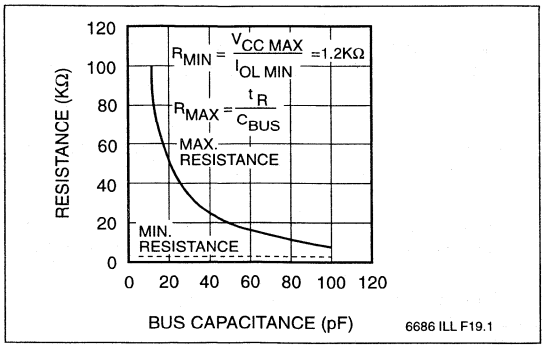
The program cycle time is the time from a valid stop condition of a write sequence to the end of the internal erase/program cycle. During the program cycle, the X24F008/016/032/064 bus interface circuits are disabled, SDA is allowed to remain HIGH, and the device does not respond to its slave address.

Bus Timing



Notes: (5) Typical values are for $T_A = 25°C$ and nominal supply voltage (2.7V).
(6) t_{WR} is the minimum cycle time to be allowed from the system perspective unless polling techniques are used. It is the maximum time the device requires to automatically complete the internal program operation.

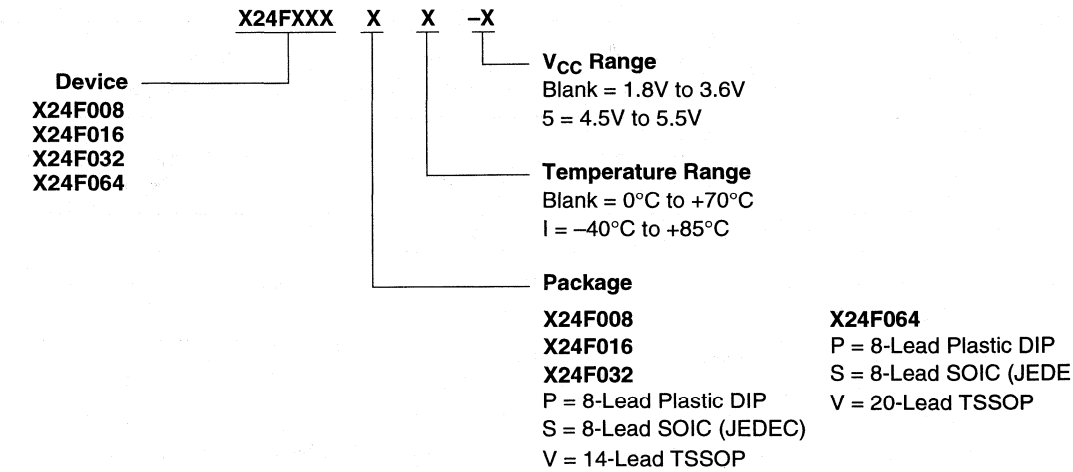
Guidelines for Calculating Typical Values of Bus Pull-Up Resistors



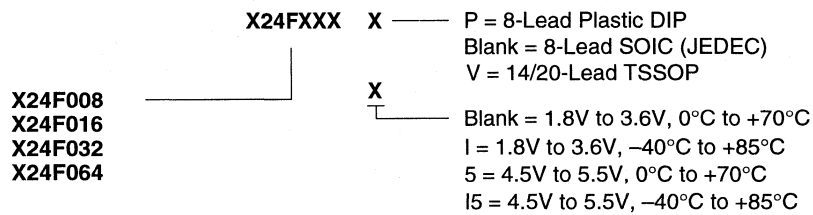
SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

ORDERING INFORMATION



Part Mark Convention



X25F008/016/032/064

SerialFlash™ Memory With Block Lock™ Protection

FEATURES

- 1MHz Clock Rate
- SPI Serial Interface
- 8K/16K/32K/64K Bits
  - —32 Byte Small Sector Program Mode
- Low Power CMOS
  - —<1μA Standby Current
  - —<5mA Active Current
- 1.8V – 3.6V and 5V "Univolt" Read and Program Power Supply
- Block Lock Protection
  - —Protect 1/4, 1/2, or all of E²PROM Array
- Built-in Inadvertent Program Protection
  - —Power-Up/Power-Down protection circuitry
  - —Program Enable Latch
  - —Program Protect Pin
- Self-Timed Program Cycle
  - —5ms Program Cycle Time (Typical)
- High Reliability
  - —Endurance: 100,000 cycles per byte
  - —Data Retention: 100 Years
  - —ESD protection: 2000V on all pins
- 8-Pin Mini-DIP Package
- 8-Lead 150 mil SOIC Packages
- 8K, 16K, 32K available in 14-Lead TSSOP, 64K available in 20-Lead TSSOP

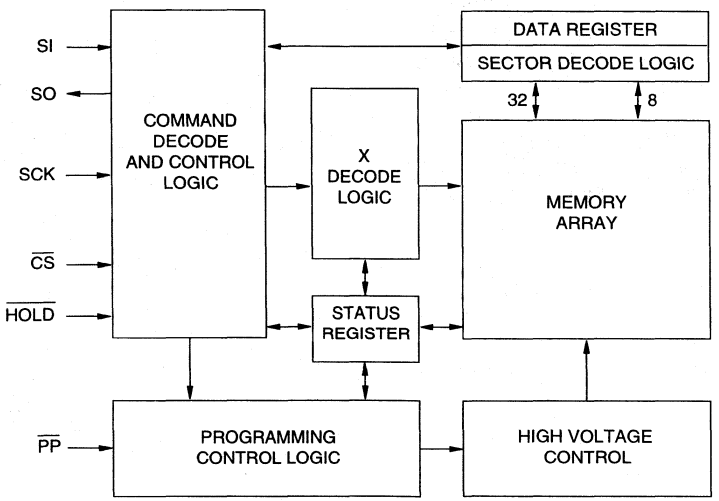
DESCRIPTION

The X25F008/016/032/064 family are 8/16/32/64K-bit CMOS SerialFlash memory, internally organized X 8. They feature a "Univolt" Program and Read voltage, Serial Peripheral Interface (SPI), and software protocol allowing operation on a simple three-wire bus. The bus signals are a clock input (SCK), plus separate data in (SI) and data out (SO) lines. Access to the device is controlled through a chip select ($\overline{CS}$) input, allowing any number of devices to share the same bus.

The X25F008/016/032/064 also features two additional inputs that provide the end user with added flexibility. By asserting the $\overline{HOLD}$ input, the X25F008/016/032/064 will ignore transitions on its inputs, thus allowing the host to service higher priority interrupts. The $\overline{PP}$ input can be used as a hardwire input to the X25F008/016/032/064 disabling all program attempts to the status register, thus providing a mechanism for limiting end user capability of altering 0, 1/4, 1/2, or all of the memory.

The X25F008/016/032/064 utilizes Xicor's proprietary flash cell, providing a minimum endurance of 100,000 cycles and a minimum data retention of 100 years.

FUNCTIONAL DIAGRAM



6685 ILL F01.4

SerialFlash™ and Block Lock™ Protection are trademarks of Xicor, Inc.

PIN DESCRIPTIONS

Serial Output (SO)

SO is a push-pull serial data output pin. During a read cycle, data is shifted out on this pin. Data is clocked out by the falling edge of the serial clock.

Serial Input (SI)

SI is the serial data input pin. All opcodes, byte addresses, and data to be written to the memory are input on this pin. Data is latched by the rising edge of the serial clock.

Serial Clock (SCK)

The Serial Clock controls the serial bus timing for data input and output. Opcodes, addresses, or data present on the SI pin are latched on the rising edge of the clock input, while data on the SO pin change after the falling edge of the clock input.

Chip Select ($\overline{CS}$)

When $\overline{CS}$ is HIGH, the X25F008/016/032/064 is deselected and the SO output pin is at high impedance and unless an internal program operation is underway the X25F008/016/032/064 will be in the standby power mode. $\overline{CS}$ LOW enables the X25F008/016/032/064, placing it in the active power mode. It should be noted that after power-up, a HIGH to LOW transition on $\overline{CS}$ is required prior to the start of any operation.

Program Protect ($\overline{PP}$)

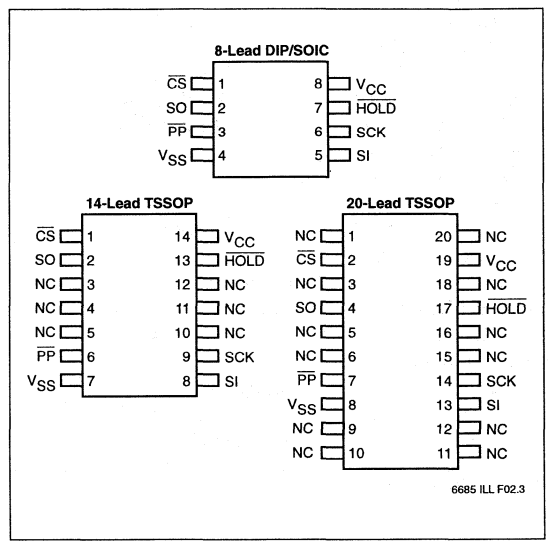
When $\overline{PP}$ is LOW and the nonvolatile bit PPEN is "1", nonvolatile programming of the X25F008/016/032/064 status register is disabled, but the part otherwise functions normally. When $\overline{PP}$ is held HIGH, all functions, including nonvolatile programming operate normally. $\overline{PP}$ going LOW while $\overline{CS}$ is still LOW will interrupt programming of the X25F008/016/032/064 status register. If the internal program cycle has already been initiated, $\overline{PP}$ going LOW will have no effect on programming.

The $\overline{PP}$ pin function is blocked when the PPEN bit in the status register is "0". This allows the user to install the X25F008/016/032/064 into a system with $\overline{PP}$ pin grounded and still be able to program the status register. The $\overline{PP}$ pin functions will be enabled when the PPEN bit is set "0".

Hold ($\overline{HOLD}$)

$\overline{HOLD}$ is used in conjunction with the $\overline{CS}$ pin to select the device. Once the part is selected and a serial sequence is underway, $\overline{HOLD}$ may be used to pause the serial communication with the controller without resetting the serial sequence. To pause, $\overline{HOLD}$ must be brought LOW while SCK is LOW. To resume communication, $\overline{HOLD}$ is brought HIGH, again while SCK is LOW. If the pause feature is not used, $\overline{HOLD}$ should be held HIGH at all times.

PIN CONFIGURATION



PIN NAMES

SYMBOL	DESCRIPTION
$\overline{CS}$	Chip Select Input
SO	Serial Output
SI	Serial Input
SCK	Serial Clock Input
$\overline{PP}$	Program Protect Input
V_{SS}	Ground
V_{CC}	Supply Voltage
$\overline{HOLD}$	Hold Input
NC	No Connect

6685 PGM T01.1

PRINCIPLES OF OPERATION

The X25F008/016/032/064 family are SerialFlash Memory designed to interface directly with the synchronous serial peripheral interface (SPI) of many popular microcontroller families.

The X25F008/016/032/064 family contains an 8-bit instruction register. It is accessed via the SI input, with data being clocked in on the rising SCK. $\overline{CS}$ must be LOW and the $\overline{HOLD}$ and $\overline{PP}$ inputs must be HIGH during the entire operation. The $\overline{PP}$ input is "Don't Care" if PPEN is set "0".

Table 1 contains a list of the instructions and their operation codes. All instructions, addresses and data are transferred MSB first.

Data input is sampled on the first rising edge of SCK after $\overline{CS}$ goes LOW. SCK is static, allowing the user to stop the clock and then resume operations. If the clock line is shared with other peripheral devices on the SPI bus, the user can assert the $\overline{HOLD}$ input to place the X25F008/016/032/064 into a "PAUSE" condition. After releasing $\overline{HOLD}$, the X25F008/016/032/064 device will resume operation from the point when $\overline{HOLD}$ was first asserted.

Program Enable Latch

The X25F008/016/032/064 device contains a program enable latch. This latch must be SET before a program operation will be completed internally. The PREN instruction will set the latch and the PRDI instruction will reset the latch. This latch is automatically reset on power-up and after the completion of a sector program or status register write cycle.

Status Register

The RDSR instruction provides access to the status register. The status register may be read at any time, even during a program cycle. The status register is formatted as follows:

7	6	5	4	3	2	1	0
PPEN	X	X	X	BL1	BL0	PEL	PIP

6685 PGM T02.2

PPEN, BL0, and BL1 are set by the PRSR instruction. PEL and PIP are "read-only" and automatically set by other operations.

The Programming-In-Process (PIP) bit indicates whether the X25F008/016/032/064 device is busy with a program operation. When set to a "1" programming is in progress, when set to a "0" no programming is in progress. During programming, all other bits are set to "1".

The Program Enable Latch (PEL) bit indicates the status of the program enable latch. When set to a "1" the latch is set; when set to a "0" the latch is reset.

The Block Lock (BL0 and BL1) bits are nonvolatile and allow the user to select one of four levels of protection. The X25F008/016/032/064 device array is divided into four equal segments. One, two, or all four of the segments may be locked. That is, the user may read the segments, but will be unable to alter (program) data within the selected segments. The partitioning is controlled as illustrated below.

Status Register Bits		Array Addresses
BL1	BL0	Locked
0	0	None
0	1	upper fourth
1	0	upper half
1	1	All

6685 PGM T03.1

Program-Protect Enable

The Program-Protect-Enable bit (PPEN) in the X25F008/016/032/064 status register acts as an enable bit for the $\overline{PP}$ pin.

Table 1. Instruction Set

Instruction Name	Instruction Format*	Operation
PREN	0000 0110	Set the Program Enable Latch (Enable Program Operations)
PRDI	0000 0100	Reset the Program Enable Latch (Disable Program Operations)
RDSR	0000 0101	Read Status Register
PRSR	0000 0001	Program Status Register
READ	0000 0011	Read from Memory Array beginning at Selected Address
PROGRAM	0000 0010	Program Memory Array beginning at Selected Address (32 Bytes)

6685 PGM T04.2

*Instructions are shown MSB in leftmost position. Instructions are transferred MSB first.

PPEN	$\overline{PP}$	PEL	Locked Blocks	Unlocked Blocks	Status Register
0	X	0	Locked	Locked	Locked
0	X	1	Locked	Programmable	Programmable
1	LOW	0	Locked	Locked	Locked
1	LOW	1	Locked	Programmable	Locked
X	HIGH	0	Locked	Locked	Locked
X	HIGH	1	Locked	Programmable	Programmable

6685 PGM T05.2

The Program Protect ($\overline{PP}$) pin and the nonvolatile Program Protect Enable (PPEN) bit in the Status Register control the programmable hardware write protect feature. Hardware program protection is enabled when $\overline{PP}$ pin is LOW, and the PPEN bit is "1". Hardware program protection is disabled when either the $\overline{PP}$ pin is HIGH or the PPEN bit is "0". When the chip is hardware program protected, nonvolatile programming of the Status Register in disabled, including the Block Lock bits and the PPEN bit itself, as well as the Block Lock sections in the memory array. Only the sections of the memory array that are not Block Locked can be programmed.

Note: Since the PPEN bit is program protected, it cannot be changed back to a "0", as long as the $\overline{PP}$ pin is held LOW.

Clock and Data Timing

Data input on the SI line is latched on the rising edge of SCK. Data is output on the SO line by the falling edge of SCK.

Read Sequence

When reading from the SerialFlash memory array, $\overline{CS}$ is first pulled LOW to select the device. The 8-bit READ instruction is transmitted to the X25F008/016/032/064 device, followed by the 16-bit address. After the read opcode and address are sent, the data stored in the memory at the selected address is shifted out on the SO line. The data stored in memory at the next address can be read sequentially by continuing to provide clock pulses. The address is automatically incremented to the next higher address after each byte of data is shifted out. When the highest address is reached the address counter rolls over to address $0000, allowing the read cycle to be continued indefinitely. The read operation is terminated by taking $\overline{CS}$ HIGH. Refer to the Read SerialFlash Memory Array Operation Sequence illustrated in Figure 1.

To read the status register, the $\overline{CS}$ line is first pulled LOW to select the device followed by the 8-bit instruction. After the read status register opcode is sent, the contents of the status register are shifted out on the SO line. The Read Status Register Sequence is illustrated in Figure 2.

Programming Sequence

Prior to any attempt to program the X25F008/016/032/064 device, the program enable latch must first be set by issuing the PREN instruction (See Figure 3). $\overline{CS}$ is first taken LOW, then the PREN instruction is clocked into the X25F008/016/032/064 device. After all eight bits of the instruction are transmitted, $\overline{CS}$ must then be taken HIGH. If the user continues the programming operation without taking $\overline{CS}$ HIGH after issuing the PREN instruction, the programming operation will be ignored.

To program the SerialFlash memory array, the user issues the PROGRAM instruction, followed by the address of the first location in the sector and then the data to be programmed. The data is programmed in a 256-clock operation. $\overline{CS}$ must go LOW and remain LOW for the duration of the operation. The 32 bytes must reside in the same sector and cannot cross sector boundaries. If the address counter reaches the end of the sector and the clock continues, or if fewer than 32 bytes are clocked in, the contents of the sector cannot be guaranteed.

For the program operation to be completed, $\overline{CS}$ can only be brought HIGH after bit 0 of data byte 32 is clocked in. If it is brought HIGH at any other time the program operation will not be completed. Refer to Figure 4 below for a detailed illustration of the programming sequence and time frames in which $\overline{CS}$ going HIGH is valid.

To program the status register, the PRSR instruction is followed by the data to be programmed. Data bits 0, 1, 4, 5 and 6 must be "0". This sequence is shown in Figure 5.

While the program cycle is in progress, following a status register or memory write sequence, the status register may be read to check the PIP bit. During this time the PIP bit will be HIGH.

Hold Operation

The $\overline{HOLD}$ input should be HIGH (at V_{IH}) under normal operation. If a data transfer is to be interrupted $\overline{HOLD}$ can be pulled LOW to suspend the transfer until it can be resumed. The only restriction is that the SCK input must be LOW when $\overline{HOLD}$ is first pulled LOW and SCK must also be LOW when $\overline{HOLD}$ is released.

The $\overline{HOLD}$ input may be tied HIGH either directly to V_{CC} or tied to V_{CC} through a resistor.

Operational Notes

The device powers-up in the following state:

- The device is in the low power standby state.
- A HIGH to LOW transition on $\overline{CS}$ is required to enter an active state and receive an instruction.
- SO pin is high impedance.
- The program enable latch is reset.

Data Protection

The following circuitry has been included to prevent inadvertent programming:

- The program enable latch is reset upon power-up.
- A program enable instruction must be issued to set the program enable latch.
- $\overline{CS}$ must come HIGH at the proper clock count in order to start a program cycle.

2

Figure 1. Read SerialFlash Memory Array Operation Sequence

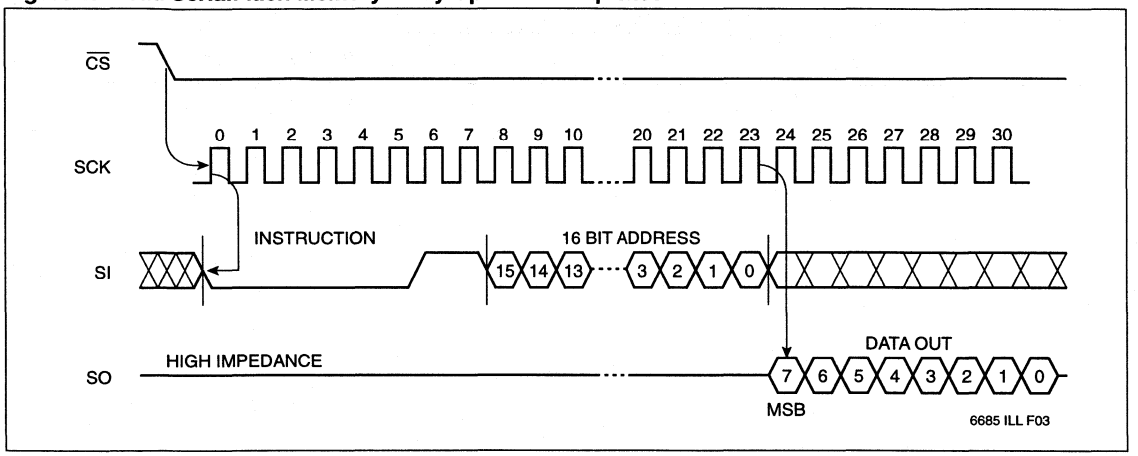


Figure 2. Read Status Register Operation Sequence

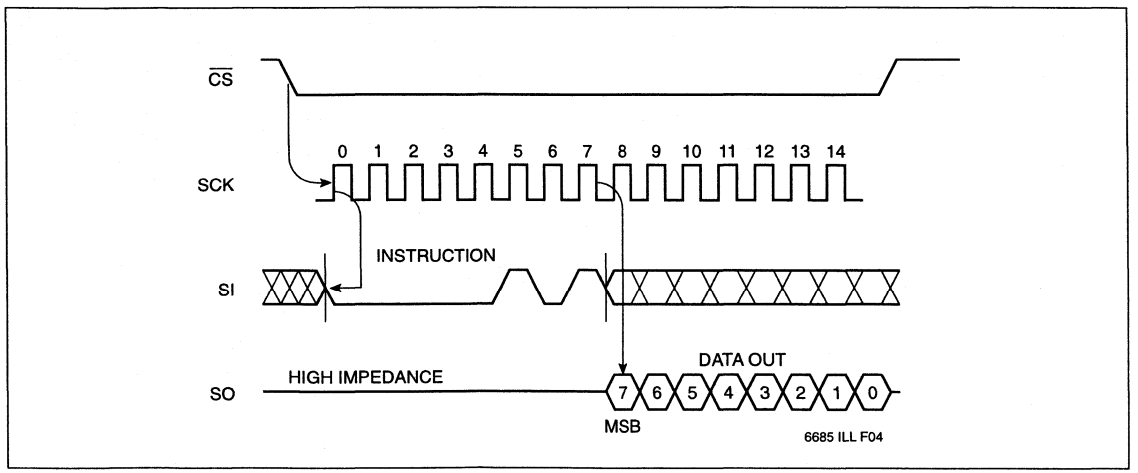


Figure 3. Program Enable Latch Sequence

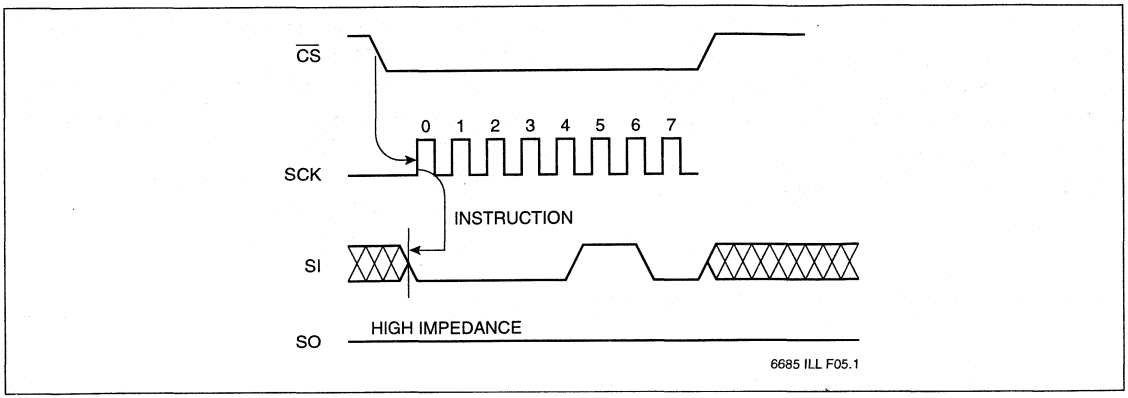


Figure 4. Programming Sequence

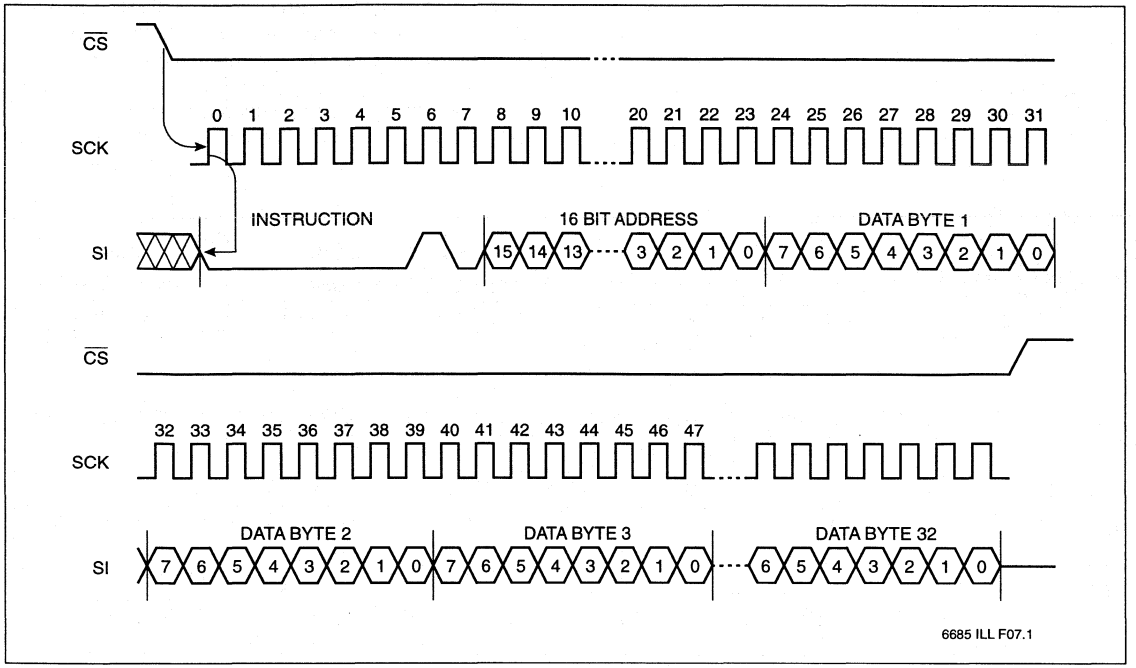
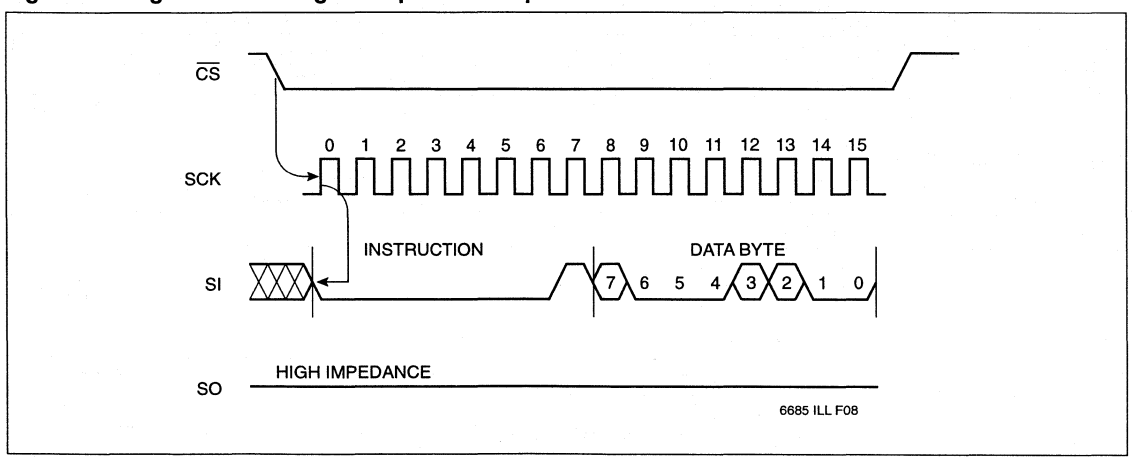


Figure 5. Program Status Register Operation Sequence



ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... –65°C to +135°C
Storage Temperature ..... –65°C to +150°C
Voltage on any Pin with Respect to V_{SS} ..... –1V to +7V
D.C. Output Current 5mA
Lead Temperature
(Soldering, 10 Seconds) ..... 300°C

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temp	Min.	Max.
Commercial	0°C	70°C
Industrial	–40°C	+85°C

6685 PGM T06.1

Supply Voltage	Limits
X25F008/016/032/064	1.8V to 3.6V
X25F008/016/032/064–5	4.5V to 5.5V

6685 PGM T07.3

D.C. OPERATING CHARACTERISTICS (Over the recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
I_{CC}	V_{CC} Supply Current (Active)		5	mA	SCK = V_{CC} x 0.1/V_{CC} x 0.9 @ 1MHz, SO = Open, $\overline{CS}$ = V_{SS}
I_{SB1}(2)	V_{CC} Supply Current (Standby)		1	µA	$\overline{CS}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}, V_{CC} = 3.6V
I_{SB2}	V_{CC} Supply Current (Standby)		10	µA	$\overline{CS}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}, V_{CC} = 5V
I_{LI}	Input Leakage Current		10	µA	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output Leakage Current	–1	10	µA	V_{OUT} = V_{SS} to V_{CC}
V_{IL}(1)	Input LOW Voltage	V_{CC} x 0.7	V_{CC} x 0.3	V	
V_{IH}(1)	Input HIGH Voltage		V_{CC} + 0.5	V	
V_{OL1}	Output LOW Voltage		0.4	V	I_{OL} = 1.5mA, V_{CC} = 2.7V
V_{OH1}	Output HIGH Voltage	V_{CC} – 0.3		V	I_{OH} = –0.4mA, V_{CC} = 2.7V
V_{OL2}	Output LOW Voltage		0.4	V	I_{OL} = 3mA, V_{CC} = 5V
V_{OH2}	Output HIGH Voltage	V_{CC} – 0.8		V	I_{OH} = –1.6mA, V_{CC} = 5V

6685 PGM T08.4

POWER-UP TIMING

Symbol	Parameter	Min.	Max.	Units
t_{PUR}(3)	Power-up to Read Operation		1	ms
t_{PUW}(3)	Power-up to Write Operation		5	ms

6685 PGM T09

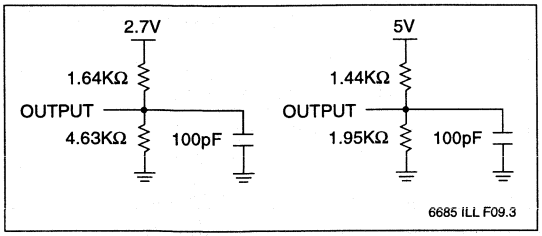
CAPACITANCE T_A = 25°C, f = 1MHz, V_{CC} = 5V.

Symbol	Test	Max.	Units	Conditions
C_{OUT}(2)	Output Capacitance (SO)	8	pF	V_{OUT} = 0V
C_{IN}(2)	Input Capacitance (SCK, SI, $\overline{CS}$, $\overline{WP}$, $\overline{HOLD}$)	6	pF	V_{IN} = 0V

6685 PGM T10.1

Notes: (1) V_{IL} min. and V_{IH} max. are for reference only and are not tested.
(2) This parameter is periodically sampled and not 100% tested.
(3) t_{PUR} and t_{PUW} are the delays required from the time V_{CC} is stable until the specified operation can be initiated. These parameters are periodically sampled and not 100% tested.

EQUIVALENT A.C. LOAD CIRCUIT



A.C. TEST CONDITIONS

Input Pulse Levels	V_{CC} x 0.1 to V_{CC} x 0.9
Input Rise and Fall Times	10ns
Input and Output Timing Level	V_{CC} x 0.5

6685 PGM T11

2

A.C. CHARACTERISTICS (Over recommended operating conditions, unless otherwise specified)

Data Input Timing

Symbol	Parameter	Min.	Max.	Units
f_{SCK}	Clock Frequency	0	1	MHz
t_{CYC}	Cycle Time	1000		ns
t_{LEAD}	$\overline{CS}$ Lead Time	500		ns
t_{LAG}	$\overline{CS}$ Lag Time	500		ns
t_{WH}	Clock HIGH Time	400		ns
t_{WL}	Clock LOW Time	400		ns
t_{SU}	Data Setup Time	100		ns
t_H	Data Hold Time	100		ns
t_{RI}(4)	Data In Rise Time		2	µs
t_{FI}(4)	Data In Fall Time		2	µs
t_{HD}	$\overline{HOLD}$ Setup Time	200		ns
t_{CD}	$\overline{HOLD}$ Hold Time	200		ns
t_{CS}	$\overline{CS}$ Deselect Time	2		µs
t_{PC}(5)	Program Cycle Time		10	ms

6685 PGM T12.3

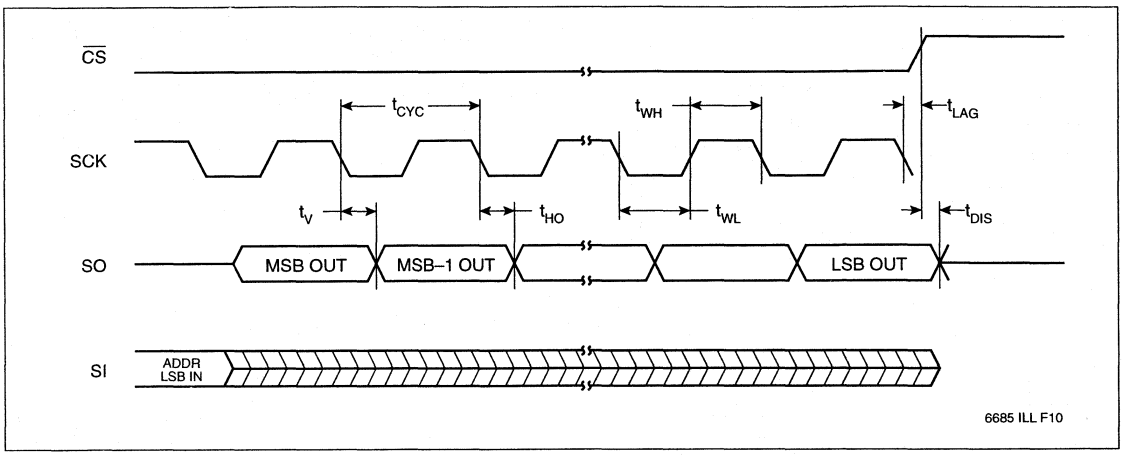
Data Output Timing

Symbol	Parameter	Min.	Max.	Units
f_{SCK}	Clock Frequency	0	1	MHz
t_{DIS}	Output Disable Time		500	ns
t_V	Output Valid from Clock LOW		400	ns
t_{HO}	Output Hold Time	0		ns
t_{RO}(4)	Output Rise Time		300	ns
t_{FO}(4)	Output Fall Time		300	ns
t_{LZ}(4)	$\overline{HOLD}$ HIGH to Output in Low Z	100		ns
t_{HZ}(4)	$\overline{HOLD}$ LOW to Output in High Z	100		ns

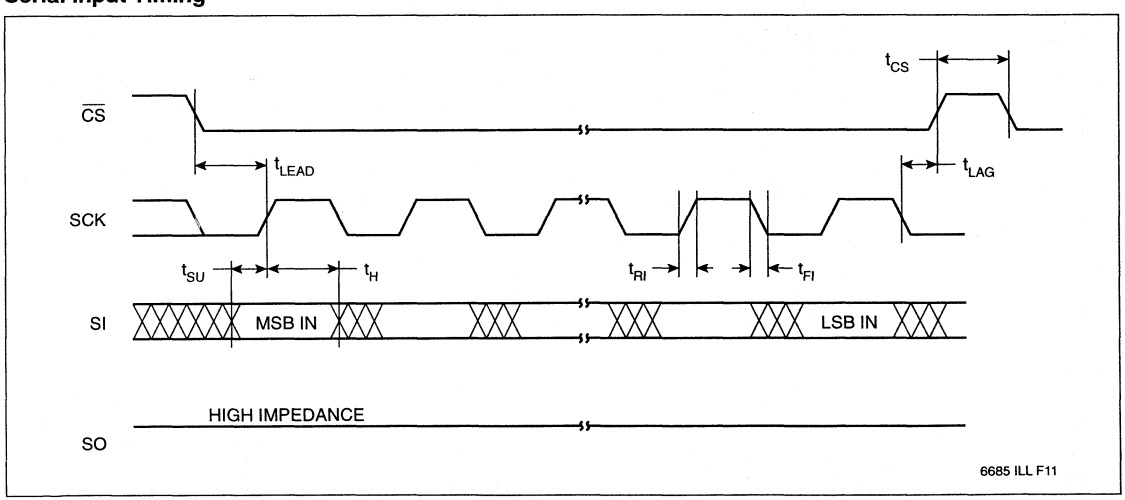
6685 PGM T13.2

Notes: (4) This parameter is periodically sampled and not 100% tested.
(5) t_{WC} is the time from the rising edge of $\overline{CS}$ after a valid write sequence has been sent to the end of the self-timed internal nonvolatile program cycle.

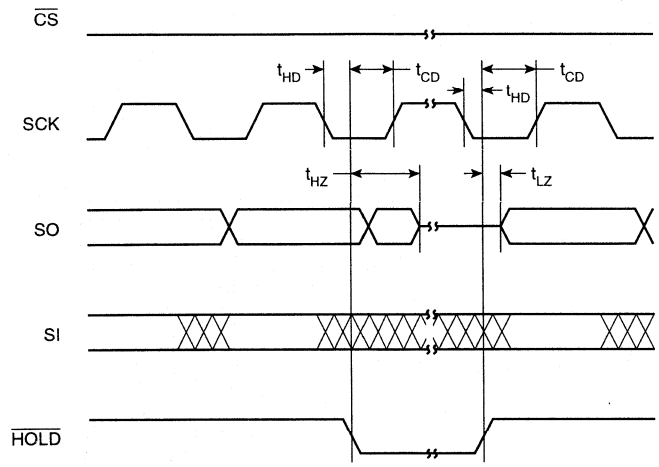
Serial Output Timing



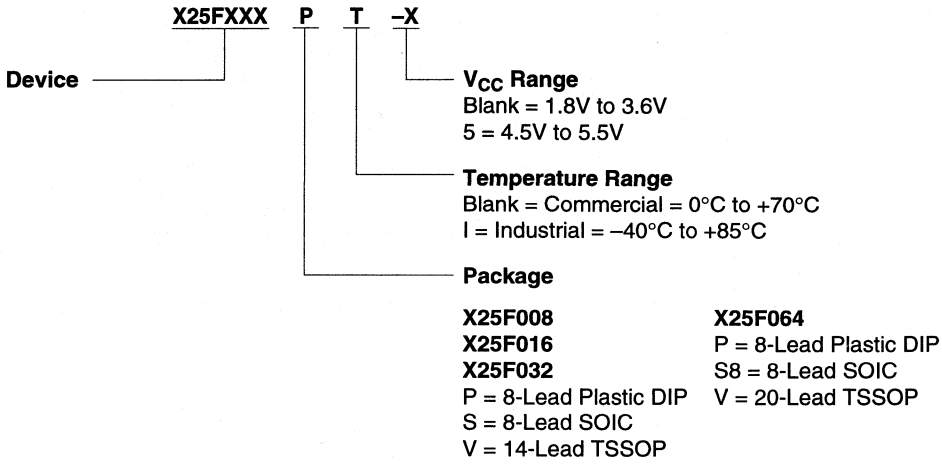
Serial Input Timing



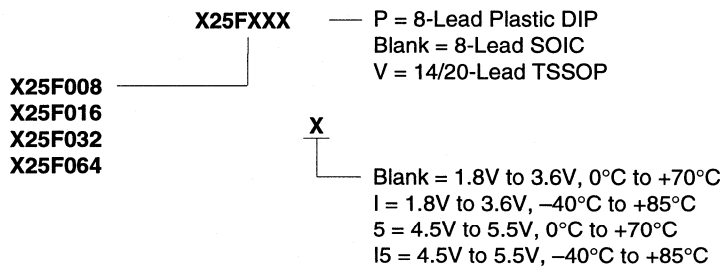
Hold Timing



ORDERING INFORMATION



Part Mark Convention



Xicor®

3807-2.3 12/4/95 T12/C0/D0 NS

5 Volt, Byte Alterable E²PROM

FEATURES

- 90ns Access Time
- Simple Byte and Page Write
  - —Single 5V Supply
    - —No External High Voltages or V_{PP} Control Circuits
  - —Self-Timed
    - —No Erase Before Write
    - —No Complex Programming Algorithms
    - —No Overerase Problem
- High Performance Advanced NMOS Technology
- Fast Write Cycle Times
  - —16 Byte Page Write Operation
  - —Byte or Page Write Cycle: 5ms Typical
  - —Complete Memory Rewrite: 640ms Typical
  - —Effective Byte Write Cycle Time: 300µs Typical
- $\overline{\text{DATA}}$ Polling
  - —Allows User to Minimize Write Cycle Time
- JEDEC Approved Byte-Wide Pinout
- High Reliability
  - —Endurance: 10,000 Cycles
  - —Data Retention: 100 Years

DESCRIPTION

The Xicor X2804C is a 512 x 8 E²PROM, fabricated with an advanced, high performance N-channel floating gate MOS technology. Like all Xicor Programmable nonvolatile memories it is a 5V only device. The X2804C features the JEDEC approved pinout for byte-wide memories, compatible with industry standard RAMs, ROMs and EPROMs.

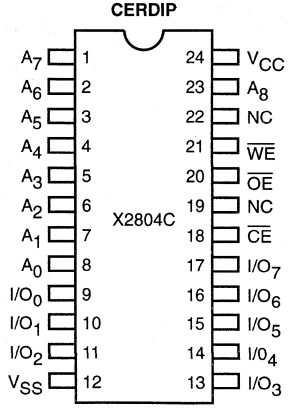
The X2804C supports a 16-byte page write operation, typically providing a 300µs/byte write cycle, enabling the entire memory to be written in less than 640ms. The X2804C also features $\overline{\text{DATA}}$ Polling, a system software support scheme used to indicate the early completion of a write cycle.

Xicor E²PROMs are designed and tested for applications requiring extended endurance. Inherent data retention is greater than 100 years.

3

PIN CONFIGURATION

PLASTIC DIP
CERDIP



6612 FHD F02

PIN DESCRIPTIONS

Addresses (A_0–A_8)

The Address inputs select an 8-bit memory location during a read or write operation.

Chip Enable ($\overline{CE}$)

The Chip Enable input must be LOW to enable all read/write operations. When $\overline{CE}$ is HIGH, power consumption is reduced.

Output Enable ($\overline{OE}$)

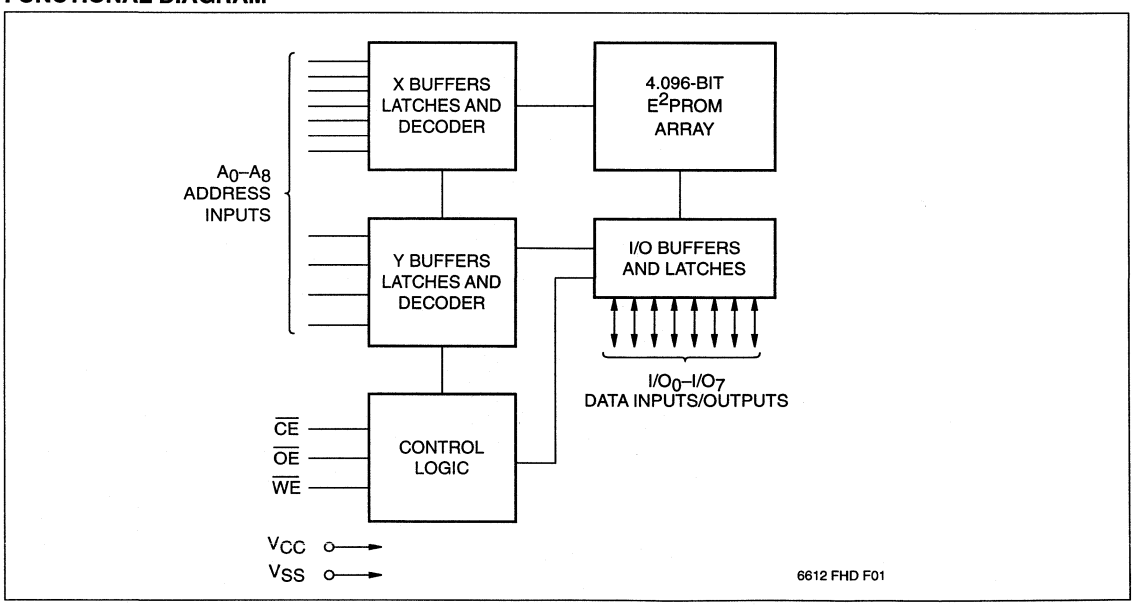
The Output Enable input controls the data output buffers and is used to initiate read operations.

PIN NAMES

Symbol	Description
A_0–A_8	Address Inputs
I/O_0–I/O_7	Data Input/Output
$\overline{WE}$	Write Enable
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
V_{CC}	+5V
V_{SS}	Ground
NC	No Connect

6612 PGM T01

FUNCTIONAL DIAGRAM



6612 FHD F01

DEVICE OPERATION

Read

Read operations are initiated by both $\overline{OE}$ and $\overline{CE}$ LOW and $\overline{WE}$ HIGH. The read operation is terminated by either $\overline{CE}$ or $\overline{OE}$ returning HIGH. This two line control architecture eliminates bus contention in a system environment. The data bus will be in a high impedance state when either $\overline{OE}$ or $\overline{CE}$ is HIGH.

Write

Write operations are initiated when both $\overline{CE}$ and $\overline{WE}$ are LOW and $\overline{OE}$ is HIGH. The X2804C supports both a $\overline{CE}$ and $\overline{WE}$ controlled write cycle. That is, the address is latched by the falling edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs last. Similarly, the data is latched internally by the rising edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs first. A byte write operation, once initiated, will automatically continue to completion, typically within 5ms.

Page Write Operation

The page write feature of the X2804C allows the entire memory to be typically written in 450ms. Page write allows two to sixteen bytes of data to be consecutively written to the X2804C prior to the commencement of the internal programming cycle. Although the host system may read data from any other device in the system to transfer to the X2804C, the destination page address of the X2804C should be the same on each subsequent strobe of the $\overline{WE}$ and $\overline{CE}$ inputs. That is, A_4 through A_{10} must be the same for each transfer of data to the X2804C during a page write cycle.

The page write mode can be entered during any write operation. Following the initial byte write cycle, the host can write an additional one to fifteen bytes in the same manner as the first byte was written. Each successive byte load cycle, started by the $\overline{WE}$ HIGH to LOW transition, must begin within 20μs of the falling edge of the preceding $\overline{WE}$. If a subsequent $\overline{WE}$ HIGH to LOW transition is not detected within 20μs, the internal automatic programming cycle will commence. There is no page write window limitation. The page write window is infinitely wide, so long as the host continues to access the device within the byte load cycle time of 20μs.

$\overline{DATA}$ Polling

The X2804C features $\overline{DATA}$ Polling as a method to indicate to the host system that the byte write or page write cycle has completed. $\overline{DATA}$ Polling allows a simple bit test operation to determine the status of the X2804C, eliminating additional interrupt inputs or external hardware. During the internal programming cycle, any attempt to read the last byte written will produce the complement of that data on I/O_7 (i.e., write data = 0xxx xxxx, read data = 1xxx xxxx). Once the programming cycle is complete, I/O_7 will reflect true data.

WRITE PROTECTION

There are three features that protect the nonvolatile data from inadvertent writes.

- Noise Protection—A $\overline{WE}$ pulse which is typically less than 10ns will not initiate a write cycle.
- V_{CC} Sense—All functions are inhibited when V_{CC} is ≤3V, typically.
- Write Inhibit—Holding either $\overline{OE}$ LOW, $\overline{WE}$ HIGH, or $\overline{CE}$ HIGH during power-up and power-down, will inhibit inadvertent writes. Write cycle timing specifications must be observed concurrently.

ENDURANCE

Xicor E²PROMs are designed and tested for applications requiring extended endurance.

SYSTEM CONSIDERATIONS

Because the X2804C is frequently used in large memory arrays, it is provided with a two line control architecture for both read and write operations. Proper usage can provide the lowest possible power dissipation and eliminate the possibility of contention where multiple I/O pins share the same bus.

To gain the most benefit, it is recommended that $\overline{CE}$ be decoded from the address bus and be used as the primary device selection input. Both $\overline{OE}$ and $\overline{WE}$ would then be common among all devices in the array. For a read operation this assures that all deselected devices are in their standby mode and that only the selected device(s) is outputting data on the bus.

Because the X2804C has two power modes, standby and active, proper decoupling of the memory array is of prime concern. Enabling $\overline{CE}$ will cause transient current spikes. The magnitude of these spikes is dependent on the output capacitive loading of the I/Os. Therefore, the larger the array sharing a common bus, the larger the transient spikes. The voltage peaks associated with the current transients can be suppressed by the proper selection and placement of decoupling capacitors. As a minimum, it is recommended that a 0.1µF high frequency ceramic capacitor be used between V_{CC} and V_{SS} at each device. Depending on the size of the array, the value of the capacitor may have to be larger.

In addition, it is recommended that a 4.7µF electrolytic bulk capacitor be placed between V_{CC} and V_{SS} for each eight devices employed in the array. This bulk capacitor is employed to overcome the voltage droop caused by the inductive effects of the PC board traces.

ABSOLUTE MAXIMUM RATINGS*

Temperature under Bias
- X2804C ..... –10°C to +85°C
- X2804CI ..... –65°C to +135°C

Storage Temperature ..... –65°C to +150°C

Voltage on any Pin with
- Respect to V_{SS} ..... –1V to +7V

D.C. Output Current 5mA

Lead Temperature (Soldering, 10 seconds) ..... 300°C

***COMMENT**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	+70°C
Industrial	–40°C	+85°C

6612 PGM T02.2

Supply Voltage	Limits
X2804C	5V ±10%

6612 PGM T03

3

D.C. OPERATING CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.(1)	Max.		
I_{CC}	V_{CC} Current (Active)		70	110	mA	$\overline{CE}$ = $\overline{OE}$ = V_{IL} All I/O's = Open Other Inputs = V_{CC}
I_{SB}	V_{CC} Current (Standby)		35	50	mA	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IL} All I/O's = Open Other Inputs = V_{CC}
I_{LI}	Input Leakage Current			10	µA	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output Leakage Current			10	µA	V_{OUT} = V_{SS} to V_{CC}, $\overline{CE}$ = V_{IH}
V_{IL}(2)	Input LOW Voltage	–1		0.8	V	
V_{IH}(2)	Input HIGH Voltage	2		V_{CC} +1	V	
V_{OL}	Output LOW Voltage			0.4	V	I_{OL} = 2.1mA
V_{OH}	Output HIGH Voltage	2.4			V	I_{OH} = –400µA

6612 PGM T02.1

Notes: (1) Typical values are for T_A = 25°C and nominal supply voltage and are not tested.
(2) V_{IL} min. and V_{IH} max. are for reference only and are not tested.

ENDURANCE AND DATA RETENTION

Parameter	Min.	Max.	Unit
Minimum Endurance	10,000		Cycles/Byte
Data Retention	100		Years

6612 PGM T03

POWER-UP TIMING

Symbol	Parameter	Typ.(1)	Units
t_{PUR}(3)	Power-Up to Read Operation	1	ms
t_{PUW}(3)	Power-Up to Write Operation	5	ms

6612 PGM T04

CAPACITANCE T_A = +25°C, f = 1MHz, V_{CC} = 5V

Symbol	Test	Max.	Units	Conditions
$C_{I/O}$(3)	Input/Output Capacitance	10	pF	$V_{I/O}$ = 0V
C_{IN}(3)	Input Capacitance	6	pF	V_{IN} = 0V

6612 PGM T05.1

A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3V
Input Rise and Fall Times	5ns
Input and Output Timing Levels	1.5V

3852 PGM T06.1

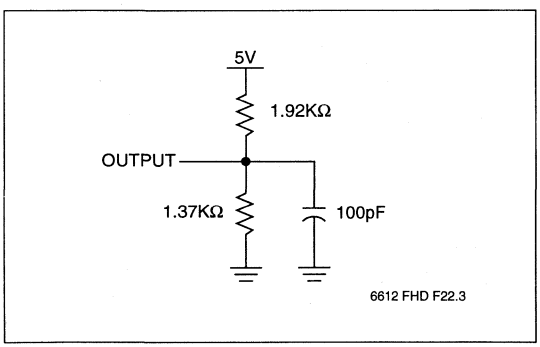
MODE SELECTION

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O	Power
L	L	H	Read	D_{OUT}	Active
L	H	L	Write	D_{IN}	Active
H	X	X	Standby and Write Inhibit	High Z	Standby
X	L	X	Write Inhibit	—	—
X	X	H	Write Inhibit	—	—

6612 PGM T07

Note: (3) This parameter is periodically sampled and not 100% tested.

EQUIVALENT A.C. LOAD CIRCUITS



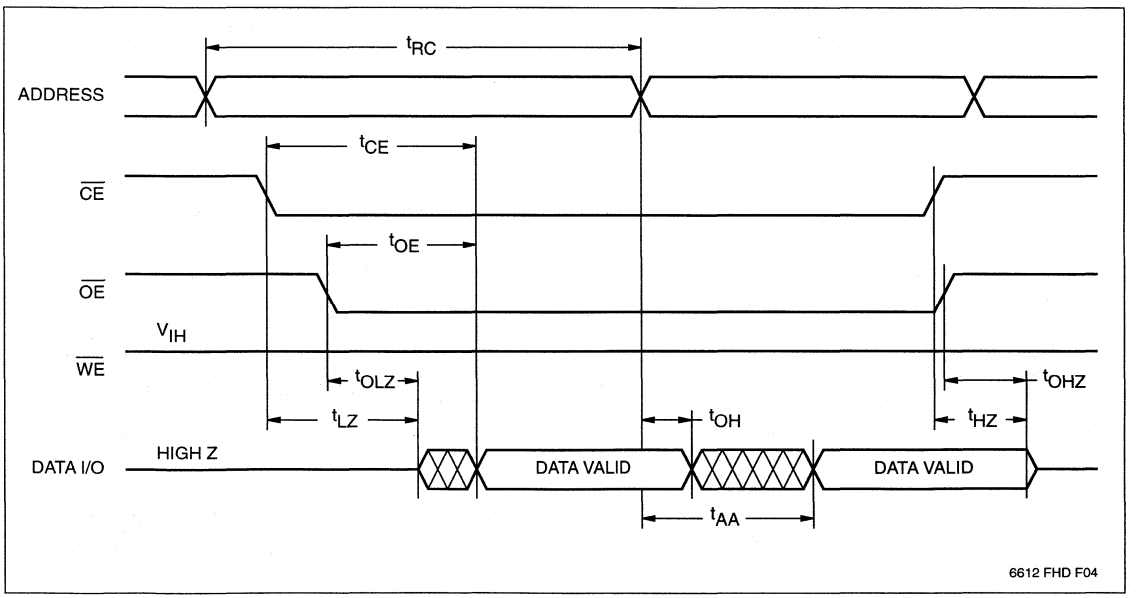
A.C. CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Read Cycle Limits

Symbol	Parameter	X2804C-90		X2804C-15		X2804C-20		X2804C-25		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	90		150		200		250		ns
t_{CE}	Chip Enable Access Time		90		150		200		250	ns
t_{AA}	Address Access Time		90		150		200		250	ns
t_{OE}	Output Enable Access Time		60		80		100		100	ns
t_{LZ}(4)	$\overline{CE}$ LOW to Active Output	0		0		0		0		ns
t_{OLZ}(4)	$\overline{OE}$ LOW to Active Output	0		0		0		0		ns
t_{HZ}(4)	$\overline{CE}$ HIGH to High Z Output		50		60		60		60	ns
t_{OHZ}(4)	$\overline{OE}$ HIGH to High Z Output		50		60		60		60	ns
t_{OH}	Output Hold from Address Change	0		0		0		0		ns

6612 PGM T10.1

Read Cycle



6612 FHD F04

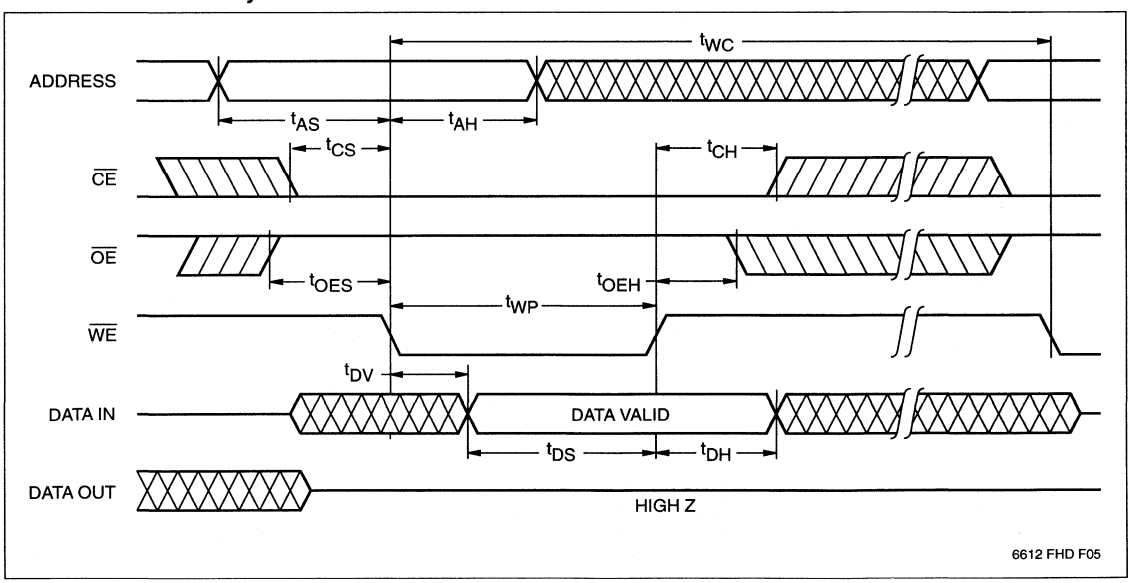
Notes: (4) t_{LZ} min., t_{HZ}, t_{OLZ}, and t_{OHZ} are periodically sampled and not 100% tested. t_{HZ} max. and t_{OHZ} max. are measured from the point when $\overline{CE}$ or $\overline{OE}$ return HIGH (whichever occurs first) to the time when the outputs are no longer driven.

Write Cycle Limits

Symbol	Parameter	X2804C-90		X2804C-15,-20,-25		Units
		Min.	Max.	Min.	Max.	
t_{WC}(5)	Write Cycle Time		10		10	ms
t_{AS}	Address Setup Time	5		5		ns
t_{AH}	Address Hold Time	80		100		ns
t_{CS}	Write Setup Time	0		0		ns
t_{CH}	Write Hold Time	0		0		ns
t_{CW}	$\overline{CE}$ Pulse Width	80		100		ns
t_{OES}	$\overline{OE}$ HIGH Setup Time	10		10		ns
t_{OEH}	$\overline{OE}$ HIGH Hold Time	5		10		ns
t_{WP}	$\overline{WE}$ Pulse Width	80		100		ns
t_{WPH}	$\overline{WE}$ HIGH Recovery	50		50		ns
t_{DV}	Data Valid		100		100	µs
t_{DS}	Data Setup	35		50		ns
t_{DH}	Data Hold	5		10		ns
t_{DW}	Delay to Next Write	10		10		µs
t_{BLC}	Byte Load Cycle	1	100	1	100	µs

6612 PGM T09.1

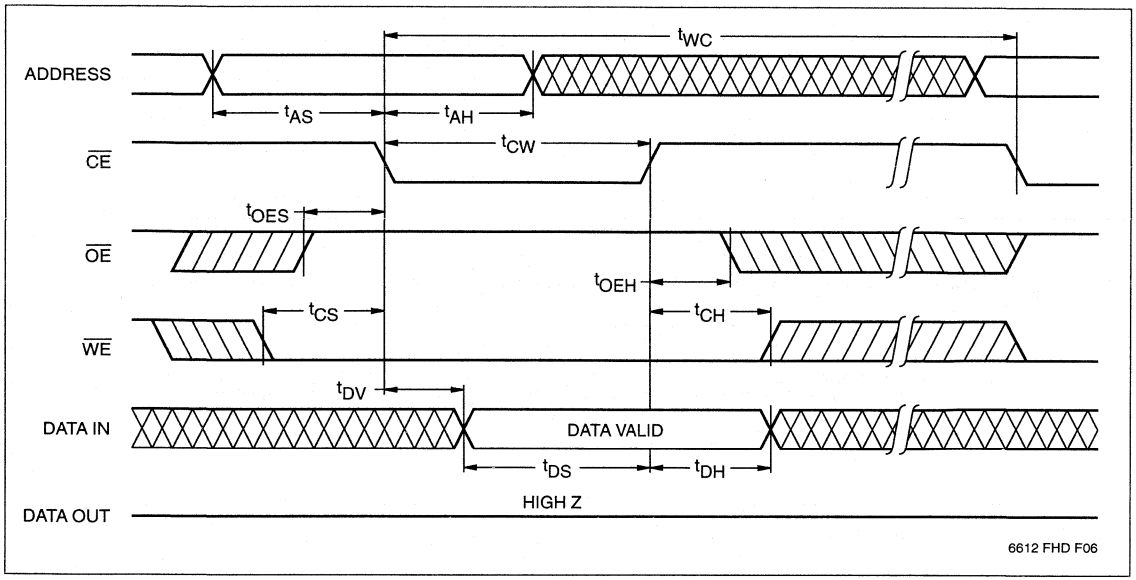
$\overline{WE}$ Controlled Write Cycle



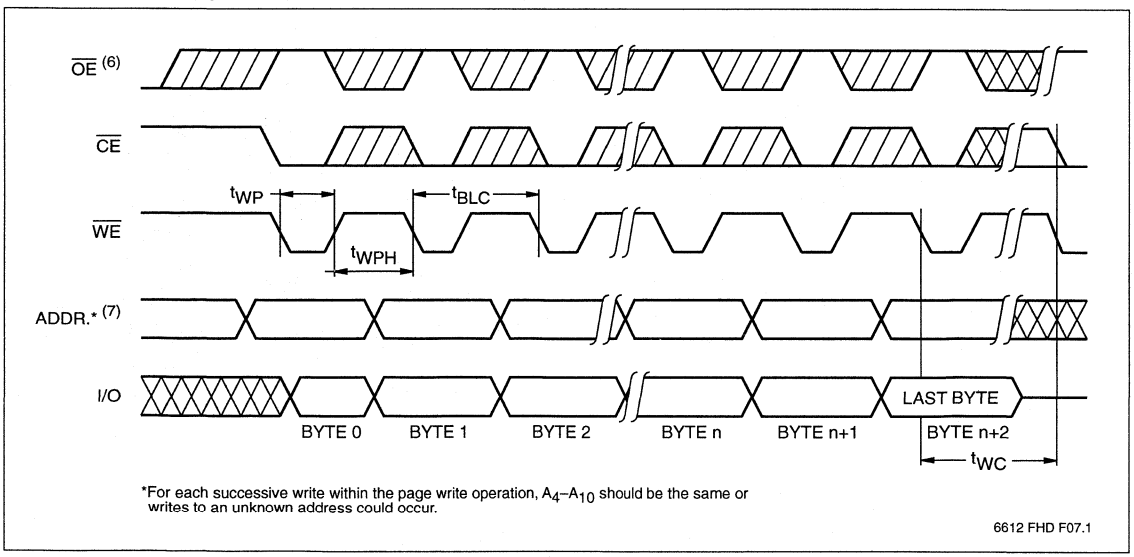
6612 FHD F05

Notes: (5) t_{WC} is the minimum cycle time to be allowed from the system perspective unless polling techniques are used. It is the maximum time the device requires to automatically complete the internal write operation. For faster t_{WC}, please refer to X28C16 and X28HC16 product data sheets.

$\overline{CE}$ Controlled Write Cycle



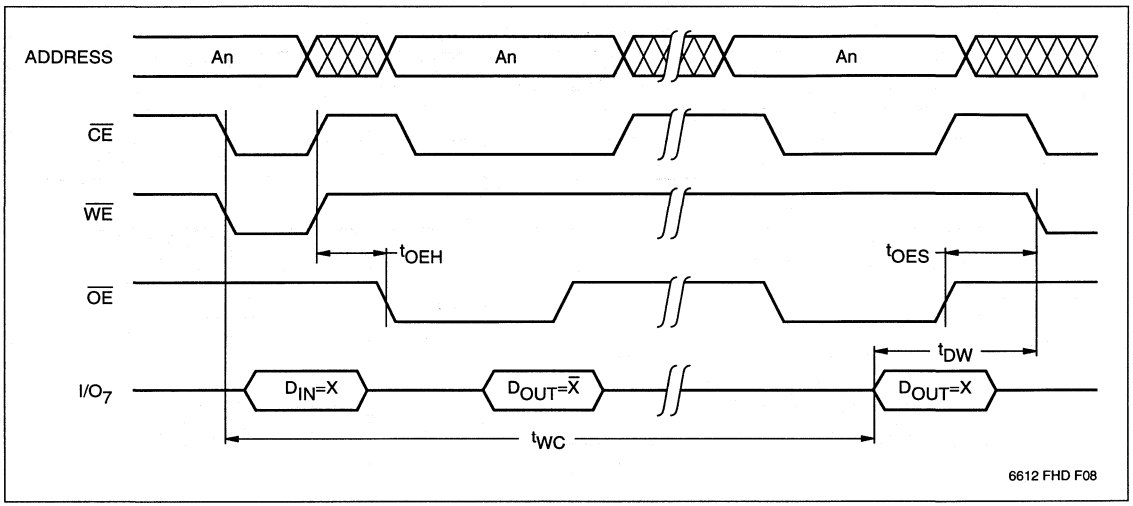
Page Mode Write Cycle



Notes: (6) Between successive byte writes within a page write operation, $\overline{OE}$ can be strobed LOW: e.g. this can be done with $\overline{CE}$ and $\overline{WE}$ HIGH to fetch data from another memory device within the system for the next write; or with $\overline{WE}$ HIGH and $\overline{CE}$ LOW effectively performing a polling operation.

(7) The timings shown above are unique to page write operations. Individual byte load operations within the page write must conform to either the $\overline{CE}$ or $\overline{WE}$ controlled write cycle timing.

$\overline{\text{DATA}}$ Polling Timing Diagram[10]

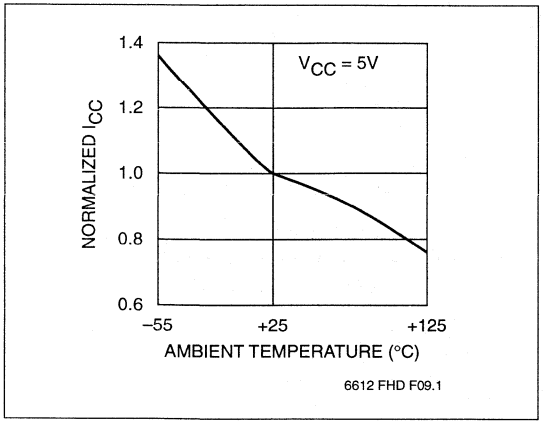


Note: (10) Polling operations are by definition read cycles and are therefore subject to read cycle timings.

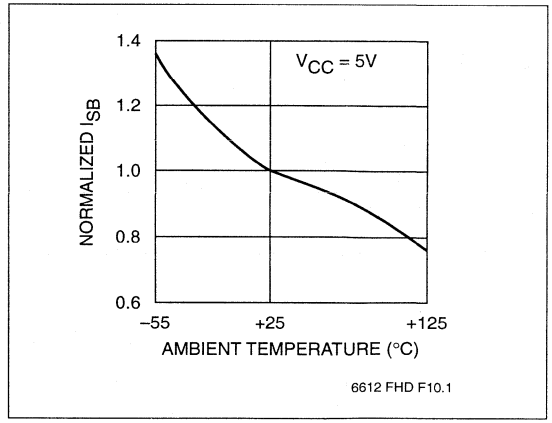
SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

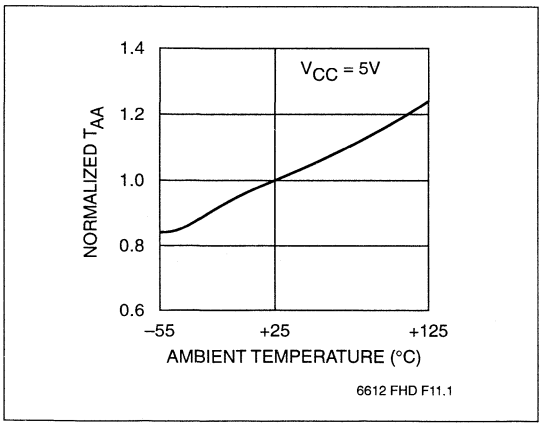
Normalized Active Supply Current vs. Ambient Temperature



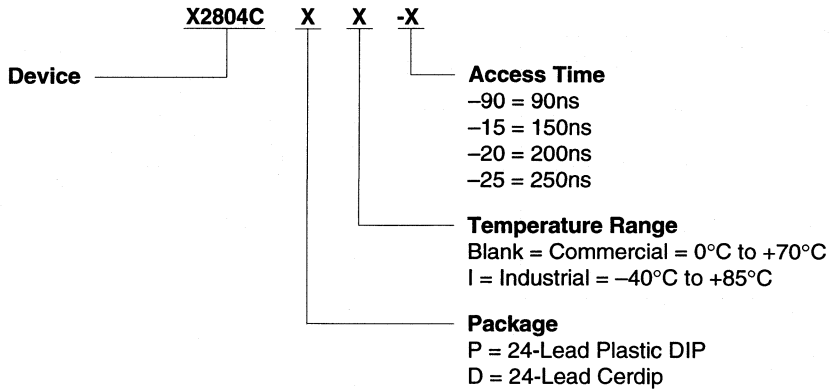
Normalized Standby Supply Current vs. Ambient Temperature



Normalized Access Time vs. Ambient Temperature



ORDERING INFORMATION



5 Volt, Byte Alterable E²PROM

FEATURES

- 90ns Access Time
- Simple Byte and Page Write
  - —Single 5V Supply
    - —No External High Voltages or V_{PP} Control Circuits
  - —Self-Timed
    - —No Erase Before Write
    - —No Complex Programming Algorithms
    - —No Overerase Problem
- High Performance Advanced NMOS Technology
- Fast Write Cycle Times
  - —16 Byte Page Write Operation
  - —Byte or Page Write Cycle: 5ms Typical
  - —Complete Memory Rewrite: 640ms Typical
  - —Effective Byte Write Cycle Time: 300µs Typical
- $\overline{DATA}$ Polling
  - —Allows User to Minimize Write Cycle Time
- JEDEC Approved Byte-Wide Pinout
- High Reliability
  - —Endurance: 10,000 Cycles
  - —Data Retention: 100 Years

DESCRIPTION

The Xicor X2816C is a 2K x 8 E²PROM, fabricated with an advanced, high performance N-channel floating gate MOS technology. Like all Xicor Programmable nonvolatile memories it is a 5V only device. The X2816C features the JEDEC approved pinout for byte-wide memories, compatible with industry standard RAMs, ROMs and EPROMs.

The X2816C supports a 16-byte page write operation, typically providing a 300µs/byte write cycle, enabling the entire memory to be written in less than 640ms. The X2816C also features $\overline{DATA}$ Polling, a system software support scheme used to indicate the early completion of a write cycle.

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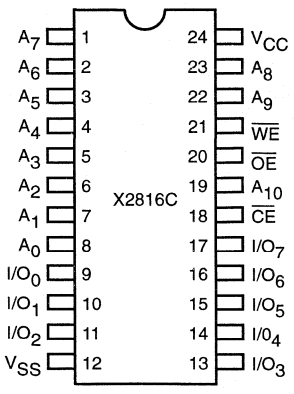
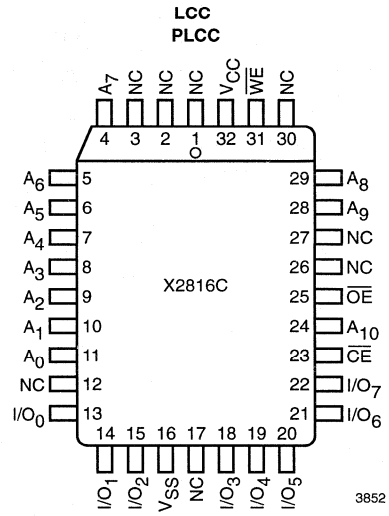
PIN CONFIGURATION

PLASTIC DIP
CERDIP
SOIC



3852 FHD F02

LCC
PLCC



3852 FHD F03

PIN DESCRIPTIONS

Addresses (A_0–A_{10})

The Address inputs select an 8-bit memory location during a read or write operation.

Chip Enable ($\overline{CE}$)

The Chip Enable input must be LOW to enable all read/write operations. When $\overline{CE}$ is HIGH, power consumption is reduced.

Output Enable ($\overline{OE}$)

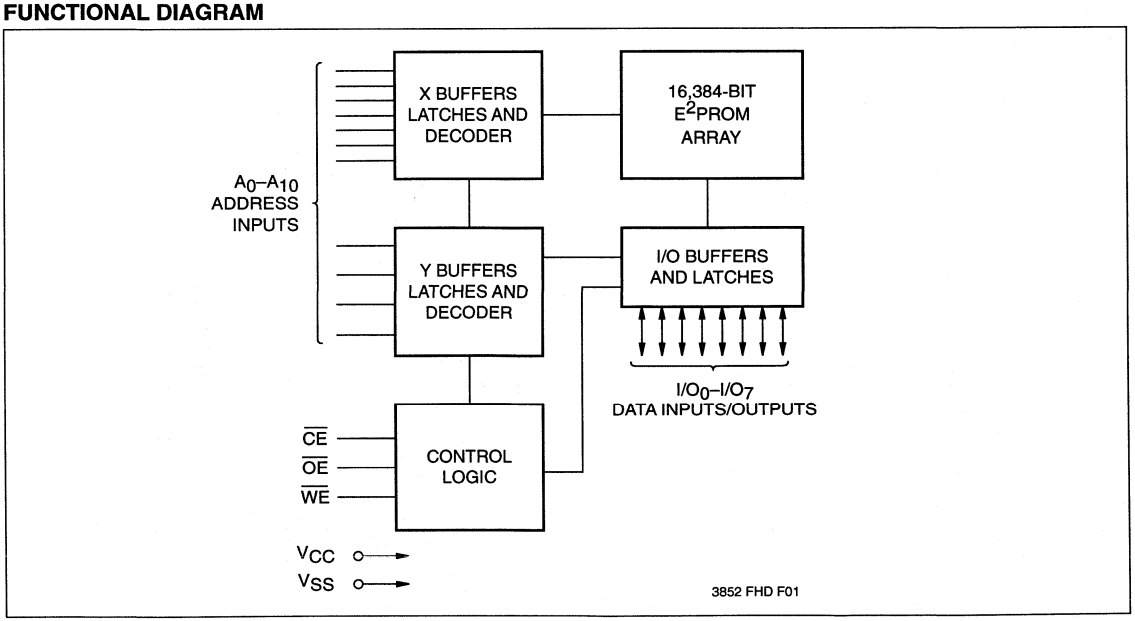
The Output Enable input controls the data output buffers and is used to initiate read operations.

PIN NAMES

Symbol	Description
A_0–A_{10}	Address Inputs
I/O_0–I/O_7	Data Input/Output
$\overline{WE}$	Write Enable
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
V_{CC}	+5V
V_{SS}	Ground
NC	No Connect

3852 PGM T01

FUNCTIONAL DIAGRAM



DEVICE OPERATION

Read

Read operations are initiated by both $\overline{OE}$ and $\overline{CE}$ LOW and $\overline{WE}$ HIGH. The read operation is terminated by either $\overline{CE}$ or $\overline{OE}$ returning HIGH. This two line control architecture eliminates bus contention in a system environment. The data bus will be in a high impedance state when either $\overline{OE}$ or $\overline{CE}$ is HIGH.

Write

Write operations are initiated when both $\overline{CE}$ and $\overline{WE}$ are LOW and $\overline{OE}$ is HIGH. The X2816C supports both a $\overline{CE}$ and $\overline{WE}$ controlled write cycle. That is, the address is latched by the falling edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs last. Similarly, the data is latched internally by the rising edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs first. A byte write operation, once initiated, will automatically continue to completion, typically within 5ms.

Page Write Operation

The page write feature of the X2816C allows the entire memory to be typically written in 640ms. Page write allows two to sixteen bytes of data to be consecutively written to the X2816C prior to the commencement of the internal programming cycle. Although the host system may read data from any other device in the system to transfer to the X2816C, the destination page address of the X2816C should be the same on each subsequent strobe of the $\overline{WE}$ and $\overline{CE}$ inputs. That is, A_4 through A_{10} must be the same for each transfer of data to the X2816C during a page write cycle.

The page write mode can be entered during any write operation. Following the initial byte write cycle, the host can write an additional one to fifteen bytes in the same manner as the first byte was written. Each successive byte load cycle, started by the $\overline{WE}$ HIGH to LOW transition, must begin within 20µs of the falling edge of the preceding $\overline{WE}$. If a subsequent $\overline{WE}$ HIGH to LOW transition is not detected within 20µs, the internal automatic programming cycle will commence. There is no page write window limitation. The page write window is infinitely wide, so long as the host continues to access the device within the byte load cycle time of 20µs.

$\overline{DATA}$ Polling

The X2816C features $\overline{DATA}$ Polling as a method to indicate to the host system that the byte write or page write cycle has completed. $\overline{DATA}$ Polling allows a simple bit test operation to determine the status of the X2816C, eliminating additional interrupt inputs or external hardware. During the internal programming cycle, any attempt to read the last byte written will produce the complement of that data on I/O_7 (i.e., write data = 0xxx xxxx, read data = 1xxx xxxx). Once the programming cycle is complete, I/O_7 will reflect true data.

WRITE PROTECTION

There are three features that protect the nonvolatile data from inadvertent writes.

- Noise Protection—A $\overline{WE}$ pulse which is typically less than 10ns will not initiate a write cycle.
- V_{CC} Sense—All functions are inhibited when V_{CC} is ≤3V, typically.
- Write Inhibit—Holding either $\overline{OE}$ LOW, $\overline{WE}$ HIGH, or $\overline{CE}$ HIGH during power-up and power-down, will inhibit inadvertent writes. Write cycle timing specifications must be observed concurrently.

ENDURANCE

Xicor E²PROMs are designed and tested for applications requiring extended endurance.

SYSTEM CONSIDERATIONS

Because the X2816C is frequently used in large memory arrays, it is provided with a two line control architecture for both read and write operations. Proper usage can provide the lowest possible power dissipation and eliminate the possibility of contention where multiple I/O pins share the same bus.

To gain the most benefit, it is recommended that $\overline{CE}$ be decoded from the address bus and be used as the primary device selection input. Both $\overline{OE}$ and $\overline{WE}$ would then be common among all devices in the array. For a read operation this assures that all deselected devices are in their standby mode and that only the selected device(s) is outputting data on the bus.

Because the X2816C has two power modes, standby and active, proper decoupling of the memory array is of prime concern. Enabling $\overline{CE}$ will cause transient current spikes. The magnitude of these spikes is dependent on the output capacitive loading of the I/Os. Therefore, the larger the array sharing a common bus, the larger the transient spikes. The voltage peaks associated with the current transients can be suppressed by the proper selection and placement of decoupling capacitors. As a minimum, it is recommended that a 0.1µF high frequency ceramic capacitor be used between V_{CC} and V_{SS} at each device. Depending on the size of the array, the value of the capacitor may have to be larger.

In addition, it is recommended that a 4.7µF electrolytic bulk capacitor be placed between V_{CC} and V_{SS} for each eight devices employed in the array. This bulk capacitor is employed to overcome the voltage droop caused by the inductive effects of the PC board traces.

ABSOLUTE MAXIMUM RATINGS*

Temperature under Bias
- X2816C ..... −10°C to +85°C
- X2816CI ..... −65°C to +135°C

Storage Temperature ..... −65°C to +150°C
Voltage on any Pin with
- Respect to V_{SS} ..... −1V to +7V

D.C. Output Current 5mA
Lead Temperature (Soldering, 10 seconds) ..... 300°C

***COMMENT**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	+70°C
Industrial	−40°C	+85°C

3852 PGM T02.2

Supply Voltage	Limits
X2816C	5V ±10%

3852 PGM T03.1

3

D.C. OPERATING CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.(1)	Max.		
I_{CC}	V_{CC} Current (Active)		70	110	mA	$\overline{CE}$ = $\overline{OE}$ = V_{IL} All I/O's = Open Other Inputs = V_{CC}
I_{SB1}	V_{CC} Current (Standby)		35	50	mA	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IL} All I/O's = Open Other Inputs = V_{CC}
I_{LI}	Input Leakage Current			10	µA	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output Leakage Current			10	µA	V_{OUT} = V_{SS} to V_{CC}, $\overline{CE}$ = V_{IH}
V_{IL}(2)	Input LOW Voltage	−1		0.8	V	
V_{IH}(2)	Input HIGH Voltage	2		V_{CC} +1	V	
V_{OL}	Output LOW Voltage			0.4	V	I_{OL} = 2.1mA
V_{OH}	Output HIGH Voltage	2.4			V	I_{OH} = −400µA

3852 PGM T02.2

Notes: (1) Typical values are for T_A = 25°C and nominal supply voltage and are not tested.
(2) V_{IL} min. and V_{IH} max. are for reference only and are not tested.

ENDURANCE AND DATA RETENTION

Parameter	Min.	Max.	Unit
Minimum Endurance	10,000		Cycles/Byte
Data Retention	100		Years

3852 PGM T03

POWER-UP TIMING

Symbol	Parameter	Typ.(1)	Units
t_{PUR}(3)	Power-Up to Read Operation	1	ms
t_{PUW}(3)	Power-Up to Write Operation	5	ms

3852 PGM T04

CAPACITANCE T_A = +25°C, f = 1MHz, V_{CC} = 5V

Symbol	Test	Max.	Units	Conditions
$C_{I/O}$(3)	Input/Output Capacitance	10	pF	$V_{I/O}$ = 0V
C_{IN}(3)	Input Capacitance	6	pF	V_{IN} = 0V

3852 PGM T05.1

A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3V
Input Rise and Fall Times	5ns
Input and Output Timing Levels	1.5V

3852 PGM T06.1

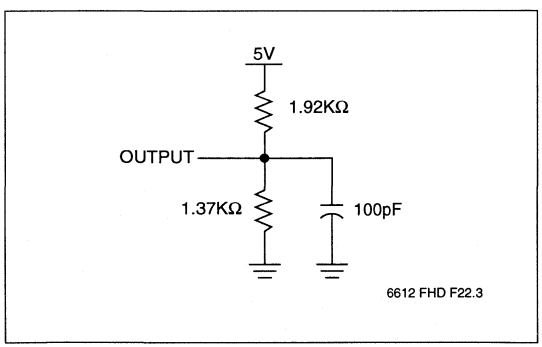
MODE SELECTION

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O	Power
L	L	H	Read	D_{OUT}	Active
L	H	L	Write	D_{IN}	Active
H	X	X	Standby and Write Inhibit	High Z	Standby
X	L	X	Write Inhibit	—	—
X	X	H	Write Inhibit	—	—

3852 PGM T07

Note: (3) This parameter is periodically sampled and not 100% tested.

EQUIVALENT A.C. LOAD CIRCUITS



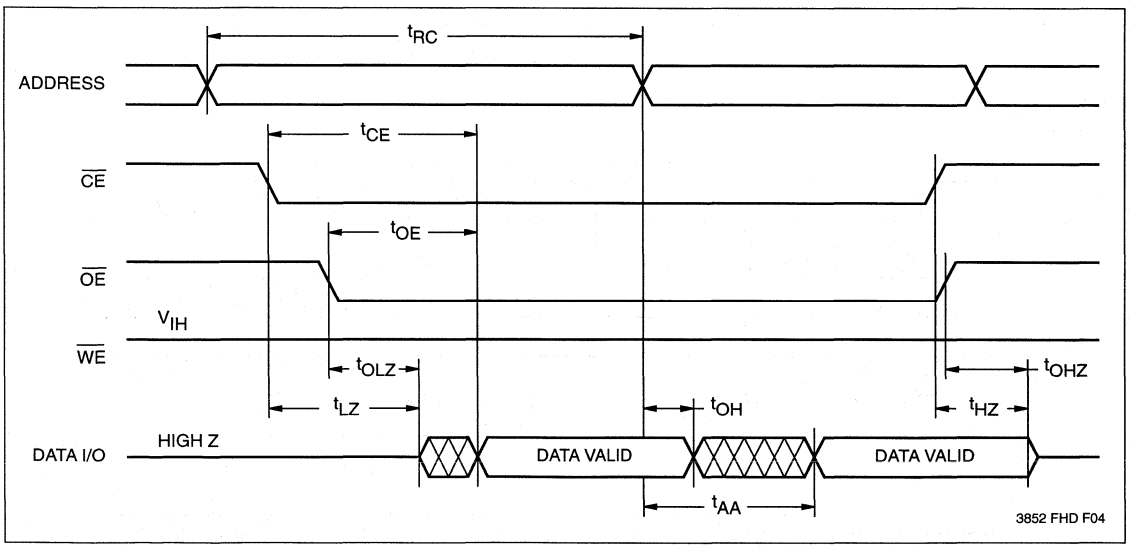
A.C. CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Read Cycle Limits

Symbol	Parameter	X2816C-90		X2816C-12		X2816C-15		X2816C-20		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	90		120		150		200		ns
t_{CE}	Chip Enable Access Time		90		120		150		200	ns
t_{AA}	Address Access Time		90		120		150		200	ns
t_{OE}	Output Enable Access Time		60		60		80		100	ns
t_{LZ}(4)	$\overline{CE}$ LOW to Active Output	0		0		0		0		ns
t_{OLZ}(4)	$\overline{OE}$ LOW to Active Output	0		0		0		0		ns
t_{HZ}(4)	$\overline{CE}$ HIGH to High Z Output		50		60		60		60	ns
t_{OHZ}(4)	$\overline{OE}$ HIGH to High Z Output		50		60		60		60	ns
t_{OH}	Output Hold from Address Change	0		0		0		0		ns

3852 PGM T10.1

Read Cycle



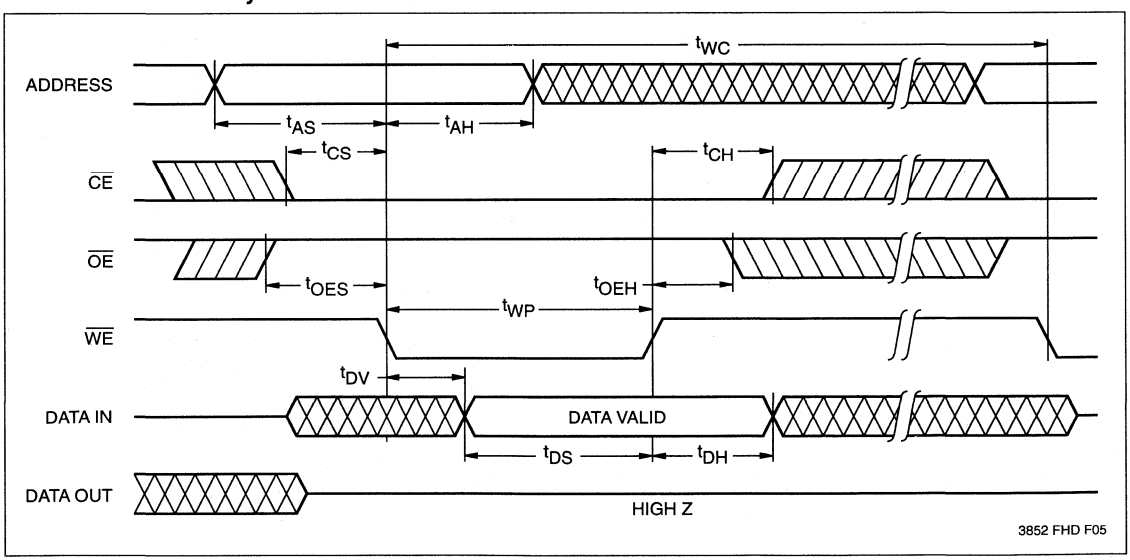
Notes: (4) t_{LZ} min., t_{HZ}, t_{OLZ}, and t_{OHZ} are periodically sampled and not 100% tested. t_{HZ} max. and t_{OHZ} max. are measured from the point when $\overline{CE}$ or $\overline{OE}$ return HIGH (whichever occurs first) to the time when the outputs are no longer driven.

Write Cycle Limits

Symbol	Parameter	X2816C-90		X2816C-12,-15,-20		Units
		Min.	Max.	Min.	Max.	
t_{WC}(5)	Write Cycle Time		10		10	ms
t_{AS}	Address Setup Time	5		5		ns
t_{AH}	Address Hold Time	80		100		ns
t_{CS}	Write Setup Time	0		0		ns
t_{CH}	Write Hold Time	0		0		ns
t_{CW}	$\overline{CE}$ Pulse Width	80		100		ns
t_{OES}	$\overline{OE}$ HIGH Setup Time	10		10		ns
t_{OEH}	$\overline{OE}$ HIGH Hold Time	5		10		ns
t_{WP}	$\overline{WE}$ Pulse Width	80		100		ns
t_{WPH}	$\overline{WE}$ HIGH Recovery	50		50		ns
t_{DV}	Data Valid		100		100	µs
t_{DS}	Data Setup	35		50		ns
t_{DH}	Data Hold	5		10		ns
t_{DW}	Delay to Next Write	10		10		µs
t_{BLC}	Byte Load Cycle	1	100	1	100	µs

3852 PGM T09.1

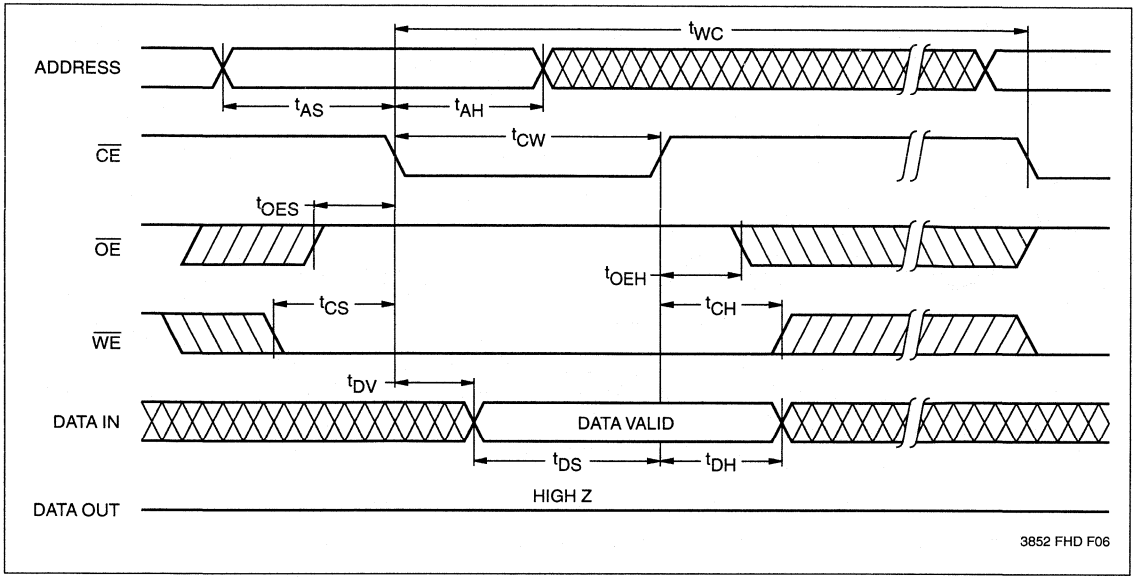
$\overline{WE}$ Controlled Write Cycle



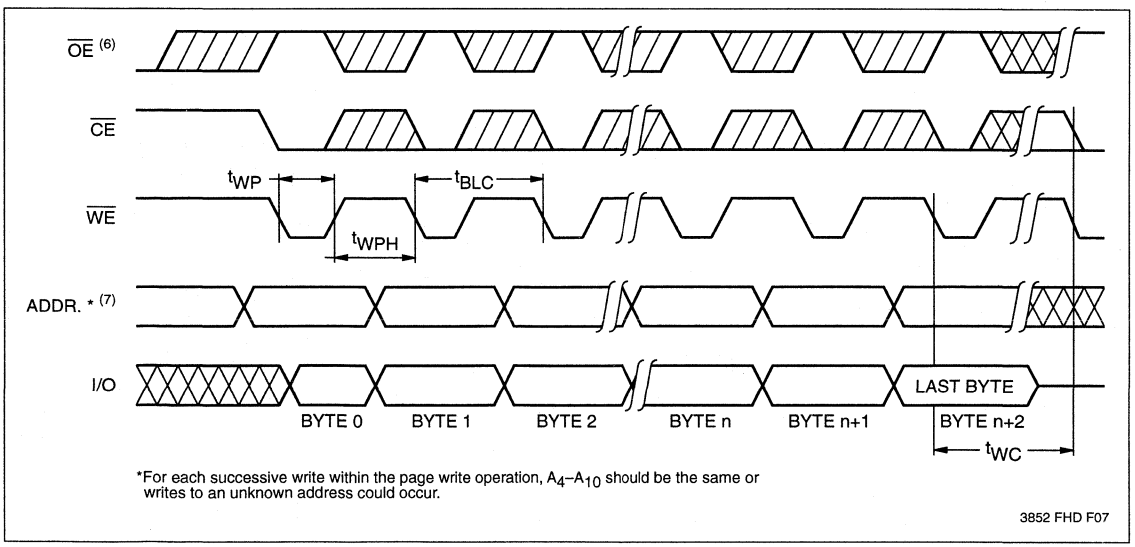
3852 FHD F05

Notes: (5) t_{WC} is the minimum cycle time to be allowed from the system perspective unless polling techniques are used. It is the maximum time the device requires to automatically complete the internal write operation.

$\overline{CE}$ Controlled Write Cycle



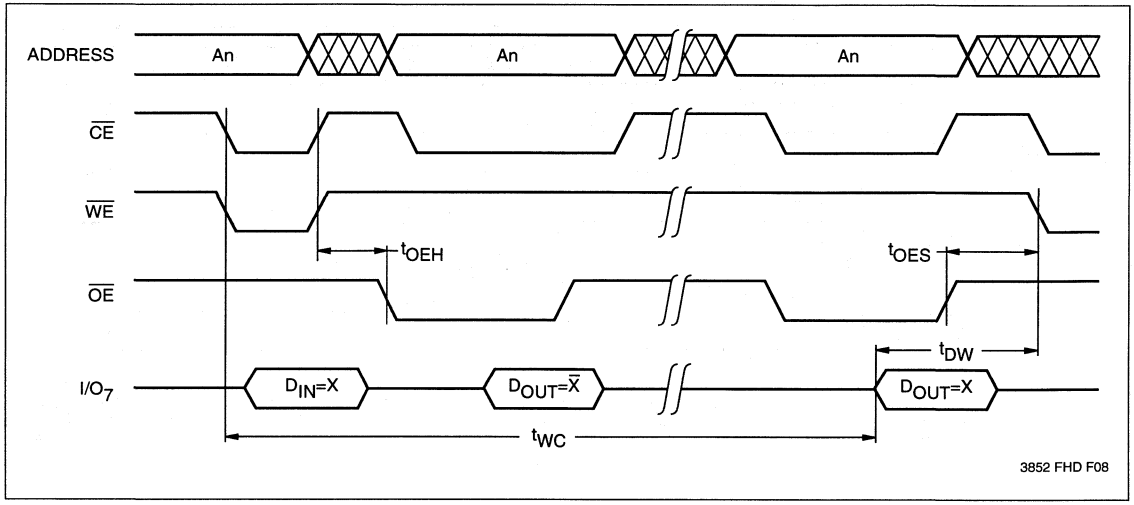
Page Mode Write Cycle



Notes: (6) Between successive byte writes within a page write operation, $\overline{OE}$ can be strobed LOW: e.g. this can be done with $\overline{CE}$ and $\overline{WE}$ HIGH to fetch data from another memory device within the system for the next write; or with $\overline{WE}$ HIGH and $\overline{CE}$ LOW effectively performing a polling operation.

(7) The timings shown above are unique to page write operations. Individual byte load operations within the page write must conform to either the $\overline{CE}$ or $\overline{WE}$ controlled write cycle timing.

$\overline{\text{DATA}}$ Polling Timing Diagram[10]

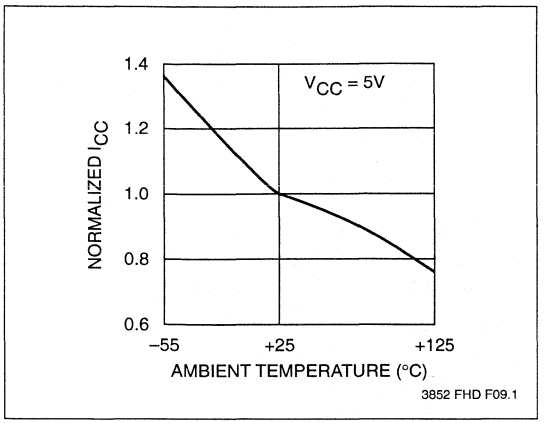


Note: (10) Polling operations are by definition read cycles and are therefore subject to read cycle timings.

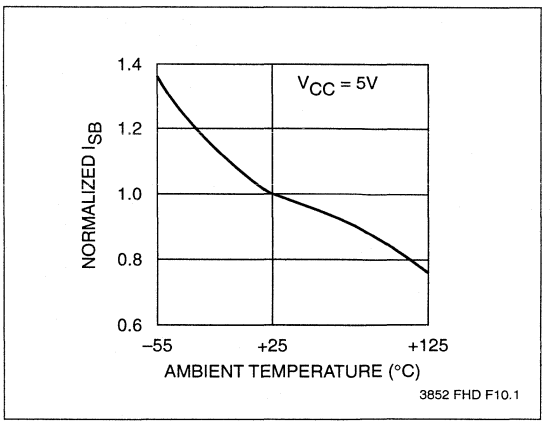
SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

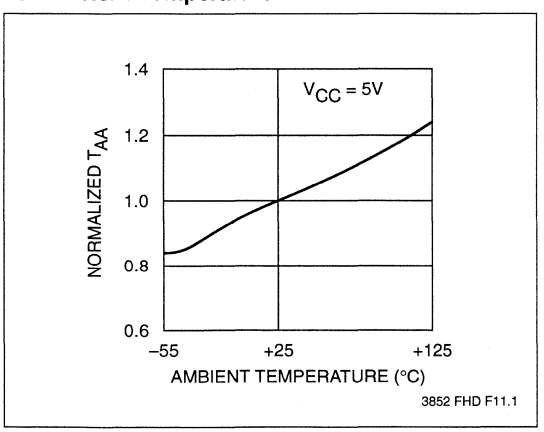
Normalized Active Supply Current vs. Ambient Temperature



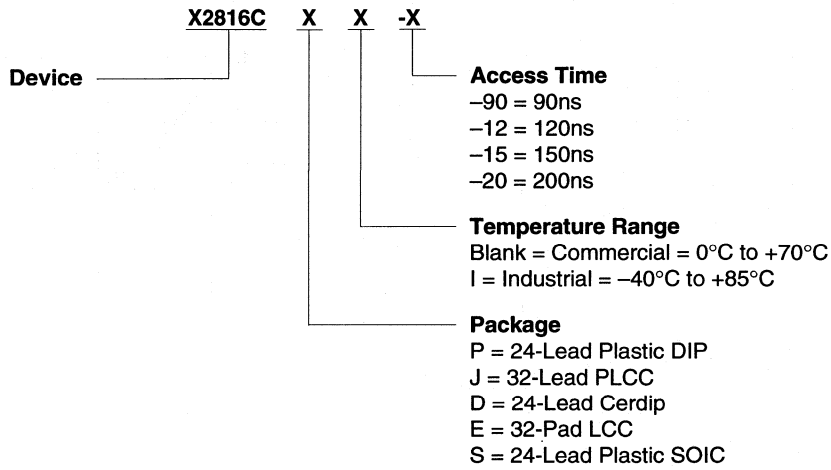
Normalized Standby Supply Current vs. Ambient Temperature



Normalized Access Time vs. Ambient Temperature



ORDERING INFORMATION



5 Volt, Byte Alterable E²PROM

FEATURES

- 150ns Access Time
- Simple Byte and Page Write
  - —Single 5V Supply
    - —No External High Voltages or V_{PP} Control Circuits
  - —Self-Timed
    - —No Erase Before Write
    - —No Complex Programming Algorithms
    - —No Overerase Problem
- Low Power CMOS
  - —60mA Active Current Max.
  - —200µA Standby Current Max.
- Fast Write Cycle Times
  - —64 Byte Page Write Operation
  - —Byte or Page Write Cycle: 5ms Typical
  - —Complete Memory Rewrite: 0.625 sec. Typical
  - —Effective Byte Write Cycle Time: 78µs Typical
- Software Data Protection
- End of Write Detection
  - —$\overline{DATA}$ Polling
  - —Toggle Bit
- High Reliability
  - —Endurance: 100,000 Cycles
  - —Data Retention: 100 Years
- JEDEC Approved Byte-Wide Pinout

DESCRIPTION

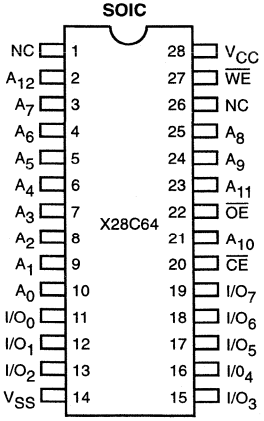
The X28C64 is an 8K x 8 E²PROM, fabricated with Xicor's proprietary, high performance, floating gate CMOS technology. Like all Xicor programmable nonvolatile memories the X28C64 is a 5V only device. The X28C64 features the JEDEC approved pinout for byte-wide memories, compatible with industry standard RAMs.

The X28C64 supports a 64-byte page write operation, effectively providing a 78µs/byte write cycle and enabling the entire memory to be typically written in 0.625 seconds. The X28C64 also features $\overline{DATA}$ and Toggle Bit Polling, a system software support scheme used to indicate the early completion of a write cycle. In addition, the X28C64 includes a user-optional software data protection mode that further enhances Xicor's hardware write protect capability.

Xicor E²PROMs are designed and tested for applications requiring extended endurance. Inherent data retention is greater than 100 years.

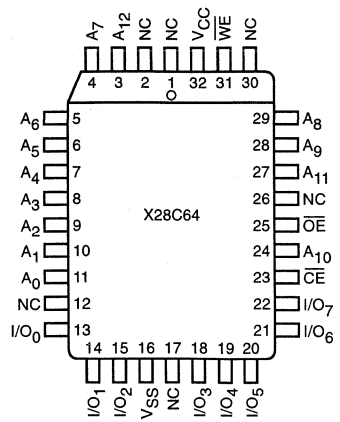
PIN CONFIGURATION

PLASTIC DIP
CERDIP
FLAT PACK
SOIC



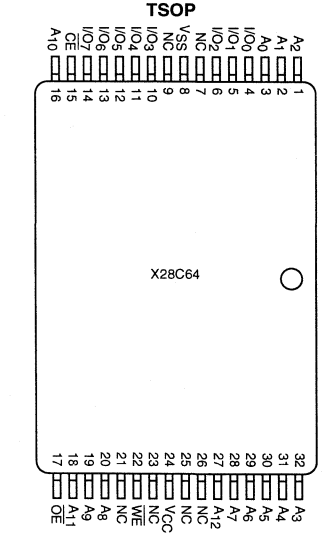
3853 FHD F02

LCC
PLCC



3853 FHD F03

TSOP



3853 FHD F23.1

3853-2.6 1/11/96 T1/C0/D0 NS

PIN DESCRIPTIONS

Addresses (A_0–A_{12})

The Address inputs select an 8-bit memory location during a read or write operation.

Chip Enable ($\overline{CE}$)

The Chip Enable input must be LOW to enable all read/write operations. When $\overline{CE}$ is HIGH, power consumption is reduced.

Output Enable ($\overline{OE}$)

The Output Enable input controls the data output buffers and is used to initiate read operations.

Data In/Data Out (I/O_0–I/O_7)

Data is written to or read from the X28C64 through the I/O pins.

Write Enable ($\overline{WE}$)

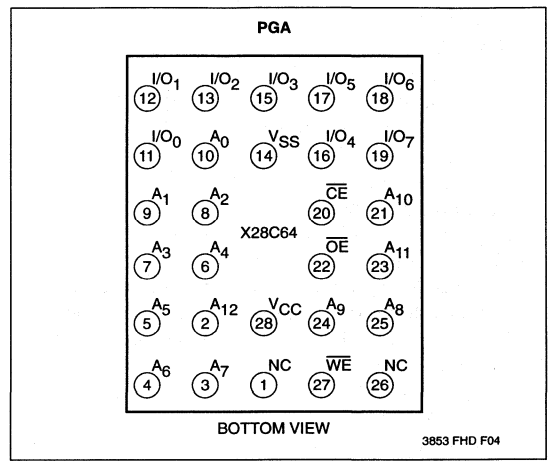
The Write Enable input controls the writing of data to the X28C64.

PIN NAMES

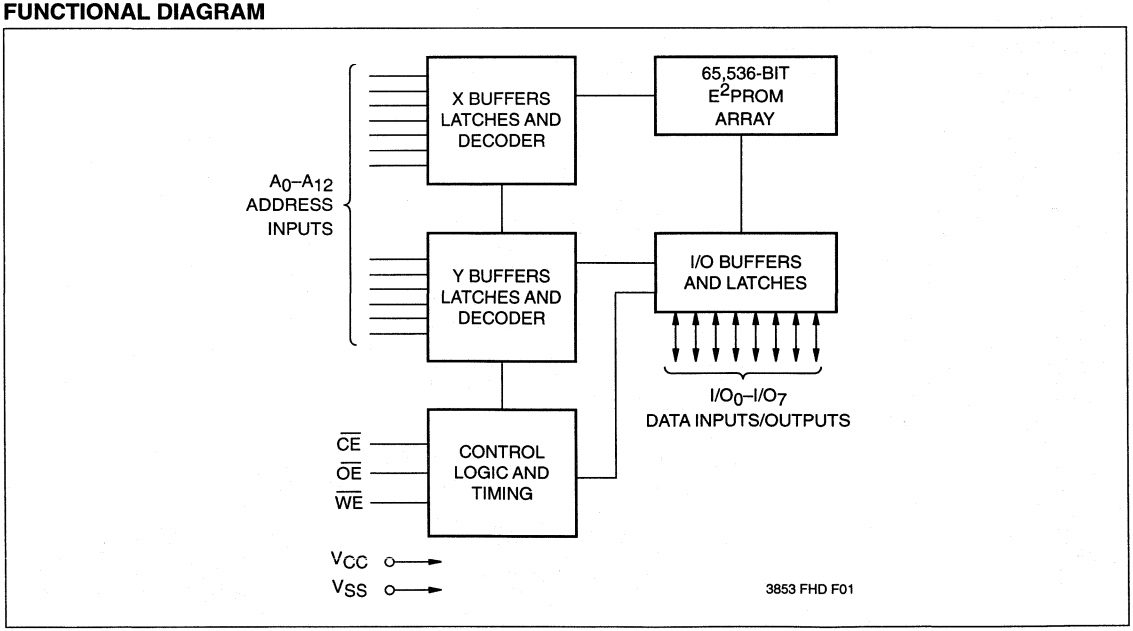
Symbol	Description
A_0–A_{12}	Address Inputs
I/O_0–I/O_7	Data Input/Output
$\overline{WE}$	Write Enable
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
V_{CC}	+5V
V_{SS}	Ground
NC	No Connect

3853 PGM T01

PIN CONFIGURATION



FUNCTIONAL DIAGRAM



DEVICE OPERATION

Read

Read operations are initiated by both $\overline{OE}$ and $\overline{CE}$ LOW. The read operation is terminated by either $\overline{CE}$ or $\overline{OE}$ returning HIGH. This two line control architecture eliminates bus contention in a system environment. The data bus will be in a high impedance state when either $\overline{OE}$ or $\overline{CE}$ is HIGH.

Write

Write operations are initiated when both $\overline{CE}$ and $\overline{WE}$ are LOW and $\overline{OE}$ is HIGH. The X28C64 supports both a $\overline{CE}$ and $\overline{WE}$ controlled write cycle. That is, the address is latched by the falling edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs last. Similarly, the data is latched internally by the rising edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs first. A byte write operation, once initiated, will automatically continue to completion, typically within 5ms.

Page Write Operation

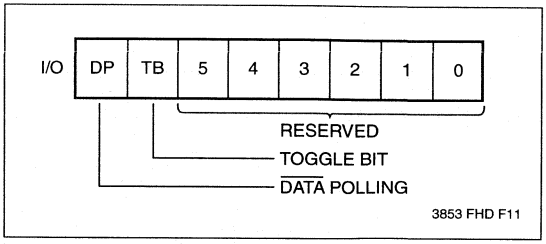
The page write feature of the X28C64 allows the entire memory to be written in 0.625 seconds. Page write allows two to sixty-four bytes of data to be consecutively written to the X28C64 prior to the commencement of the internal programming cycle. The host can fetch data from another device within the system during a page write operation (change the source address), but the page address (A_6 through A_{12}) for each subsequent valid write cycle to the part during this operation must be the same as the initial page address.

The page write mode can be initiated during any write operation. Following the initial byte write cycle, the host can write an additional one to sixty-three bytes in the same manner as the first byte was written. Each successive byte load cycle, started by the $\overline{WE}$ HIGH to LOW transition, must begin within 100µs of the falling edge of the preceding $\overline{WE}$. If a subsequent $\overline{WE}$ HIGH to LOW transition is not detected within 100µs, the internal automatic programming cycle will commence. There is no page write window limitation. Effectively the page write window is infinitely wide, so long as the host continues to access the device within the byte load cycle time of 100µs.

Write Operation Status Bits

The X28C64 provides the user two write operation status bits. These can be used to optimize a system write cycle time. The status bits are mapped onto the I/O bus as shown in Figure 1.

Figure 1. Status Bit Assignment



$\overline{DATA}$ Polling (I/O_7)

The X28C64 features $\overline{DATA}$ Polling as a method to indicate to the host system that the byte write or page write cycle has completed. $\overline{DATA}$ Polling allows a simple bit test operation to determine the status of the X28C64, eliminating additional interrupt inputs or external hardware. During the internal programming cycle, any attempt to read the last byte written will produce the complement of that data on I/O_7 (i.e. write data = 0xxx xxxx, read data = 1xxx xxxx). Once the programming cycle is complete, I/O_7 will reflect true data. Note: If the X28C64 is in the protected state and an illegal write operation is attempted $\overline{DATA}$ Polling will not operate.

Toggle Bit (I/O_6)

The X28C64 also provides another method for determining when the internal write cycle is complete. During the internal programming cycle I/O_6 will toggle from HIGH to LOW and LOW to HIGH on subsequent attempts to read the device. When the internal cycle is complete the toggling will cease and the device will be accessible for additional read or write operations.

$\overline{DATA}$ Polling I/O_7

Figure 2. $\overline{DATA}$ Polling Bus Sequence

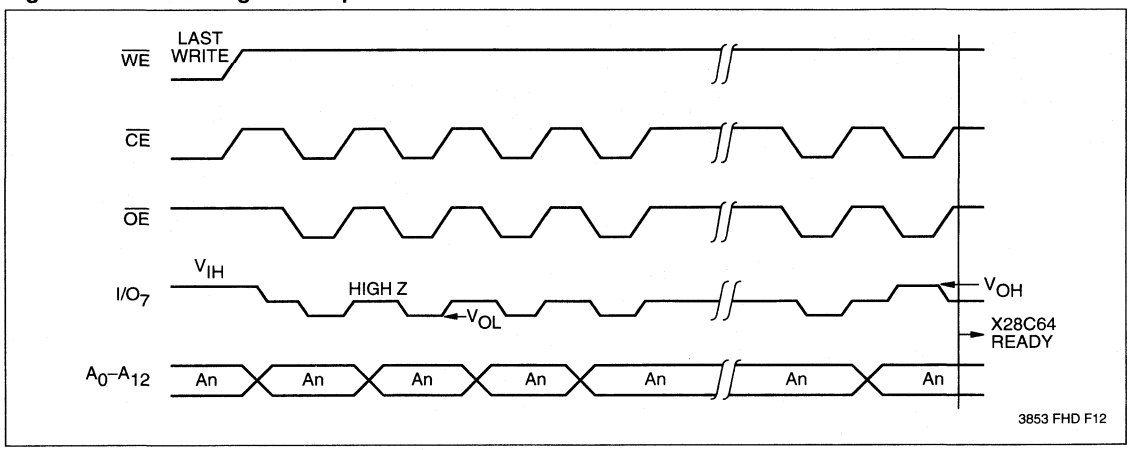
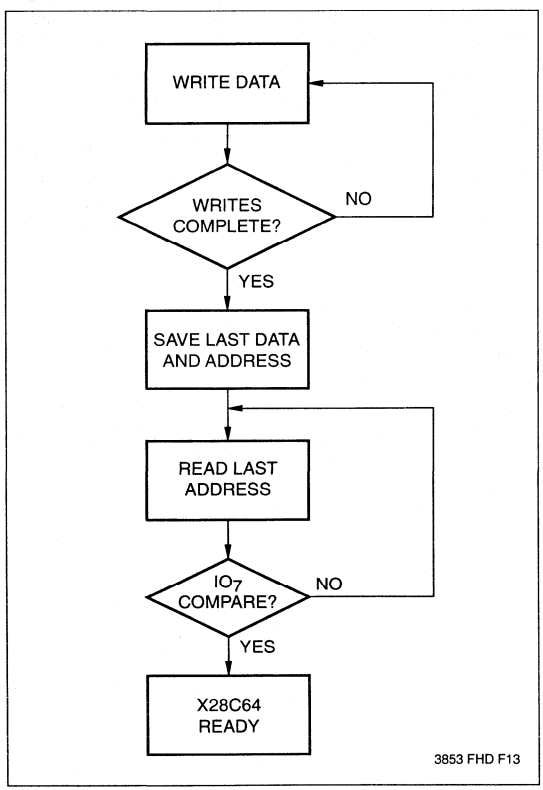


Figure 3. $\overline{DATA}$ Polling Software Flow



$\overline{DATA}$ Polling can effectively halve the time for writing to the X28C64. The timing diagram in Figure 2 illustrates the sequence of events on the bus. The software flow diagram in Figure 3 illustrates one method of implementing the routine.

The Toggle Bit I/O_6

Figure 4. Toggle Bit Bus Sequence

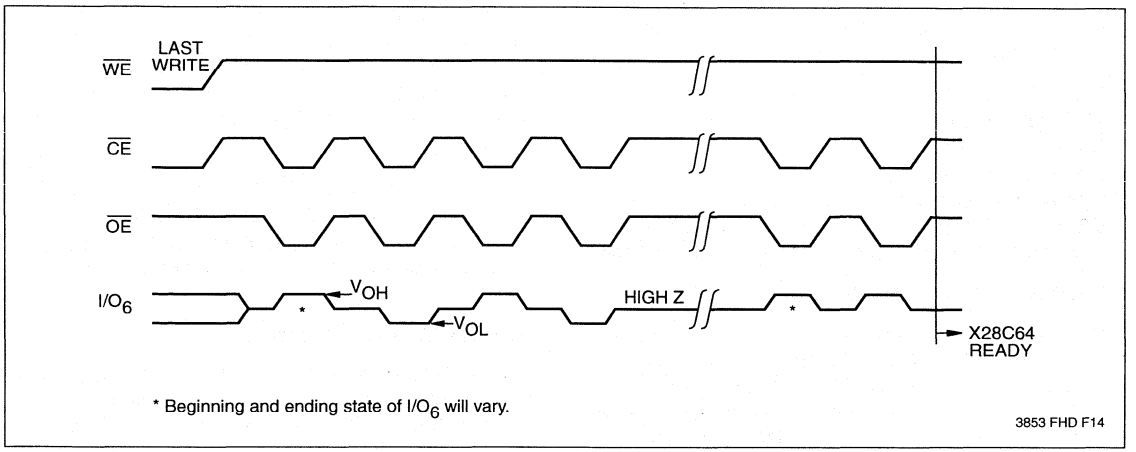
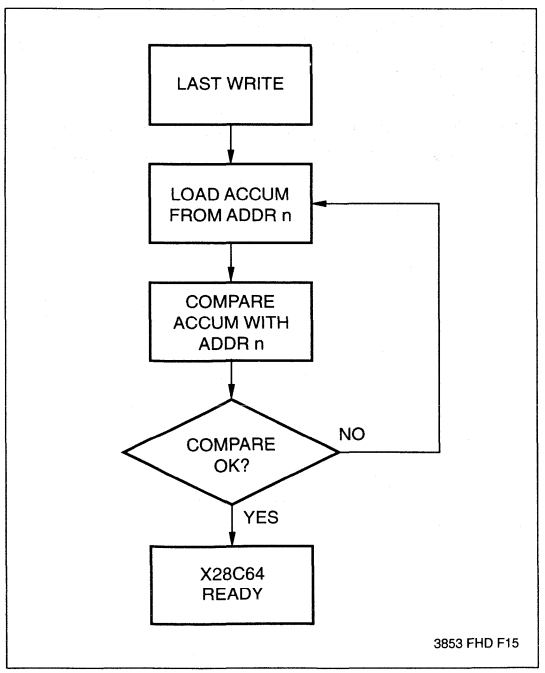


Figure 5. Toggle Bit Software Flow



The Toggle Bit can eliminate the software housekeeping chore of saving and fetching the last address and data written to a device in order to implement $\overline{DATA}$ Polling. This can be especially helpful in an array comprised of multiple X28C64 memories that is frequently updated. Toggle Bit Polling can also provide a method for status checking in multiprocessor applications. The timing diagram in Figure 4 illustrates the sequence of events on the bus. The software flow diagram in Figure 5 illustrates a method for polling the Toggle Bit.

HARDWARE DATA PROTECTION

The X28C64 provides three hardware features (compatible with X2864A) that protect nonvolatile data from inadvertent writes.

- Noise Protection—A $\overline{WE}$ pulse typically less than 20ns will not initiate a write cycle.
- Default V_{CC} Sense—All write functions are inhibited when V_{CC} is ≤3V typically.
- Write Inhibit—Holding either $\overline{OE}$ LOW, $\overline{WE}$ HIGH, or $\overline{CE}$ HIGH will prevent an inadvertent write cycle during power-up and power-down, maintaining data integrity.

SOFTWARE DATA PROTECTION

The X28C64 offers a software controlled data protection feature. The X28C64 is shipped from Xicor with the software data protection NOT ENABLED; that is, the device will be in the standard operating mode. In this mode data should be protected during power-up/-down operations through the use of external circuits. The host would then have open read and write access of the device once V_{CC} was stable.

The X28C64 can be automatically protected during power-up and power-down without the need for external circuits by employing the software data protection feature. The internal software data protection circuit is enabled after the first write operation utilizing the software algorithm. This circuit is nonvolatile and will remain set for the life of the device unless the reset command is issued.

Once the software protection is enabled, the X28C64 is also protected from inadvertent and accidental writes in the powered-on state. That is, the software algorithm must be issued prior to writing additional data to the device.

SOFTWARE ALGORITHM

Selecting the software data protection mode requires the host system to precede data write operations by a series of three write operations to three specific addresses. Refer to Figure 6 and 7 for the sequence. The three-byte sequence opens the page write window enabling the host to write from one to sixty-four bytes of data*. Once the page load cycle has been completed, the device will automatically be returned to the data protected state.

*Note: *Once the three-byte sequence is issued it must be followed by a valid byte or page write operation.*

Software Data Protection

Figure 6. Timing Sequence—Byte or Page Write

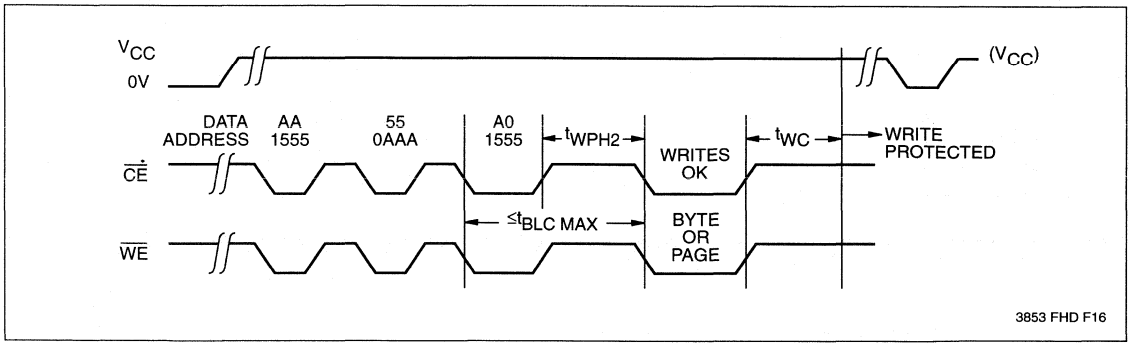
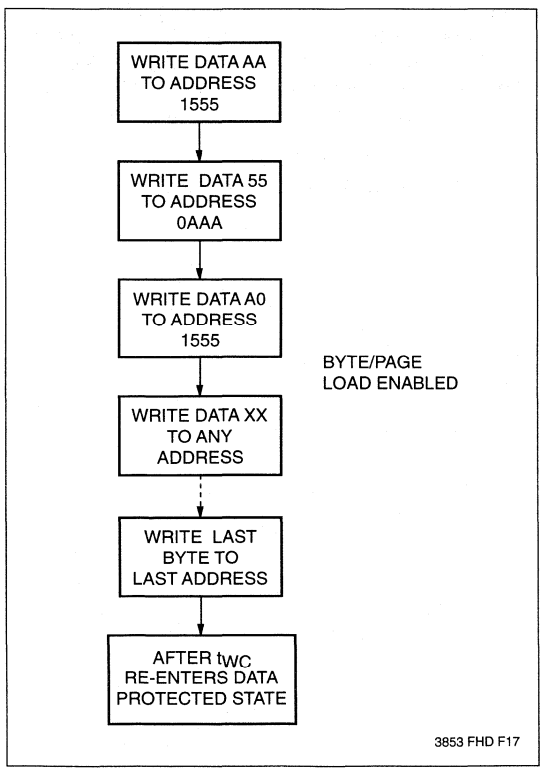


Figure 7. Write Sequence for Software Data Protection



Regardless of whether the device has previously been protected or not, once the software data protection algorithm is used and data has been written, the X28C64 will automatically disable further writes unless another command is issued to cancel it. If no further commands are issued the X28C64 will be write protected during power-down and after any subsequent power-up.

Note: Once initiated, the sequence of write operations should not be interrupted.

3

Resetting Software Data Protection

Figure 8. Reset Software Data Protection Timing Sequence

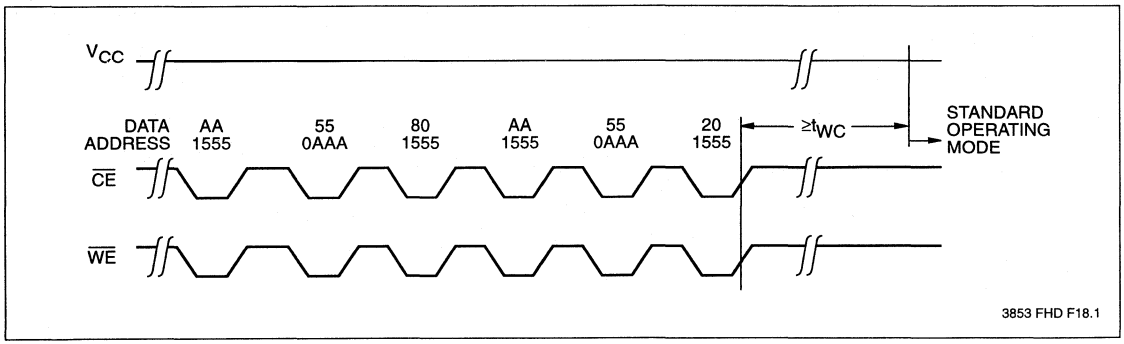
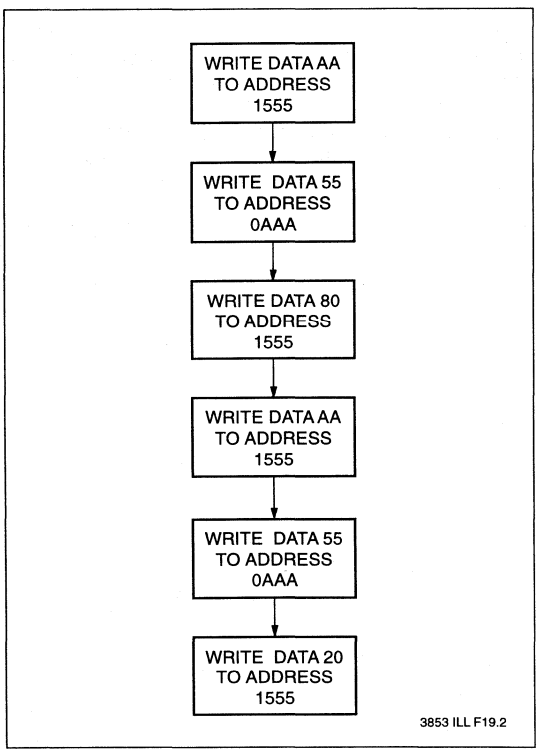


Figure 9. Software Sequence to Deactivate Software Data Protection



In the event the user wants to deactivate the software data protection feature for testing or reprogramming in an E^2PROM programmer, the following six step algorithm will reset the internal protection circuit. After t_{WC}, the X28C64 will be in standard operating mode.

Note: Once initiated, the sequence of write operations should not be interrupted.

SYSTEM CONSIDERATIONS

Because the X28C64 is frequently used in large memory arrays, it is provided with a two line control architecture for both read and write operations. Proper usage can provide the lowest possible power dissipation and eliminate the possibility of contention where multiple I/O pins share the same bus.

To gain the most benefit it is recommended that $\overline{CE}$ be decoded from the address bus and be used as the primary device selection input. Both $\overline{OE}$ and $\overline{WE}$ would then be common among all devices in the array. For a read operation, this assures that all deselected devices are in their standby mode and that only the selected device(s) is outputting data on the bus.

Because the X28C64 has two power modes, standby and active, proper decoupling of the memory array is of prime concern. Enabling $\overline{CE}$ will cause transient current spikes. The magnitude of these spikes is dependent on the output capacitive loading of the I/Os. Therefore, the larger the array sharing a common bus, the larger the transient spikes. The voltage peaks associated with the current transients can be suppressed by the proper selection and placement of decoupling capacitors. As a minimum, it is recommended that a 0.1μF high frequency ceramic capacitor be used between V_{CC} and V_{SS} at each device. Depending on the size of the array, the value of the capacitor may have to be larger.

In addition, it is recommended that a 4.7μF electrolytic bulk capacitor be placed between V_{CC} and V_{SS} for each eight devices employed in the array. This bulk capacitor is employed to overcome the voltage droop caused by the inductive effects of the PC board traces.

ABSOLUTE MAXIMUM RATINGS*

Temperature under Bias
- X28C64 ..... −10°C to +85°C
- X28C64I, X28C64M ..... −65°C to +135°C

Storage Temperature ..... −65°C to +150°C

Voltage on any Pin with
- Respect to V_{SS} ..... −1V to +7V

D.C. Output Current 5mA

Lead Temperature
- (Soldering, 10 seconds) ..... 300°C

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	+70°C
Industrial	−40°C	+85°C
Military	−55°C	+125°C

3853 PGM T02.1

Supply Voltage	Limits
X28C64	5V ±10%

3853 PGM T03.1

D.C. OPERATING CHARACTERISTICS (Over the recommended operating conditions, unless otherwise specified)

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.(1)	Max.		
I_{CC}	V_{CC} Current (Active) (TTL Inputs)		30	60	mA	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}, All I/O's = Open, Address Inputs = 0.4V/2.4V Levels @ f = 5MHz
I_{SB1}	V_{CC} Current (Standby) (TTL Inputs)		1	2	mA	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IL} All I/O's = Open, Other Inputs = V_{IH}
I_{SB2}	V_{CC} Current (Standby) (CMOS Inputs)		100	200	µA	$\overline{CE}$ = $\overline{WE}$ = V_{CC} − 0.3V All I/O's = Open, Other Inputs = Don't Care
I_{LI}	Input Leakage Current			10	µA	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output Leakage Current			10	µA	V_{OUT} = V_{SS} to V_{CC}, $\overline{CE}$ = V_{IH}
V_{IL}(2)	Input LOW Voltage	−1		0.8	V	
V_{IH}(2)	Input HIGH Voltage	2		V_{CC} + 1	V	
V_{OL}	Output LOW Voltage			0.4	V	I_{OL} = 2.1mA
V_{OH}	Output HIGH Voltage	2.4			V	I_{OH} = −400µA

3853 PGM T04.2

Notes: (1) Typical values are for T_A = 25°C and nominal supply voltage and are not tested.
(2) V_{IL} min. and V_{IH} max. are for reference only and are not tested.

ENDURANCE AND DATA RETENTION

Parameter	Min.	Units
Minimum Endurance	100,000	Cycles
Data Retention	100	Years

3853 PGM T05.1

POWER-UP TIMING

Symbol	Parameter	Typ.(1)	Units
t_{PUR}(3)	Power-up to Read Operation	100	µs
t_{PUW}(3)	Power-up to Write Operation	5	ms

3853 PGM T06

CAPACITANCE T_A = +25°C, f = 1MHz, V_{CC} = 5V

Symbol	Parameter	Max.	Units	Test Conditions
$C_{I/O}$(3)	Input/Output Capacitance	10	pF	$V_{I/O}$ = 0V
C_{IN}(3)	Input Capacitance	6	pF	V_{IN} = 0V

3853 PGM T07.1

A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3V
Input Rise and Fall Times	10ns
Input and Output Timing Levels	1.5V

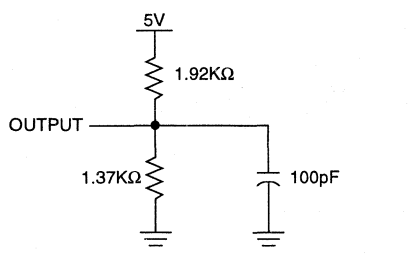
3853 PGM T08.1

MODE SELECTION

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O	Power
L	L	H	Read	D_{OUT}	Active
L	H	L	Write	D_{IN}	Active
H	X	X	Standby and Write Inhibit	High Z	Standby
X	L	X	Write Inhibit	—	—
X	X	H	Write Inhibit	—	—

3853 PGM T09

EQUIVALENT A.C. LOAD CIRCUIT



3853 FHD F20.3

SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

Note: (3) This parameter is periodically sampled and not 100% tested.

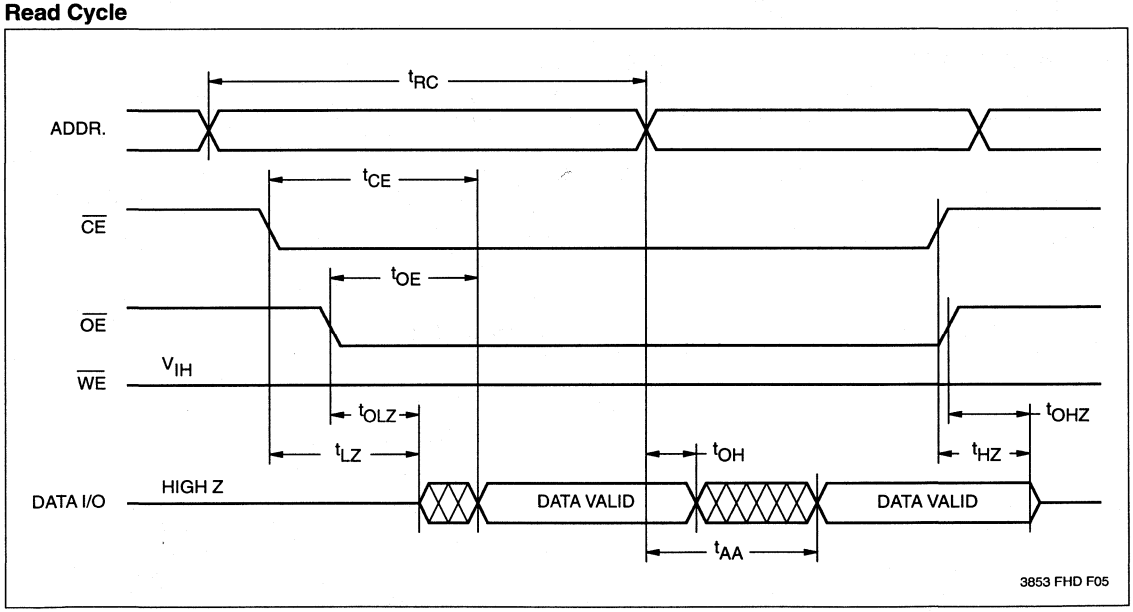
A.C. CHARACTERISTICS (Over recommended operating conditions, unless otherwise specified.)

Read Cycle Limits

Symbol	Parameter	X28C64-15		X28C64-20		X28C64-25		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	150		200		250		ns
t_{CE}	Chip Enable Access Time		150		200		250	ns
t_{AA}	Address Access Time		150		200		250	ns
t_{OE}	Output Enable Access Time		70		80		100	ns
t_{LZ}(4)	$\overline{CE}$ LOW to Active Output	0		0		0		ns
t_{OLZ}(4)	$\overline{OE}$ LOW to Active Output	0		0		0		ns
t_{HZ}(4)	$\overline{CE}$ HIGH to High Z Output		50		50		50	ns
t_{OHZ}(4)	$\overline{OE}$ HIGH to High Z Output		50		50		50	ns
t_{OH}	Output Hold from Address Change	0		0		0		ns

3856 PGM T10.1

Read Cycle



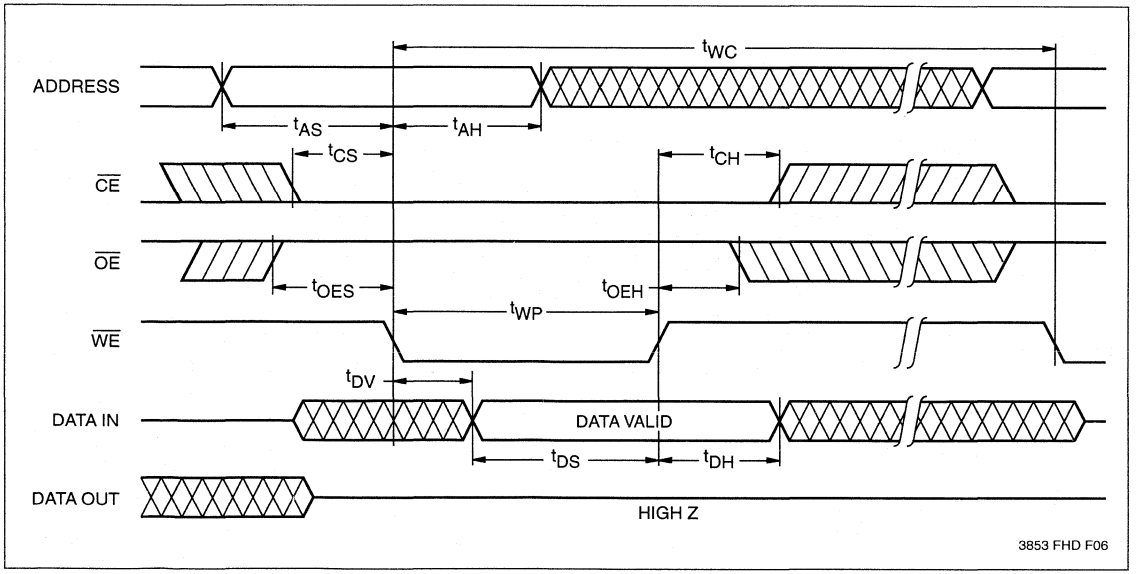
Notes: (4) t_{LZ} min., t_{HZ}, t_{OLZ} min., and t_{OHZ} are periodically sampled and not 100% tested. t_{HZ} max. and t_{OHZ} max. are measured, with C_L = 5pF, from the point when $\overline{CE}$ or $\overline{OE}$ return HIGH (whichever occurs first) to the time when the outputs are no longer driven.

WRITE CYCLE LIMITS

Symbol	Parameter	Min.(7)	Typ.(1)	Max.	Units
t_{WC}(5)	Write Cycle Time		5	10	ms
t_{AS}	Address Setup Time	0			ns
t_{AH}	Address Hold Time	100			ns
t_{CS}	Write Setup Time	0			ns
t_{CH}	Write Hold Time	0			ns
t_{CW}	$\overline{CE}$ Pulse Width	100			ns
t_{OES}	$\overline{OE}$ HIGH Setup Time	10			ns
t_{OEH}	$\overline{OE}$ HIGH Hold Time	10			ns
t_{WP}	$\overline{WE}$ Pulse Width	100			ns
t_{WPH}	$\overline{WE}$ HIGH Recovery	200			ns
t_{WPH2}(6)	SDP $\overline{WE}$ Recovery	1			µs
t_{DV}	Data Valid			1	µs
t_{DS}	Data Setup	50			ns
t_{DH}	Data Hold	10			ns
t_{DW}	Delay to Next Write	10			µs
t_{BLC}(7)	Byte Load Cycle	1		100	µs

3853 PGM T11.1

$\overline{WE}$ Controlled Write Cycle



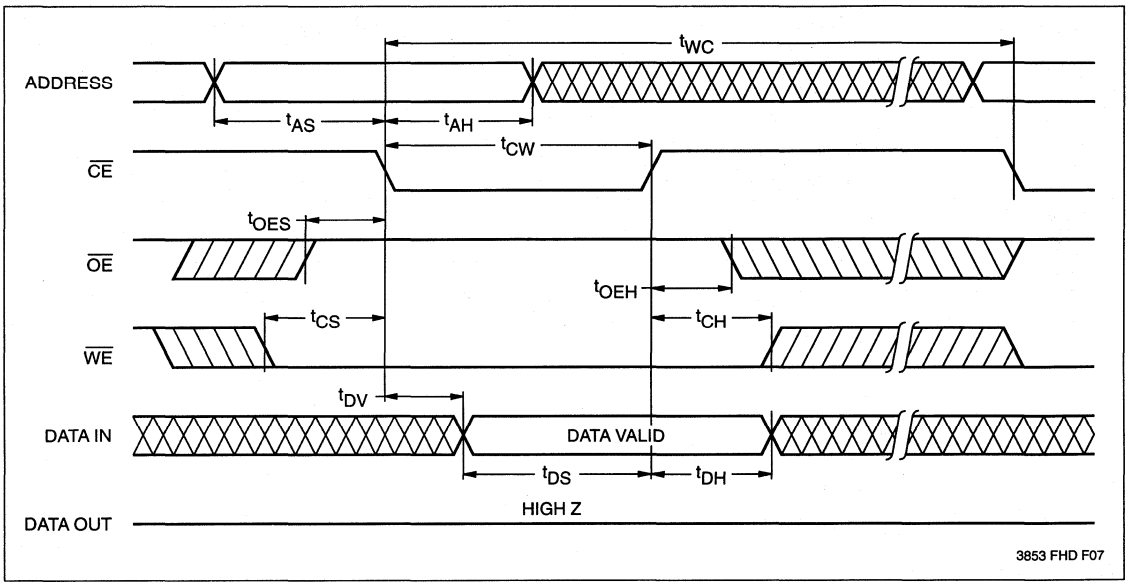
3853 FHD F06

Notes: (5) t_{WC} is the minimum cycle time to be allowed from the system perspective unless polling techniques are used. It is the maximum time the device requires to automatically complete the internal write operation.

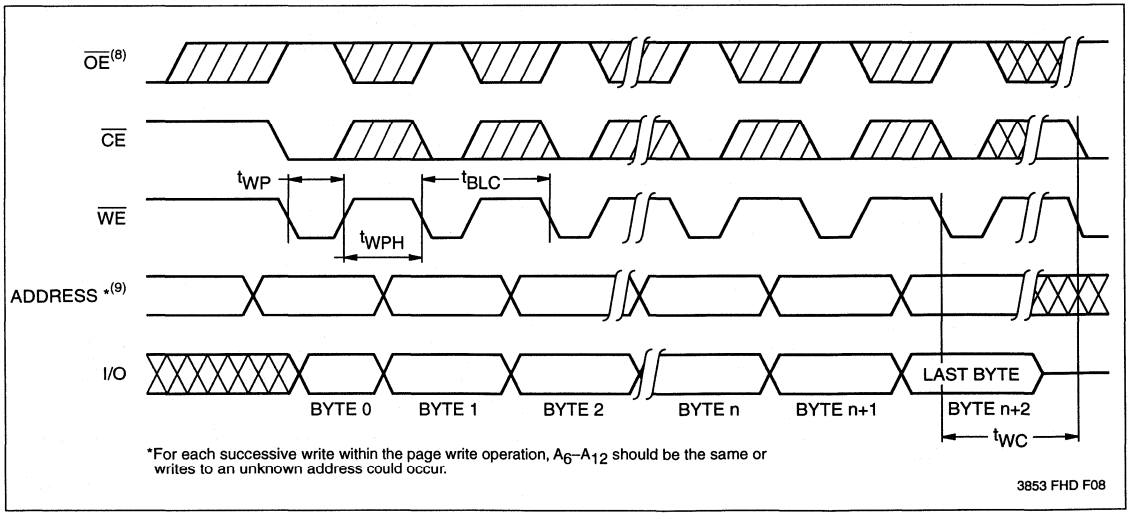
(6) t_{WPH} is the normal page write operation $\overline{WE}$ recovery time. t_{WPH2} is the $\overline{WE}$ recovery time needed only after the end of issuing the three-byte SDP command sequence and before writing the first byte of data to the array. Refer to Figure 6 which illustrates the t_{WPH2} requirement.

(7) For faster t_{WC} and t_{BLC} times, refer to X28HC64.

$\overline{CE}$ Controlled Write Cycle



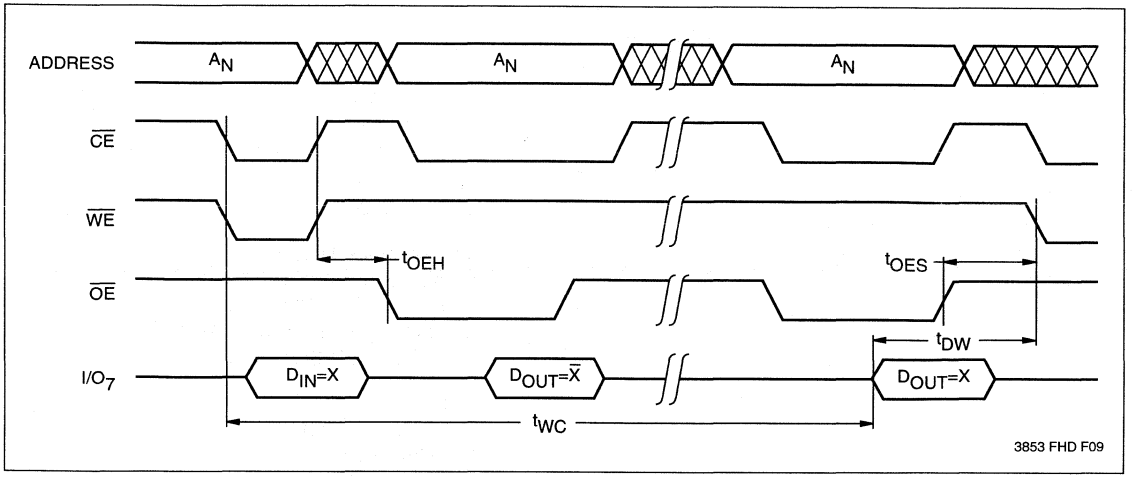
Page Write Cycle



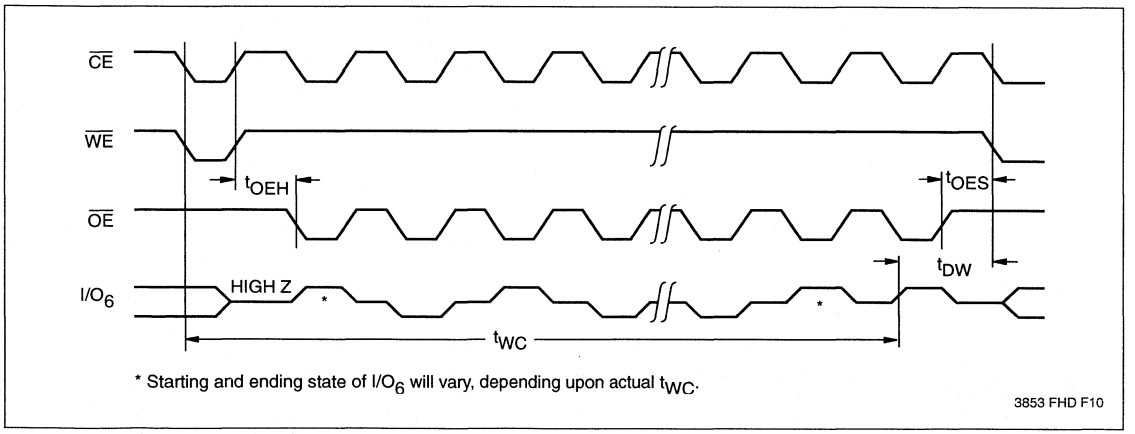
Notes: (8) Between successive byte writes within a page write operation, $\overline{OE}$ can be strobed LOW: e.g. this can be done with $\overline{CE}$ and $\overline{WE}$ HIGH to fetch data from another memory device within the system for the next write; or with $\overline{WE}$ HIGH and $\overline{CE}$ LOW effectively performing a polling operation.

(9) The timings shown above are unique to page write operations. Individual byte load operations within the page write must conform to either the $\overline{CE}$ or $\overline{WE}$ controlled write cycle timing.

$\overline{DATA}$ Polling Timing Diagram(10)

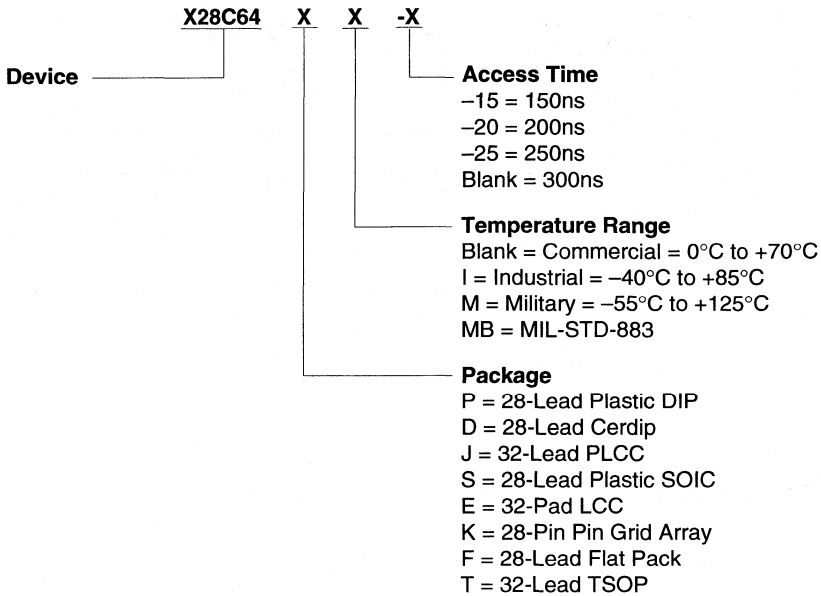


Toggle Bit Timing Diagram(10)



Note: (10) Polling operations are by definition read cycles and are therefore subject to read cycle timings.

ORDERING INFORMATION



5 Volt, Byte Alterable E²PROM

FEATURES

- 55ns Access Time
- Simple Byte and Page Write
  - —Single 5V Supply
    - —No External High Voltages or V_{PP} Control Circuits
  - —Self-Timed
    - —No Erase Before Write
    - —No Complex Programming Algorithms
    - —No Overerase Problem
- Low Power CMOS
  - —40 mA Active Current Max.
  - —200 µA Standby Current Max.
- Fast Write Cycle Times
  - —64 Byte Page Write Operation
  - —Byte or Page Write Cycle: 2ms Typical
  - —Complete Memory Rewrite: 0.25 sec. Typical
  - —Effective Byte Write Cycle Time: 32µs Typical
- Software Data Protection
- End of Write Detection
  - —$\overline{DATA}$ Polling
  - —Toggle Bit
- High Reliability
  - —Endurance: 100,000 Cycles
  - —Data Retention: 100 Years
- JEDEC Approved Byte-Wide Pinout

DESCRIPTION

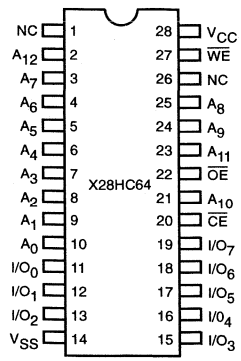
The X28HC64 is an 8K x 8 E²PROM, fabricated with Xicor's proprietary, high performance, floating gate CMOS technology. Like all Xicor programmable nonvolatile memories the X28HC64 is a 5V only device. The X28HC64 features the JEDEC approved pinout for byte-wide memories, compatible with industry standard RAMs.

The X28HC64 supports a 64-byte page write operation, effectively providing a 32µs/byte write cycle and enabling the entire memory to be typically written in 0.25 seconds. The X28HC64 also features $\overline{DATA}$ Polling and Toggle Bit Polling, two methods providing early end of write detection. In addition, the X28HC64 includes a user-optional software data protection mode that further enhances Xicor's hardware write protect capability.

Xicor E²PROMs are designed and tested for applications requiring extended endurance. Inherent data retention is greater than 100 years.

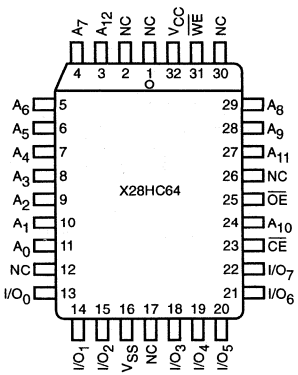
PIN CONFIGURATION

PLASTIC DIP
CERDIP
SOIC



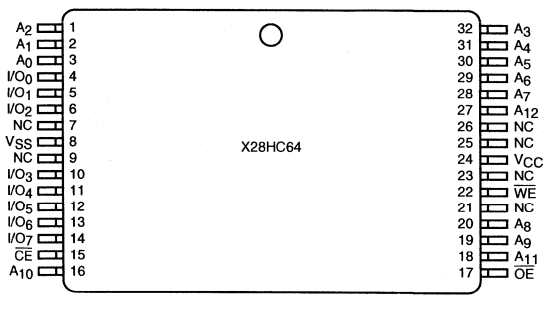
3857 FHD F02

LCC
PLCC



3857 FHD F03

TSOP



3857 ILL F22

PIN DESCRIPTIONS

Addresses (A_0–A_{12})

The Address inputs select an 8-bit memory location during a read or write operation.

Chip Enable ($\overline{CE}$)

The Chip Enable input must be LOW to enable all read/write operations. When $\overline{CE}$ is HIGH, power consumption is reduced.

Output Enable ($\overline{OE}$)

The Output Enable input controls the data output buffers and is used to initiate read operations.

Data In/Data Out (I/O_0–I/O_7)

Data is written to or read from the X28HC64 through the I/O pins.

Write Enable ($\overline{WE}$)

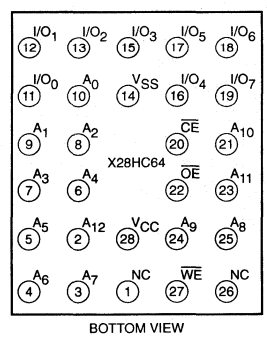
The Write Enable input controls the writing of data to the X28HC64.

PIN NAMES

Symbol	Description
A_0–A_{12}	Address Inputs
I/O_0–I/O_7	Data Input/Output
$\overline{WE}$	Write Enable
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
V_{CC}	+5V
V_{SS}	Ground
NC	No Connect

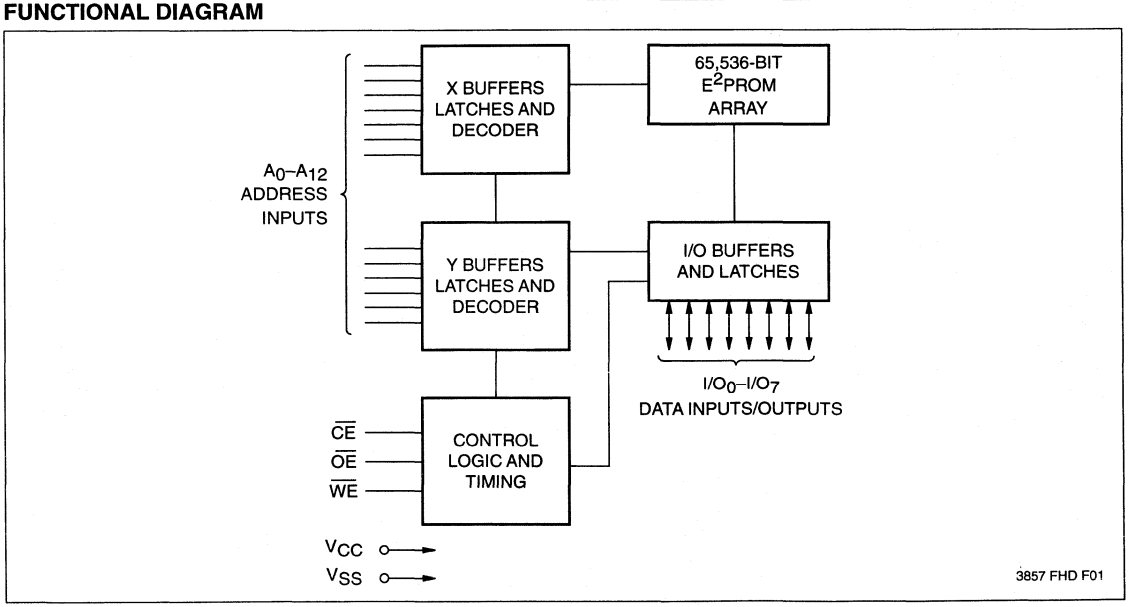
3857 PGM T01

PIN CONFIGURATION



3857 FHD F04

FUNCTIONAL DIAGRAM



3857 FHD F01

DEVICE OPERATION

Read

Read operations are initiated by both $\overline{OE}$ and $\overline{CE}$ LOW. The read operation is terminated by either $\overline{CE}$ or $\overline{OE}$ returning HIGH. This two line control architecture eliminates bus contention in a system environment. The data bus will be in a high impedance state when either $\overline{OE}$ or $\overline{CE}$ is HIGH.

Write

Write operations are initiated when both $\overline{CE}$ and $\overline{WE}$ are LOW and $\overline{OE}$ is HIGH. The X28HC64 supports both a $\overline{CE}$ and $\overline{WE}$ controlled write cycle. That is, the address is latched by the falling edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs last. Similarly, the data is latched internally by the rising edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs first. A byte write operation, once initiated, will automatically continue to completion, typically within 2ms.

Page Write Operation

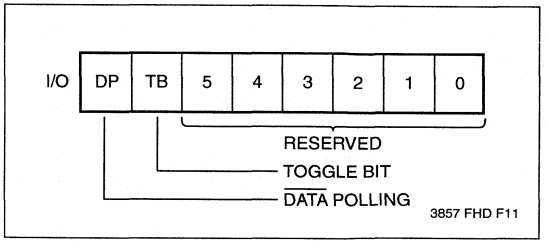
The page write feature of the X28HC64 allows the entire memory to be written in 0.25 seconds. Page write allows two to sixty-four bytes of data to be consecutively written to the X28HC64 prior to the commencement of the internal programming cycle. The host can fetch data from another device within the system during a page write operation (change the source address), but the page address (A_6 through A_{12}) for each subsequent valid write cycle to the part during this operation must be the same as the initial page address.

The page write mode can be initiated during any write operation. Following the initial byte write cycle, the host can write an additional one to sixty-three bytes in the same manner as the first byte was written. Each successive byte load cycle, started by the $\overline{WE}$ HIGH to LOW transition, must begin within 100µs of the falling edge of the preceding $\overline{WE}$. If a subsequent $\overline{WE}$ HIGH to LOW transition is not detected within 100µs, the internal automatic programming cycle will commence. There is no page write window limitation. Effectively the page write window is infinitely wide, so long as the host continues to access the device within the byte load cycle time of 100µs.

Write Operation Status Bits

The X28HC64 provides the user two write operation status bits. These can be used to optimize a system write cycle time. The status bits are mapped onto the I/O bus as shown in Figure 1.

Figure 1. Status Bit Assignment



$\overline{DATA}$ Polling (I/O_7)

The X28HC64 features $\overline{DATA}$ Polling as a method to indicate to the host system that the byte write or page write cycle has completed. $\overline{DATA}$ Polling allows a simple bit test operation to determine the status of the X28HC64, eliminating additional interrupt inputs or external hardware. During the internal programming cycle, any attempt to read the last byte written will produce the complement of that data on I/O_7 (i.e. write data = 0xxx xxxx, read data = 1xxx xxxx). Once the programming cycle is complete, I/O_7 will reflect true data.

Toggle Bit (I/O_6)

The X28HC64 also provides another method for determining when the internal write cycle is complete. During the internal programming cycle I/O_6 will toggle from HIGH to LOW and LOW to HIGH on subsequent attempts to read the device. When the internal cycle is complete the toggling will cease and the device will be accessible for additional read or write operations.

$\overline{DATA}$ POLLING I/O_7

Figure 2. $\overline{DATA}$ Polling Bus Sequence

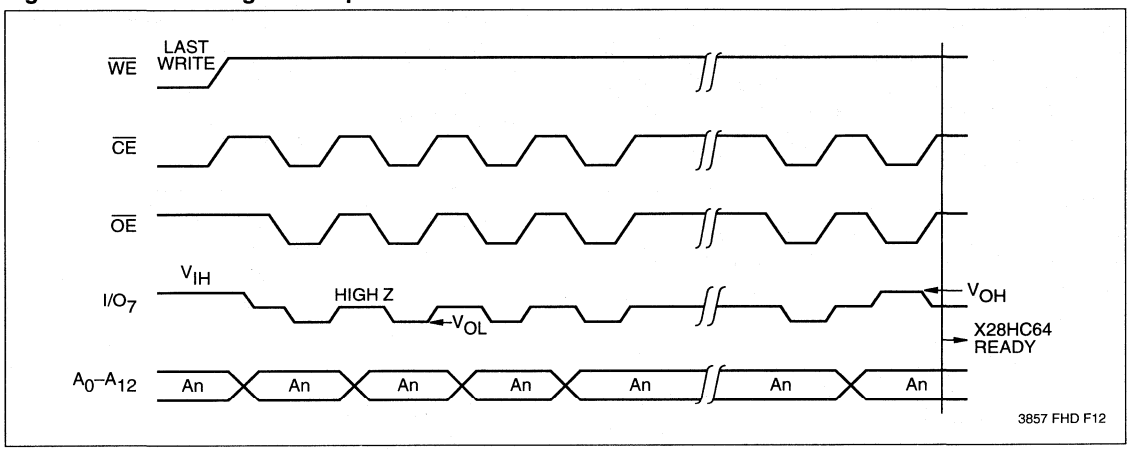
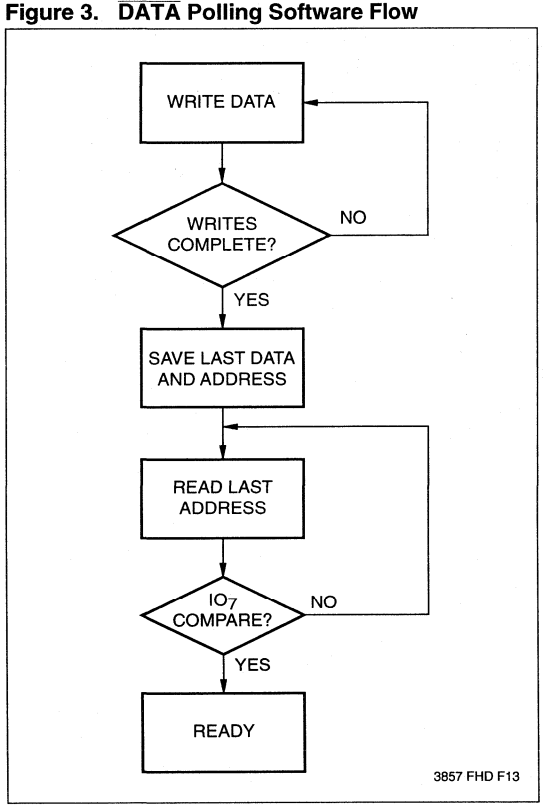


Figure 3. $\overline{DATA}$ Polling Software Flow



$\overline{DATA}$ Polling can effectively reduce the time for writing to the X28HC64. The timing diagram in Figure 2 illustrates the sequence of events on the bus. The software flow diagram in Figure 3 illustrates one method of implementing the routine.

THE TOGGLE BIT I/O_6

Figure 4. Toggle Bit Bus Sequence

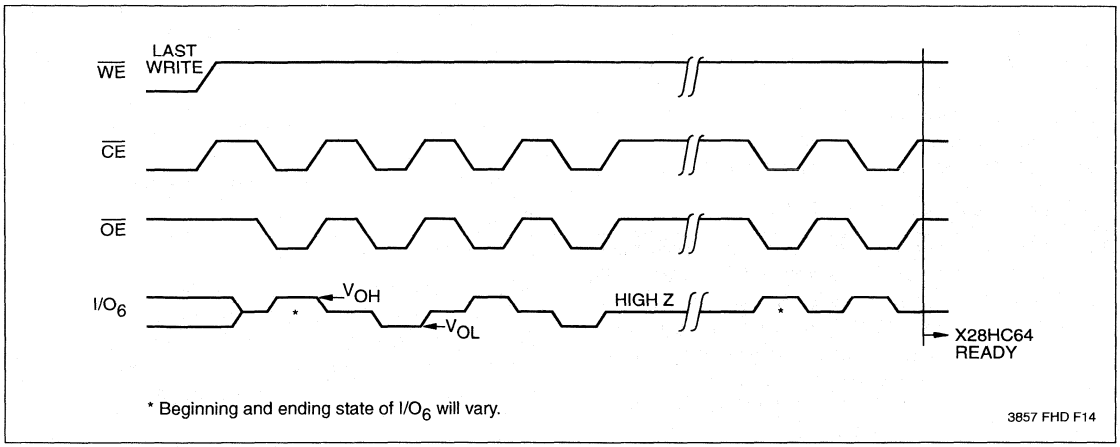
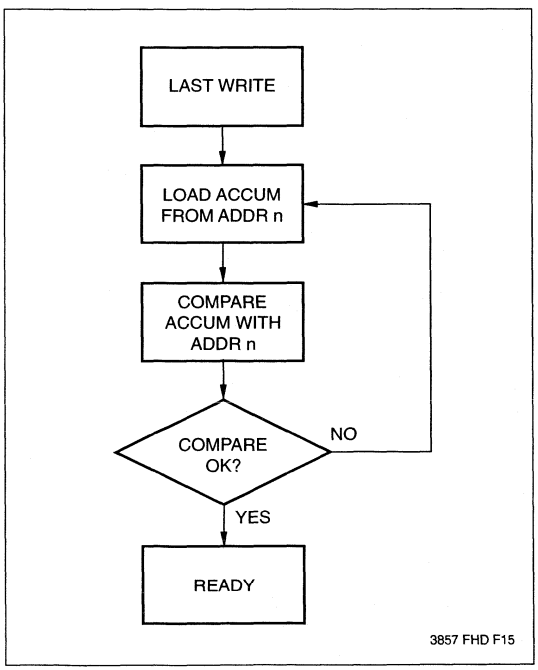


Figure 5. Toggle Bit Software Flow



The Toggle Bit can eliminate the software housekeeping chore of saving and fetching the last address and data written to a device in order to implement $\overline{DATA}$ Polling. This can be especially helpful in an array comprised of multiple X28HC64 memories that is frequently updated. Toggle Bit Polling can also provide a method for status checking in multiprocessor applications. The timing diagram in Figure 4 illustrates the sequence of events on the bus. The software flow diagram in Figure 5 illustrates a method for polling the Toggle Bit.

HARDWARE DATA PROTECTION

The X28HC64 provides two hardware features that protect nonvolatile data from inadvertent writes.

- Default V_{CC} Sense—All write functions are inhibited when V_{CC} is ≤3V typically.
- Write Inhibit—Holding either $\overline{OE}$ LOW, $\overline{WE}$ HIGH, or $\overline{CE}$ HIGH will prevent an inadvertent write cycle during power-up and power-down, maintaining data integrity.

SOFTWARE DATA PROTECTION

The X28HC64 offers a software controlled data protection feature. The X28HC64 is shipped from Xicor with the software data protection NOT ENABLED; that is, the device will be in the standard operating mode. In this mode data should be protected during power-up/-down operations through the use of external circuits. The host would then have open read and write access of the device once V_{CC} was stable.

The X28HC64 can be automatically protected during power-up and power-down without the need for external circuits by employing the software data protection feature. The internal software data protection circuit is enabled after the first write operation utilizing the software algorithm. This circuit is nonvolatile and will remain set for the life of the device unless the reset command is issued.

Once the software protection is enabled, the X28HC64 is also protected from inadvertent and accidental writes in the powered-up state. That is, the software algorithm must be issued prior to writing additional data to the device.

SOFTWARE ALGORITHM

Selecting the software data protection mode requires the host system to precede data write operations by a series of three write operations to three specific addresses. Refer to Figure 6 and 7 for the sequence. The three-byte sequence opens the page write window enabling the host to write from one to sixty-four bytes of data. Once the page load cycle has been completed, the device will automatically be returned to the data protected state.

SOFTWARE DATA PROTECTION

Figure 6. Timing Sequence—Byte or Page Write

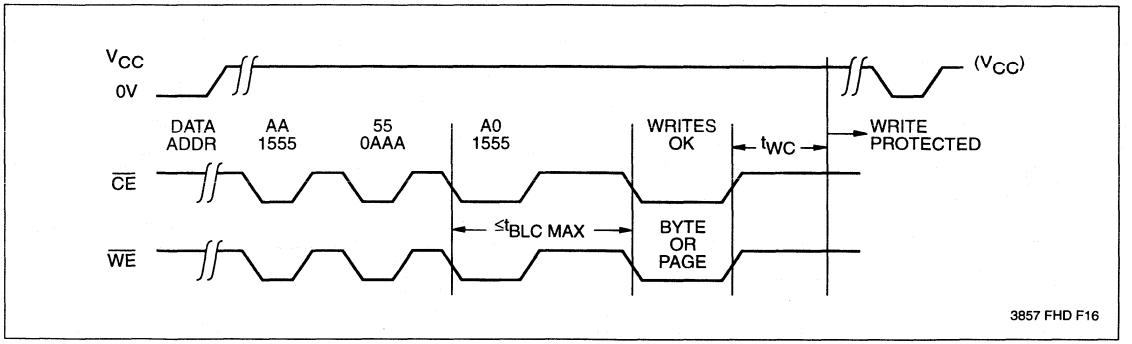
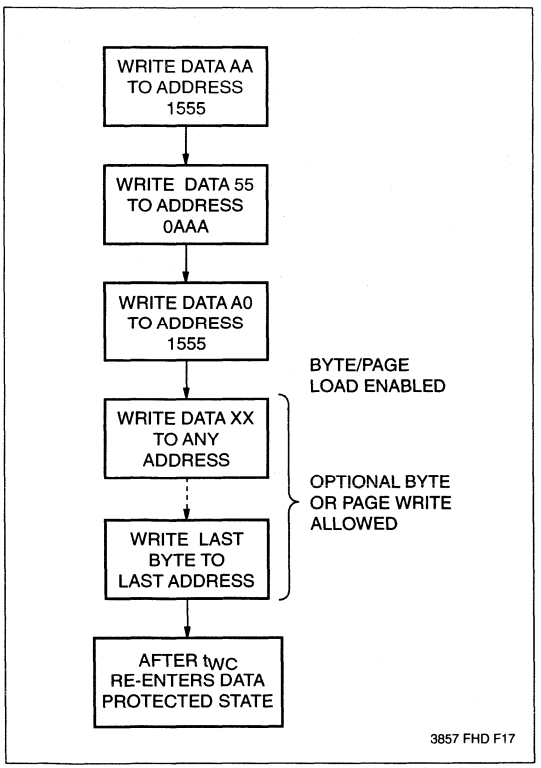


Figure 7. Write Sequence for Software Data Protection



Regardless of whether the device has previously been protected or not, once the software data protection algorithm is used, the X28HC64 will automatically disable further writes unless another command is issued to deactivate it. If no further commands are issued the X28HC64 will be write protected during power-down and after any subsequent power-up.

Note: Once initiated, the sequence of write operations should not be interrupted.

3

RESETTING SOFTWARE DATA PROTECTION

Figure 8. Reset Software Data Protection Timing Sequence

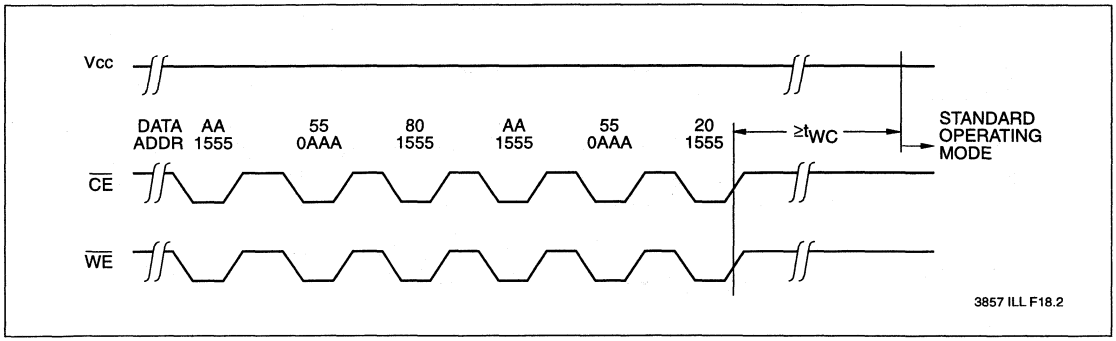
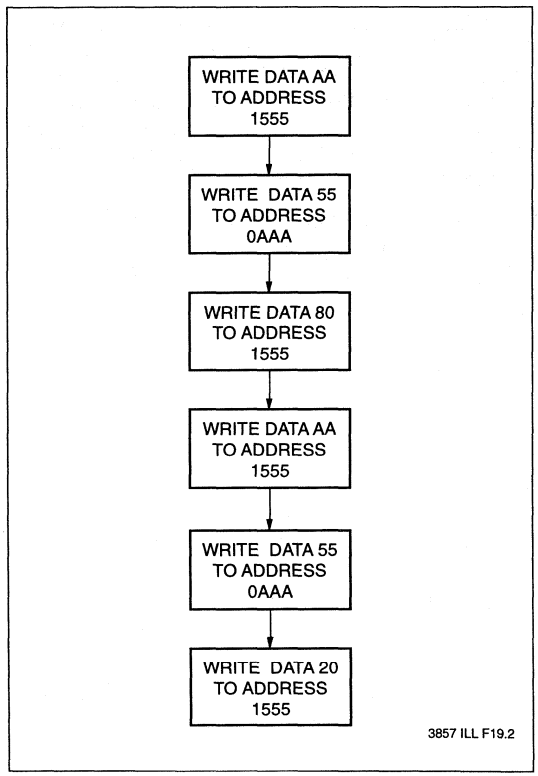


Figure 9. Software Sequence to Deactivate Software Data Protection



In the event the user wants to deactivate the software data protection feature for testing or reprogramming in an E^2PROM programmer, the following six step algorithm will reset the internal protection circuit. After t_{WC}, the X28HC64 will be in standard operating mode.

Note: Once initiated, the sequence of write operations should not be interrupted.

SYSTEM CONSIDERATIONS

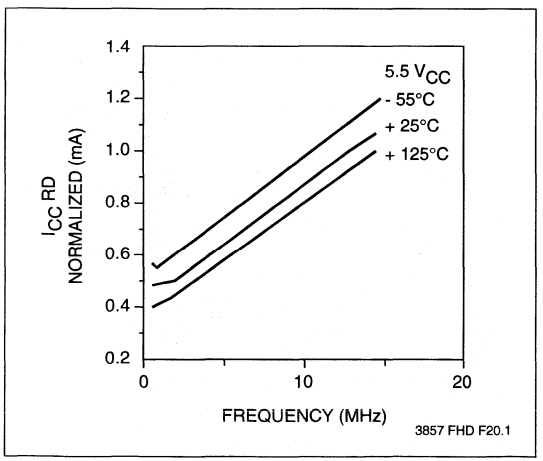
Because the X28HC64 is frequently used in large memory arrays, it is provided with a two line control architecture for both read and write operations. Proper usage can provide the lowest possible power dissipation and eliminate the possibility of contention where multiple I/O pins share the same bus.

To gain the most benefit it is recommended that $\overline{CE}$ be decoded from the address bus and be used as the primary device selection input. Both $\overline{OE}$ and $\overline{WE}$ would then be common among all devices in the array. For a read operation, this assures that all deselected devices are in their standby mode and that only the selected device(s) is outputting data on the bus.

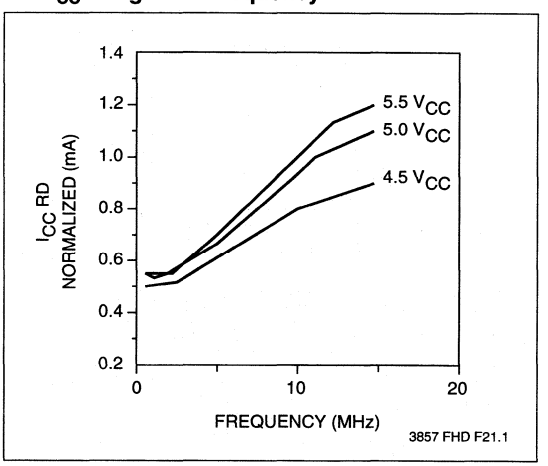
Because the X28HC64 has two power modes, standby and active, proper decoupling of the memory array is of prime concern. Enabling $\overline{CE}$ will cause transient current spikes. The magnitude of these spikes is dependent on the output capacitive loading of the I/Os. Therefore, the larger the array sharing a common bus, the larger the transient spikes. The voltage peaks associated with the current transients can be suppressed by the proper selection and placement of decoupling capacitors. As a minimum, it is recommended that a 0.1μF high frequency ceramic capacitor be used between V_{CC} and V_{SS} at each device. Depending on the size of the array, the value of the capacitor may have to be larger.

In addition, it is recommended that a 4.7μF electrolytic bulk capacitor be placed between V_{CC} and V_{SS} for each eight devices employed in the array. This bulk capacitor is employed to overcome the voltage droop caused by the inductive effects of the PC board traces.

Normalized I_{CC}(RD) by Temperature Over Frequency



Normalized I_{CC}(RD) @ 25% Over the V_{CC} Range and Frequency



ABSOLUTE MAXIMUM RATINGS*

Temperature under Bias
- X28HC64 ..... −10°C to +85°C
- X28HC64I, X28HC64M ..... −65°C to +135°C

Storage Temperature ..... −65°C to +150°C

Voltage on any Pin with
- Respect to V_{SS} ..... −1V to +7V

D.C. Output Current 5mA

Lead Temperature
- (Soldering, 10 seconds) ..... 300°C

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	+70°C
Industrial	−40°C	+85°C
Military	−55°C	+125°C

3857 PGM T02.1

Supply Voltage	Limits
X28HC64	5V ±10%

3857 PGM T03.1

D.C. OPERATING CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.(1)	Max.		
I_{CC}	V_{CC} Current (Active) (TTL Inputs)		15	40	mA	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}, All I/O's = Open, Address Inputs = TTL Levels @ f = 10 MHz
I_{SB1}	V_{CC} Current (Standby) (TTL Inputs)		1	2	mA	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IL} All I/O's = Open, Other Inputs = V_{IH}
I_{SB2}	V_{CC} Current (Standby) (CMOS Inputs)		100	200	µA	$\overline{CE}$ = V_{CC} − 0.3V, $\overline{OE}$ = GND All I/O's = Open, Other Inputs = V_{CC} − 0.3V
I_{LI}	Input Leakage Current			±10	µA	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output Leakage Current			±10	µA	V_{OUT} = V_{SS} to V_{CC}, $\overline{CE}$ = V_{IH}
V_{IL}(2)	Input LOW Voltage	−1		0.8	V	
V_{IH}(2)	Input HIGH Voltage	2		V_{CC} + 1	V	
V_{OL}	Output LOW Voltage			0.4	V	I_{OL} = 5mA
V_{OH}	Output HIGH Voltage	2.4			V	I_{OH} = −5mA

3857 PGM T04.2

Notes: (1) Typical values are for T_A = 25°C and nominal supply voltage
(2) V_{IL} min. and V_{IH} max. are for reference only and are not tested.

ENDURANCE AND DATA RETENTION

Parameter	Min.	Max.	Unit
Minimum Endurance	100,000		Cycles
Data Retention	100		Years

3857 PGM T05.3

POWER-UP TIMING

Symbol	Parameter	Typ. (1)	Units
t_{PUR}(3)	Power-up to Read Operation	100	µs
t_{PUW}(3)	Power-up to Write Operation	5	ms

3857 PGM T06

CAPACITANCE T_A = +25°C, f = 1MHz, V_{CC} = 5V

Symbol	Parameter	Max.	Units	Test Conditions
$C_{I/O}$(3)	Input/Output Capacitance	10	pF	$V_{I/O}$ = 0V
C_{IN}(3)	Input Capacitance	6	pF	V_{IN} = 0V

3857 PGM T07.1

A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3V
Input Rise and Fall Times	5ns
Input and Output Timing Levels	1.5V

3857 PGM T08.1

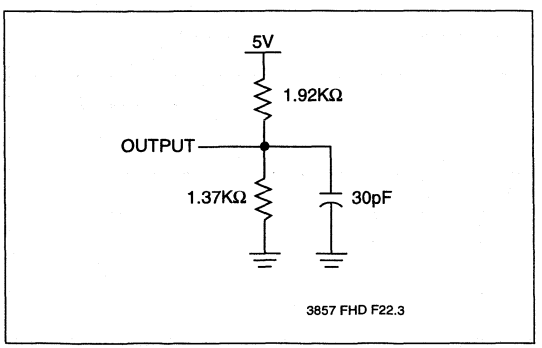
MODE SELECTION

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O	Power
L	L	H	Read	D_{OUT}	Active
L	H	L	Write	D_{IN}	Active
H	X	X	Standby and Write Inhibit	High Z	Standby
X	L	X	Write Inhibit	—	—
X	X	H	Write Inhibit	—	—

3857 PGM T09

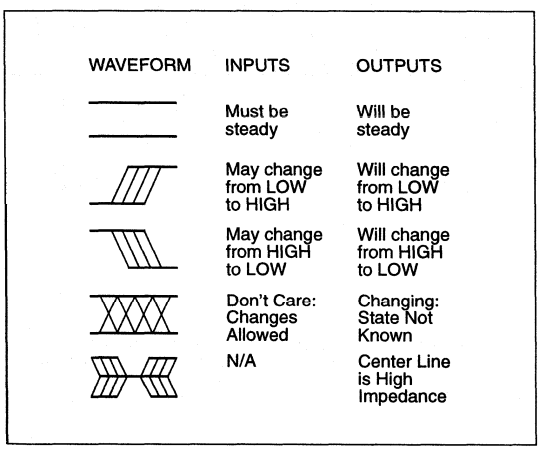
Note: (3) This parameter is periodically sampled and not 100% tested.

EQUIVALENT A.C. LOAD CIRCUITS



3857 FHD F22.3

SYMBOL TABLE



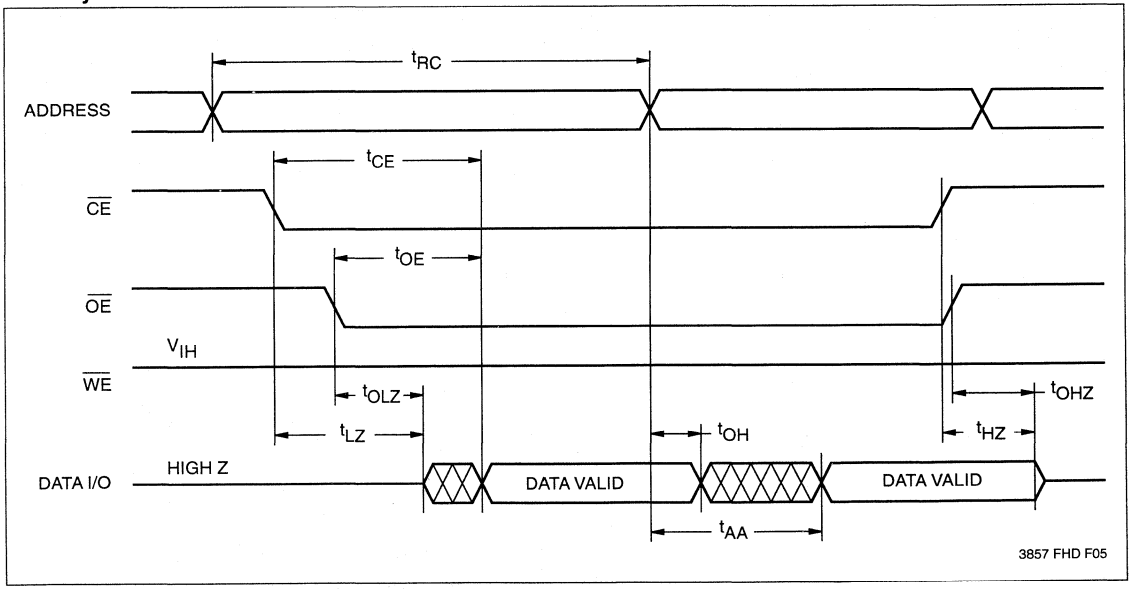
A.C. CHARACTERISTICS (Over the recommended operating conditions unless otherwise specified.)

Read Cycle Limits

Symbol	Parameter	X28HC64-55 –40°C to +85°C		X28HC64-70 –55°C to +125°C		X28HC64-90 –55°C to +125°C		X28HC64-12 –55°C to +125°C		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	55		70		90		120		ns
t_{CE}	Chip Enable Access Time		55		70		90		120	ns
t_{AA}	Address Access Time		55		70		90		120	ns
t_{OE}	Output Enable Access Time		30		35		40		50	ns
t_{LZ}(4)	$\overline{CE}$ LOW to Active Output	0		0		0		0		ns
t_{OLZ}(4)	$\overline{OE}$ LOW to Active Output	0		0		0		0		ns
t_{HZ}(4)	$\overline{CE}$ HIGH to High Z Output		30		30		30		30	ns
t_{OHZ}(4)	$\overline{OE}$ HIGH to High Z Output		30		30		30		30	ns
t_{OH}	Output Hold from Address Change	0		0		0		0		ns

3857 PGM T10.1

Read Cycle



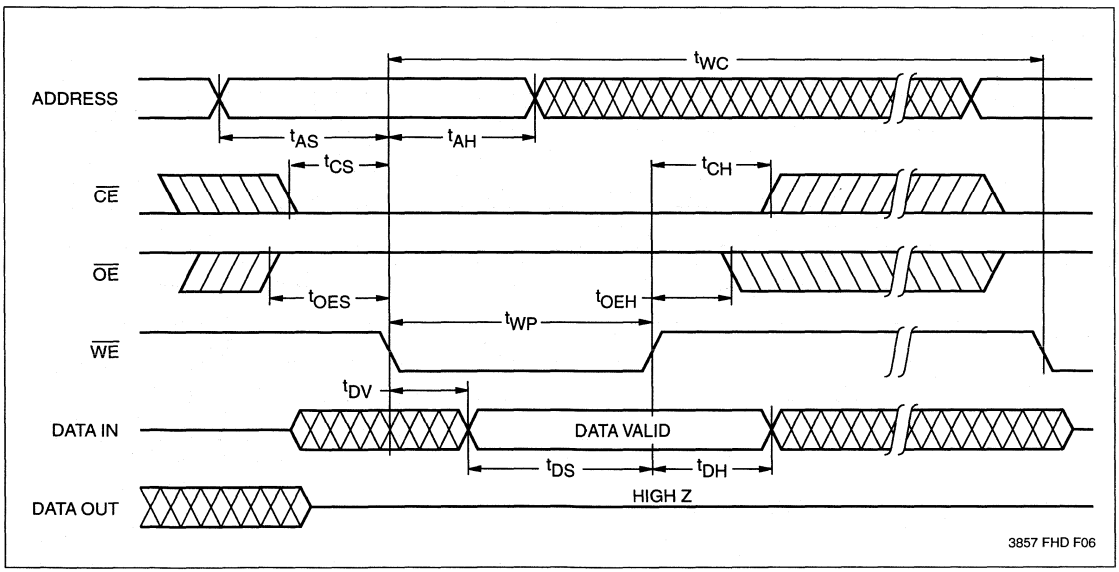
Notes: (4) t_{LZ} min., t_{HZ}, t_{OLZ} min., and t_{OHZ} are periodically sampled and not 100% tested. t_{HZ} max. and t_{OHZ} max. are measured from the point when $\overline{CE}$ or $\overline{OE}$ return HIGH (whichever occurs first) to the time when the outputs are no longer driven.

WRITE CYCLE LIMITS

Symbol	Parameter	Min.	Typ.(1)	Max.	Units
t_{WC}(5)	Write Cycle Time		2	5	ms
t_{AS}	Address Setup Time	0			ns
t_{AH}	Address Hold Time	50			ns
t_{CS}	Write Setup Time	0			ns
t_{CH}	Write Hold Time	0			ns
t_{CW}	$\overline{CE}$ Pulse Width	50			ns
t_{OES}	$\overline{OE}$ HIGH Setup Time	0			ns
t_{OEH}	$\overline{OE}$ HIGH Hold Time	0			ns
t_{WP}	$\overline{WE}$ Pulse Width	50			ns
t_{WPH}(6)	$\overline{WE}$ HIGH Recovery	50			ns
t_{DV}(6)	Data Valid			1	µs
t_{DS}	Data Setup	50			ns
t_{DH}	Data Hold	0			ns
t_{DW}(6)	Delay to Next Write	10			µs
t_{BLC}	Byte Load Cycle	0.15		100	µs

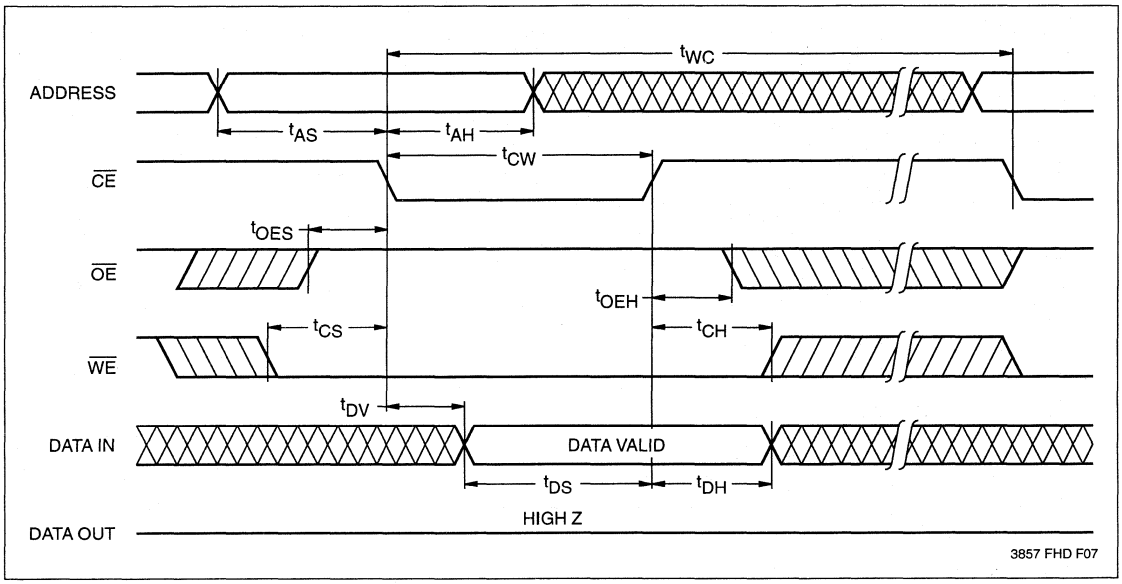
3857 PGM T11.2

$\overline{WE}$ Controlled Write Cycle

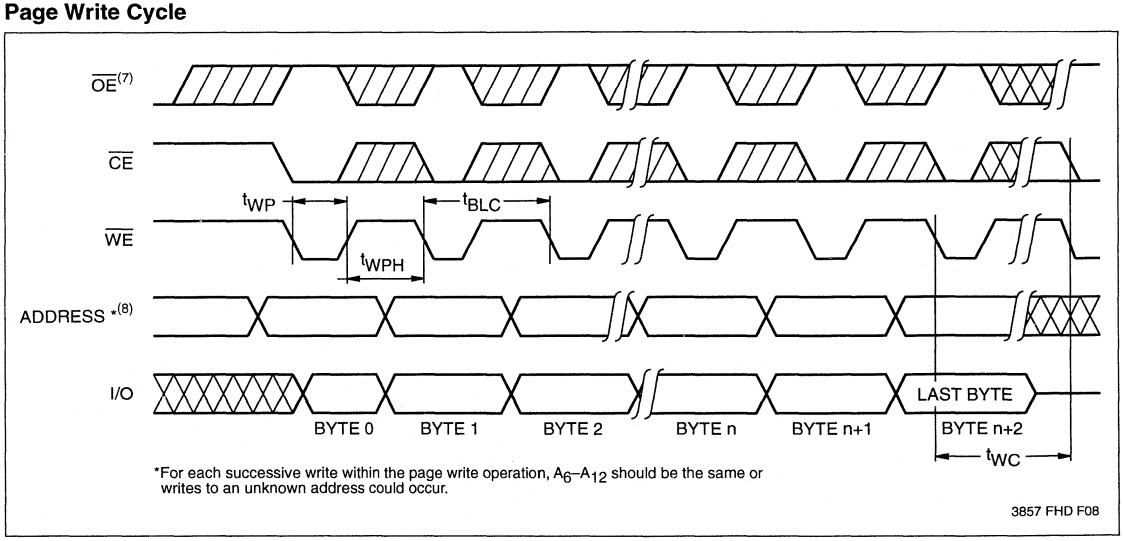


Notes: (5) t_{WC} is the minimum cycle time to be allowed from the system perspective unless polling techniques are used. It is the maximum time the device requires to automatically complete the internal write operation.
(6) t_{WPH} and t_{DW} are periodically sampled and not 100% tested.

$\overline{CE}$ Controlled Write Cycle



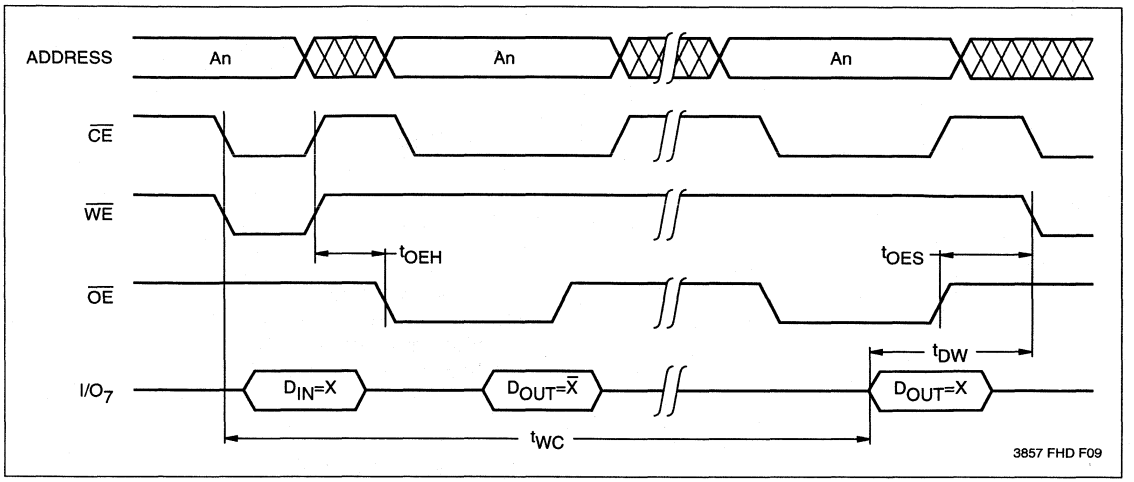
Page Write Cycle



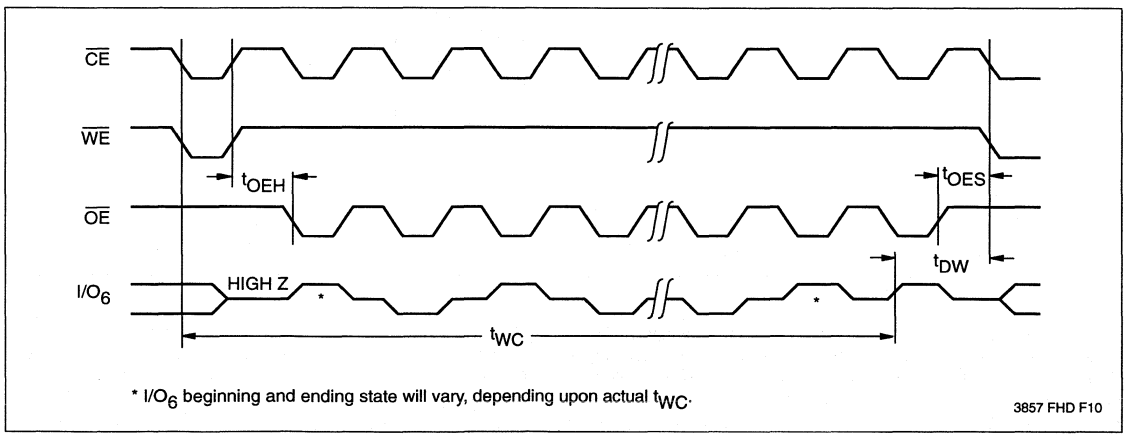
Notes: (7) Between successive byte writes within a page write operation, $\overline{OE}$ can be strobed LOW: e.g. this can be done with $\overline{CE}$ and $\overline{WE}$ HIGH to fetch data from another memory device within the system for the next write; or with $\overline{WE}$ HIGH and $\overline{CE}$ LOW effectively performing a polling operation.

(8) The timings shown above are unique to page write operations. Individual byte load operations within the page write must conform to either the $\overline{CE}$ or $\overline{WE}$ controlled write cycle timing.

$\overline{DATA}$ Polling Timing Diagram(9)

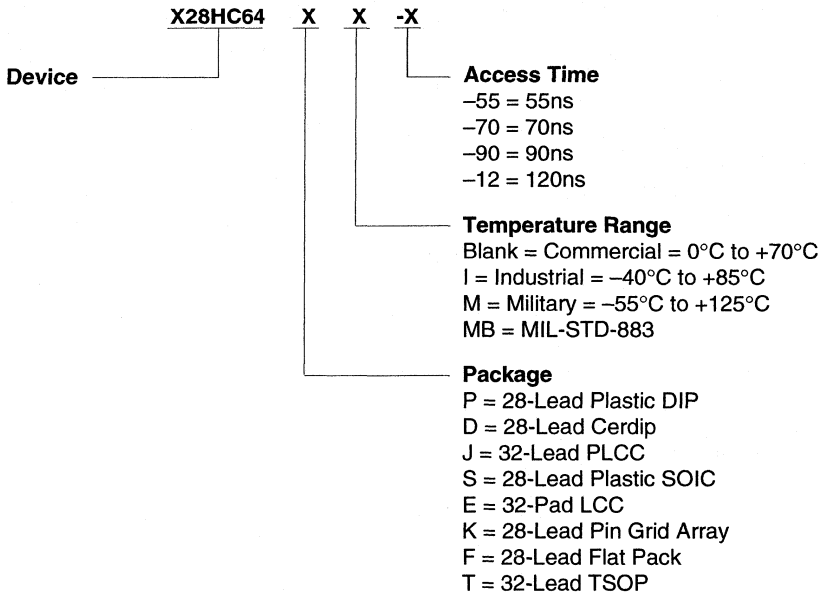


Toggle Bit Timing Diagram(9)



Note: (9) Polling operations are by definition read cycles and are therefore subject to read cycle timings.

ORDERING INFORMATION



5 Volt, Byte Alterable E²PROM

FEATURES

- Access Time: 200ns
- Simple Byte and Page Write
  - Single 5V Supply
    - No External High Voltages or V_{PP} Control Circuits
  - Self-Timed
    - No Erase Before Write
    - No Complex Programming Algorithms
    - No Overerase Problem
- Low Power CMOS:
  - Active: 60mA
  - Standby: 200µA
- Software Data Protection
  - Protects Data Against System Level Inadvertent Writes
- High Speed Page Write Capability
- Highly Reliable Direct Write™ Cell
  - Endurance: 100,000 Write Cycles
  - Data Retention: 100 Years
- Early End of Write Detection
  - $\overline{DATA}$ Polling
  - Toggle Bit Polling

DESCRIPTION

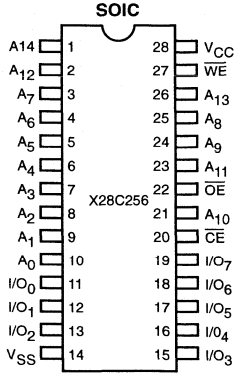
The X28C256 is an 32K x 8 E²PROM, fabricated with Xicor's proprietary, high performance, floating gate CMOS technology. Like all Xicor programmable nonvolatile memories the X28C256 is a 5V only device. The X28C256 features the JEDEC approved pinout for byte-wide memories, compatible with industry standard RAMs.

The X28C256 supports a 64-byte page write operation, effectively providing a 78µs/byte write cycle and enabling the entire memory to be typically written in less than 2.5 seconds. The X28C256 also features $\overline{DATA}$ and Toggle Bit Polling, a system software support scheme used to indicate the early completion of a write cycle. In addition, the X28C256 includes a user-optional software data protection mode that further enhances Xicor's hardware write protect capability.

Xicor E²PROMs are designed and tested for applications requiring extended endurance. Inherent data retention is greater than 100 years.

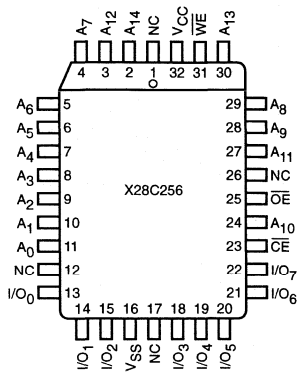
PIN CONFIGURATION

PLASTIC DIP
CERDIP
FLAT PACK
SOIC



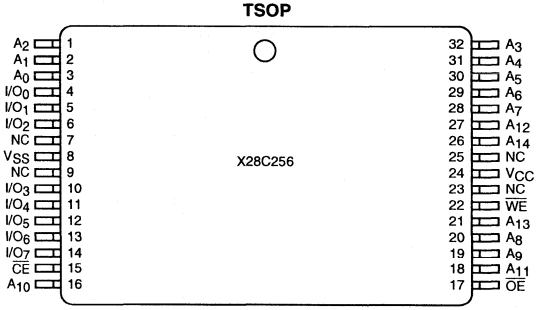
3855 FHD F02

LCC
PLCC



3855 FHD F03

TSOP



3855 ILL F23

PIN DESCRIPTIONS

Addresses (A_0–A_{14})

The Address inputs select an 8-bit memory location during a read or write operation.

Chip Enable ($\overline{CE}$)

The Chip Enable input must be LOW to enable all read/write operations. When $\overline{CE}$ is HIGH, power consumption is reduced.

Output Enable ($\overline{OE}$)

The Output Enable input controls the data output buffers and is used to initiate read operations.

Data In/Data Out (I/O_0–I/O_7)

Data is written to or read from the X28C256 through the I/O pins.

Write Enable ($\overline{WE}$)

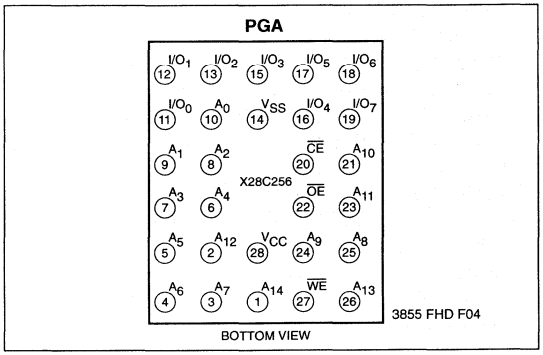
The Write Enable input controls the writing of data to the X28C256.

PIN NAMES

Symbol	Description
A_0–A_{14}	Address Inputs
I/O_0–I/O_7	Data Input/Output
$\overline{WE}$	Write Enable
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
V_{CC}	+5V
V_{SS}	Ground
NC	No Connect

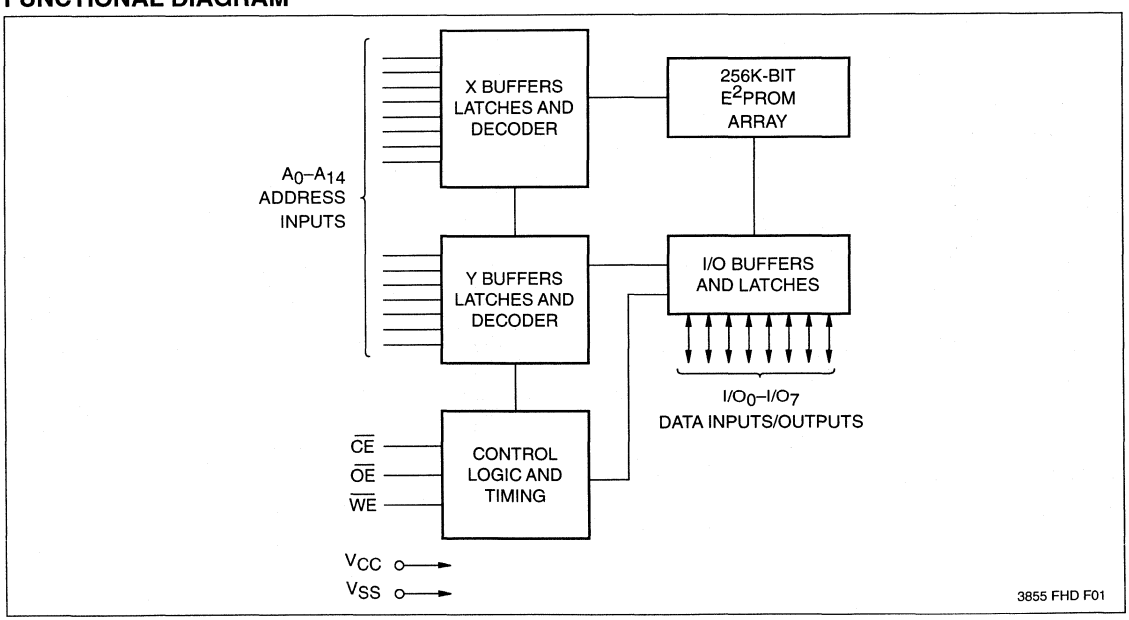
3855 PGM T01

PIN CONFIGURATION



3855 FHD F04

FUNCTIONAL DIAGRAM



3855 FHD F01

DEVICE OPERATION

Read

Read operations are initiated by both $\overline{OE}$ and $\overline{CE}$ LOW. The read operation is terminated by either $\overline{CE}$ or $\overline{OE}$ returning HIGH. This two line control architecture eliminates bus contention in a system environment. The data bus will be in a high impedance state when either $\overline{OE}$ or $\overline{CE}$ is HIGH.

Write

Write operations are initiated when both $\overline{CE}$ and $\overline{WE}$ are LOW and $\overline{OE}$ is HIGH. The X28C256 supports both a $\overline{CE}$ and $\overline{WE}$ controlled write cycle. That is, the address is latched by the falling edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs last. Similarly, the data is latched internally by the rising edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs first. A byte write operation, once initiated, will automatically continue to completion, typically within 5ms.

Page Write Operation

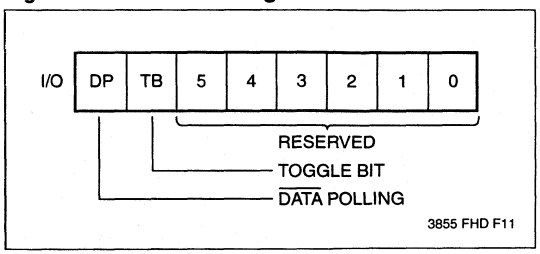
The page write feature of the X28C256 allows the entire memory to be written in 2.5 seconds. Page write allows two to sixty-four bytes of data to be consecutively written to the X28C256 prior to the commencement of the internal programming cycle. The host can fetch data from another device within the system during a page write operation (change the source address), but the page address (A_6 through A_{14}) for each subsequent valid write cycle to the part during this operation must be the same as the initial page address.

The page write mode can be initiated during any write operation. Following the initial byte write cycle, the host can write an additional one to sixty-three bytes in the same manner as the first byte was written. Each successive byte load cycle, started by the $\overline{WE}$ HIGH to LOW transition, must begin within 100µs of the falling edge of the preceding $\overline{WE}$. If a subsequent $\overline{WE}$ HIGH to LOW transition is not detected within 100µs, the internal automatic programming cycle will commence. There is no page write window limitation. Effectively the page write window is infinitely wide, so long as the host continues to access the device within the byte load cycle time of 100µs.

Write Operation Status Bits

The X28C256 provides the user two write operation status bits. These can be used to optimize a system write cycle time. The status bits are mapped onto the I/O bus as shown in Figure 1.

Figure 1. Status Bit Assignment



$\overline{DATA}$ Polling (I/O_7)

The X28C256 features $\overline{DATA}$ Polling as a method to indicate to the host system that the byte write or page write cycle has completed. $\overline{DATA}$ Polling allows a simple bit test operation to determine the status of the X28C256, eliminating additional interrupt inputs or external hardware. During the internal programming cycle, any attempt to read the last byte written will produce the complement of that data on I/O_7 (i.e. write data = 0xxx xxxx, read data = 1xxx xxxx). Once the programming cycle is complete, I/O_7 will reflect true data. Note: If the X28C256 is in the protected state and an illegal write operation is attempted $\overline{DATA}$ Polling will not operate.

Toggle Bit (I/O_6)

The X28C256 also provides another method for determining when the internal write cycle is complete. During the internal programming cycle I/O_6 will toggle from HIGH to LOW and LOW to HIGH on subsequent attempts to read the device. When the internal cycle is complete the toggling will cease and the device will be accessible for additional read or write operations.

$\overline{DATA}$ POLLING I/O_7

Figure 2. $\overline{DATA}$ Polling Bus Sequence

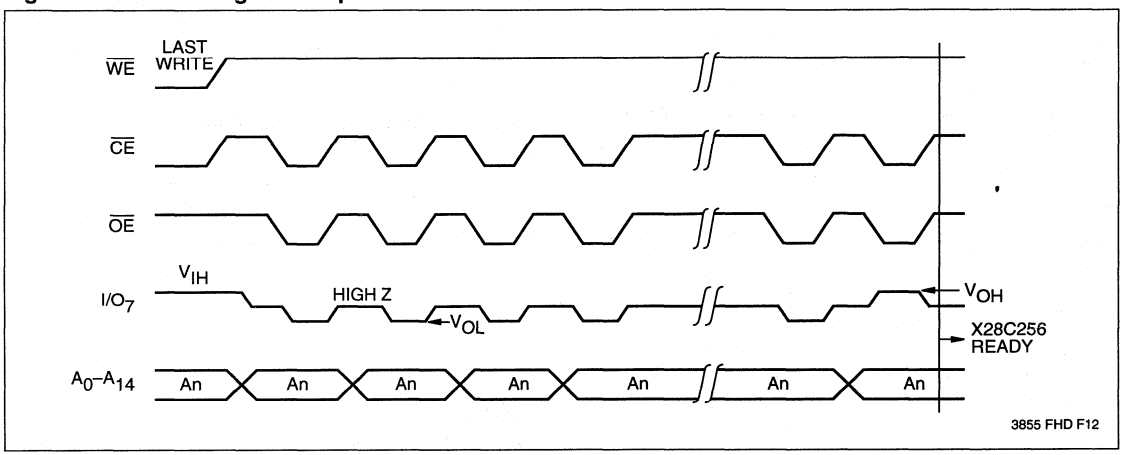
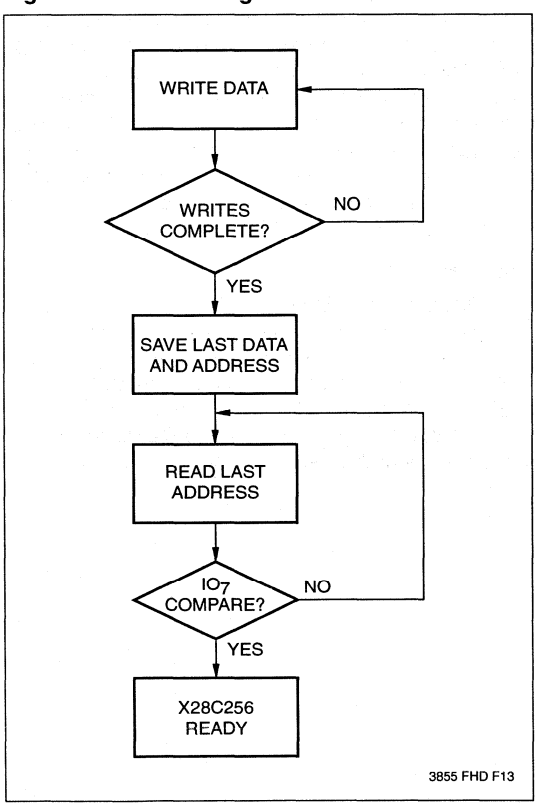


Figure 3. $\overline{DATA}$ Polling Software Flow



$\overline{DATA}$ Polling can effectively halve the time for writing to the X28C256. The timing diagram in Figure 2 illustrates the sequence of events on the bus. The software flow diagram in Figure 3 illustrates one method of implementing the routine.

THE TOGGLE BIT I/O_6

Figure 4. Toggle Bit Bus Sequence

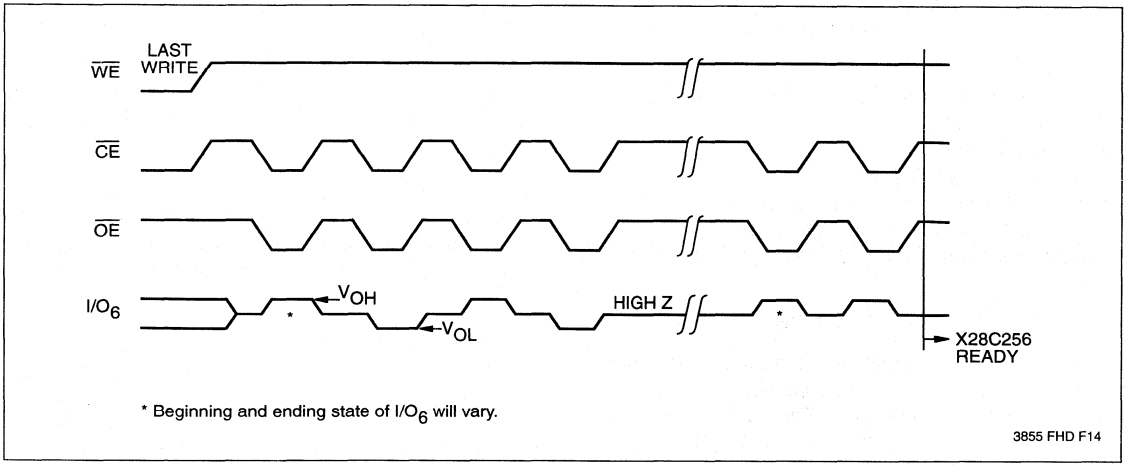
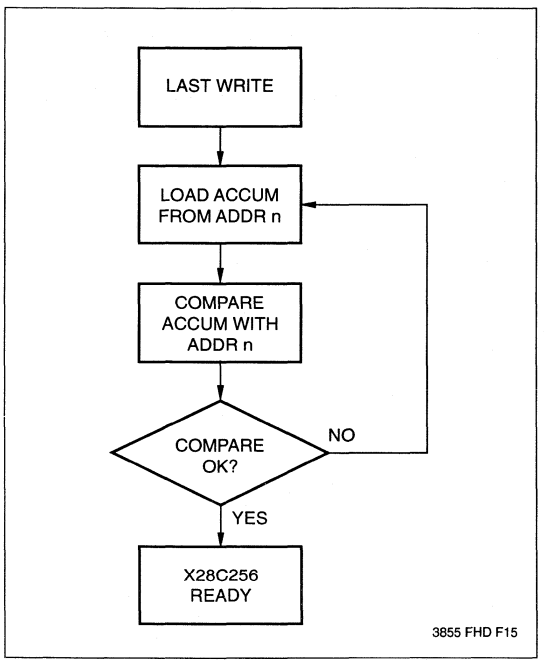


Figure 5. Toggle Bit Software Flow



The Toggle Bit can eliminate the software housekeeping chore of saving and fetching the last address and data written to a device in order to implement $\overline{DATA}$ Polling. This can be especially helpful in an array comprised of multiple X28C256 memories that is frequently updated. The timing diagram in Figure 4 illustrates the sequence of events on the bus. The software flow diagram in Figure 5 illustrates a method for polling the Toggle Bit.

HARDWARE DATA PROTECTION

The X28C256 provides three hardware features (compatible with X28C64) that protect nonvolatile data from inadvertent writes.

- Noise Protection—A $\overline{WE}$ pulse typically less than 20ns will not initiate a write cycle.
- Default V_{CC} Sense—All write functions are inhibited when V_{CC} is ≤3.5V typically.
- Write Inhibit—Holding either $\overline{OE}$ LOW, $\overline{WE}$ HIGH, or $\overline{CE}$ HIGH will prevent an inadvertent write cycle during power-up and power-down, maintaining data integrity.

SOFTWARE DATA PROTECTION

The X28C256 offers a software controlled data protection feature. The X28C256 is shipped from Xicor with the software data protection NOT ENABLED; that is, the device will be in the standard operating mode. In this mode data should be protected during power-up/-down operations through the use of external circuits. The host would then have open read and write access of the device once V_{CC} was stable.

The X28C256 can be automatically protected during power-up and power-down without the need for external circuits by employing the software data protection feature. The internal software data protection circuit is enabled after the first write operation utilizing the software algorithm. This circuit is nonvolatile and will remain set for the life of the device unless the reset command is issued.

Once the software protection is enabled, the X28C256 is also protected from inadvertent and accidental writes in the powered-up state. That is, the software algorithm must be issued prior to writing additional data to the device.

Software Algorithm

Selecting the software data protection mode requires the host system to precede data write operations by a series of three write operations to three specific addresses. Refer to Figure 6 and 7 for the sequence. The three-byte sequence opens the page write window enabling the host to write from one to sixty-four bytes of data.* Once the page load cycle has been completed, the device will automatically be returned to the data protected state.

**Note: Once the three-byte sequence is issued it must be followed by a valid byte or page write operation.*

SOFTWARE DATA PROTECTION

Figure 6. Timing Sequence—Byte or Page Write

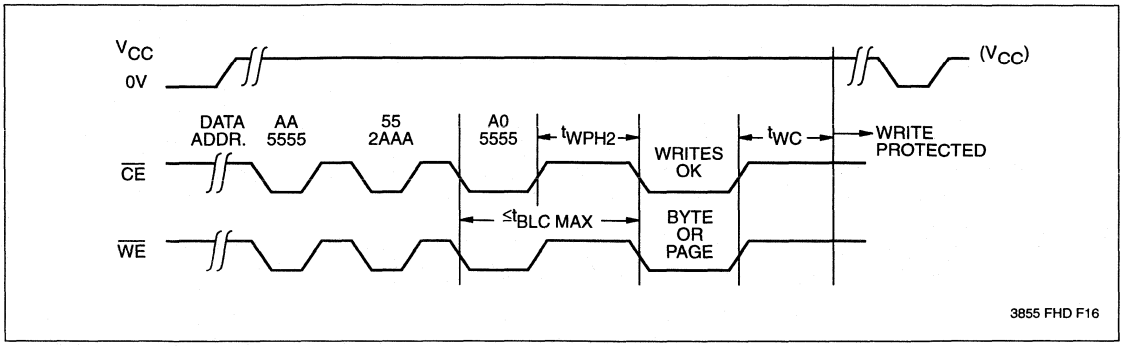
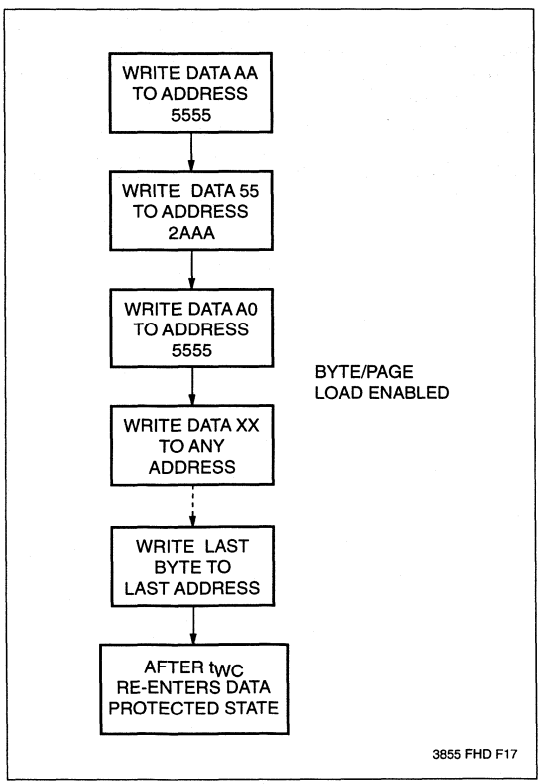


Figure 7. Write Sequence for Software Data Protection



Regardless of whether the device has previously been protected or not, once the software data protection algorithm is used and data has been written, the X28C256 will automatically disable further writes unless another command is issued to cancel it. If no further commands are issued the X28C256 will be write protected during power-down and after any subsequent power-up.

Note: Once initiated, the sequence of write operations should not be interrupted.

RESETTING SOFTWARE DATA PROTECTION

Figure 8. Reset Software Data Protection Timing Sequence

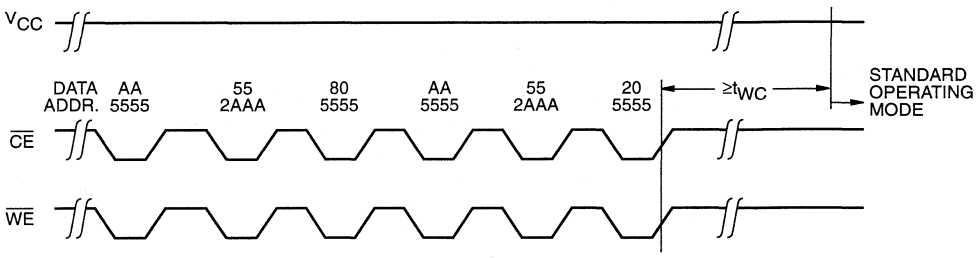
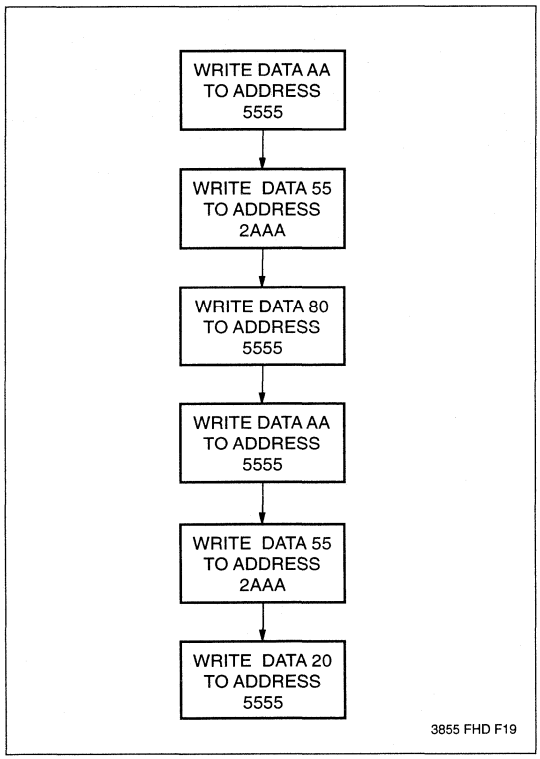


Figure 9. Software Sequence to Deactivate Software Data Protection



In the event the user wants to deactivate the software data protection feature for testing or reprogramming in an E²PROM programmer, the following six step algorithm will reset the internal protection circuit. After t_{WC}, the X28C256 will be in standard operating mode.

Note: Once initiated, the sequence of write operations should not be interrupted.

SYSTEM CONSIDERATIONS

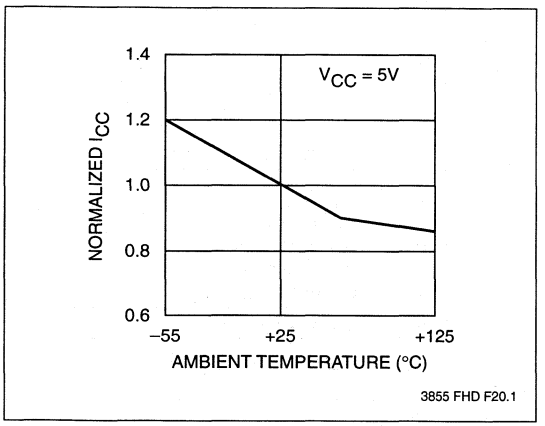
Because the X28C256 is frequently used in large memory arrays it is provided with a two line control architecture for both read and write operations. Proper usage can provide the lowest possible power dissipation and eliminate the possibility of contention where multiple I/O pins share the same bus.

To gain the most benefit it is recommended that $\overline{CE}$ be decoded from the address bus and be used as the primary device selection input. Both $\overline{OE}$ and $\overline{WE}$ would then be common among all devices in the array. For a read operation this assures that all deselected devices are in their standby mode and that only the selected device(s) is outputting data on the bus.

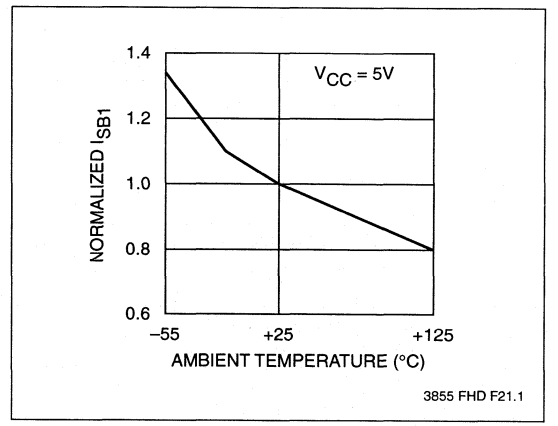
Because the X28C256 has two power modes, standby and active, proper decoupling of the memory array is of prime concern. Enabling $\overline{CE}$ will cause transient current spikes. The magnitude of these spikes is dependent on the output capacitive loading of the I/Os. Therefore, the larger the array sharing a common bus, the larger the transient spikes. The voltage peaks associated with the current transients can be suppressed by the proper selection and placement of decoupling capacitors. As a minimum, it is recommended that a 0.1μF high frequency ceramic capacitor be used between V_{CC} and V_{SS} at each device. Depending on the size of the array, the value of the capacitor may have to be larger.

In addition, it is recommended that a 4.7μF electrolytic bulk capacitor be placed between V_{CC} and V_{SS} for each eight devices employed in the array. This bulk capacitor is employed to overcome the voltage droop caused by the inductive effects of the PC board traces.

Normalized Active Supply Current vs. Ambient Temperature



Normalized Standby Supply Current vs. Ambient Temperature



ABSOLUTE MAXIMUM RATINGS*

Temperature under Bias
- X28C256 ..... −10°C to +85°C
- X28C256I, X28C256M ..... −65°C to +135°C

Storage Temperature ..... −65°C to +150°C

Voltage on any Pin with
- Respect to V_{SS} ..... −1V to +7V

D.C. Output Current 5mA

Lead Temperature
- (Soldering, 10 seconds) ..... 300°C

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	+70°C
Industrial	−40°C	+85°C
Military	−55°C	+125°C

3855 PGM T02.1

Supply Voltage	Limits
X28C256	5V ±10%

3855 PGM T03.1

D.C. OPERATING CHARACTERISTICS (over recommended operating conditions, unless otherwise specified)

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.(1)	Max.		
I_{CC}	V_{CC} Current (Active) (TTL Inputs)			60	mA	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}, All I/O's = Open, Address Inputs = .4V/2.4V @ f = 5MHz
I_{SB1}	V_{CC} Current (Standby) (TTL Inputs)			2	mA	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IL} All I/O's = Open, Other Inputs = V_{IH}
I_{SB2}(2)	V_{CC} Current (Standby) (CMOS Inputs)		200	500	µA	$\overline{CE}$ = V_{CC} − 0.3V, $\overline{OE}$ = V_{IL} All I/O's = Open, Other Inputs = V_{CC} − 0.3V
I_{LI}	Input Leakage Current			10	µA	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output Leakage Current			10	µA	V_{OUT} = V_{SS} to V_{CC}, $\overline{CE}$ = V_{IH}
V_{IL}(3)	Input LOW Voltage	−1		0.8	V	
V_{IH}(3)	Input HIGH Voltage	2		V_{CC} + 1	V	
V_{OL}	Output LOW Voltage			0.4	V	I_{OL} = 2.1mA
V_{OH}	Output HIGH Voltage	2.4			V	I_{OH} = −400µA

3855 PGM T04.2

Notes: (1) Typical values are for T_A = 25°C and nominal supply voltage and are not tested
(2) I_{SB2} max. of 200µA available from Xicor. Contact local sales office and reference X28C256 C7125.
(3) V_{IL} min. and V_{IH} max. are for reference only and are not tested.

ENDURANCE AND DATA RETENTION

Parameter	Min.	Units
Endurance	100,000	Cycles
Data Retention	100	Years

3855 PGM T05.1

POWER-UP TIMING

Symbol	Parameter	Max.	Units
t_{PUR}(4)	Power-up to Read Operation	100	µs
t_{PUW}(4)	Power-up to Write Operation	5	ms

3855 PGM T06

CAPACITANCE T_A = +25°C, f = 1MHz, V_{CC} = 5V

Symbol	Parameter	Max.	Units	Test Conditions
$C_{I/O}$(4)	Input/Output Capacitance	10	pF	$V_{I/O}$ = 0V
C_{IN}(4)	Input Capacitance	6	pF	V_{IN} = 0V

3855 PGM T07.1

A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3V
Input Rise and Fall Times	10ns
Input and Output Timing Levels	1.5V

3855 PGM T08.1

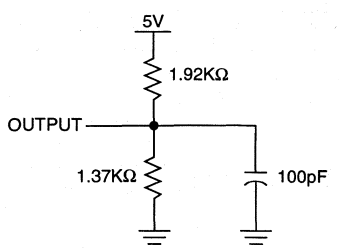
MODE SELECTION

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O	Power
L	L	H	Read	D_{OUT}	Active
L	H	L	Write	D_{IN}	Active
H	X	X	Standby and Write Inhibit	High Z	Standby
X	L	X	Write Inhibit	—	—
X	X	H	Write Inhibit	—	—

3855 PGM T09

Note: (4) This parameter is periodically sampled and not 100% tested.

EQUIVALENT A.C. LOAD CIRCUIT



3855 FHD F22.3

SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

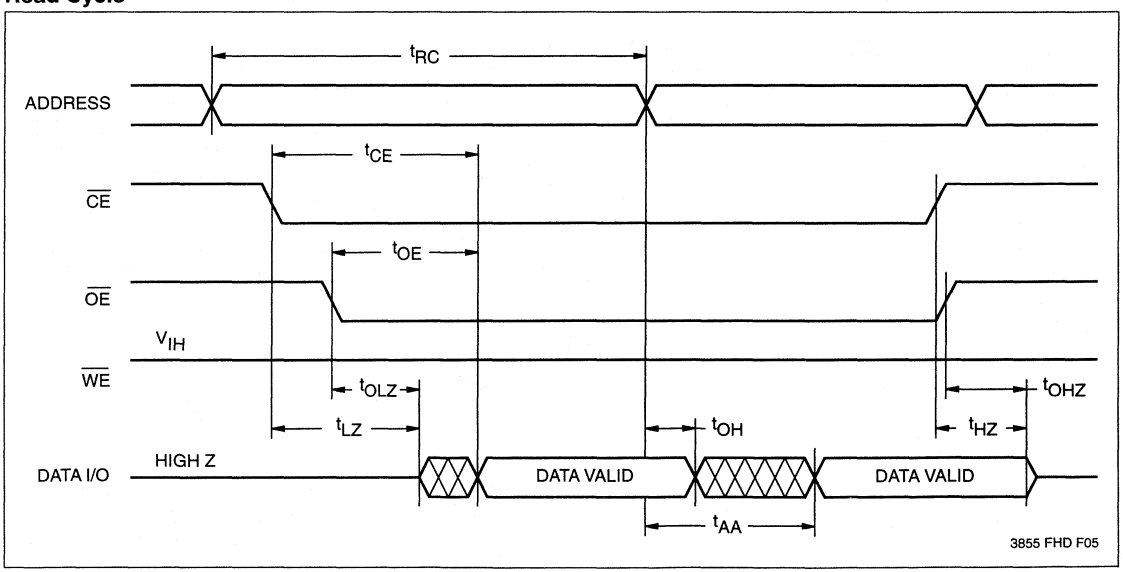
A.C. CHARACTERISTICS (over recommended operating conditions, unless otherwise specified)

Read Cycle Limits

Symbol	Parameter	X28C256-20		X28C256-25		X28C256		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	200		250		300		ns
t_{CE}	Chip Enable Access Time		200		250		300	ns
t_{AA}	Address Access Time		200		250		300	ns
t_{OE}	Output Enable Access Time		80		100		100	ns
t_{LZ}(5)	$\overline{CE}$ LOW to Active Output	0		0		0		ns
t_{OLZ}(5)	$\overline{OE}$ LOW to Active Output	0		0		0		ns
t_{HZ}(5)	$\overline{CE}$ HIGH to High Z Output		50		50		50	ns
t_{OHZ}(5)	$\overline{OE}$ HIGH to High Z Output		50		50		50	ns
t_{OH}	Output Hold from Address Change	0		0		0		ns

3855 PGM T10.1

Read Cycle



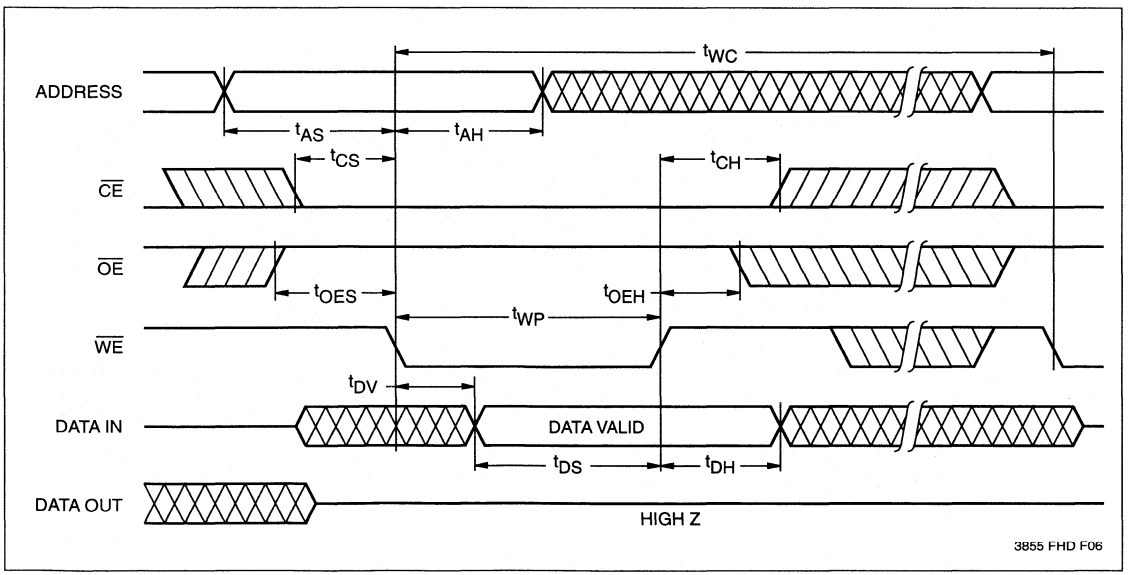
Note: (5) t_{LZ} min., t_{HZ}, t_{OLZ} min., and t_{OHZ} are peridocally sampled and not 100% tested. t_{HZ} and t_{OHZ} are measured, with C_L = 5pF, from the point when $\overline{CE}$ or $\overline{OE}$ return HIGH (whichever occurs first) to the time when the outputs are no longer driven.

WRITE CYCLE LIMITS

Symbol	Parameter	Min.(9)	Typ.(6)	Max.	Units
t_{WC}(7)	Write Cycle Time		5	10	ms
t_{AS}	Address Setup Time	0			ns
t_{AH}	Address Hold Time	150			ns
t_{CS}	Write Setup Time	0			ns
t_{CH}	Write Hold Time	0			ns
t_{CW}	$\overline{CE}$ Pulse Width	100			ns
t_{OES}	$\overline{OE}$ HIGH Setup Time	10			ns
t_{OEH}	$\overline{OE}$ HIGH Hold Time	10			ns
t_{WP}	$\overline{WE}$ Pulse Width	100			ns
t_{WPH}	$\overline{WE}$ HIGH Recovery	50			ns
t_{WPH2}(8)	SDP $\overline{WE}$ Recovery	1			µs
t_{DV}	Data Valid			1	µs
t_{DS}	Data Setup	50			ns
t_{DH}	Data Hold	10			ns
t_{DW}	Delay to Next Write	10			µs
t_{BLC}(9)	Byte Load Cycle	1		100	µs

3855 PGM T11.1

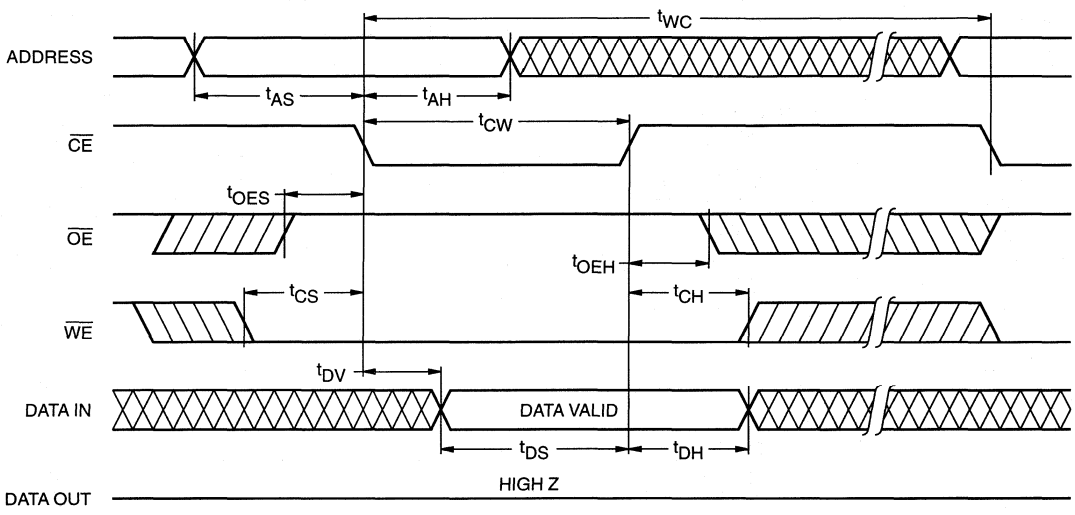
$\overline{WE}$ Controlled Write Cycle



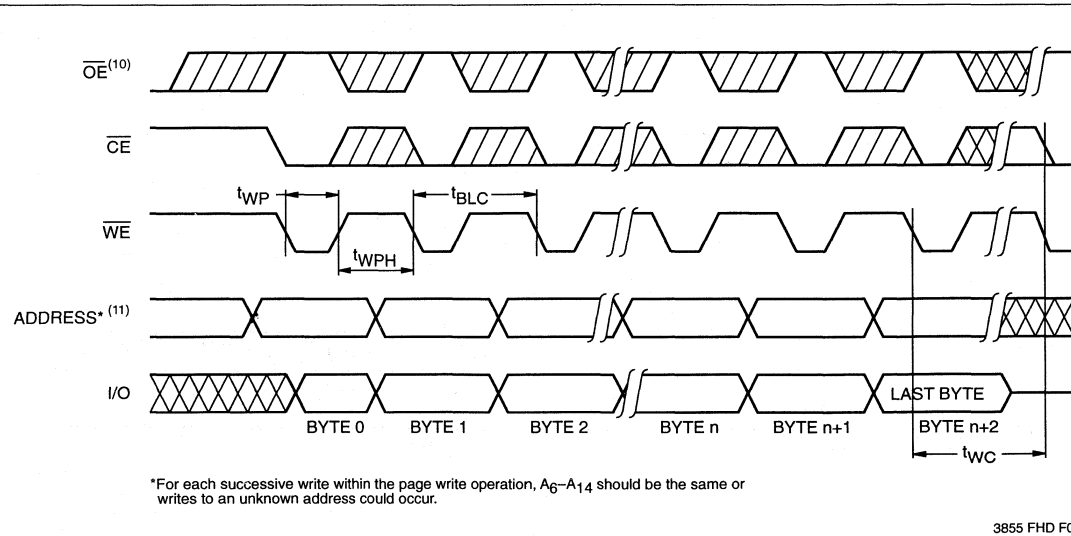
3855 FHD F06

Notes: (6) Typical values are for $T_A = 25°C$ and nominal supply voltage.
(7) t_{WC} is the minimum cycle time to be allowed from the system perspective unless polling techniques are used. It is the maximum time the device requires to automatically complete the internal write operation.
(8) t_{WPH} is the normal page write operation $\overline{WE}$ recovery time. t_{WPH2} is the $\overline{WE}$ recovery time needed only after the end of issuing the three-byte SDP command sequence and before writing the first byte of data to the array. Refer to Figure 6 which illustrates the t_{WPH2} requirement.
(9) For faster t_{WC} and t_{BLC}, refer to X28HC256 or X28VC256.

$\overline{CE}$ Controlled Write Cycle



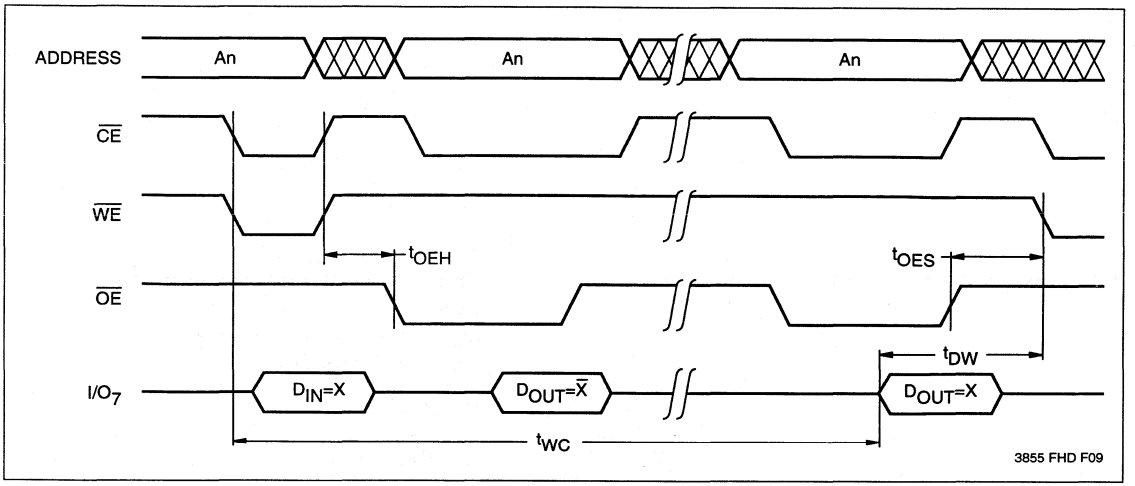
Page Write Cycle



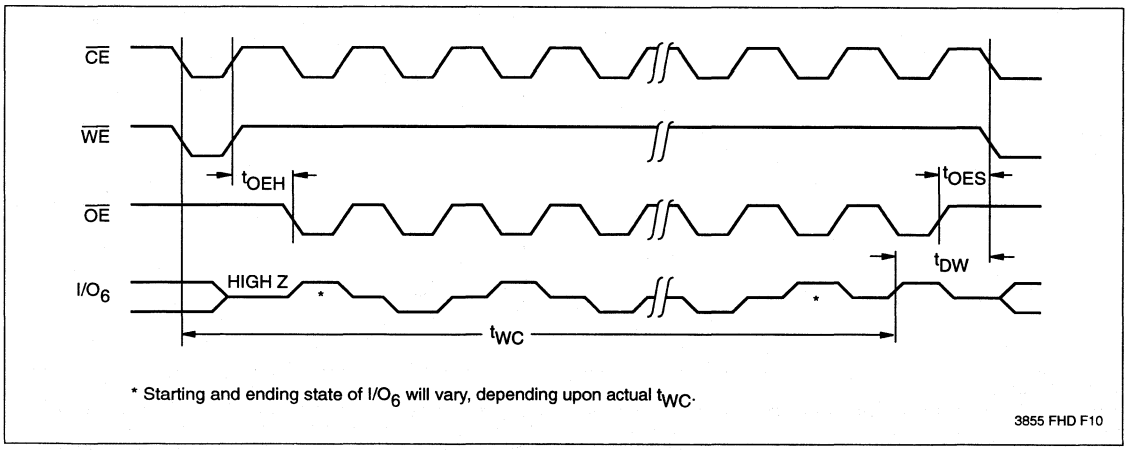
Notes: (10) Between successive byte writes within a page write operation, $\overline{OE}$ can be strobed LOW: e.g. this can be done with $\overline{CE}$ and $\overline{WE}$ HIGH to fetch data from another memory device within the system for the next write; or with $\overline{WE}$ HIGH and $\overline{CE}$ LOW effectively performing a polling operation.

(11) The timings shown above are unique to page write operations. Individual byte load operations within the page write must conform to either the $\overline{CE}$ or $\overline{WE}$ controlled write cycle timing.

$\overline{\text{DATA}}$ Polling Timing Diagram(12)

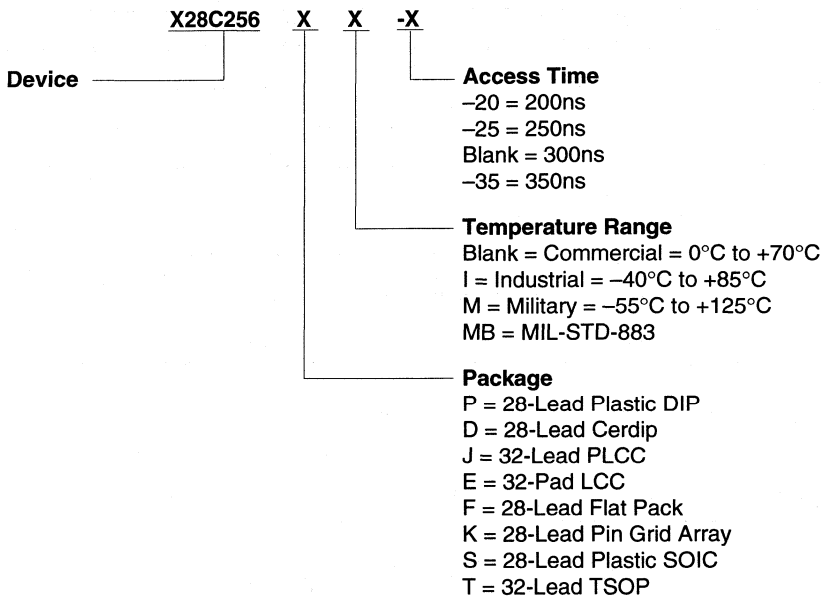


Toggle Bit Timing Diagram(12)



Note: (12) Polling operations are by definition read cycles and are therefore subject to read cycle timings.

ORDERING INFORMATION



5 Volt, Byte Alterable E²PROM

FEATURES

- Access Time: 70ns
- Simple Byte and Page Write
  - —Single 5V Supply
    - —No External High Voltages or V_{PP} Control Circuits
  - —Self-Timed
    - —No Erase Before Write
    - —No Complex Programming Algorithms
    - —No Overerase Problem
- Low Power CMOS:
  - —Active: 60mA
  - —Standby: 500µA
- Software Data Protection
  - —Protects Data Against System Level Inadvertent Writes
- High Speed Page Write Capability
- Highly Reliable Direct Write™ Cell
  - —Endurance: 100,000 Write Cycles
  - —Data Retention: 100 Years
- Early End of Write Detection
  - —$\overline{DATA}$ Polling
  - —Toggle Bit Polling

DESCRIPTION

The X28HC256 is a second generation high performance CMOS 32K x 8 E²PROM. It is fabricated with Xicor's proprietary, textured poly floating gate technology, providing a highly reliable 5 Volt only nonvolatile memory.

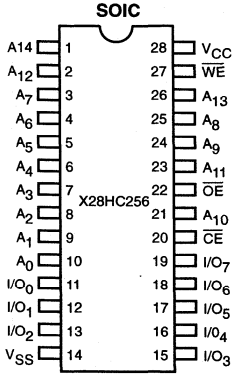
The X28HC256 supports a 128-byte page write operation, effectively providing a 24µs/byte write cycle and enabling the entire memory to be typically rewritten in less than 0.8 seconds. The X28HC256 also features $\overline{DATA}$ Polling and Toggle Bit Polling, two methods of providing early end of write detection. The X28HC256 also supports the JEDEC standard Software Data Protection feature for protecting against inadvertent writes during power-up and power-down.

Endurance for the X28HC256 is specified as a minimum 100,000 write cycles per byte and an inherent data retention of 100 years.

3

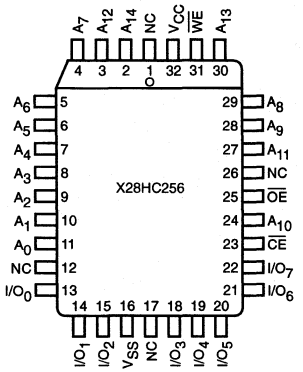
PIN CONFIGURATION

PLASTIC DIP
CERDIP
FLAT PACK
SOIC



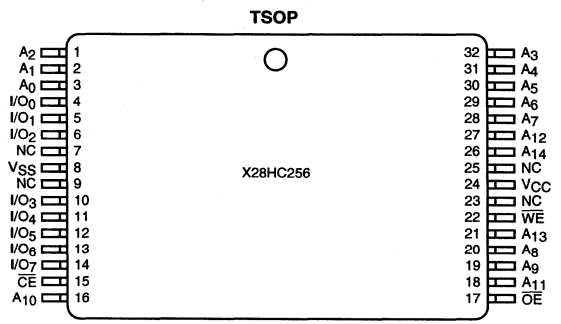
3859 FHD F02

LCC
PLCC



3859 FHD F03

TSOP



3859 ILL F22

PIN DESCRIPTIONS

Addresses (A_0–A_{14})

The Address inputs select an 8-bit memory location during a read or write operation.

Chip Enable ($\overline{CE}$)

The Chip Enable input must be LOW to enable all read/write operations. When $\overline{CE}$ is HIGH, power consumption is reduced.

Output Enable ($\overline{OE}$)

The Output Enable input controls the data output buffers and is used to initiate read operations.

Data In/Data Out (I/O_0–I/O_7)

Data is written to or read from the X28HC256 through the I/O pins.

Write Enable ($\overline{WE}$)

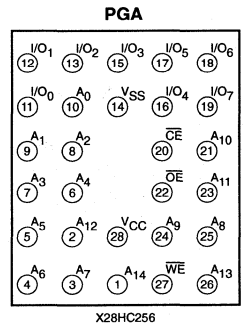
The Write Enable input controls the writing of data to the X28HC256.

PIN NAMES

Symbol	Description
A_0–A_{14}	Address Inputs
I/O_0–I/O_7	Data Input/Output
$\overline{WE}$	Write Enable
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
V_{CC}	+5V
V_{SS}	Ground
NC	No Connect

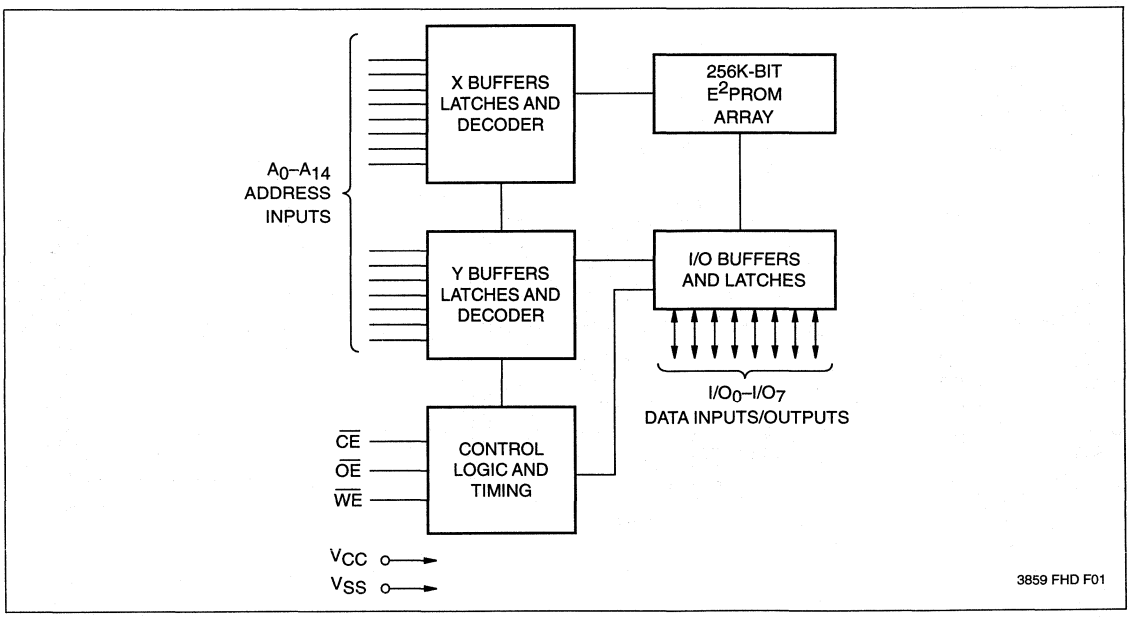
3859 PGM T01

PIN CONFIGURATION



3859 FHD F04

FUNCTIONAL DIAGRAM



3859 FHD F01

DEVICE OPERATION

Read

Read operations are initiated by both $\overline{OE}$ and $\overline{CE}$ LOW. The read operation is terminated by either $\overline{CE}$ or $\overline{OE}$ returning HIGH. This two line control architecture eliminates bus contention in a system environment. The data bus will be in a high impedance state when either $\overline{OE}$ or $\overline{CE}$ is HIGH.

Write

Write operations are initiated when both $\overline{CE}$ and $\overline{WE}$ are LOW and $\overline{OE}$ is HIGH. The X28HC256 supports both a $\overline{CE}$ and $\overline{WE}$ controlled write cycle. That is, the address is latched by the falling edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs last. Similarly, the data is latched internally by the rising edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs first. A byte write operation, once initiated, will automatically continue to completion, typically within 3ms.

Page Write Operation

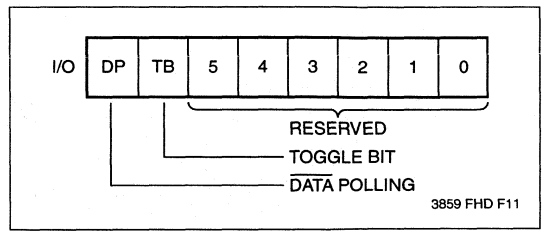
The page write feature of the X28HC256 allows the entire memory to be written in typically 0.8 seconds. Page write allows up to one hundred twenty-eight bytes of data to be consecutively written to the X28HC256 prior to the commencement of the internal programming cycle. The host can fetch data from another device within the system during a page write operation (change the source address), but the page address (A_7 through A_{14}) for each subsequent valid write cycle to the part during this operation must be the same as the initial page address.

The page write mode can be initiated during any write operation. Following the initial byte write cycle, the host can write an additional one to one hundred twenty-seven bytes in the same manner as the first byte was written. Each successive byte load cycle, started by the $\overline{WE}$ HIGH to LOW transition, must begin within 100µs of the falling edge of the preceding $\overline{WE}$. If a subsequent $\overline{WE}$ HIGH to LOW transition is not detected within 100µs, the internal automatic programming cycle will commence. There is no page write window limitation. Effectively the page write window is infinitely wide, so long as the host continues to access the device within the byte load cycle time of 100µs.

Write Operation Status Bits

The X28HC256 provides the user two write operation status bits. These can be used to optimize a system write cycle time. The status bits are mapped onto the I/O bus as shown in Figure 1.

Figure 1. Status Bit Assignment



$\overline{DATA}$ Polling (I/O_7)

The X28HC256 features $\overline{DATA}$ Polling as a method to indicate to the host system that the byte write or page write cycle has completed. $\overline{DATA}$ Polling allows a simple bit test operation to determine the status of the X28HC256, eliminating additional interrupt inputs or external hardware. During the internal programming cycle, any attempt to read the last byte written will produce the complement of that data on I/O_7 (i.e., write data = 0xxx xxxx, read data = 1xxx xxxx). Once the programming cycle is complete, I/O_7 will reflect true data.

Toggle Bit (I/O_6)

The X28HC256 also provides another method for determining when the internal write cycle is complete. During the internal programming cycle I/O_6 will toggle from HIGH to LOW and LOW to HIGH on subsequent attempts to read the device. When the internal cycle is complete the toggling will cease and the device will be accessible for additional read and write operations.

$\overline{DATA}$ POLLING I/O_7

Figure 2. $\overline{DATA}$ Polling Bus Sequence

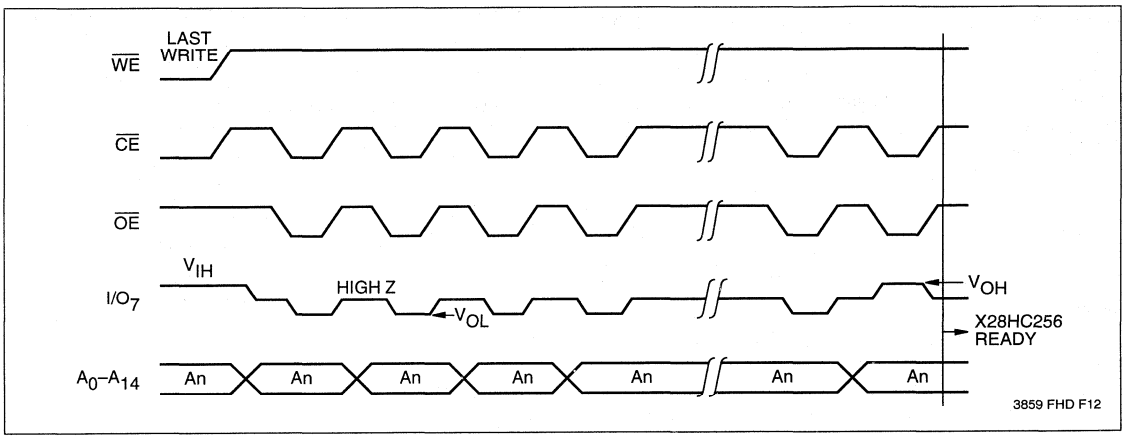
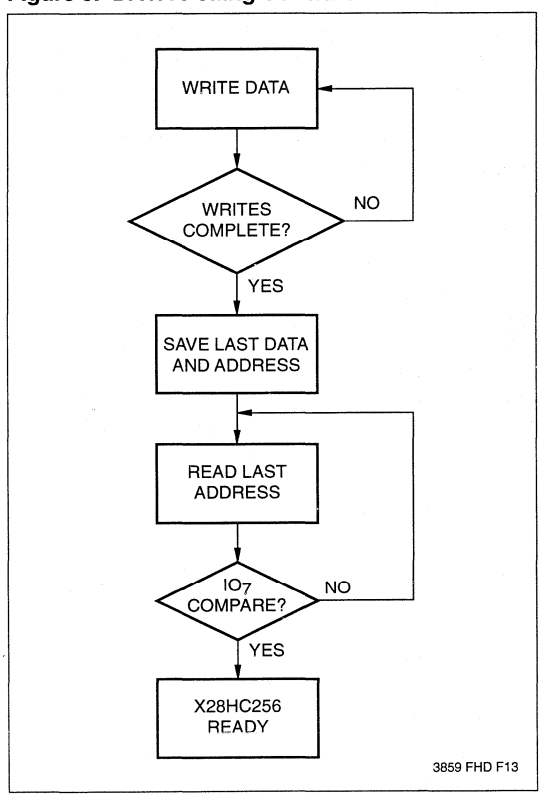


Figure 3. $\overline{DATA}$ Polling Software Flow



$\overline{DATA}$ Polling can effectively halve the time for writing to the X28HC256. The timing diagram in Figure 2 illustrates the sequence of events on the bus. The software flow diagram in Figure 3 illustrates one method of implementing the routine.

THE TOGGLE BIT I/O_6

Figure 4. Toggle Bit Bus Sequence

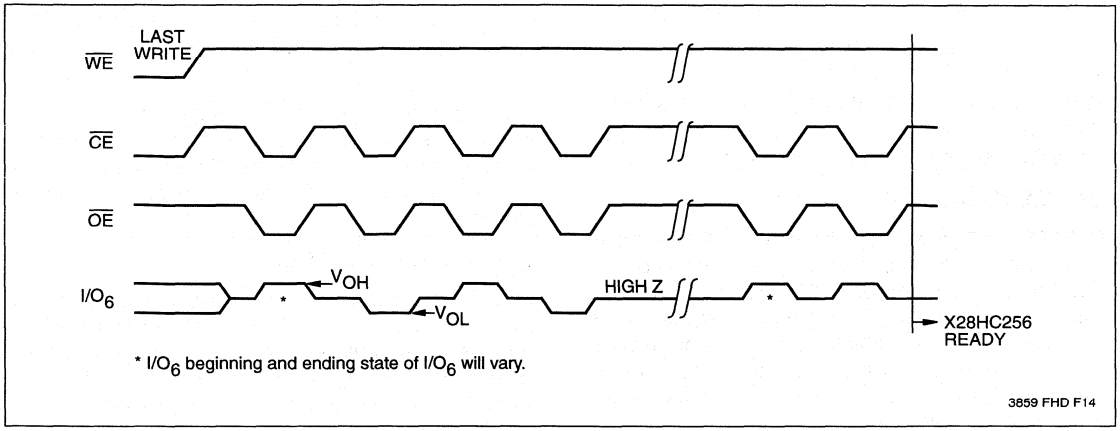
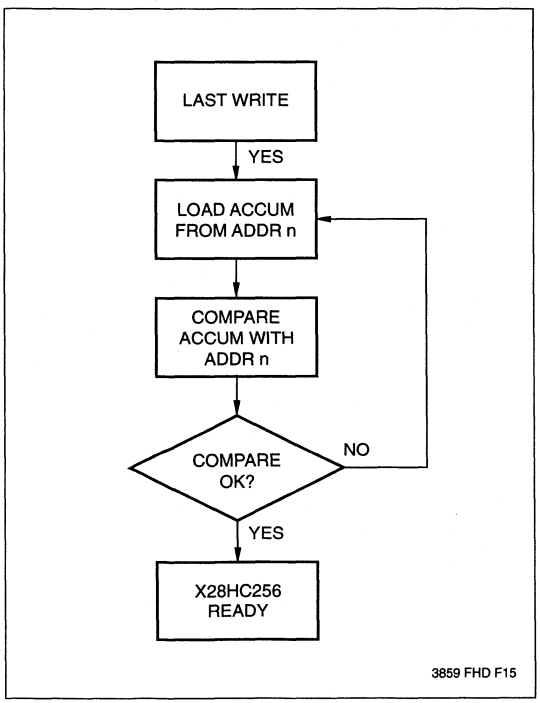


Figure 5. Toggle Bit Software Flow



The Toggle Bit can eliminate the software housekeeping chore of saving and fetching the last address and data written to a device in order to implement $\overline{DATA}$ Polling. This can be especially helpful in an array comprised of multiple X28HC256 memories that is frequently updated. The timing diagram in Figure 4 illustrates the sequence of events on the bus. The software flow diagram in Figure 5 illustrates a method for polling the Toggle Bit.

HARDWARE DATA PROTECTION

The X28HC256 provides two hardware features that protect nonvolatile data from inadvertent writes.

- Default V_{CC} Sense—All write functions are inhibited when V_{CC} is ≤ 3.5V Typically.
- Write Inhibit—Holding either $\overline{OE}$ LOW, $\overline{WE}$ HIGH, or $\overline{CE}$ HIGH will prevent an inadvertent write cycle during power-up and power-down, maintaining data integrity.

SOFTWARE DATA PROTECTION

The X28HC256 offers a software controlled data protection feature. The X28HC256 is shipped from Xicor with the software data protection NOT ENABLED; that is, the device will be in the standard operating mode. In this mode data should be protected during power-up/down operations through the use of external circuits. The host would then have open read and write access of the device once V_{CC} was stable.

The X28HC256 can be automatically protected during power-up and power-down without the need for external circuits by employing the software data protection feature. The internal software data protection circuit is enabled after the first write operation utilizing the software algorithm. This circuit is nonvolatile and will remain set for the life of the device unless the reset command is issued.

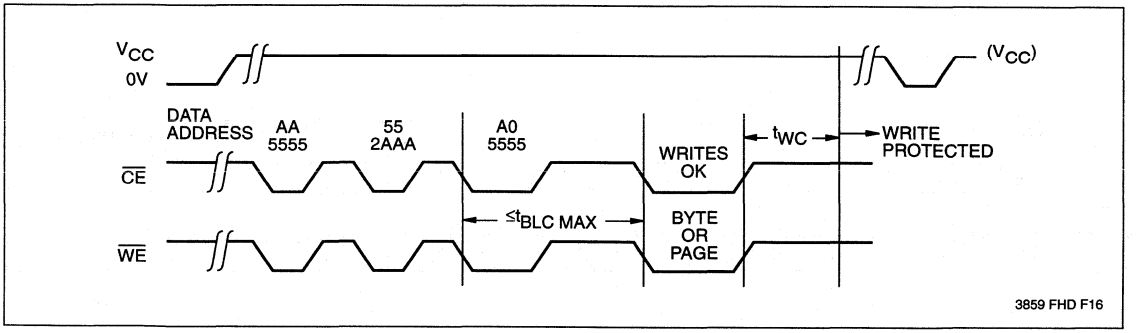
Once the software protection is enabled, the X28HC256 is also protected from inadvertent and accidental writes in the powered-up state. That is, the software algorithm must be issued prior to writing additional data to the device.

SOFTWARE ALGORITHM

Selecting the software data protection mode requires the host system to precede data write operations by a series of three write operations to three specific addresses. Refer to Figure 6 and 7 for the sequence. The three-byte sequence opens the page write window enabling the host to write from one to one hundred twenty-eight bytes of data. Once the page load cycle has been completed, the device will automatically be returned to the data protected state.

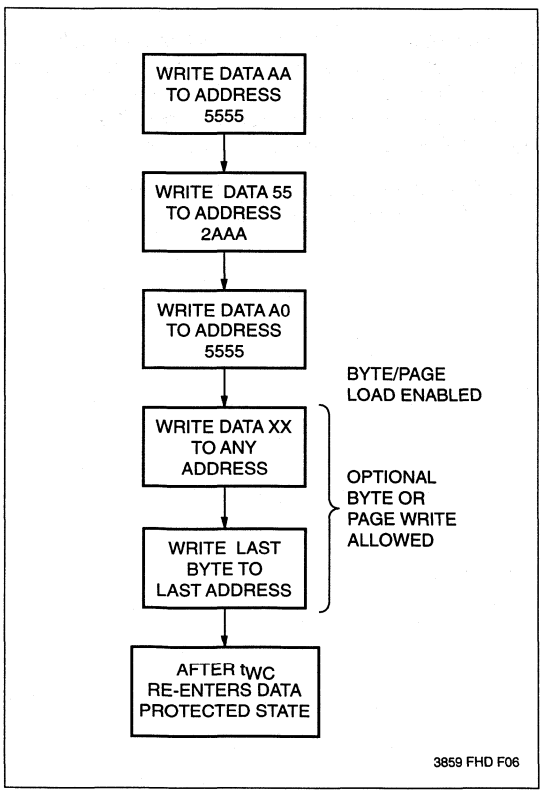
SOFTWARE DATA PROTECTION

Figure 6. Timing Sequence—Byte or Page Write



3

Figure 7. Write Sequence for Software Data Protection



Regardless of whether the device has previously been protected or not, once the software data protection algorithm is used and data has been written, the X28HC256 will automatically disable further writes unless another command is issued to cancel it. If no further commands are issued the X28HC256 will be write protected during power-down and after any subsequent power-up.

Note: Once initiated, the sequence of write operations should not be interrupted.

RESETTING SOFTWARE DATA PROTECTION

Figure 8. Reset Software Data Protection Timing Sequence

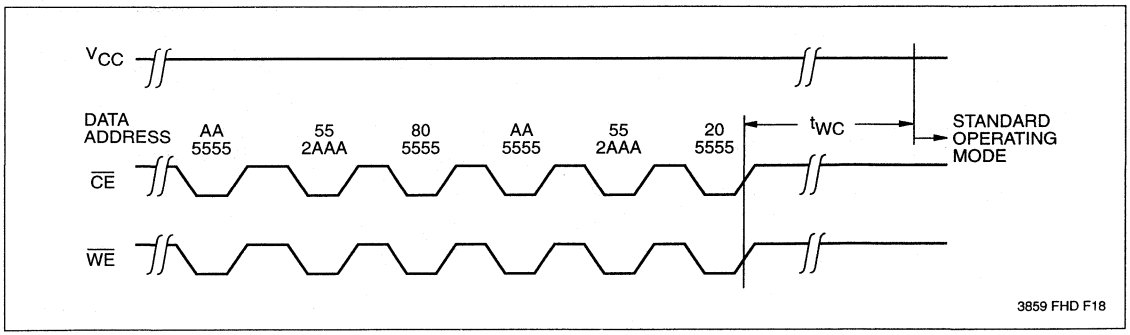
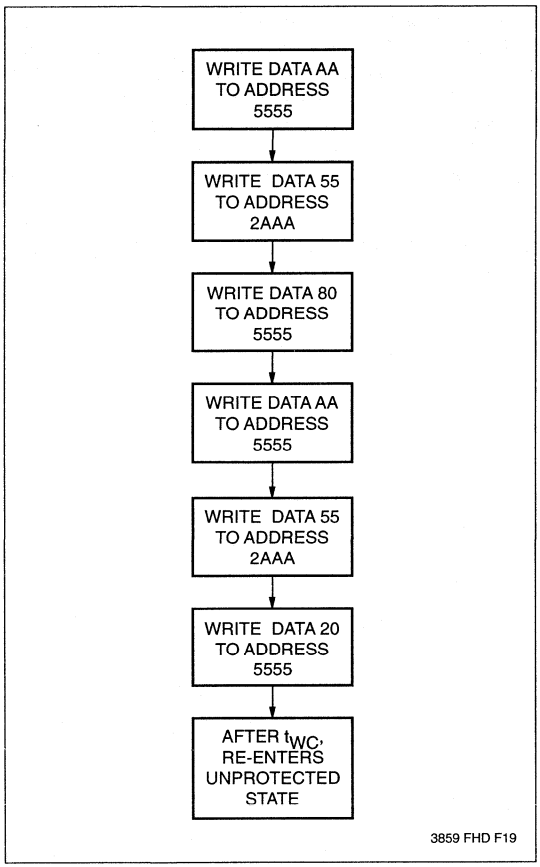


Figure 9. Write Sequence for resetting Software Data Protection



In the event the user wants to deactivate the software data protection feature for testing or reprogramming in an E²PROM programmer, the following six step algorithm will reset the internal protection circuit. After t_{WC}, the X28HC256 will be in standard operating mode.

Note: Once initiated, the sequence of write operations should not be interrupted.

SYSTEM CONSIDERATIONS

Because the X28HC256 is frequently used in large memory arrays it is provided with a two line control architecture for both read and write operations. Proper usage can provide the lowest possible power dissipation and eliminate the possibility of contention where multiple I/O pins share the same bus.

To gain the most benefit it is recommended that $\overline{CE}$ be decoded from the address bus and be used as the primary device selection input. Both $\overline{OE}$ and $\overline{WE}$ would then be common among all devices in the array. For a read operation this assures that all deselected devices are in their standby mode and that only the selected device(s) is outputting data on the bus.

Because the X28HC256 has two power modes, standby and active, proper decoupling of the memory array is of prime concern. Enabling $\overline{CE}$ will cause transient current spikes. The magnitude of these spikes is dependent on the output capacitive loading of the I/Os. Therefore, the larger the array sharing a common bus, the larger the transient spikes. The voltage peaks associated with the current transients can be suppressed by the proper selection and placement of decoupling capacitors. As a minimum, it is recommended that a 0.1μF high frequency ceramic capacitor be used between V_{CC} and V_{SS} at each device. Depending on the size of the array, the value of the capacitor may have to be larger.

In addition, it is recommended that a 4.7μF electrolytic bulk capacitor be placed between V_{CC} and V_{SS} for each eight devices employed in the array. This bulk capacitor is employed to overcome the voltage droop caused by the inductive effects of the PC board traces.

ABSOLUTE MAXIMUM RATINGS*

Temperature under Bias
- X28HC256 ..... –10°C to +85°C
- X28HC256I, X28HC256M ..... –65°C to +135°C

Storage Temperature ..... –65°C to +150°C
Voltage on any Pin with
- Respect to V_{SS} ..... –1V to +7V

D.C. Output Current 10mA
Lead Temperature (Soldering, 10 seconds) ..... 300°C

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	+70°C
Industrial	–40°C	+85°C
Military	–55°C	+125°C

3859 PGM T02.1

Supply Voltage	Limits
X28HC256	5V ±10%

3859 PGM T03.1

D.C. OPERATING CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.(7)	Max.		
I_{CC}	V_{CC} Active Current (TTL Inputs)		30	80	mA	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}, All I/O's = Open, Address Inputs = .4V/2.4V Levels @ f = 10MHz
I_{SB1}	V_{CC} Standby Current (TTL Inputs)		1	2	mA	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IL}, All I/O's = Open, Other Inputs = V_{IH}
I_{SB2}	V_{CC} Standby Current (CMOS Inputs)		200	500	µA	$\overline{CE}$ = V_{CC} – 0.3V, $\overline{OE}$ = GND, All I/Os = Open, Other Inputs = V_{CC} – 0.3V
I_{LI}	Input Leakage Current			10	µA	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output Leakage Current			10	µA	V_{OUT} = V_{SS} to V_{CC}, $\overline{CE}$ = V_{IH}
V_{IL}(2)	Input LOW Voltage	–1		0.8	V	
V_{IH}(2)	Input HIGH Voltage	2		V_{CC} + 1	V	
V_{OL}	Output LOW Voltage			0.4	V	I_{OL} = 6mA
V_{OH}	Output HIGH Voltage	2.4			V	I_{OH} = –4mA

3859 PGM T04.2

Notes: (1) Typical values are for T_A = 25°C and nominal supply voltage.
(2) V_{IL} min. and V_{IH} max. are for reference only and are not tested.

POWER-UP TIMING

Symbol	Parameter	Max.	Units
t_{PUR}(3)	Power-Up to Read	100	µs
t_{PUW}(3)	Power-Up to Write	5	ms

3859 PGM T05

CAPACITANCE T_A = +25°C, f = 1MHz, V_{CC} = 5V.

Symbol	Test	Max.	Units	Conditions
$C_{I/O}$(9)	Input/Output Capacitance	10	pF	$V_{I/O}$ = 0V
C_{IN}(9)	Input Capacitance	6	pF	V_{IN} = 0V

3859 PGM T06.2

ENDURANCE AND DATA RETENTION

Parameter	Min.	Max.	Units
Endurance	100,000		Cycles
Data Retention	100		Years

3859 PGM T07.1

A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3V
Input Rise and Fall Times	5ns
Input and Output Timing Levels	1.5V

3859 PGM T08.1

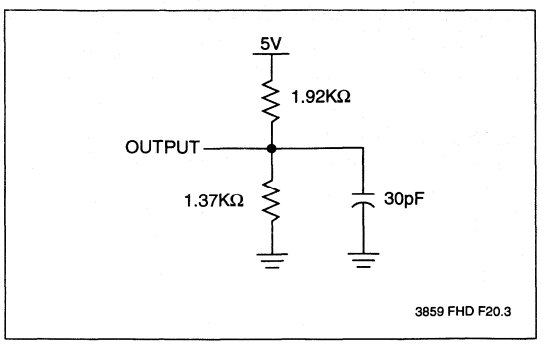
MODE SELECTION

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O	Power
L	L	H	Read	D_{OUT}	Active
L	H	L	Write	D_{IN}	Active
H	X	X	Standby and Write Inhibit	High Z	Standby
X	L	X	Write Inhibit	—	—
X	X	H	Write Inhibit	—	—

3859 PGM T09

Note: (3) This parameter is periodically sampled and not 100% tested.

EQUIVALENT A.C. LOAD CIRCUIT



SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

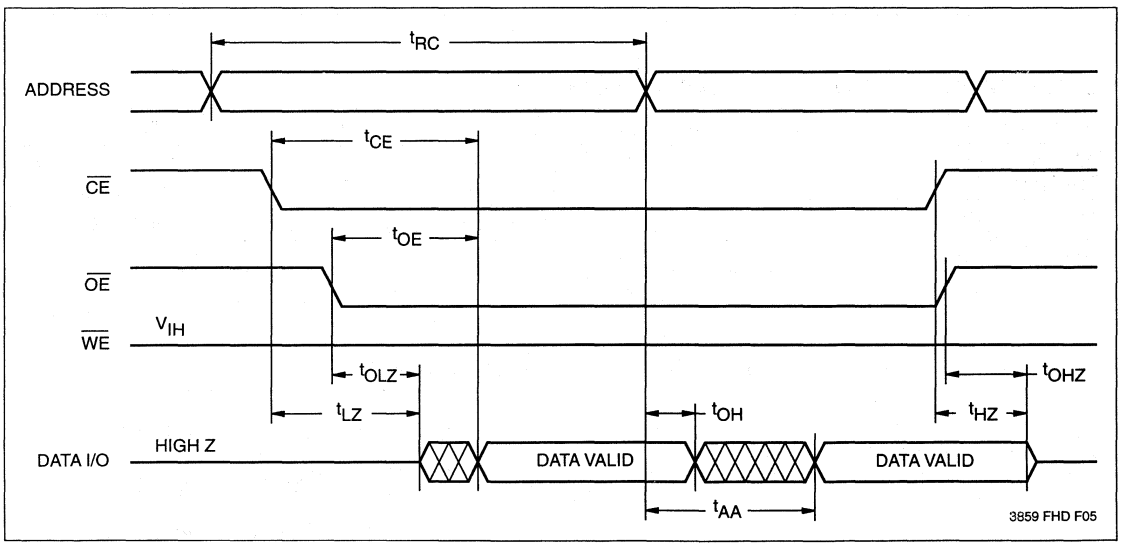
A.C. CHARACTERISTICS (Over the recommended operating conditions, unless otherwise specified.)

Read Cycle Limits

Symbol	Parameter	X28HC256-70		X28HC256-90		X28HC256-12		X28HC256-15		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}(5)	Read Cycle Time	70		90		120		150		ns
t_{CE}(5)	Chip Enable Access Time		70		90		120		150	ns
t_{AA}(5)	Address Access Time		70		90		120		150	ns
t_{OE}	Output Enable Access Time		35		40		50		50	ns
t_{LZ} (4)	$\overline{CE}$ LOW to Active Output	0		0		0		0		ns
t_{OLZ} (4)	$\overline{OE}$ LOW to Active Output	0		0		0		0		ns
t_{HZ} (4)	$\overline{CE}$ HIGH to High Z Output		35		40		50		50	ns
t_{OHZ} (4)	$\overline{OE}$ HIGH to High Z Output		35		40		50		50	ns
t_{OH}	Output Hold From Address Change	0		0		0		0		ns

3859 PGM T10.2

Read Cycle



Notes: (4) t_{LZ} min., t_{HZ}, t_{OLZ} min. and t_{OHZ} are periodically sampled and not 100% tested, t_{HZ} and t_{OHZ} are measured, with CL = 5pF, from the point whin $\overline{CE}$, $\overline{OE}$ return HIGH (whichever occurs first) to the time when the outputs are no longer driven.

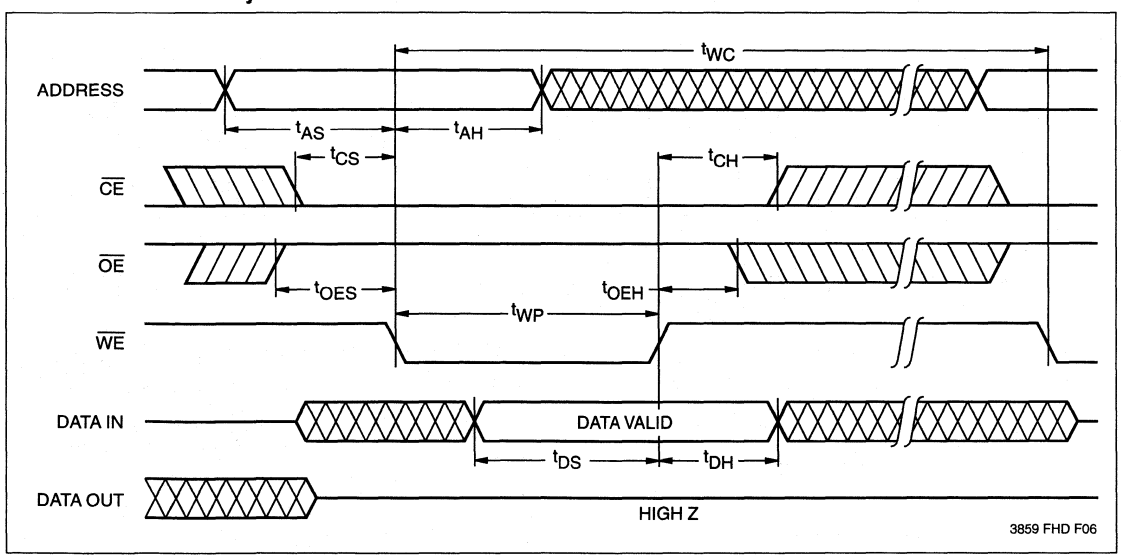
(5) For faster 256K products, refer to X28VC256 product line.

Write Cycle Limits

Symbol	Parameter	Min.	Typ.(6)	Max.	Units
t_{WC}(7)	Write Cycle Time		3	5	ms
t_{AS}	Address Setup Time	0			ns
t_{AH}	Address Hold Time	50			ns
t_{CS}	Write Setup Time	0			ns
t_{CH}	Write Hold Time	0			ns
t_{CW}	$\overline{CE}$ Pulse Width	50			ns
t_{OES}	$\overline{OE}$ HIGH Setup Time	0			ns
t_{OEH}	$\overline{OE}$ HIGH Hold Time	0			ns
t_{WP}	$\overline{WE}$ Pulse Width	50			ns
t_{WPH}(8)	$\overline{WE}$ HIGH Recovery (page write only)	50			ns
t_{DV}	Data Valid			1	µs
t_{DS}	Data Setup	50			ns
t_{DH}	Data Hold	0			ns
t_{DW}(8)	Delay to Next Write after Polling is True	10			µs
t_{BLC}	Byte Load Cycle	0.15		100	µs

3859 PGM T11.3

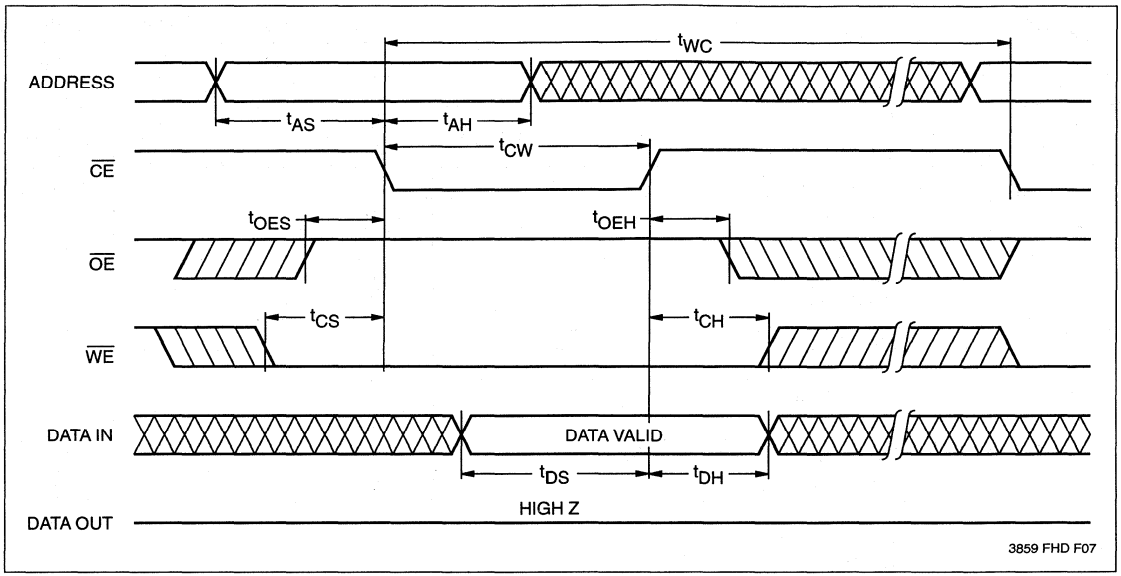
$\overline{WE}$ Controlled Write Cycle



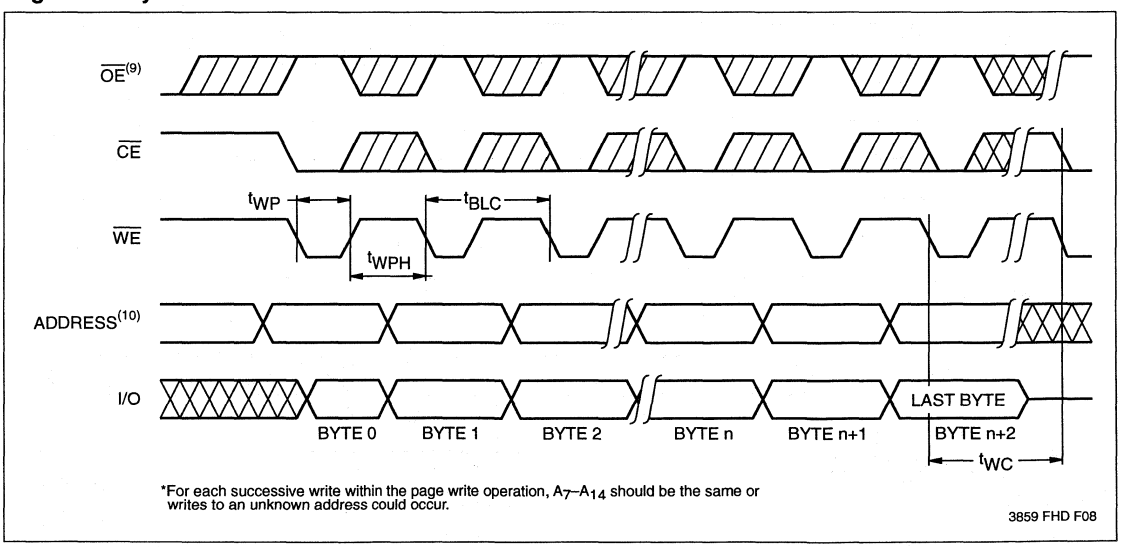
3859 FHD F06

Notes: (6) Typical values are for T_A = 25°C and nominal supply voltage.
(7) t_{WC} is the minimum cycle time to be allowed from the system perspective unless polling techniques are used. It is the maximum time the device requires to automatically complete the internal write operation.
(8) t_{WPH} and t_{DW} are periodically sampled and not 100% tested.

$\overline{CE}$ Controlled Write Cycle



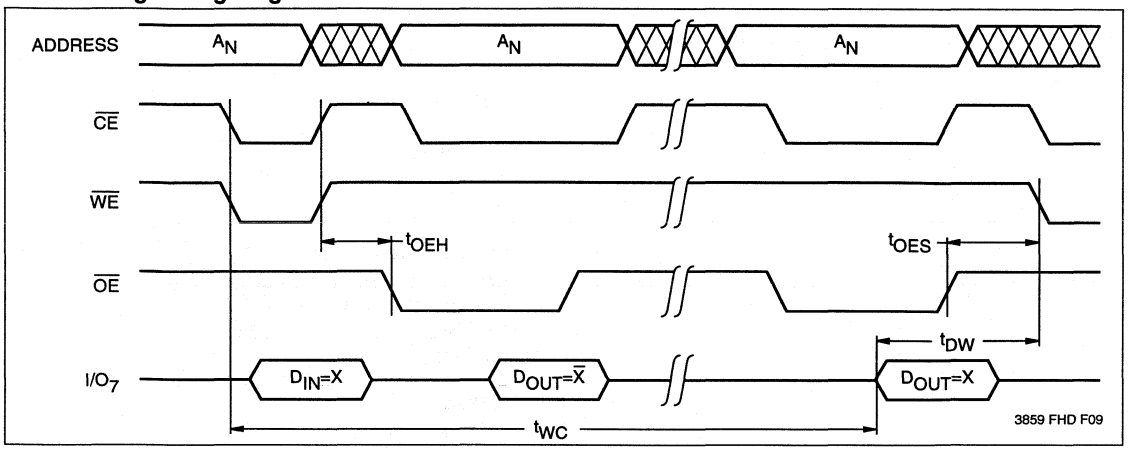
Page Write Cycle



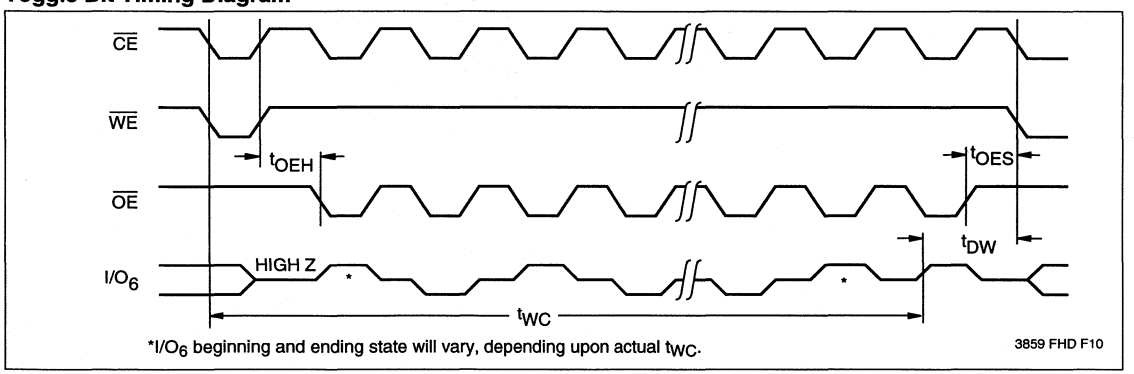
Notes: (9) Between successive byte writes within a page write operation, $\overline{OE}$ can be strobed LOW: e.g. this can be done with $\overline{CE}$ and $\overline{WE}$ HIGH to fetch data from another memory device within the system for the next write; or with $\overline{WE}$ HIGH and $\overline{CE}$ LOW effectively performing a polling operation.

(10) The timings shown above are unique to page write operations. Individual byte load operations within the page write must conform to either the $\overline{CE}$ or $\overline{WE}$ controlled write cycle timing.

$\overline{DATA}$ Polling Timing Diagram(11)

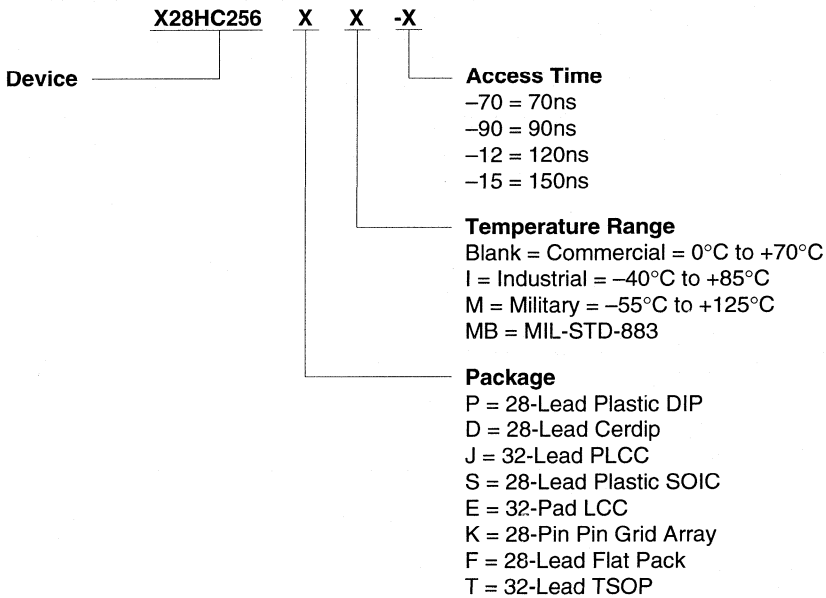


Toggle Bit Timing Diagram(11)



Note: (11) Polling operations are by definition read cycles and are therefore subject to read cycle timings.

ORDERING INFORMATION



5 Volt, Byte Alterable E²PROM

FEATURES

- **Access Time: 45ns**
- **Simple Byte and Page Write**
  - **—Single 5V Supply**
    - **—No External High Voltages or V_{PP} Control Circuits**
  - **—Self-Timed**
    - **—No Erase Before Write**
    - **—No Complex Programming Algorithms**
    - **—No Overerase Problem**
- **Low Power CMOS:**
  - **—Active: 80mA**
  - **—Standby: 10mA**
- **Software Data Protection**
  - **—Protects Data Against System Level Inadvertent Writes**
- **High Speed Page Write Capability**
- **Highly Reliable Direct Write™ Cell**
  - **—Endurance: 100,000 Write Cycles**
  - **—Data Retention: 100 Years**
- **Early End of Write Detection**
  - **—$\overline{DATA}$ Polling**
  - **—Toggle Bit Polling**

DESCRIPTION

The X28VC256 is a second generation high performance CMOS 32K x 8 E²PROM. It is fabricated with Xicor's proprietary, textured poly floating gate technology, providing a highly reliable 5 Volt only nonvolatile memory.

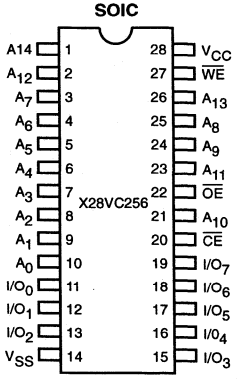
The X28VC256 supports a 128-byte page write operation, effectively providing a 24µs/byte write cycle and enabling the entire memory to be typically rewritten in less than 0.8 seconds. The X28VC256 also features $\overline{DATA}$ Polling and Toggle Bit Polling, two methods of providing early end of write detection. The X28VC256 also supports the JEDEC standard Software Data Protection feature for protecting against inadvertent writes during power-up and power-down.

Endurance for the X28VC256 is specified as a minimum 100,000 write cycles per byte and an inherent data retention of 100 years.

3

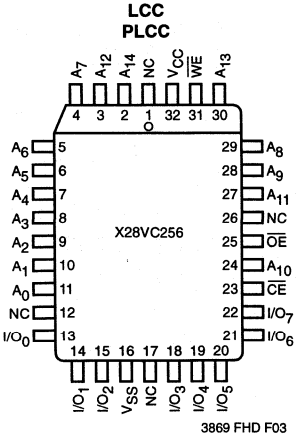
PIN CONFIGURATION

PLASTIC DIP
CERDIP
FLAT PACK
SOIC



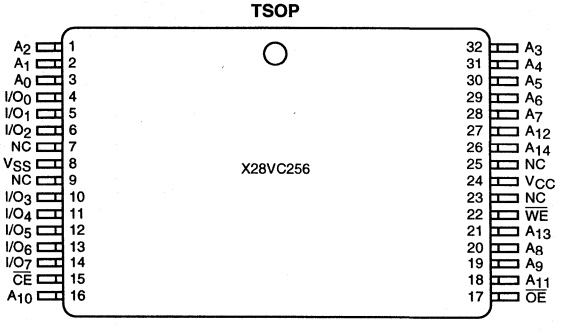
3869 FHD F02

LCC
PLCC



3869 FHD F03

TSOP



3869 ILL F22

PIN DESCRIPTIONS

Addresses (A_0–A_{14})

The Address inputs select an 8-bit memory location during a read or write operation.

Chip Enable ($\overline{CE}$)

The Chip Enable input must be LOW to enable all read/write operations. When $\overline{CE}$ is HIGH, power consumption is reduced.

Output Enable ($\overline{OE}$)

The Output Enable input controls the data output buffers and is used to initiate read operations.

Data In/Data Out (I/O_0–I/O_7)

Data is written to or read from the X28VC256 through the I/O pins.

Write Enable ($\overline{WE}$)

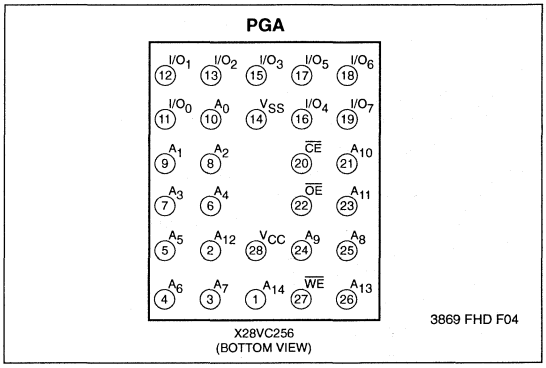
The Write Enable input controls the writing of data to the X28VC256.

PIN NAMES

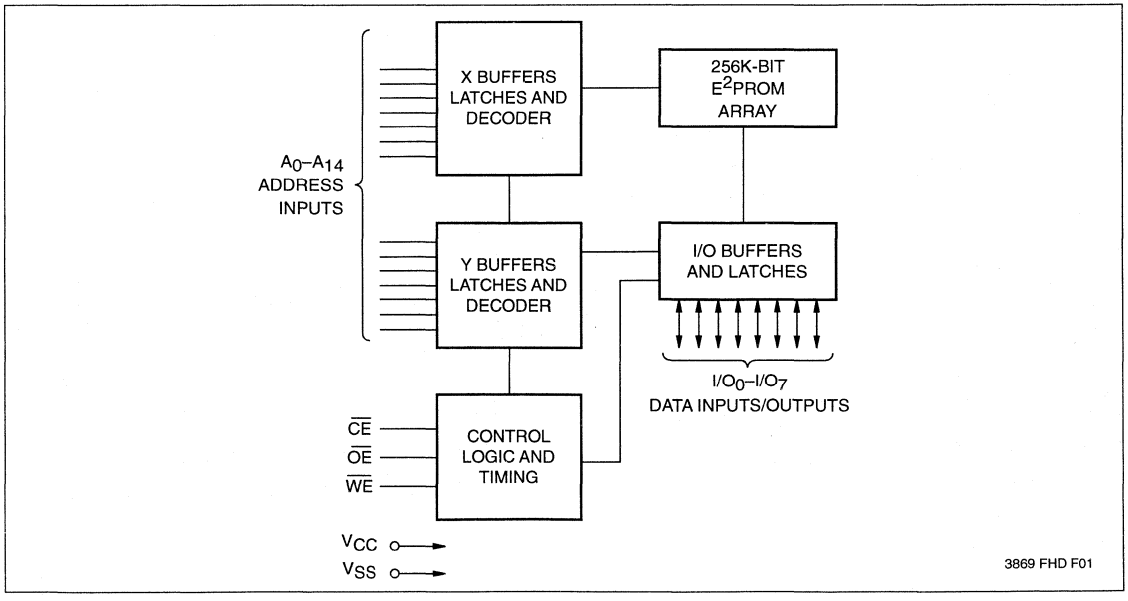
Symbol	Description
A_0–A_{14}	Address Inputs
I/O_0–I/O_7	Data Input/Output
$\overline{WE}$	Write Enable
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
V_{CC}	+5V
V_{SS}	Ground
NC	No Connect

3869 PGM T01

PIN CONFIGURATION



FUNCTIONAL DIAGRAM



DEVICE OPERATION

Read

Read operations are initiated by both $\overline{OE}$ and $\overline{CE}$ LOW. The read operation is terminated by either $\overline{CE}$ or $\overline{OE}$ returning HIGH. This two line control architecture eliminates bus contention in a system environment. The data bus will be in a high impedance state when either $\overline{OE}$ or $\overline{CE}$ is HIGH.

Write

Write operations are initiated when both $\overline{CE}$ and $\overline{WE}$ are LOW and $\overline{OE}$ is HIGH. The X28VC256 supports both a $\overline{CE}$ and $\overline{WE}$ controlled write cycle. That is, the address is latched by the falling edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs last. Similarly, the data is latched internally by the rising edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs first. A byte write operation, once initiated, will automatically continue to completion, typically within 3ms.

Page Write Operation

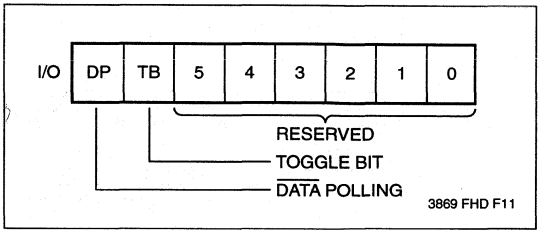
The page write feature of the X28VC256 allows the entire memory to be written in typically 0.8 seconds. Page write allows up to one hundred twenty-eight bytes of data to be consecutively written to the X28VC256 prior to the commencement of the internal programming cycle. The host can fetch data from another device within the system during a page write operation (change the source address), but the page address (A_7 through A_{14}) for each subsequent valid write cycle to the part during this operation must be the same as the initial page address.

The page write mode can be initiated during any write operation. Following the initial byte write cycle, the host can write an additional one to one hundred twenty-seven bytes in the same manner as the first byte was written. Each successive byte load cycle, started by the $\overline{WE}$ HIGH to LOW transition, must begin within 100µs of the falling edge of the preceding $\overline{WE}$. If a subsequent $\overline{WE}$ HIGH to LOW transition is not detected within 100µs, the internal automatic programming cycle will commence. There is no page write window limitation. Effectively the page write window is infinitely wide, so long as the host continues to access the device within the byte load cycle time of 100µs.

Write Operation Status Bits

The X28VC256 provides the user two write operation status bits. These can be used to optimize a system write cycle time. The status bits are mapped onto the I/O bus as shown in Figure 1.

Figure 1. Status Bit Assignment



$\overline{DATA}$ Polling (I/O_7)

The X28VC256 features $\overline{DATA}$ Polling as a method to indicate to the host system that the byte write or page write cycle has completed. $\overline{DATA}$ Polling allows a simple bit test operation to determine the status of the X28VC256, eliminating additional interrupt inputs or external hardware. During the internal programming cycle, any attempt to read the last byte written will produce the complement of that data on I/O_7 (i.e., write data = 0xxx xxxx, read data = 1xxx xxxx). Once the programming cycle is complete, I/O_7 will reflect true data.

Toggle Bit (I/O_6)

The X28VC256 also provides another method for determining when the internal write cycle is complete. During the internal programming cycle I/O_6 will toggle from HIGH to LOW and LOW to HIGH on subsequent attempts to read the device. When the internal cycle is complete the toggling will cease and the device will be accessible for additional read and write operations.

$\overline{DATA}$ POLLING I/O_7

Figure 2. $\overline{DATA}$ Polling Bus Sequence

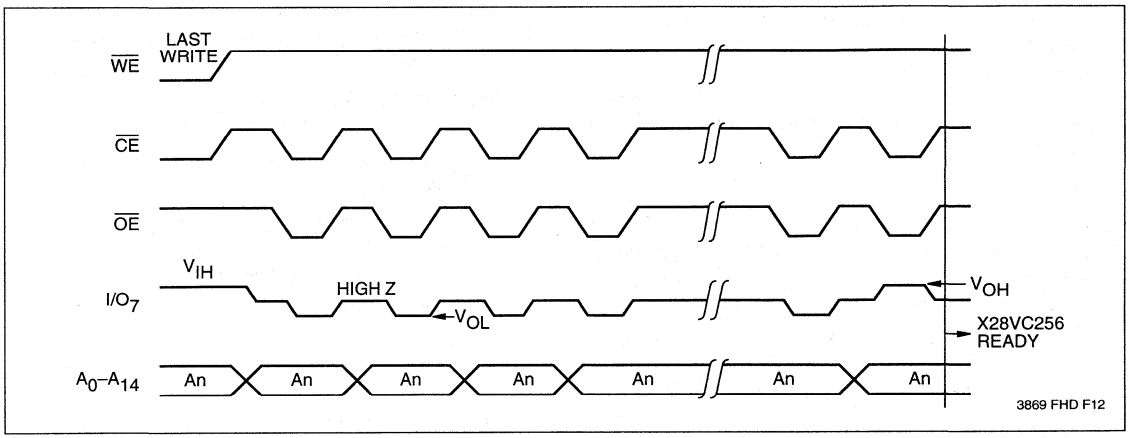
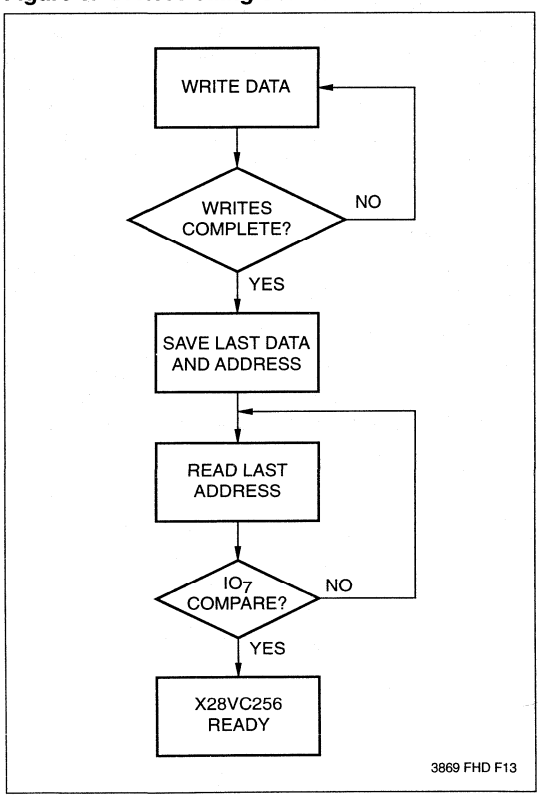


Figure 3. $\overline{DATA}$ Polling Software Flow



$\overline{DATA}$ Polling can effectively halve the time for writing to the X28VC256. The timing diagram in Figure 2 illustrates the sequence of events on the bus. The software flow diagram in Figure 3 illustrates one method of implementing the routine.

THE TOGGLE BIT I/O_6

Figure 4. Toggle Bit Bus Sequence

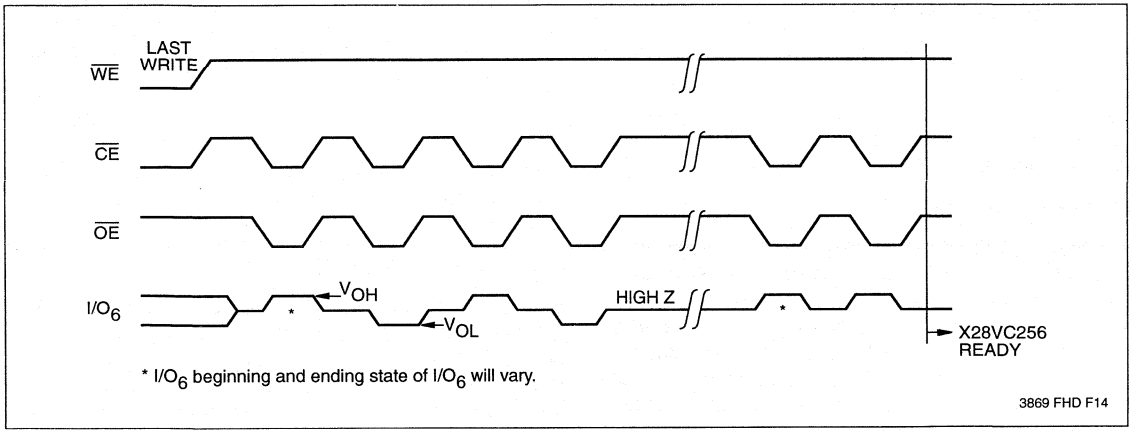
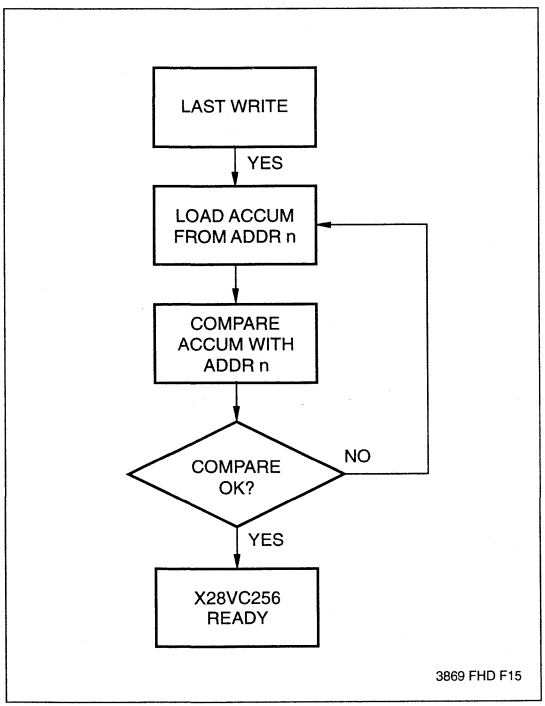


Figure 5. Toggle Bit Software Flow



The Toggle Bit can eliminate the software housekeeping chore of saving and fetching the last address and data written to a device in order to implement $\overline{DATA}$ Polling. This can be especially helpful in an array comprised of multiple X28VC256 memories that is frequently updated. The timing diagram in Figure 4 illustrates the sequence of events on the bus. The software flow diagram in Figure 5 illustrates a method for polling the Toggle Bit.

HARDWARE DATA PROTECTION

The X28VC256 provides two hardware features that protect nonvolatile data from inadvertent writes.

- Default V_{CC} Sense—All write functions are inhibited when V_{CC} is ≤ 3.5V typically.
- Write Inhibit—Holding either $\overline{OE}$ LOW, $\overline{WE}$ HIGH, or $\overline{CE}$ HIGH will prevent an inadvertent write cycle during power-up and power-down, maintaining data integrity.

SOFTWARE DATA PROTECTION

The X28VC256 offers a software controlled data protection feature. The X28VC256 is shipped from Xicor with the software data protection NOT ENABLED; that is, the device will be in the standard operating mode. In this mode data should be protected during power-up/down operations through the use of external circuits. The host would then have open read and write access of the device once V_{CC} was stable.

The X28VC256 can be automatically protected during power-up and power-down without the need for external circuits by employing the software data protection feature. The internal software data protection circuit is enabled after the first write operation utilizing the software algorithm. This circuit is nonvolatile and will remain set for the life of the device unless the reset command is issued.

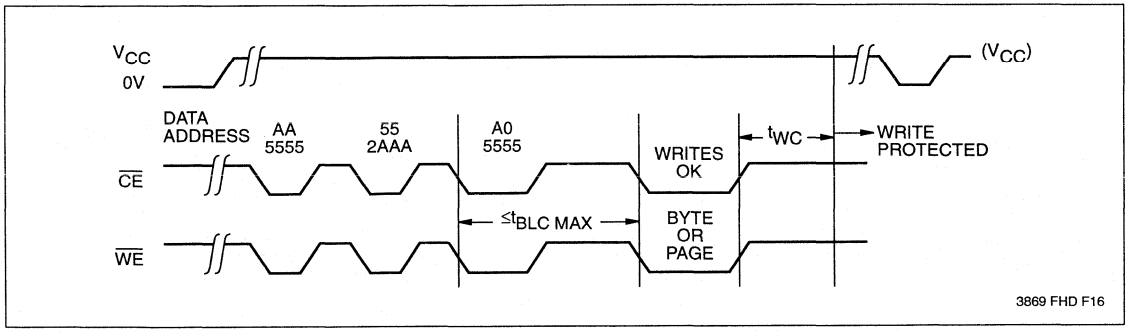
Once the software protection is enabled, the X28VC256 is also protected from inadvertent and accidental writes in the powered-up state. That is, the software algorithm must be issued prior to writing additional data to the device.

SOFTWARE ALGORITHM

Selecting the software data protection mode requires the host system to precede data write operations by a series of three write operations to three specific addresses. Refer to Figure 6 and 7 for the sequence. The three-byte sequence opens the page write window enabling the host to write from one to one hundred twenty-eight bytes of data. Once the page load cycle has been completed, the device will automatically be returned to the data protected state.

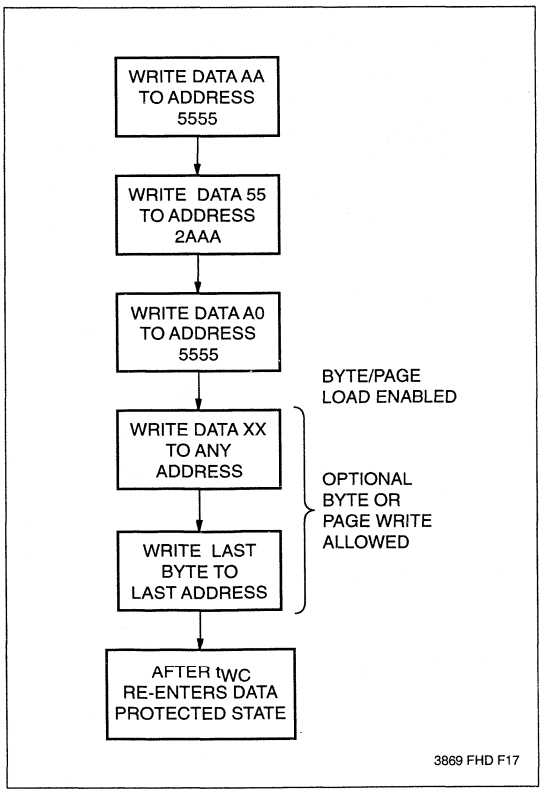
SOFTWARE DATA PROTECTION

Figure 6. Timing Sequence—Byte or Page Write



3

Figure 7. Write Sequence for Software Data Protection



Regardless of whether the device has previously been protected or not, once the software data protection algorithm is used and data has been written, the X28VC256 will automatically disable further writes unless another command is issued to cancel it. If no further commands are issued the X28VC256 will be write protected during power-down and after any subsequent power-up.

Note: Once initiated, the sequence of write operations should not be interrupted.

RESETTING SOFTWARE DATA PROTECTION

Figure 8. Reset Software Data Protection Timing Sequence

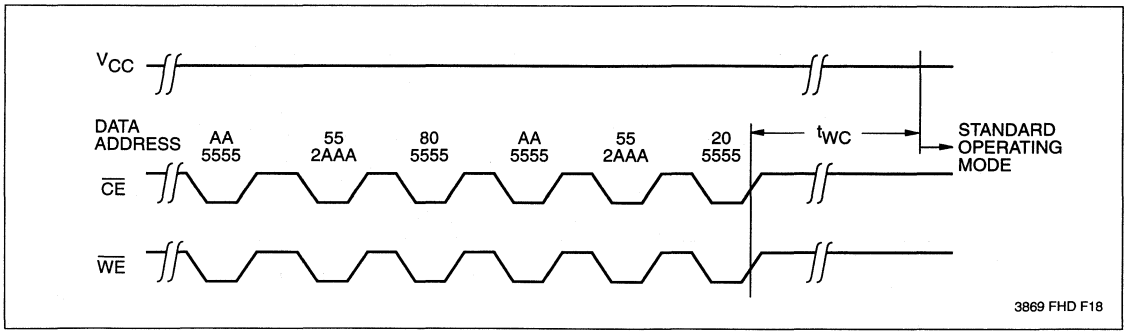
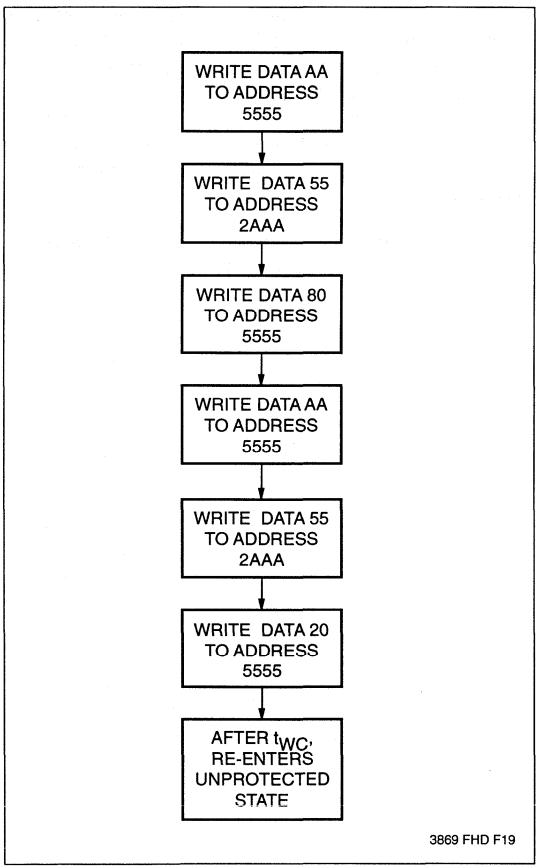


Figure 9. Write Sequence for Resetting Software Data Protection



In the event the user wants to deactivate the software data protection feature for testing or reprogramming in an E²PROM programmer, the following six step algorithm will reset the internal protection circuit. After t_{WC}, the X28VC256 will be in standard operating mode.

Note: Once initiated, the sequence of write operations should not be interrupted.

SYSTEM CONSIDERATIONS

Because the X28VC256 is frequently used in large memory arrays it is provided with a two line control architecture for both read and write operations. Proper usage can provide the lowest possible power dissipation and eliminate the possibility of contention where multiple I/O pins share the same bus.

To gain the most benefit it is recommended that $\overline{CE}$ be decoded from the address bus and be used as the primary device selection input. Both $\overline{OE}$ and $\overline{WE}$ would then be common among all devices in the array. For a read operation this assures that all deselected devices are in their standby mode and that only the selected device(s) is outputting data on the bus.

Because the X28VC256 has two power modes, standby and active, proper decoupling of the memory array is of prime concern. Enabling $\overline{CE}$ will cause transient current spikes. The magnitude of these spikes is dependent on the output capacitive loading of the I/Os. Therefore, the larger the array sharing a common bus, the larger the transient spikes. The voltage peaks associated with the current transients can be suppressed by the proper selection and placement of decoupling capacitors. As a minimum, it is recommended that a 0.1µF high frequency ceramic capacitor be used between V_{CC} and V_{SS} at each device. Depending on the size of the array, the value of the capacitor may have to be larger.

In addition, it is recommended that a 4.7µF electrolytic bulk capacitor be placed between V_{CC} and V_{SS} for each eight devices employed in the array. This bulk capacitor is employed to overcome the voltage droop caused by the inductive effects of the PC board traces.

ABSOLUTE MAXIMUM RATINGS*

Temperature under Bias
X28VC256 ..... −10°C to +85°C
X28VC256I, X28VC256M ..... −65°C to +135°C
Storage Temperature ..... −65°C to +150°C
Voltage on any Pin with
Respect to V_{SS} ..... −1V to +7V
D.C. Output Current 10mA
Lead Temperature (Soldering, 10 seconds) ..... 300°C

***COMMENT**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	+70°C
Industrial	−40°C	+85°C
Military	−55°C	+125°C

3869 PGM T02.1

Supply Voltage	Limits
X28VC256	5V ±10%

3869 PGM T03.1

D.C. OPERATING CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.(1)	Max.		
I_{CC}	V_{CC} Active Current		30	80	mA	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}, All I/O's = Open, Address Inputs = 0.4V/2.4V Levels @ f = 10MHz
I_{SB}	V_{CC} Standby Current		10	25	mA	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IL}, All I/O's = Open, Other Inputs = V_{IH}
I_{LI}	Input Leakage Current			10	µA	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output Leakage Current			10	µA	V_{OUT} = V_{SS} to V_{CC}, $\overline{CE}$ = V_{IH}
V_{IL}(2)	Input LOW Voltage	−1		0.8	V	
V_{IH}(2)	Input HIGH Voltage	2		V_{CC} + 1	V	
V_{OL}	Output LOW Voltage			0.4	V	I_{OL} = 6mA
V_{OH}	Output HIGH Voltage	2.4			V	I_{OH} = −4mA

3869 PGM T04.2

Notes: (1) Typical values are for T_A = 25°C and nominal supply voltage.
(2) V_{IL} min. and V_{IH} max. are for reference only and are not tested.

POWER-UP TIMING

Symbol	Parameter	Max.	Units
t_{PUR}(3)	Power-Up to Read	100	µs
t_{PUW}(3)	Power-Up to Write	5	ms

3869 PGM T05

CAPACITANCE T_A = +25°C, f = 1MHz, V_{CC} = 5V.

Symbol	Test	Max.	Units	Conditions
$C_{I/O}$(3)	Input/Output Capacitance	10	pF	$V_{I/O}$ = 0V
C_{IN}(3)	Input Capacitance	6	pF	V_{IN} = 0V

3869 PGM T06.1

ENDURANCE AND DATA RETENTION

Parameter	Min.	Max.	Units
Endurance	100,000		Cycles
Data Retention	100		Years

3869 PGM T07.1

A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3V
Input Rise and Fall Times	5ns
Input and Output Timing Levels	1.5V

3869 PGM T08.1

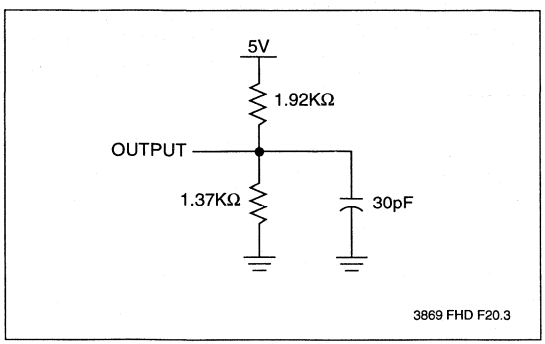
MODE SELECTION

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O	Power
L	L	H	Read	D_{OUT}	Active
L	H	L	Write	D_{IN}	Active
H	X	X	Standby and Write Inhibit	High Z	Standby
X	L	X	Write Inhibit	—	—
X	X	H	Write Inhibit	—	—

3869 PGM T09

Note: (3) This parameter is periodically sampled and not 100% tested.

EQUIVALENT A.C. LOAD CIRCUIT



3869 FHD F20.3

SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

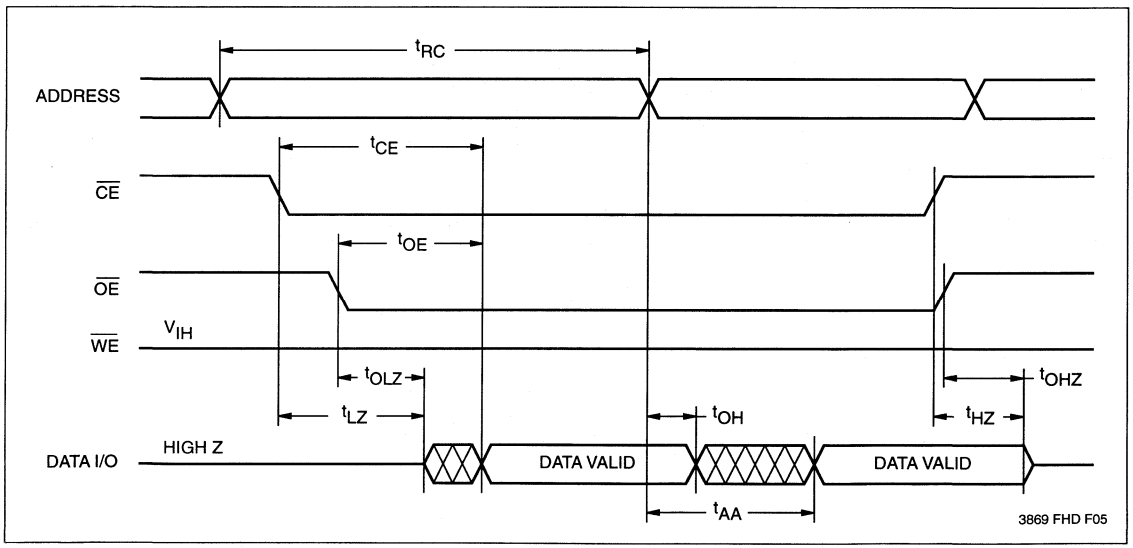
A.C. CHARACTERISTICS (Over the recommended operating conditions, unless otherwise specified.)

Read Cycle Limits

Symbol	Parameter	X28VC256-45 –40°C to 85°C		X28VC256-55 –55°C to 125°C		X28VC256-70 –55°C to 125°C		X28VC256-90 –55°C to 125°C		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	45		55		70		90	ns	
t_{CE}	Chip Enable Access Time		45		55		70		90	ns
t_{AA}	Address Access Time		45		55		70		90	ns
t_{OE}	Output Enable Access Time		30		30		35		40	ns
t_{LZ} (4)	$\overline{CE}$ LOW to Active Output	0		0		0		0		ns
t_{OLZ} (4)	$\overline{OE}$ LOW to Active Output	0		0		0		0		ns
t_{HZ} (4)	$\overline{CE}$ HIGH to High Z Output		30		30		35		40	ns
t_{OHZ} (4)	$\overline{OE}$ HIGH to High Z Output		30		30		35		40	ns
t_{OH}	Output Hold From Address Change	0		0		0		0		ns

3869 PGM T10.1

Read Cycle



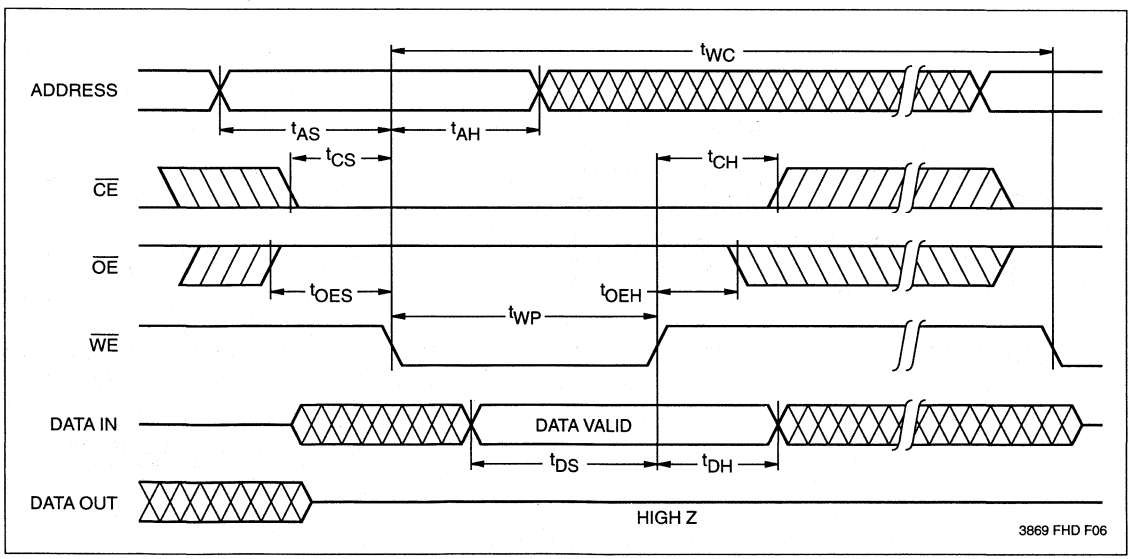
Notes: (4) t_{LZ} min., t_{HZ}, t_{OLZ} min. and t_{OHZ} are periodically sampled and not 100% tested, t_{HZ} and t_{OHZ} are measured, with CL = 5pF, from the point whin $\overline{CE}$, $\overline{OE}$ return HIGH (whichever occurs first) to the time when the outputs are no longer driven.

Write Cycle Limits

Symbol	Parameter	Min.	Typ.(5)	Max.	Units
t_{WC}(6)	Write Cycle Time		3	5	ms
t_{AS}	Address Setup Time	0			ns
t_{AH}	Address Hold Time	50			ns
t_{CS}	Write Setup Time	0			ns
t_{CH}	Write Hold Time	0			ns
t_{CW}	$\overline{CE}$ Pulse Width	50			ns
t_{OES}	$\overline{OE}$ HIGH Setup Time	0			ns
t_{OEH}	$\overline{OE}$ HIGH Hold Time	0			ns
t_{WP}	$\overline{WE}$ Pulse Width	50			ns
t_{WPH}(7)	$\overline{WE}$ HIGH Recovery (page write only)	50			ns
t_{DV}	Data Valid			1	µs
t_{DS}	Data Setup	50			ns
t_{DH}	Data Hold	0			ns
t_{DW}(7)	Delay to Next Write after Polling is True	10			µs
t_{BLC}	Byte Load Cycle	0.150		100	µs

3869 PGM T11.2

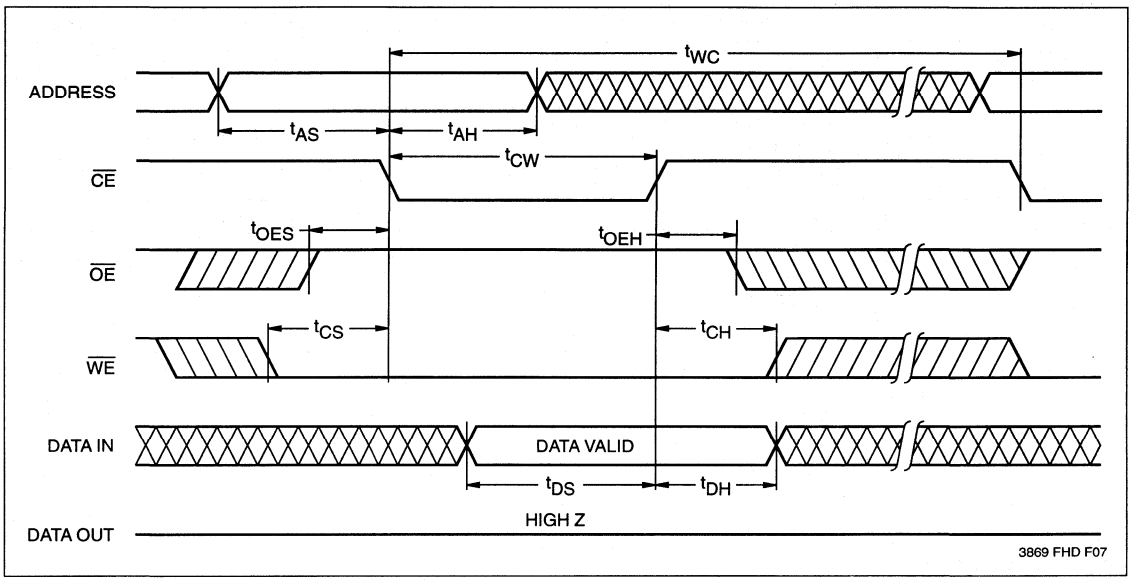
$\overline{WE}$ Controlled Write Cycle



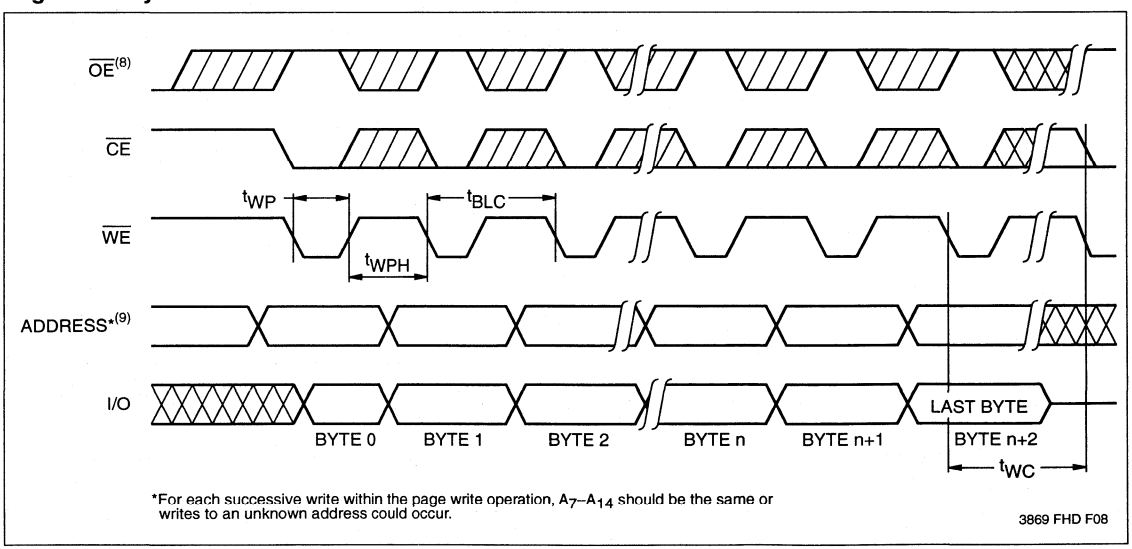
3869 FHD F06

Notes: (5) Typical values are for T_A = 25°C and nominal supply voltage.
(6) t_{WC} is the minimum cycle time to be allowed from the system perspective unless polling techniques are used. It is the maximum time the device requires to automatically complete the internal write operation.
(7) t_{WPH} and t_{DW} are periodically sampled and not 100% tested.

$\overline{CE}$ Controlled Write Cycle



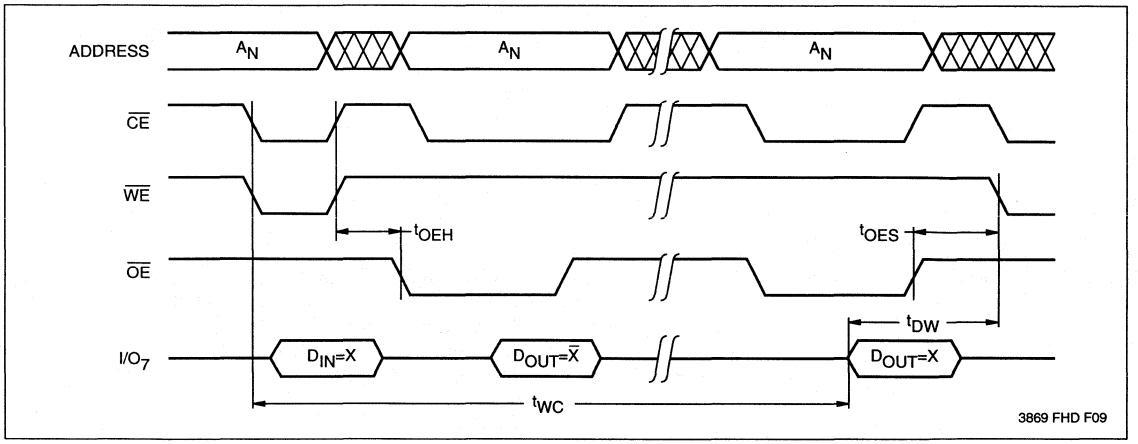
Page Write Cycle



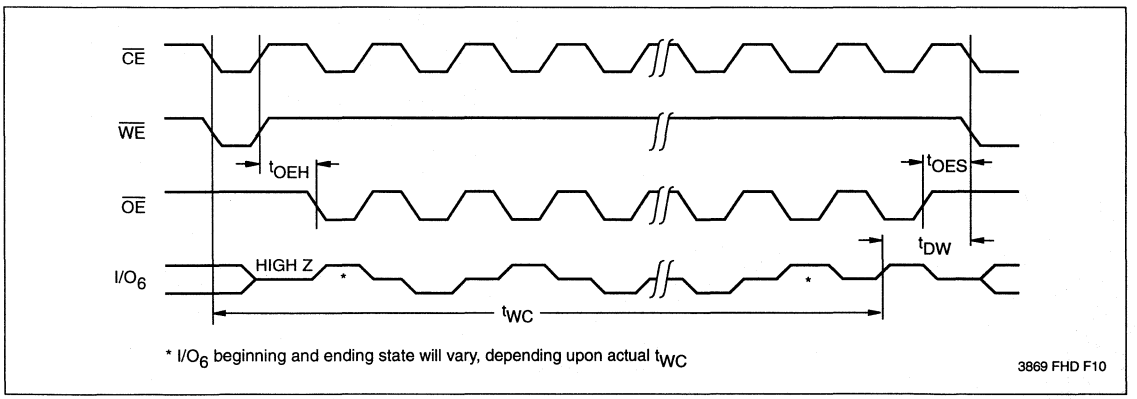
Notes: (8) Between successive byte writes within a page write operation, $\overline{OE}$ can be strobed LOW: e.g. this can be done with $\overline{CE}$ and $\overline{WE}$ HIGH to fetch data from another memory device within the system for the next write; or with $\overline{WE}$ HIGH and $\overline{CE}$ LOW effectively performing a polling operation.

(9) The timings shown above are unique to page write operations. Individual byte load operations within the page write must conform to either the $\overline{CE}$ or $\overline{WE}$ controlled write cycle timing.

$\overline{\text{DATA}}$ Polling Timing Diagram[10]

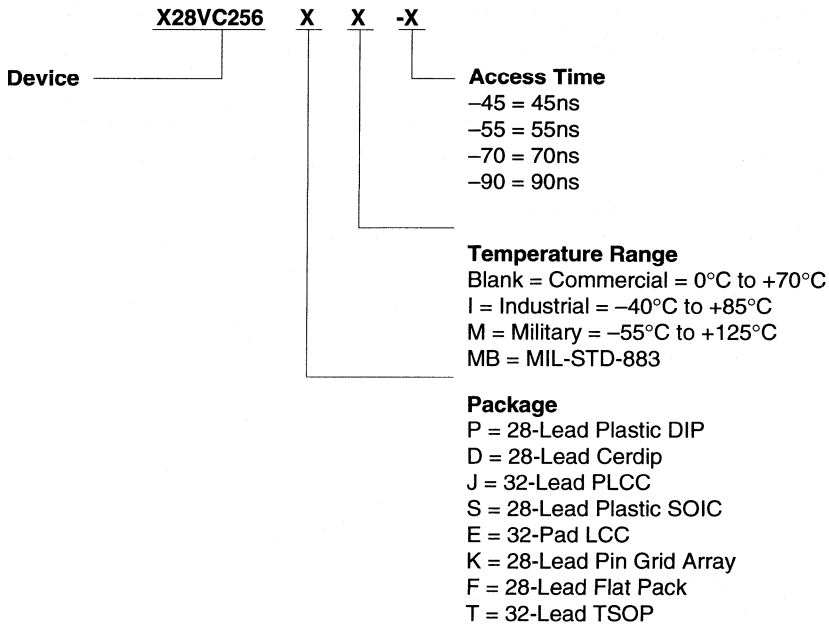


Toggle Bit Timing Diagram[10]



Note: (10) Polling operations are by definition read cycles and are therefore subject to read cycle timings.

ORDERING INFORMATION



5 Volt, Byte Alterable E²PROM

FEATURES

- Access Time: 90ns
- Simple Byte and Page Write
  - —Single 5V Supply
    - — No External High Voltages or V_{PP} Control Circuits
  - —Self-Timed
    - —No Erase Before Write
    - —No Complex Programming Algorithms
    - —No Overerase Problem
- Low Power CMOS:
  - —Active: 50mA
  - —Standby: 500µA
- Software Data Protection
  - —Protects Data Against System Level Inadvertant Writes
- High Speed Page Write Capability
- Highly Reliable Direct Write™ Cell
  - —Endurance: 100,000 Write Cycles
  - —Data Retention: 100 Years
- Early End of Write Detection
  - —$\overline{DATA}$ Polling
  - —Toggle Bit Polling
- Two PLCC and LCC Pinouts
  - —X28C512
    - —X28C010 E²PROM Pin Compatible
  - —X28C513
    - —Compatible with Lower Density E²PROMs

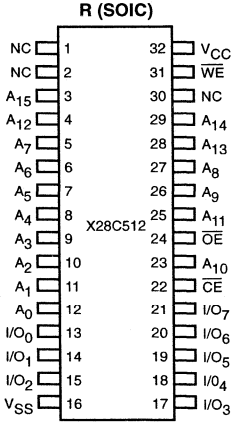
DESCRIPTION

The X28C512/513 is an 64K x 8 E²PROM, fabricated with Xicor's proprietary, high performance, floating gate CMOS technology. Like all Xicor programmable nonvolatile memories the X28C512/513 is a 5V only device. The X28C512/513 features the JEDEC approved pinout for bytewide memories, compatible with industry standard EPROMS.

The X28C512/513 supports a 128-byte page write operation, effectively providing a 39µs/byte write cycle and enabling the entire memory to be written in less than 2.5 seconds. The X28C512/513 also features $\overline{DATA}$ Polling and Toggle Bit Polling, system software support schemes used to indicate the early completion of a write cycle. In addition, the X28C512/513 supports the Software Data Protection option.

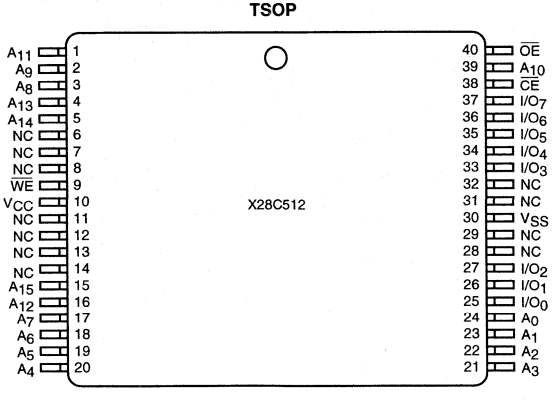
PIN CONFIGURATION

PLASTIC DIP
CERDIP
FLAT PACK
R (SOIC)



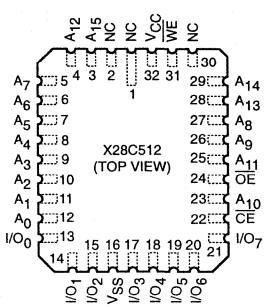
3856 FHD F01

TSOP

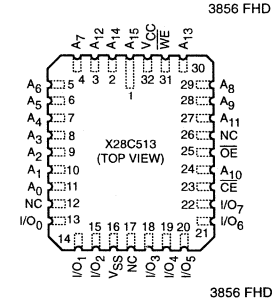


3856 ILL F22

PLCC/LCC



3856 FHD F03



3856 FHD F04

PIN DESCRIPTIONS

Addresses (A_0–A_{15})

The Address inputs select an 8-bit memory location during a read or write operation.

Chip Enable ($\overline{CE}$)

The Chip Enable input must be LOW to enable all read/write operations. When $\overline{CE}$ is HIGH, power consumption is reduced.

Output Enable ($\overline{OE}$)

The Output Enable input controls the data output buffers and is used to initiate read operations.

Data In/Data Out (I/O_0–I/O_7)

Data is written to or read from the X28C512/513 through the I/O pins.

Write Enable ($\overline{WE}$)

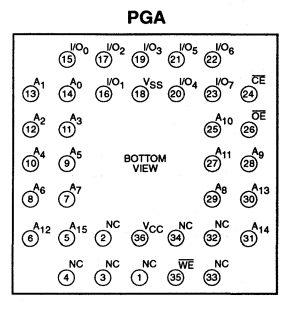
The Write Enable input controls the writing of data to the X28C512/513.

PIN NAMES

Symbol	Description
A_0–A_{15}	Address Inputs
I/O_0–I/O_7	Data Input/Output
$\overline{WE}$	Write Enable
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
V_{CC}	+5V
V_{SS}	Ground
NC	No Connect

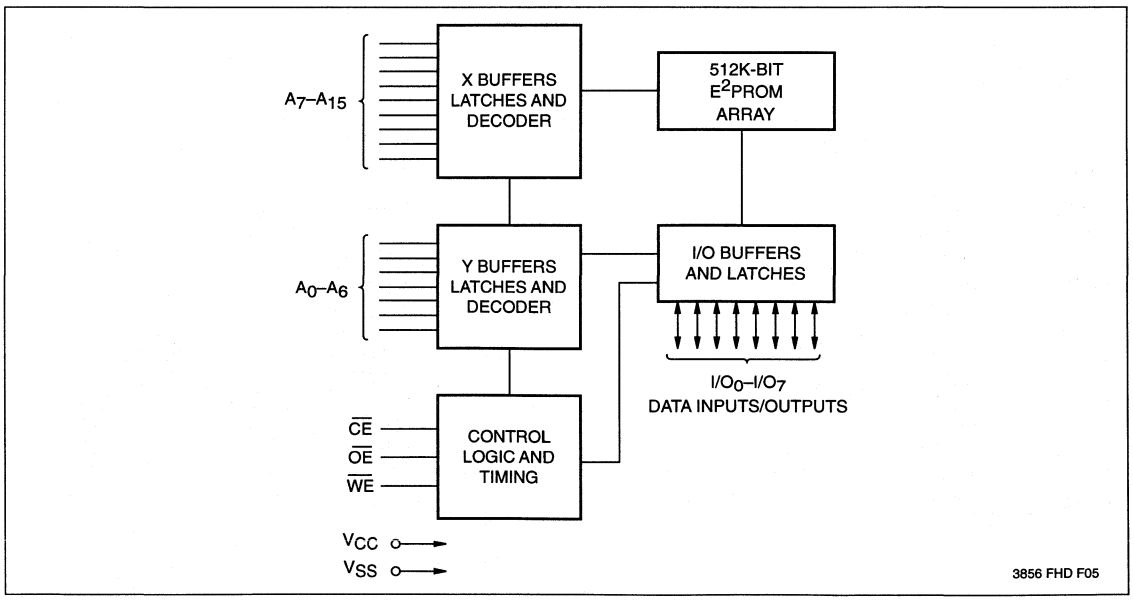
3856 PGM T01

PIN CONFIGURATION



3856 FHD F02

FUNCTIONAL DIAGRAM



3856 FHD F05

DEVICE OPERATION

Read

Read operations are initiated by both $\overline{OE}$ and $\overline{CE}$ LOW. The read operation is terminated by either $\overline{CE}$ or $\overline{OE}$ returning HIGH. This two line control architecture eliminates bus contention in a system environment. The data bus will be in a high impedance state when either $\overline{OE}$ or $\overline{CE}$ is HIGH.

Write

Write operations are initiated when both $\overline{CE}$ and $\overline{WE}$ are LOW and $\overline{OE}$ is HIGH. The X28C512/513 supports both a $\overline{CE}$ and $\overline{WE}$ controlled write cycle. That is, the address is latched by the falling edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs last. Similarly, the data is latched internally by the rising edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs first. A byte write operation, once initiated, will automatically continue to completion, typically within 5ms.

Page Write Operation

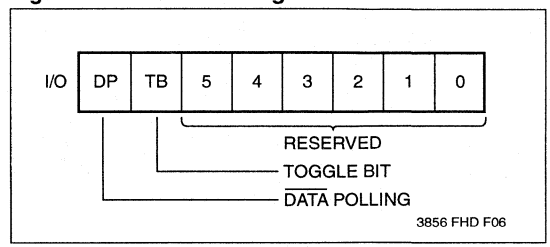
The page write feature of the X28C512/513 allows the entire memory to be written in 2.5 seconds. Page write allows two to one hundred twenty-eight bytes of data to be consecutively written to the X28C512/513 prior to the commencement of the internal programming cycle. The host can fetch data from another device within the system during a page write operation (change the source address), but the page address (A_7 through A_{15}) for each subsequent valid write cycle to the part during this operation must be the same as the initial page address.

The page write mode can be initiated during any write operation. Following the initial byte write cycle, the host can write an additional one to one hundred twenty-seven bytes in the same manner as the first byte was written. Each successive byte load cycle, started by the $\overline{WE}$ HIGH to LOW transition, must begin within 100µs of the falling edge of the preceding $\overline{WE}$. If a subsequent $\overline{WE}$ HIGH to LOW transition is not detected within 100µs, the internal automatic programming cycle will commence. There is no page write window limitation. Effectively the page write window is infinitely wide, so long as the host continues to access the device within the byte load cycle time of 100µs.

Write Operation Status Bits

The X28C512/513 provides the user two write operation status bits. These can be used to optimize a system write cycle time. The status bits are mapped onto the I/O bus as shown in Figure 1.

Figure 1. Status Bit Assignment



$\overline{DATA}$ Polling (I/O_7)

The X28C512/513 features $\overline{DATA}$ Polling as a method to indicate to the host system that the byte write or page write cycle has completed. $\overline{DATA}$ Polling allows a simple bit test operation to determine the status of the X28C512/513, eliminating additional interrupt inputs or external hardware. During the internal programming cycle, any attempt to read the last byte written will produce the complement of that data on I/O_7 (i.e. write data = 0xxx xxxx, read data = 1xxx xxxx). Once the programming cycle is complete, I/O_7 will reflect true data.

Toggle Bit (I/O_6)

The X28C512/513 also provides another method for determining when the internal write cycle is complete. During the internal programming cycle, I/O_6 will toggle from HIGH to LOW and LOW to HIGH on subsequent attempts to read the device. When the internal cycle is complete the toggling will cease and the device will be accessible for additional read or write operations.

$\overline{DATA}$ Polling I/O_7

Figure 2a. $\overline{DATA}$ Polling Bus Sequence

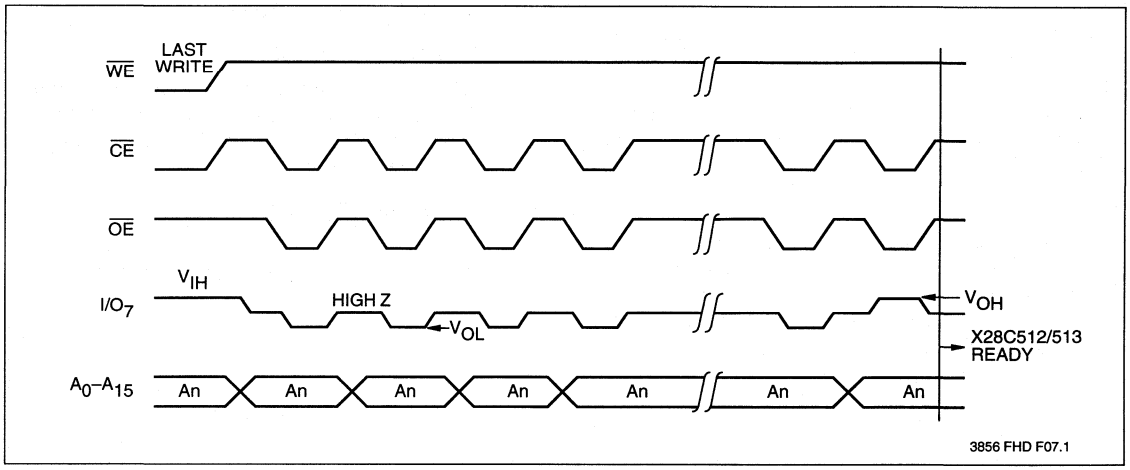
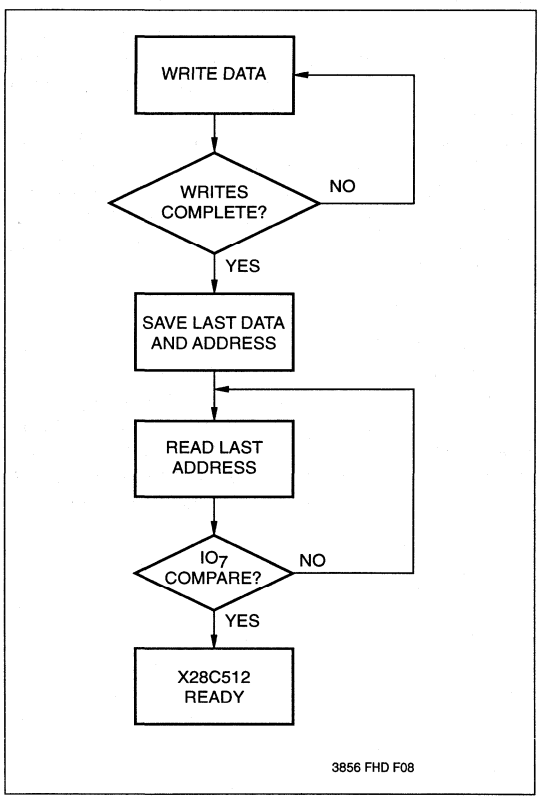


Figure 2b. $\overline{DATA}$ Polling Software Flow



$\overline{DATA}$ Polling can effectively halve the time for writing to the X28C512/513. The timing diagram in Figure 2a illustrates the sequence of events on the bus. The software flow diagram in Figure 2b illustrates one method of implementing the routine.

The Toggle Bit I/O_6

Figure 3a. Toggle Bit Bus Sequence

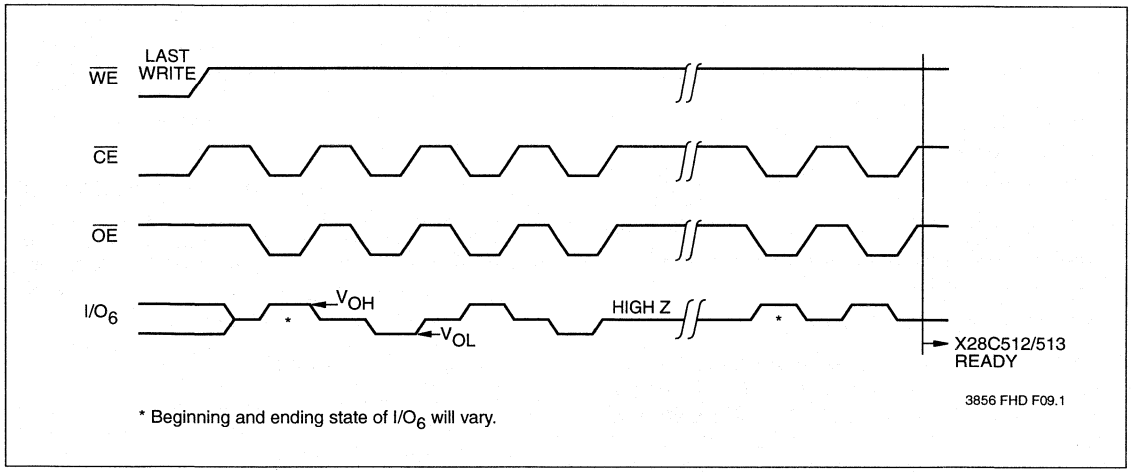
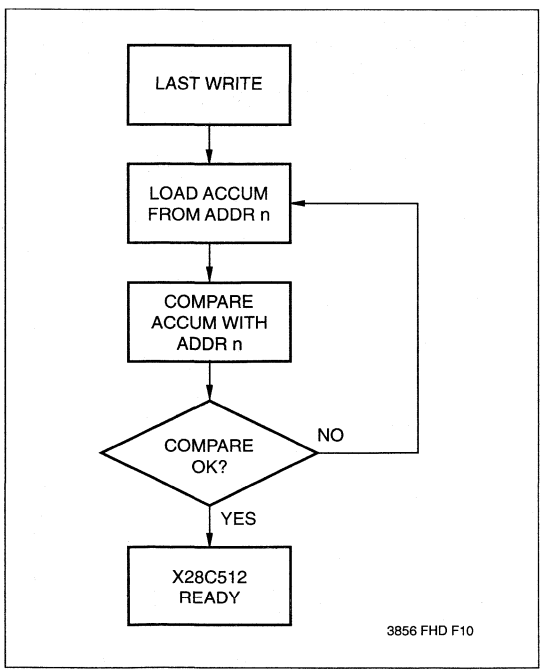


Figure 3b. Toggle Bit Software Flow



The Toggle Bit can eliminate the software housekeeping chore of saving and fetching the last address and data written to a device in order to implement $\overline{DATA}$ Polling. This can be especially helpful in an array comprised of multiple X28C512/513 memories that is frequently updated. Toggle Bit Polling can also provide a method for status checking in multiprocessor applications. The timing diagram in Figure 3a illustrates the sequence of events on the bus. The software flow diagram in Figure 3b illustrates a method for polling the Toggle Bit.

HARDWARE DATA PROTECTION

The X28C512/513 provides three hardware features that protect nonvolatile data from inadvertent writes.

- Noise Protection—A $\overline{WE}$ pulse typically less than 10ns will not initiate a write cycle.
- Default V_{CC} Sense—All write functions are inhibited when V_{CC} is ≤3.6V.
- Write Inhibit—Holding either $\overline{OE}$ LOW, $\overline{WE}$ HIGH, or $\overline{CE}$ HIGH will prevent an inadvertent write cycle during power-up and power-down, maintaining data integrity. Write cycle timing specifications must be observed concurrently.

SOFTWARE DATA PROTECTION

The X28C512/513 offers a software controlled data protection feature. The X28C512/513 is shipped from Xicor with the software data protection NOT ENABLED; that is, the device will be in the standard operating mode. In this mode data should be protected during power-up/-down operations through the use of external circuits. The host would then have open read and write access of the device once V_{CC} was stable.

The X28C512/513 can be automatically protected during power-up and power-down without the need for external circuits by employing the software data protection feature. The internal software data protection circuit is enabled after the first write operation utilizing the software algorithm. This circuit is nonvolatile and will remain set for the life of the device unless the reset command is issued.

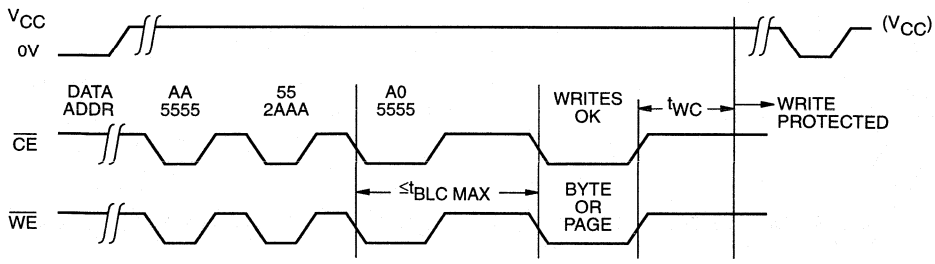
Once the software protection is enabled, the X28C512/513 is also protected from inadvertent and accidental writes in the powered-up state. That is, the software algorithm must be issued prior to writing additional data to the device. Note: The data in the three-byte enable sequence is not written to the memory array.

SOFTWARE ALGORITHM

Selecting the software data protection mode requires the host system to precede data write operations by a series of three write operations to three specific addresses. Refer to Figure 4a and 4b for the sequence. The three byte sequence opens the page write window enabling the host to write from one to one hundred twenty-eight bytes of data. Once the page load cycle has been completed, the device will automatically be returned to the data protected state.

Software Data Protection

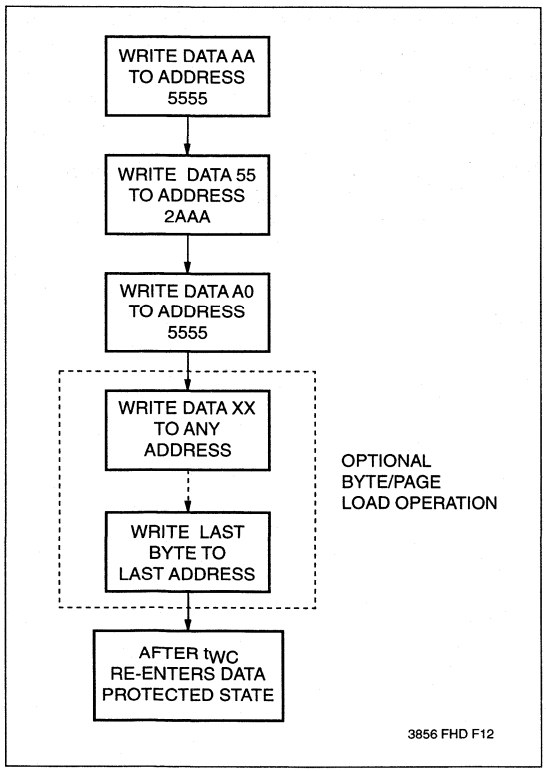
Figure 4a. Timing Sequence—Software Data Protect Enable Sequence followed by Byte or Page Write



NOTE: All other timings and control pins are per page write timing requirements.

3856 FHD F11

Figure 4b. Write Sequence for Software Data Protection



3856 FHD F12

Regardless of whether the device has previously been protected or not, once the software data protected algorithm is used and data has been written, the X28C512/513 will automatically disable further writes unless another command is issued to cancel it. If no further commands are issued the X28C512/513 will be write protected during power-down and after any subsequent power-up. The state of A_{15} while executing the algorithm is don't care.

Note: Once initiated, the sequence of write operations should not be interrupted.

Resetting Software Data Protection

Figure 5a. Reset Software Data Protection Timing Sequence

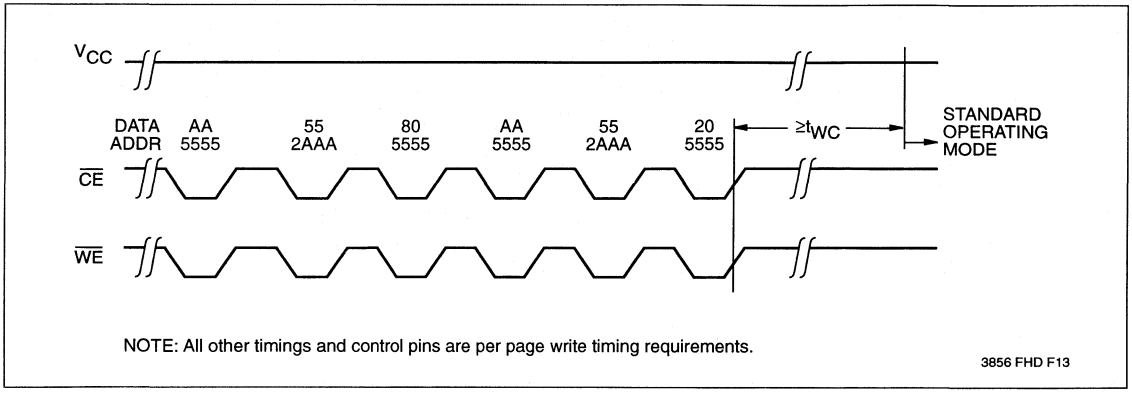
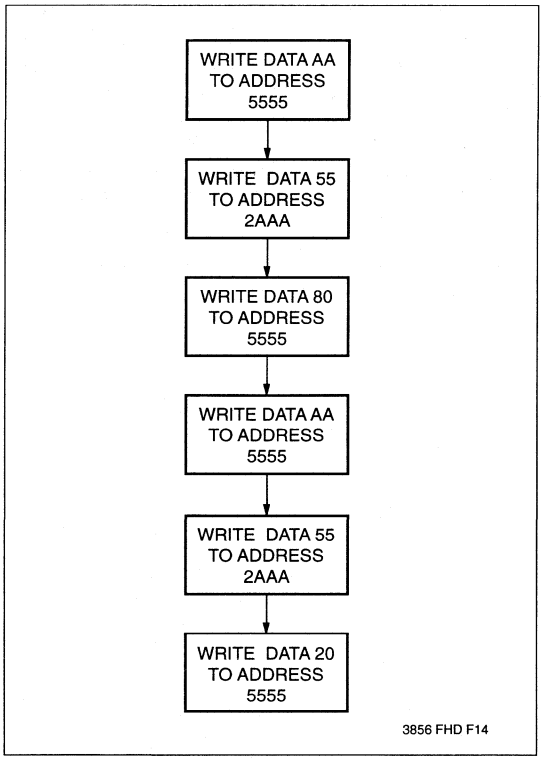


Figure 5b. Software Sequence to Deactivate Software Data Protection



In the event the user wants to deactivate the software data protection feature for testing or reprogramming in an E²PROM programmer, the following six step algorithm will reset the internal protection circuit. After t_{WC}, the X28C512/513 will be in standard operating mode.

Note: Once initiated, the sequence of write operations should not be interrupted.

SYSTEM CONSIDERATIONS

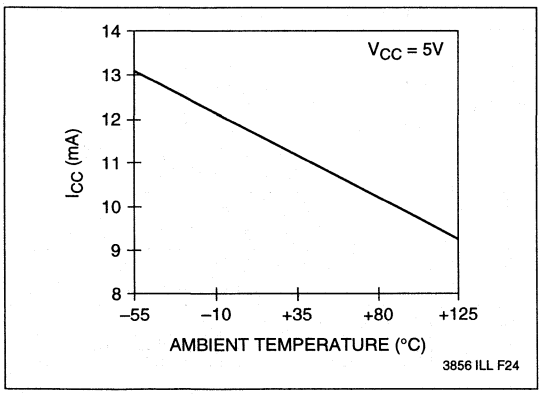
Because the X28C512/513 is frequently used in large memory arrays it is provided with a two line control architecture for both read and write operations. Proper usage can provide the lowest possible power dissipation and eliminate the possibility of contention where multiple I/O pins share the same bus.

To gain the most benefit it is recommended that $\overline{CE}$ be decoded from the address bus and be used as the primary device selection input. Both $\overline{OE}$ and $\overline{WE}$ would then be common among all devices in the array. For a read operation this assures that all deselected devices are in their standby mode and that only the selected device(s) is outputting data on the bus.

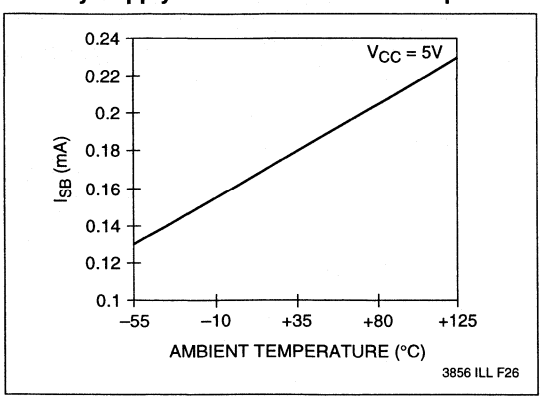
Because the X28C512/513 has two power modes, standby and active, proper decoupling of the memory array is of prime concern. Enabling $\overline{CE}$ will cause transient current spikes. The magnitude of these spikes is dependent on the output capacitive loading of the I/Os. Therefore, the larger the array sharing a common bus, the larger the transient spikes. The voltage peaks associated with the current transients can be suppressed by the proper selection and placement of decoupling capacitors. As a minimum, it is recommended that a 0.1μF high frequency ceramic capacitor be used between V_{CC} and V_{SS} at each device. Depending on the size of the array, the value of the capacitor may have to be larger.

In addition, it is recommended that a 4.7μF electrolytic bulk capacitor be placed between V_{CC} and V_{SS} for each eight devices employed in the array. This bulk capacitor is employed to overcome the voltage droop caused by the inductive effects of the PC board traces.

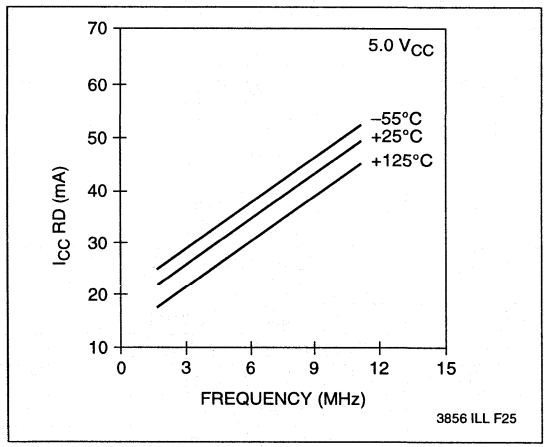
Active Supply Current vs. Ambient Temperature



Standby Supply Current vs. Ambient Temperature



I_{CC} (RD) by Temperature over Frequency



ABSOLUTE MAXIMUM RATINGS*

Temperature under Bias
- X28C512/513 ..... −10°C to +85°C
- X28C512I/513I ..... −65°C to +135°C
- X28C512M/513M ..... −65°C to +135°C

Storage Temperature ..... −65°C to +150°C
Voltage on any Pin with
- Respect to V_{SS} ..... −1V to +7V

D.C. Output Current 5mA
Lead Temperature
- (Soldering, 10 seconds) ..... 300°C

***COMMENT**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMEND OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	+70°C
Industrial	−40°C	+85°C
Military	−55°C	+125°C

3856 PGM T02

Supply Voltage	Limits
X28C512/513	5V ±10%

3856 PGM T03.1

D.C. OPERATING CHARACTERISTICS (Over recommended operating conditions, unless otherwise specified.)

		Limits			
Symbol	**Parameter**	**Min.**	**Max.**	**Units**	**Test Conditions**
I_{CC}	V_{CC} Current (Active) (TTL Inputs)		50	mA	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}, All I/O's = Open, Address Inputs = .4V/2.4V Levels @ f = 5MHz
I_{SB1}	V_{CC} Current (Standby) (TTL Inputs)		3	mA	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IL} All I/O's = Open, Other Inputs = V_{CC}
I_{SB2}	V_{CC} Current (Standby) (CMOS Inputs)		500	µA	$\overline{CE}$ = V_{CC} − 0.3V, $\overline{OE}$ = V_{IL} All I/O's = Open, Other Inputs = V_{CC}
I_{LI}	Input Leakage Current		10	µA	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output Leakage Current		10	µA	V_{OUT} = V_{SS} to V_{CC}, $\overline{CE}$ = V_{IH}
V_{IL}(1)	Input LOW Voltage	−1	0.8	V	
V_{IH}(1)	Input HIGH Voltage	2	V_{CC} + 1	V	
V_{OL}	Output LOW Voltage		0.4	V	I_{OL} = 2.1mA
V_{OH}	Output HIGH Voltage	2.4		V	I_{OH} = −400µA

3856 PGM T04.2

Notes: (1) V_{IL} min. and V_{IH} max. are for reference only and are not tested.

POWER-UP TIMING

Symbol	Parameter	Max.	Units
t_{PUR}(2)	Power-up to Read Operation	100	µs
t_{PUW}(2)	Power-up to Write Operation	5	ms

3856 PGM T05

CAPACITANCE T_A = +25°C, f = 1MHz, V_{CC} = 5V

Symbol	Parameter	Max.	Units	Test Conditions
$C_{I/O}$(2)	Input/Output Capacitance	10	pF	$V_{I/O}$ = 0V
C_{IN}(2)	Input Capacitance	10	pF	V_{IN} = 0V

3856 PGM T06.1

ENDURANCE AND DATA RETENTION

Parameter	Min.	Max.	Units
Endurance	10,000		Cycles Per Byte
Endurance	100,000		Cycles Per Page
Data Retention	100		Years

3856 PGM T07.1

A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3V
Input Rise and Fall Times	10ns
Input and Output Timing Levels	1.5V

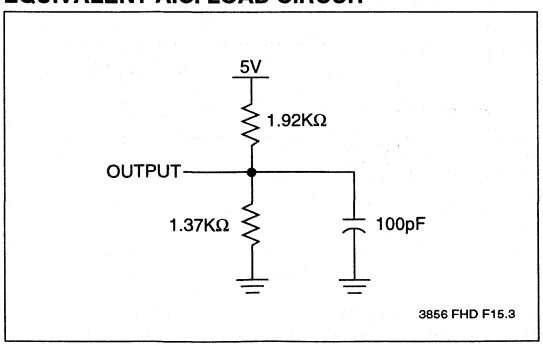
3856 PGM T07.1

MODE SELECTION

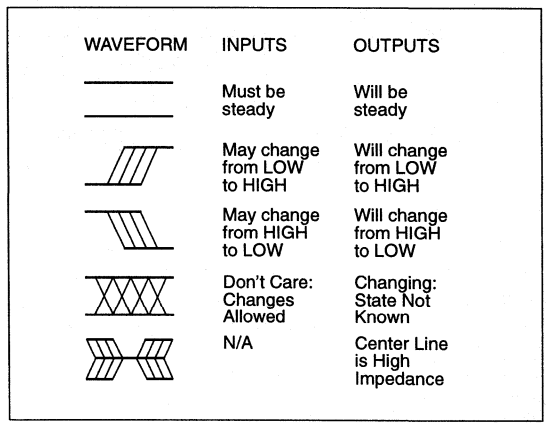
$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O	Power
L	L	H	Read	D_{OUT}	Active
L	H	L	Write	D_{IN}	Active
H	X	X	Standby and Write Inhibit	High Z	Standby
X	L	X	Write Inhibit	—	—
X	X	H	Write Inhibit	—	—

3856 PGM T08

EQUIVALENT A.C. LOAD CIRCUIT



SYMBOL TABLE



Note: (2) This parameter is periodically sampled and not 100% tested.

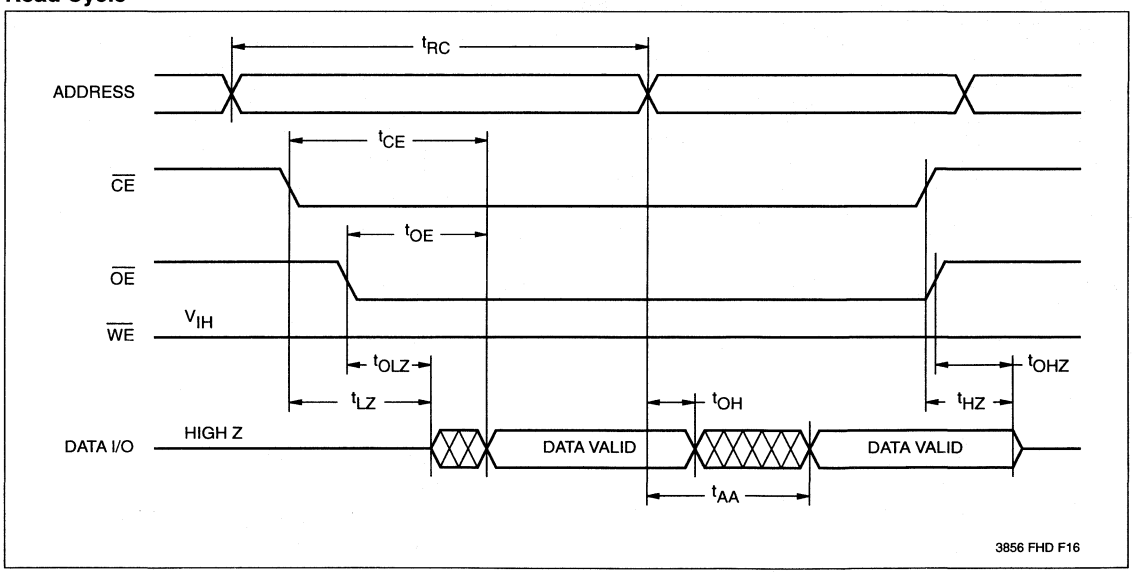
A.C. CHARACTERISTICS (Over the recommended operating conditions, unless otherwise specified.)

Read Cycle Limits

		X28C512-90 X28C513-90		X28C512-12 X28C513-12		X28C512-15 X28C513-15		X28C512-20 X28C513-20		X28C512-25 X28C513-25		
Symbol	**Parameter**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{RC}	Read Cycle Time	90		120		150		200		250		ns
t_{CE}	Chip Enable Access Time		90		120		150		200		250	ns
t_{AA}	Address Access Time		90		120		150		200		250	ns
t_{OE}	Output Enable Access Time		40		50		50		50		50	ns
t_{LZ}(3)	$\overline{CE}$ LOW to Active Output	0		0		0		0		0		ns
t_{OLZ}(3)	$\overline{OE}$ LOW to Active Output	0		0		0		0		0		ns
t_{HZ}(3)	$\overline{CE}$ HIGH to High Z Output		40		50		50		50		50	ns
t_{OHZ}(3)	$\overline{OE}$ HIGH to High Z Output		40		50		50		50		50	ns
t_{OH}	Output Hold from Address Change	0		0		0		0		0		ns

3856 PGM T09.4

Read Cycle



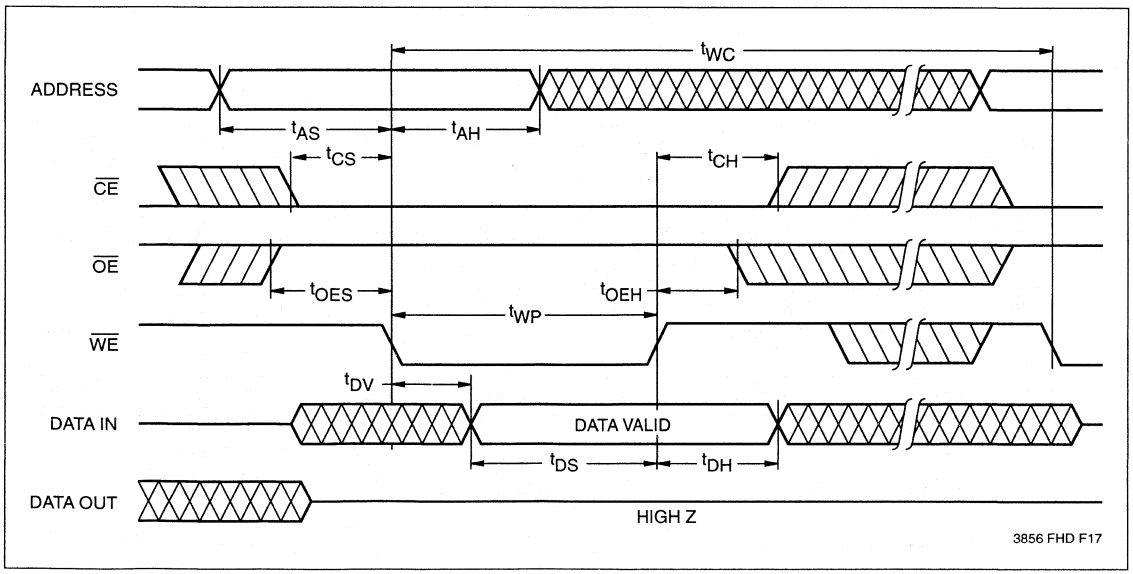
Notes: (3) t_{LZ} min., t_{HZ}, t_{OLZ} min., and tOHZ are periodically sampled and not 100% tested. t_{HZ} max. and t_{OHZ} max. are measured, with C_L = 5pF from the point when $\overline{CE}$ or $\overline{OE}$ return HIGH (whichever occurs first) to the time when the outputs are no longer driven.

WRITE CYCLE LIMITS

Symbol	Parameter	Min.	Max.	Units
t_{WC}(4)	Write Cycle Time		10	ms
t_{AS}	Address Setup Time	0		ns
t_{AH}	Address Hold Time	50		ns
t_{CS}	Write Setup Time	0		ns
t_{CH}	Write Hold Time	0		ns
t_{CW}	$\overline{CE}$ Pulse Width	100		ns
t_{OES}	$\overline{OE}$ HIGH Setup Time	10		ns
t_{OEH}	$\overline{OE}$ HIGH Hold Time	10		ns
t_{WP}	$\overline{WE}$ Pulse Width	100		ns
t_{WPH}	$\overline{WE}$ HIGH Recovery	100		ns
t_{DV}	Data Valid		1	µs
t_{DS}	Data Setup	50		ns
t_{DH}	Data Hold	10		ns
t_{DW}	Delay to Next Write	10		µs
t_{BLC}	Byte Load Cycle	0.2	100	µs

3856 PGM T10.2

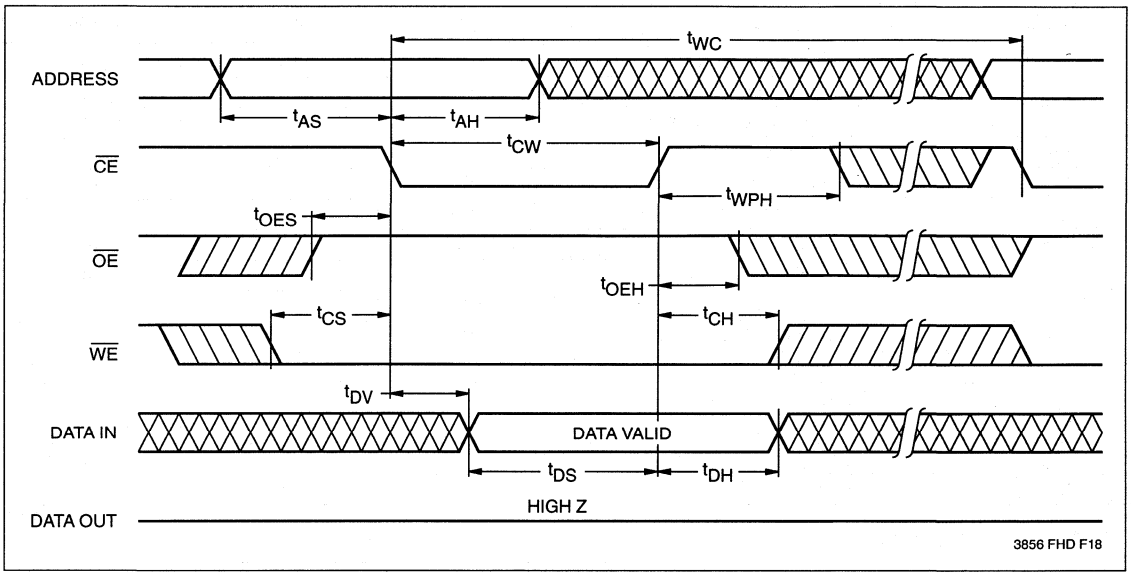
$\overline{WE}$ Controlled Write Cycle



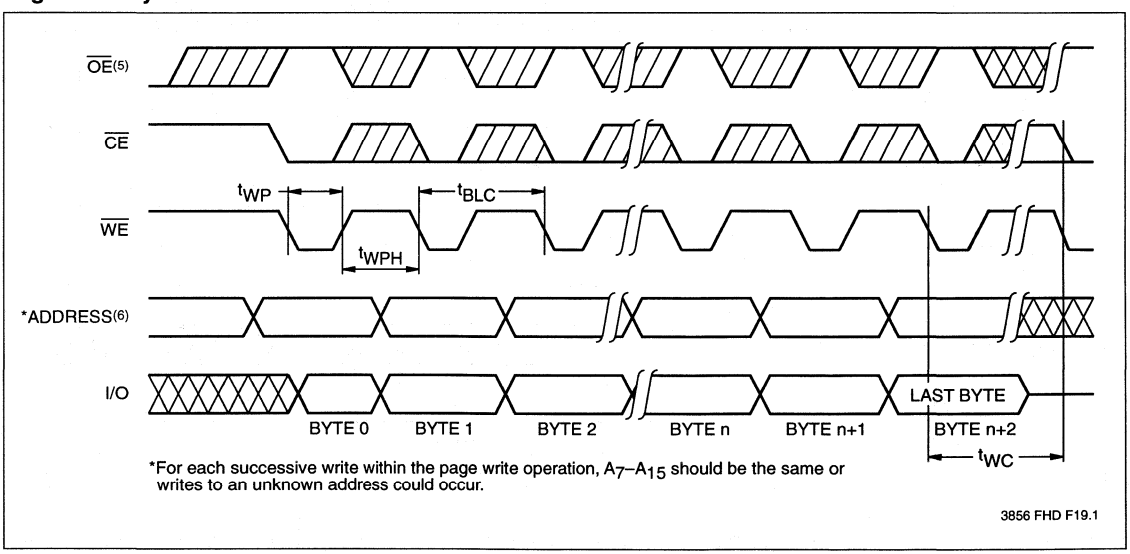
3856 FHD F17

Notes: (4) t_{WC} is the minimum cycle time to be allowed from the system perspective unless polling techniques are used. It is the maximum time the device requires to complete the internal write operation.

$\overline{CE}$ Controlled Write Cycle



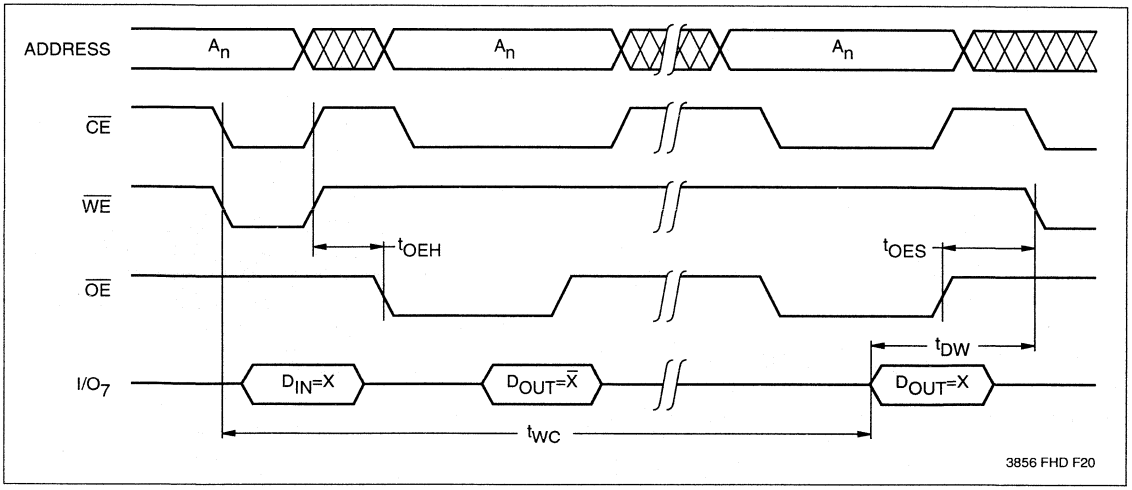
Page Write Cycle



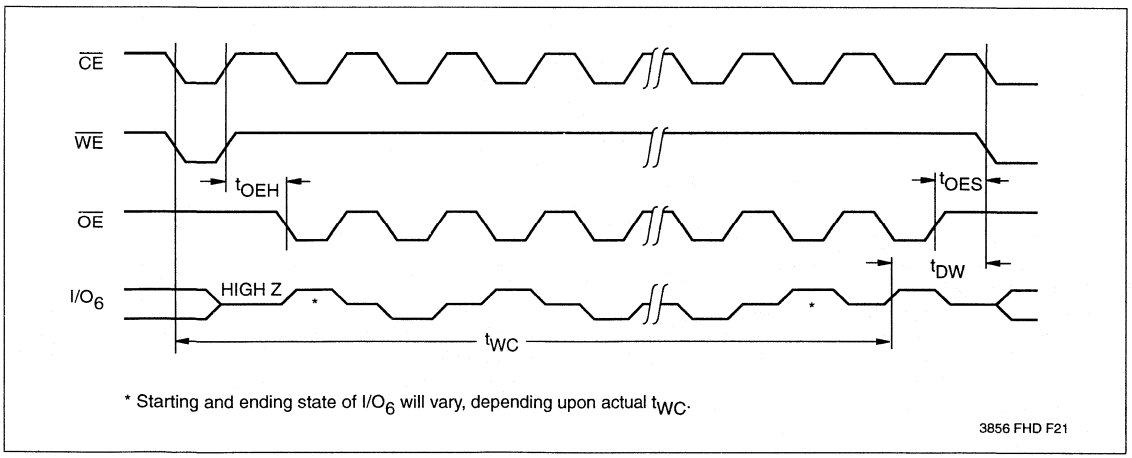
Notes: (5) Between successive byte writes within a page write operation, $\overline{OE}$ can be strobed LOW: e.g. this can be done with $\overline{CE}$ and $\overline{WE}$ HIGH to fetch data from another memory device within the system for the next write; or with $\overline{WE}$ HIGH and $\overline{CE}$ LOW effectively performing a polling operation.

(6) The timings shown above are unique to page write operations. Individual byte load operations within the page write must conform to either the $\overline{CE}$ or $\overline{WE}$ controlled write cycle timing.

$\overline{DATA}$ Polling Timing Diagram(7)

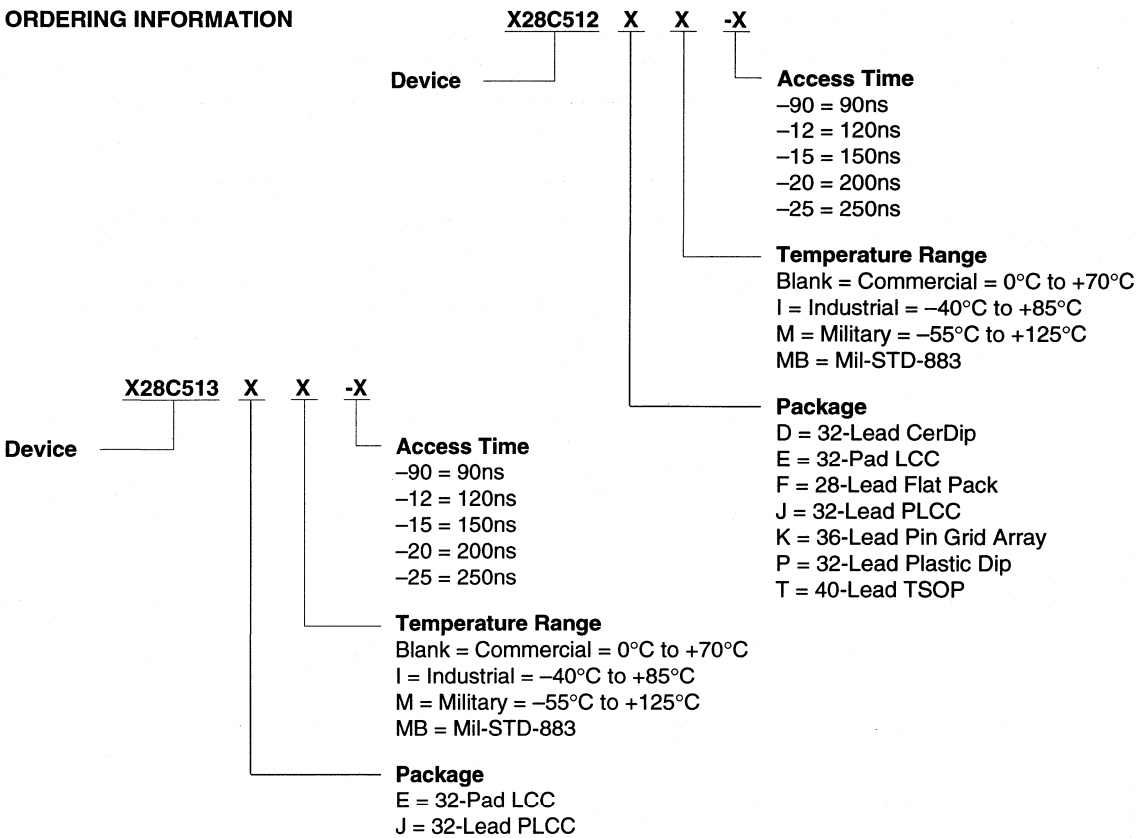


Toggle Bit Timing Diagram



Note: (7) Polling operations are by definition read cycles and are therefore subject to read cycle timings.

ORDERING INFORMATION



LIMITED WARRANTY

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US. PATENTS

Xicor products are covered by one or more of the following U.S. Patents: 4,263,664; 4,274,012; 4,300,212; 4,314,265; 4,326,134; 4,393,481; 4,404,475; 4,450,402; 4,486,769; 4,488,060; 4,520,461; 4,533,846; 4,599,706; 4,617,652; 4,668,932; 4,752,912; 4,829,482; 4,874,967; 4,883,976. Foreign patents and additional patents pending.

LIFE RELATED POLICY

In situations where semiconductor component failure may endanger life, system designers using this product should design the system with appropriate error detection and correction, redundancy and back-up features to prevent such an occurrence.

Xicor's products are not authorized for use as critical components in life support devices or systems.

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its satety or effectiveness.

High Temperature, 5 Volt, Byte Alterable E²PROM

FEATURES

- 170°C Full Functionality
- Simple Byte and Page Write
  - —Single 5V Supply
  - —Self-Timed
    - —No Erase Before Write
    - —No Complex Programming Algorithms
    - —No Overerase Problem
- Highly Reliable Direct Write™ Cell
  - —Endurance: 10,000 Write Cycles
  - —Data Retention: 100 Years
  - —Higher Temperature Functionality is Possible by Operating in the Byte Mode

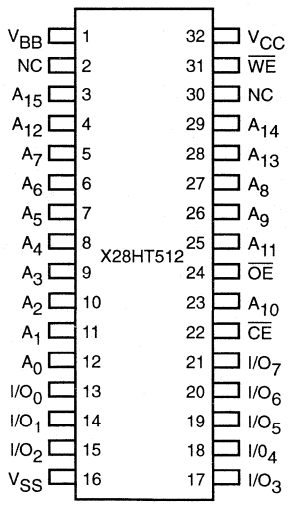
DESCRIPTION

The X28HT512 is an 64K x 8 CMOS E²PROM, fabricated with Xicor's proprietary, high performance, floating gate CMOS technology which provides Xicor products superior high temperature performance characteristics. Like all Xicor programmable nonvolatile memories the X28HT512 is a 5V only device. The X28HT512 features the JEDEC approved pinout for bytewide memories, compatible with industry standard EPROMS.

The X28HT512 supports a 128-byte page write operation, effectively providing a 39µs/byte write cycle and enabling the entire memory to be written in less than 2.5 seconds.

PIN CONFIGURATION

FLAT PACK
CERDIP



6614 FHD F02

PIN DESCRIPTIONS

Addresses (A_0–A_{15})

The Address inputs select an 8-bit memory location during a read or write operation.

Chip Enable ($\overline{CE}$)

The Chip Enable input must be LOW to enable all read/write operations. When $\overline{CE}$ is HIGH, power consumption is reduced.

Output Enable ($\overline{OE}$)

The Output Enable input controls the data output buffers and is used to initiate read operations.

Data In/Data Out (I/O_0–I/O_7)

Data is written to or read from the X28HT512 through the I/O pins.

Back Bias Voltage (V_{BB})

It is required to provide -3V on pin 1. This negative voltage improves higher temperature functionality.

Write Enable ($\overline{WE}$)

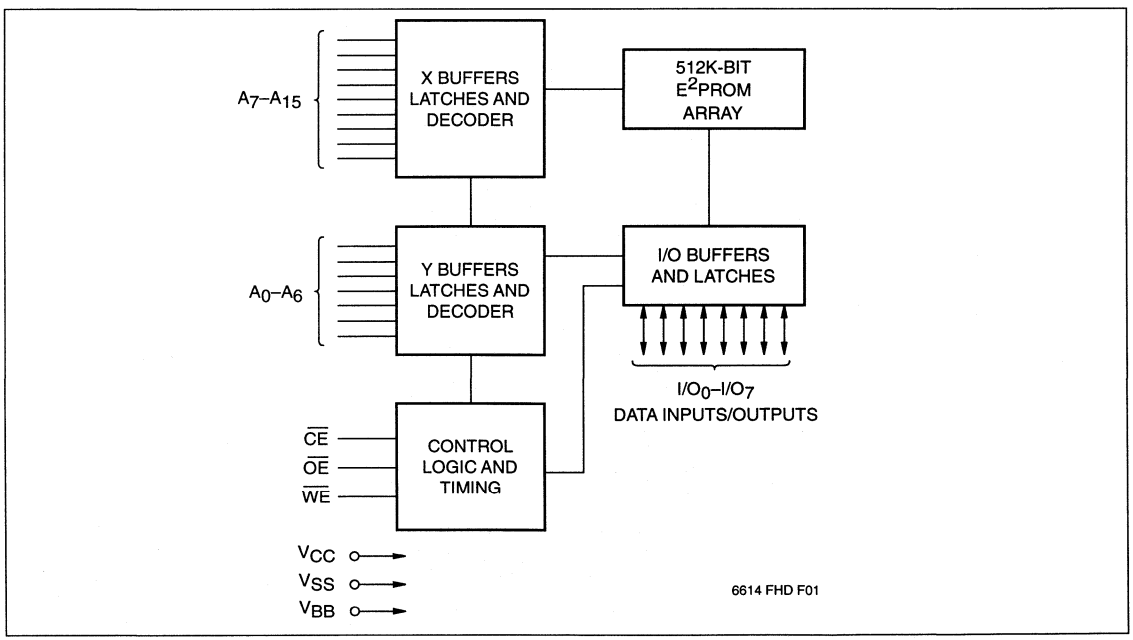
The Write Enable input controls the writing of data to the X28HT512.

PIN NAMES

Symbol	Description
A_0–A_{15}	Address Inputs
I/O_0–I/O_7	Data Input/Output
$\overline{WE}$	Write Enable
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
V_{BB}	–3V
V_{CC}	+5V
V_{SS}	Ground
NC	No Connect

6614 PGM T01

FUNCTIONAL DIAGRAM



DEVICE OPERATION

Read

Read operations are initiated by both $\overline{OE}$ and $\overline{CE}$ LOW. The read operation is terminated by either $\overline{CE}$ or $\overline{OE}$ returning HIGH. This two line control architecture eliminates bus contention in a system environment. The data bus will be in a high impedance state when either $\overline{OE}$ or $\overline{CE}$ is HIGH.

Write

Write operations are initiated when both $\overline{CE}$ and $\overline{WE}$ are LOW and $\overline{OE}$ is HIGH. The X28HT512 supports both a $\overline{CE}$ and $\overline{WE}$ controlled write cycle. That is, the address is latched by the falling edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs last. Similarly, the data is latched internally by the rising edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs first. A byte write operation, once initiated, will automatically continue to completion, typically within 5ms.

Page Write Operation

The page write feature of the X28HT512 allows the entire memory to be written in 2.5 seconds. Page write allows two to one hundred twenty-eight bytes of data to be consecutively written to the X28HT512 prior to the commencement of the internal programming cycle. The host can fetch data from another device within the system during a page write operation (change the source address), but the page address (A_7 through A_{15}) for each subsequent valid write cycle to the part during this operation must be the same as the initial page address.

The page write mode can be initiated during any write operation. Following the initial byte write cycle, the host can write an additional one to one hundred twenty-seven bytes in the same manner as the first byte was written. Each successive byte load cycle, started by the $\overline{WE}$ HIGH to LOW transition, must begin within 100µs of the falling edge of the preceding $\overline{WE}$. If a subsequent $\overline{WE}$ HIGH to LOW transition is not detected within 100µs, the internal automatic programming cycle will commence. There is no page write window limitation. Effectively the page write window is infinitely wide, so long as the host continues to access the device within the byte load cycle time of 100µs.

HARDWARE DATA PROTECTION

The X28HT512 provides three hardware features that protect nonvolatile data from inadvertent writes.

- Noise Protection—A $\overline{WE}$ pulse typically less than 10ns will not initiate a write cycle.
- Default V_{CC} Sense—All write functions are inhibited when V_{CC} is ≤3.4V.
- Write Inhibit—Holding either $\overline{OE}$ LOW, $\overline{WE}$ HIGH, or $\overline{CE}$ HIGH will prevent an inadvertent write cycle during power-up and power-down, maintaining data integrity. Write cycle timing specifications must be observed concurrently.

SYSTEM CONSIDERATIONS

Because the X28HT512 is frequently used in large memory arrays it is provided with a two line control architecture for both read and write operations. Proper usage can provide the lowest possible power dissipation and eliminate the possibility of contention where multiple I/O pins share the same bus.

It has been demonstrated that markedly higher temperature performance can be obtained from this device if $\overline{CE}$ is left enabled throughout the read and write operation.

To gain the most benefit it is recommended that $\overline{CE}$ be decoded from the address bus and be used as the primary device selection input. Both $\overline{OE}$ and $\overline{WE}$ would then be common among all devices in the array. For a read operation this assures that all deselected devices are in their standby mode and that only the selected device(s) is outputting data on the bus.

Because the X28HT512 has two power modes, standby and active, proper decoupling of the memory array is of prime concern. Enabling $\overline{CE}$ will cause transient current spikes. The magnitude of these spikes is dependent on the output capacitive loading of the I/Os. Therefore, the larger the array sharing a common bus, the larger the transient spikes. The voltage peaks associated with the current transients can be suppressed by the proper selection and placement of decoupling capacitors. As a minimum, it is recommended that a 0.1µF high frequency ceramic capacitor be used between V_{CC} and V_{SS} at each device. Depending on the size of the array, the value of the capacitor may have to be larger.

In addition, it is recommended that a 4.7µF electrolytic bulk capacitor be placed between V_{CC} and V_{SS} for each eight devices employed in the array. This bulk capacitor is employed to overcome the voltage droop caused by the inductive effects of the PC board traces.

ABSOLUTE MAXIMUM RATINGS*

Temperature under Bias
X28HT512 ..... –40°C to +170°C
Voltage on any Pin with
Respect to V_{SS} ..... –1V to +7V
D.C. Output Current 5mA
Lead Temperature
(Soldering, 10 seconds) ..... 300°C

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMEND OPERATING CONDITIONS

Temperature	Min.	Max.
High Temp	–40°C	+170°C

6614 PGM T02.1

Supply Voltage	Limits
X28HT512	5V ±5%
Back Bias Voltage (V_{BB})	3V ±10%

6614 PGM T03.1

D.C. OPERATING CHARACTERISTICS (Over recommended operating conditions, unless otherwise specified.)

		Limits			
Symbol	**Parameter**	**Min.**	**Max.**	**Units**	**Test Conditions**
I_{CC}	V_{CC} Current (Active) (TTL Inputs)		50	mA	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}, All I/O's = Open, Address Inputs = .4V/2.4V Levels @ f = 5MHz
I_{SB1}	V_{CC} Current (Standby) (TTL Inputs)		3	mA	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IL} All I/O's = Open, Other Inputs = V_{CC}
I_{LI}	Input Leakage Current		20	µA	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output Leakage Current		20	µA	V_{OUT} = V_{SS} to V_{CC}, $\overline{CE}$ = V_{IH}
V_{IL}(1)	Input LOW Voltage	–1	0.6	V	
V_{IH}(1)	Input HIGH Voltage	2.2	V_{CC} + 1	V	
V_{OL}	Output LOW Voltage		0.5	V	I_{OL} = 1mA
V_{OH}	Output HIGH Voltage	2.6		V	I_{OH} = –400µA
V_{BB}	Back Bias Voltage		200	µA	

6614 PGM T04.2

Notes: (1) V_{IL} min. and V_{IH} max. are for reference only and are not tested.

POWER-UP TIMING

Symbol	Parameter	Max.	Units
t_{PUR}(2)	Power-up to Read Operation	100	µs
t_{PUW}(2)	Power-up to Write Operation	5	ms

6614 PGM T05

CAPACITANCE T_A = +25°C, f = 1MHz, V_{CC} = 5V

Symbol	Parameter	Max.	Units	Test Conditions
$C_{I/O}$(2)	Input/Output Capacitance	10	pF	$V_{I/O}$ = 0V
C_{IN}(2)	Input Capacitance	10	pF	V_{IN} = 0V

6614 PGM T06

ENDURANCE AND DATA RETENTION

Parameter	Min.	Max.	Units
Endurance	10,000		Cycles per Byte
Data Retention	100		Years

6614 PGM T11

A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3V
Input Rise and Fall Times	10ns
Input and Output Timing Levels	1.5V

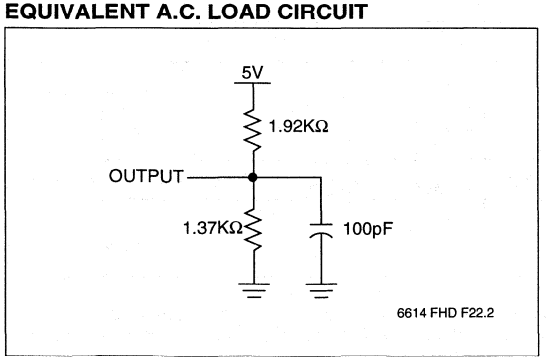
6614 PGM T07

MODE SELECTION

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O	Power
L	L	H	Read	D_{OUT}	Active
L	H	L	Write	D_{IN}	Active
H	X	X	Standby and Write Inhibit	High Z	Standby
X	L	X	Write Inhibit	—	—
X	X	H	Write Inhibit	—	—

6614 PGM T08

EQUIVALENT A.C. LOAD CIRCUIT



SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

Note: (2) This parameter is periodically sampled and not 100% tested.

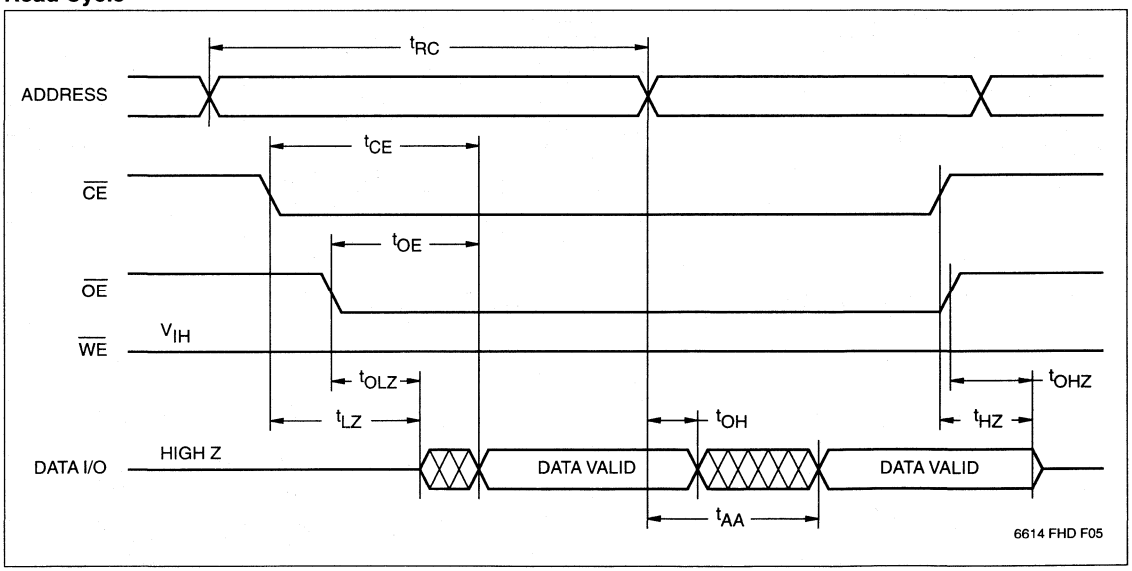
A.C. CHARACTERISTICS (Over the recommended operating conditions, unless otherwise specified.)

Read Cycle Limits

Symbol	Parameter	X28HT512-20		X28HT512-25		Units
		Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	200		250		ns
t_{CE}	Chip Enable Access Time		200		250	ns
t_{AA}	Address Access Time		200		250	ns
t_{OE}	Output Enable Access Time		80		80	ns
t_{LZ}(3)	$\overline{CE}$ LOW to Active Output	0		0		ns
t_{OLZ}(3)	$\overline{OE}$ LOW to Active Output	0		0		ns
t_{HZ}(3)	$\overline{CE}$ HIGH to High Z Output		80		80	ns
t_{OHZ}(3)	$\overline{OE}$ HIGH to High Z Output		80		80	ns
t_{OH}	Output Hold from Address Change	0		0		ns

6614 PGM T09.1

Read Cycle



Notes: (3) t_{LZ} min., t_{HZ}, t_{OLZ} min., and tOHZ are periodically sampled and not 100% tested. t_{HZ} max. and t_{OHZ} max. are measured, with C_L = 5pF from the point when $\overline{CE}$ or $\overline{OE}$ return HIGH (whichever occurs first) to the time when the outputs are no longer driven.

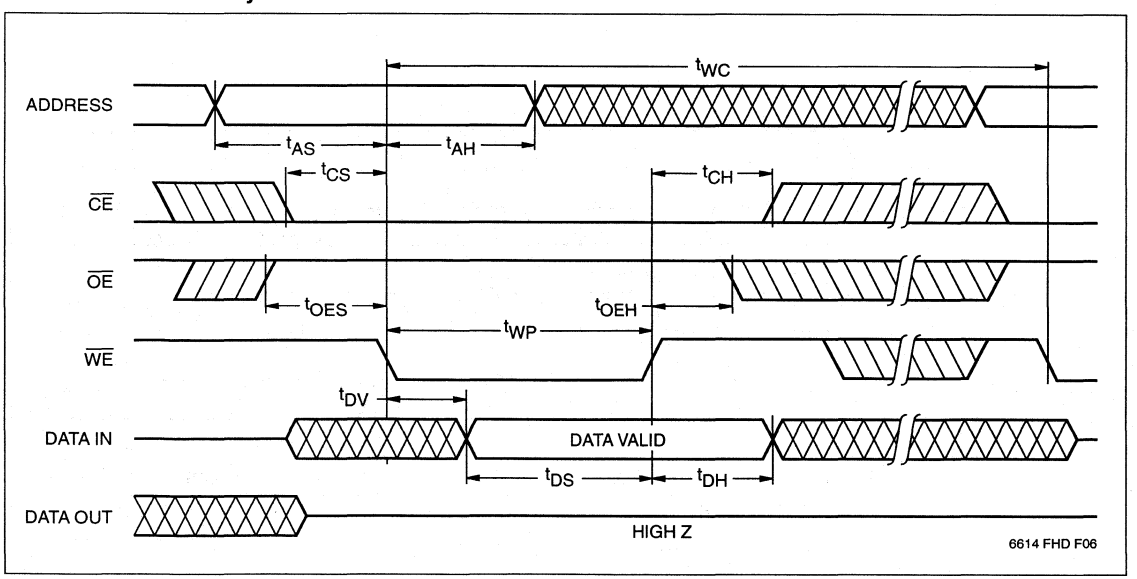
WRITE CYCLE LIMITS

Symbol	Parameter	Min.	Max.	Units
t_{WC}(4)	Write Cycle Time		10	ms
t_{AS}	Address Setup Time	20		ns
t_{AH}	Address Hold Time	100		ns
t_{CS}	Write Setup Time	0		ns
t_{CH}	Write Hold Time	0		ns
t_{CW}	$\overline{CE}$ Pulse Width	200		ns
t_{OES}	$\overline{OE}$ HIGH Setup Time	10		ns
t_{OEH}	$\overline{OE}$ HIGH Hold Time	10		ns
t_{WP}	$\overline{WE}$ Pulse Width	200		ns
t_{WPH}	$\overline{WE}$ HIGH Recovery	200		ns
t_{DV}	Data Valid		1	µs
t_{DS}	Data Setup	100		ns
t_{DH}	Data Hold	25		ns
t_{DW}	Delay to Next Write	10		µs
t_{BLC}	Byte Load Cycle	0.4	100	µs

6614 PGM T10.1

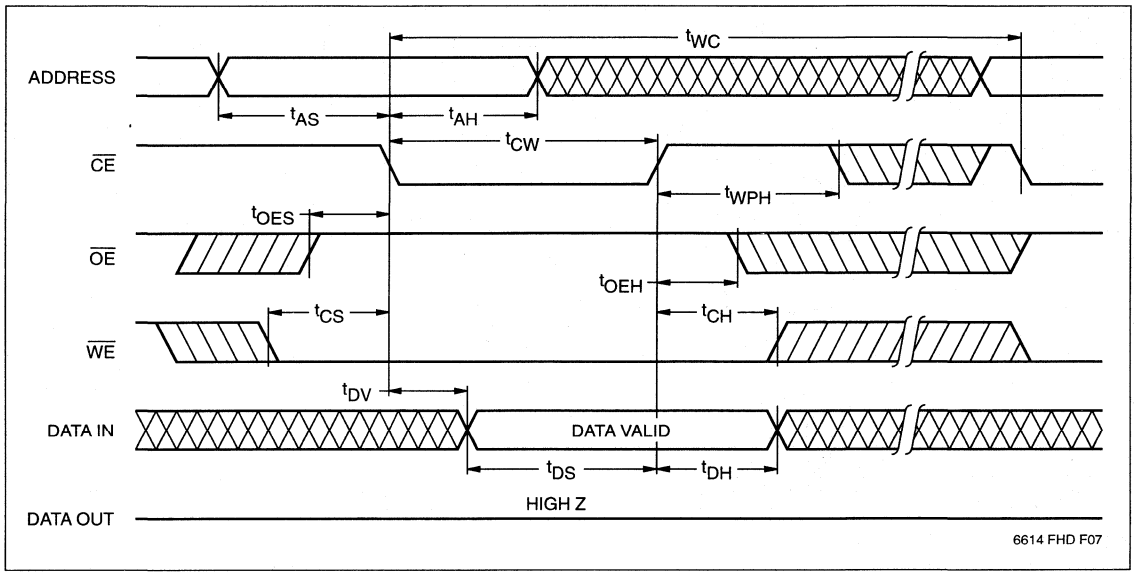
3

$\overline{WE}$ Controlled Write Cycle

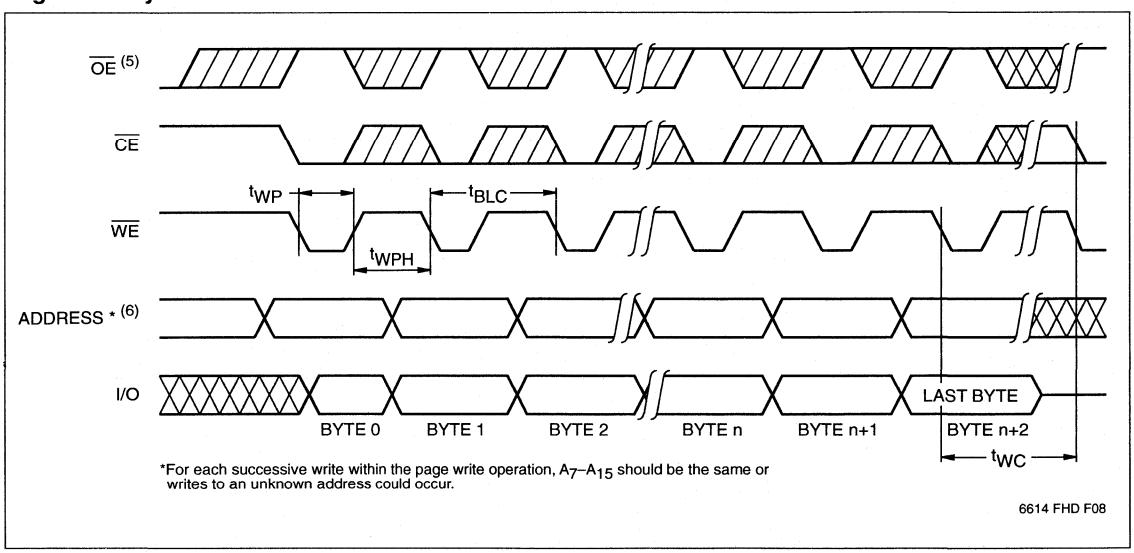


Notes: (4) t_{WC} is the minimum cycle time to be allowed from the system perspective unless polling techniques are used. It is the maximum time the device requires to complete the internal write operation.

$\overline{CE}$ Controlled Write Cycle



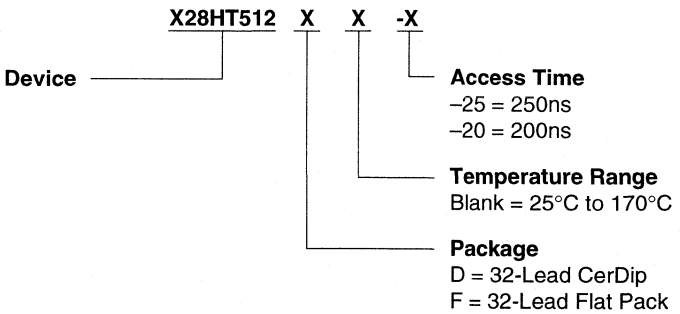
Page Write Cycle



Notes: (5) Between successive byte writes within a page write operation, $\overline{OE}$ can be strobed LOW: e.g. this can be done with $\overline{CE}$ and $\overline{WE}$ HIGH to fetch data from another memory device within the system for the next write; or with $\overline{WE}$ HIGH and $\overline{CE}$ LOW effectively performing a polling operation.

(6) The timings shown above are unique to page write operations. Individual byte load operations within the page write must conform to either the $\overline{CE}$ or $\overline{WE}$ controlled write cycle timing.

ORDERING INFORMATION



3

LIMITED WARRANTY

Devices sold by Xicor, Inc. are covered by the warranty and patent indemnification provisions appearing in its Terms of Sale only. Xicor, Inc. makes no warranty, express, statutory, implied, or by description regarding the information set forth herein or regarding the freedom of the described devices from patent infringement. Xicor, Inc. makes no warranty of merchantability or fitness tor any purpose. Xicor, Inc. reserves the right to discontinue production and change specifications and prices at any time and without notice.

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US. PATENTS

Xicor products are covered by one or more of the following U.S. Patents: 4,263,664; 4,274,012; 4,300,212; 4,314,265; 4,326,134; 4,393,481; 4,404,475; 4,450,402; 4,486,769; 4,488,060; 4,520,461; 4,533,846; 4,599,706; 4,617,652; 4,668,932; 4,752,912; 4,829,482; 4,874,967; 4,883,976. Foreign patents and additional patents pending.

LIFE RELATED POLICY

In situations where semiconductor component failure may endanger life, system designers using this product should design the system with appropriate error detection and correction, redundancy and back-up features to prevent such an occurrence.

Xicor's products are not authorized for use as critical components in life support devices or systems.

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its satety or effectiveness.

NOTES

3.3 Volt, Byte Alterable E²PROM

FEATURES

- Low V_{CC} Operation: V_{CC} = 3.3V ±10%
- Access Time: 150ns
- Simple Byte and Page Write
  - —Self-Timed
    - —No Erase Before Write
    - —No Complex Programming Algorithms
    - —No Overerase Problem
- Low Power CMOS:
  - —Active: 25mA
  - —Standby: 150µA
- Software Data Protection
  - —Protects Data Against System Level Inadvertant Writes
- High Speed Page Write Capability
- Highly Reliable Direct Write™ Cell
  - —Endurance: 10,000 Write Cycles
  - —Data Retention: 100 Years
- Early End of Write Detection
  - —$\overline{\text{DATA}}$ Polling
  - —Toggle Bit Polling
- Two PLCC and LCC Pinouts
  - —X28LC512
    - —X28LC010 E²PROM Pin Compatible
  - —X28LC513
    - —Compatible with Lower Density E²PROMs

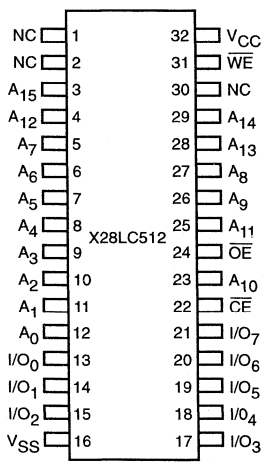
DESCRIPTION

The X28LC512/513 is a low-power 64K x 8 E²PROM, fabricated with Xicor's proprietary, high performance, floating gate CMOS technology. The X28LC512/513 features the JEDEC approved pinout for bytewide memories, compatible with industry standard EPROMS.

The X28LC512/513 supports a 128-byte page write operation, effectively providing a 39µs/byte write cycle and enabling the entire memory to be written in less than 2.5 seconds. The X28LC512/513 also features $\overline{\text{DATA}}$ Polling and Toggle Bit Polling, system software support schemes used to indicate the early completion of a write cycle. In addition, the X28LC512/513 supports the Software Data Protection option.

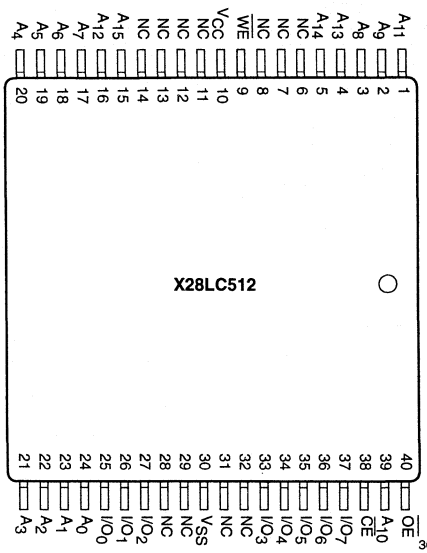
PIN CONFIGURATION

PLASTIC DIP
CERDIP



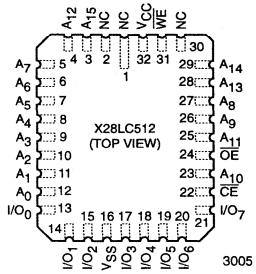
3005 ILL F02

TSOP



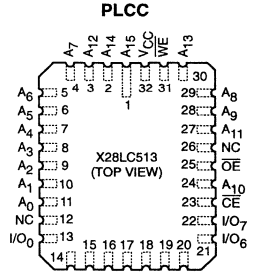
3005 ILL F22.1

PLCC



3005 ILL F03

PLCC



3005 ILL F04.1

PIN DESCRIPTIONS

Addresses (A_0–A_{15})

The Address inputs select an 8-bit memory location during a read or write operation.

Chip Enable ($\overline{CE}$)

The Chip Enable input must be LOW to enable all read/write operations. When $\overline{CE}$ is HIGH, power consumption is reduced.

Output Enable ($\overline{OE}$)

The Output Enable input controls the data output buffers and is used to initiate read operations.

Data In/Data Out (I/O_0–I/O_7)

Data is written to or read from the X28LC512/513 through the I/O pins.

Write Enable ($\overline{WE}$)

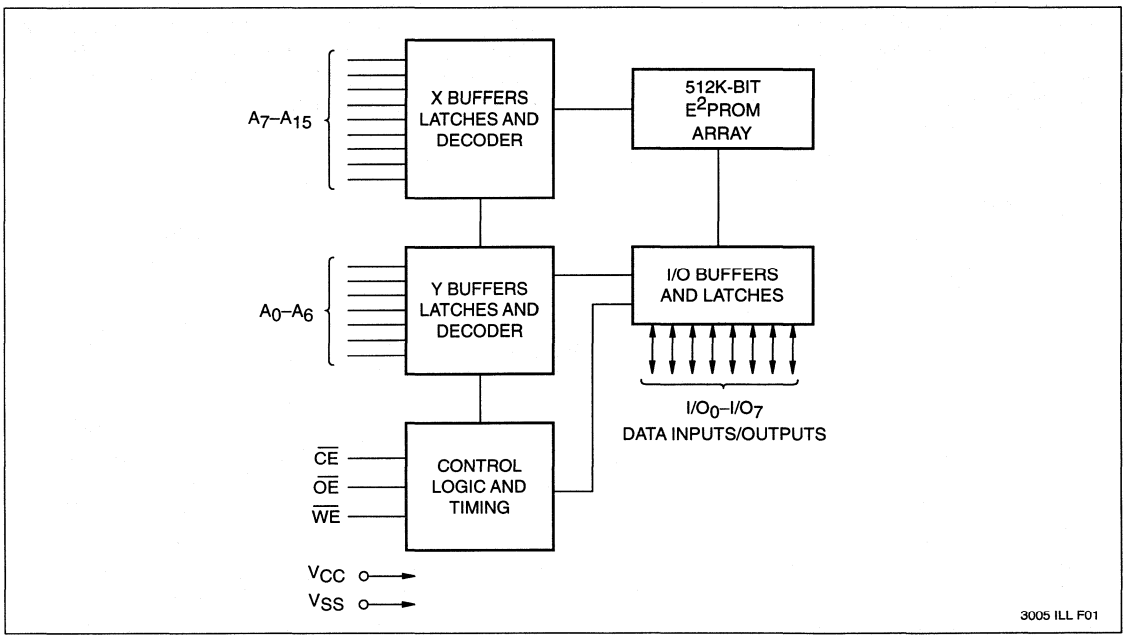
The Write Enable input controls the writing of data to the X28LC512/513.

PIN NAMES

Symbol	Description
A_0–A_{15}	Address Inputs
I/O_0–I/O_7	Data Input/Output
$\overline{WE}$	Write Enable
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
V_{CC}	3.3V ± 10%
V_{SS}	Ground
NC	No Connect

3005 PGM T01

FUNCTIONAL DIAGRAM



3005 ILL F01

DEVICE OPERATION

Read

Read operations are initiated by both $\overline{OE}$ and $\overline{CE}$ LOW. The read operation is terminated by either $\overline{CE}$ or $\overline{OE}$ returning HIGH. This two line control architecture eliminates bus contention in a system environment. The data bus will be in a high impedance state when either $\overline{OE}$ or $\overline{CE}$ is HIGH.

Write

Write operations are initiated when both $\overline{CE}$ and $\overline{WE}$ are LOW and $\overline{OE}$ is HIGH. The X28LC512/513 supports both a $\overline{CE}$ and $\overline{WE}$ controlled write cycle. That is, the address is latched by the falling edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs last. Similarly, the data is latched internally by the rising edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs first. A byte write operation, once initiated, will automatically continue to completion, typically within 5ms.

Page Write Operation

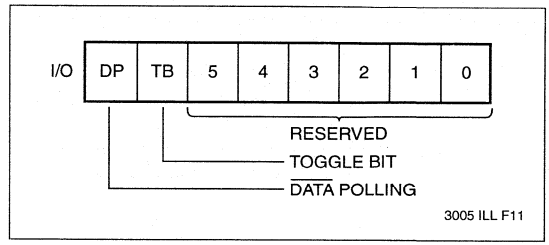
The page write feature of the X28LC512/513 allows the entire memory to be written in 2.5 seconds. Page write allows two to one hundred twenty-eight bytes of data to be consecutively written to the X28LC512/513 prior to the commencement of the internal programming cycle. The host can fetch data from another device within the system during a page write operation (change the source address), but the page address (A_7 through A_{15}) for each subsequent valid write cycle to the part during this operation must be the same as the initial page address.

The page write mode can be initiated during any write operation. Following the initial byte write cycle, the host can write an additional one to one hundred twenty-seven bytes in the same manner as the first byte was written. Each successive byte load cycle, started by the $\overline{WE}$ HIGH to LOW transition, must begin within 100µs of the falling edge of the preceding $\overline{WE}$. If a subsequent $\overline{WE}$ HIGH to LOW transition is not detected within 100µs, the internal automatic programming cycle will commence. There is no page write window limitation. Effectively the page write window is infinitely wide, so long as the host continues to access the device within the byte load cycle time of 100µs.

Write Operation Status Bits

The X28LC512/513 provides the user two write operation status bits. These can be used to optimize a system write cycle time. The status bits are mapped onto the I/O bus as shown in Figure 1.

Figure 1. Status Bit Assignment



$\overline{DATA}$ Polling (I/O_7)

The X28LC512/513 features $\overline{DATA}$ Polling as a method to indicate to the host system that the byte write or page write cycle has completed. $\overline{DATA}$ Polling allows a simple bit test operation to determine the status of the X28LC512/513, eliminating additional interrupt inputs or external hardware. During the internal programming cycle, any attempt to read the last byte written will produce the complement of that data on I/O_7 (i.e. write data = 0xxx xxxx, read data = 1xxx xxxx). Once the programming cycle is complete, I/O_7 will reflect true data.

Toggle Bit (I/O_6)

The X28LC512/513 also provides another method for determining when the internal write cycle is complete. During the internal programming cycle, I/O_6 will toggle from HIGH to LOW and LOW to HIGH on subsequent attempts to read the device. When the internal cycle is complete the toggling will cease and the device will be accessible for additional read or write operations.

$\overline{DATA}$ Polling I/O_7

Figure 2a. $\overline{DATA}$ Polling Bus Sequence

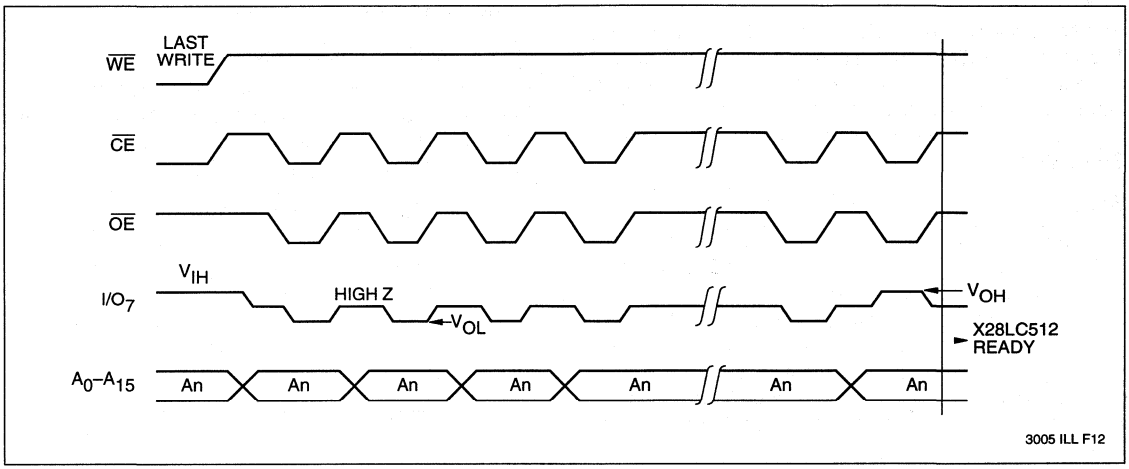
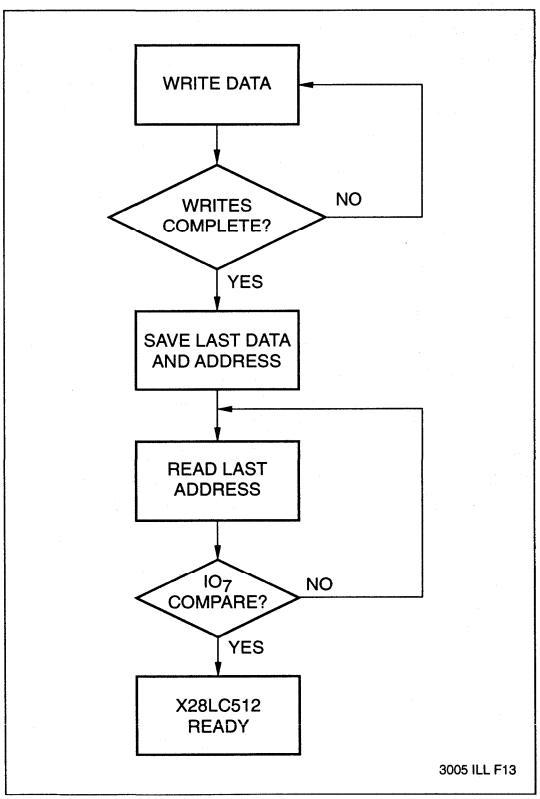


Figure 2b. $\overline{DATA}$ Polling Software Flow



$\overline{DATA}$ Polling can effectively halve the time for writing to the X28LC512/513. The timing diagram in Figure 2a illustrates the sequence of events on the bus. The software flow diagram in Figure 2b illustrates one method of implementing the routine.

The Toggle Bit I/O_6

Figure 3a. Toggle Bit Bus Sequence

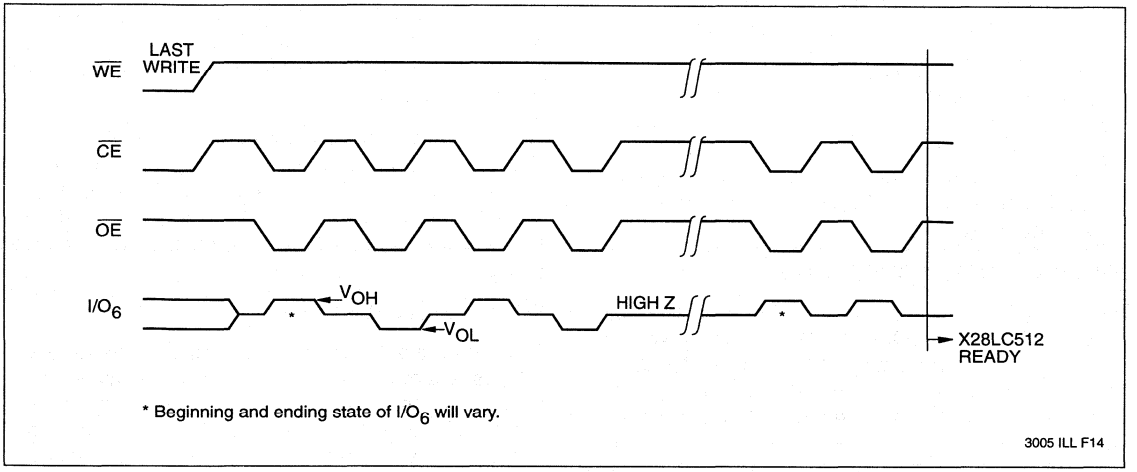
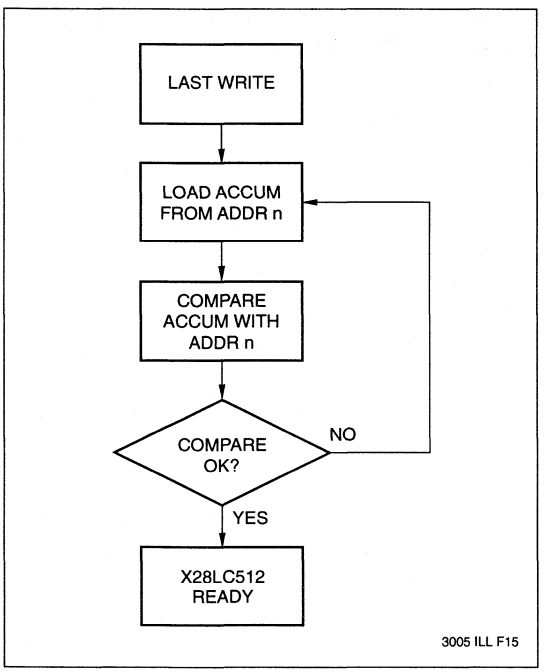


Figure 3b. Toggle Bit Software Flow



The Toggle Bit can eliminate the software housekeeping chore of saving and fetching the last address and data written to a device in order to implement $\overline{DATA}$ Polling. This can be especially helpful in an array comprised of multiple X28LC512/513 memories that is frequently updated. Toggle Bit Polling can also provide a method for status checking in multiprocessor applications. The timing diagram in Figure 3a illustrates the sequence of events on the bus. The software flow diagram in Figure 3b illustrates a method for polling the Toggle Bit.

HARDWARE DATA PROTECTION

The X28LC512/513 provides three hardware features that protect nonvolatile data from inadvertent writes.

- Noise Protection—A $\overline{WE}$ pulse typically less than 10ns will not initiate a write cycle.
- Write Inhibit—Holding either $\overline{OE}$ LOW, $\overline{WE}$ HIGH, or $\overline{CE}$ HIGH will prevent an inadvertent write cycle during power-up and power-down, maintaining data integrity. Write cycle timing specifications must be observed concurrently.

SOFTWARE DATA PROTECTION

The X28LC512/513 offers a software controlled data protection feature. The X28LC512/513 is shipped from Xicor with the software data protection NOT ENABLED; that is, the device will be in the standard operating mode. In this mode data should be protected during power-up/-down operations through the use of external circuits. The host would then have open read and write access of the device once V_{CC} was stable.

The X28LC512/513 can be automatically protected during power-up and power-down without the need for external circuits by employing the software data protection feature. The internal software data protection circuit is enabled after the first write operation utilizing the software algorithm. This circuit is nonvolatile and will remain set for the life of the device unless the reset command is issued.

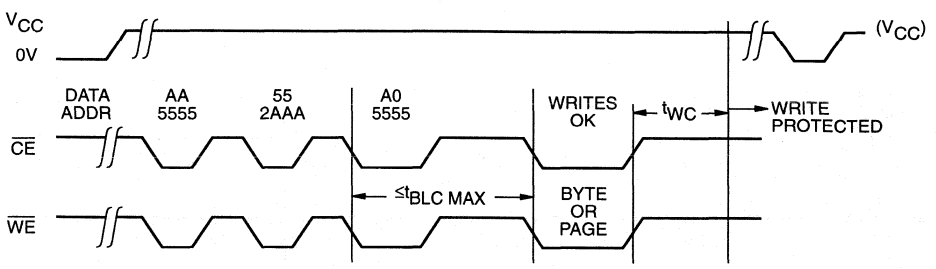
Once the software protection is enabled, the X28LC512/513 is also protected from inadvertent and accidental writes in the powered-up state. That is, the software algorithm must be issued prior to writing additional data to the device. Note: The data in the three-byte enable sequence is not written to the memory array.

SOFTWARE ALGORITHM

Selecting the software data protection mode requires the host system to precede data write operations by a series of three write operations to three specific addresses. Refer to Figure 4a and 4b for the sequence. The three byte sequence opens the page write window enabling the host to write from one to one hundred twenty-eight bytes of data. Once the page load cycle has been completed, the device will automatically be returned to the data protected state.

Software Data Protection

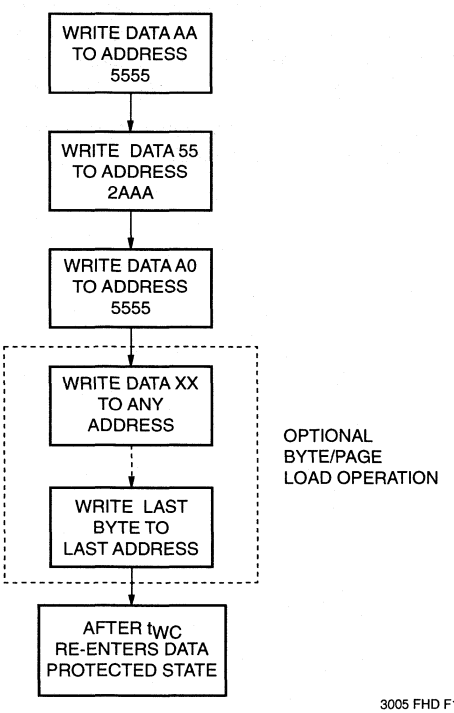
Figure 4a. Timing Sequence—Software Data Protect Enable Sequence followed by Byte or Page Write



NOTE: All other timings and control pins are per page write timing requirements.

3005 ILL F16

Figure 4b. Write Sequence for Software Data Protection



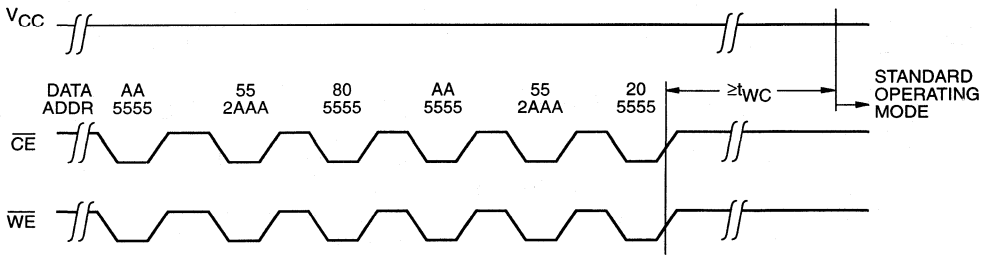
3005 FHD F17

Regardless of whether the device has previously been protected or not, once the software data protected algorithm is used and data has been written, the X28LC512/513 will automatically disable further writes unless another command is issued to cancel it. If no further commands are issued the X28LC512/513 will be write protected during power-down and after any subsequent power-up. The state of A_{15} while executing the algorithm is don't care.

Note: Once initiated, the sequence of write operations should not be interrupted.

Resetting Software Data Protection

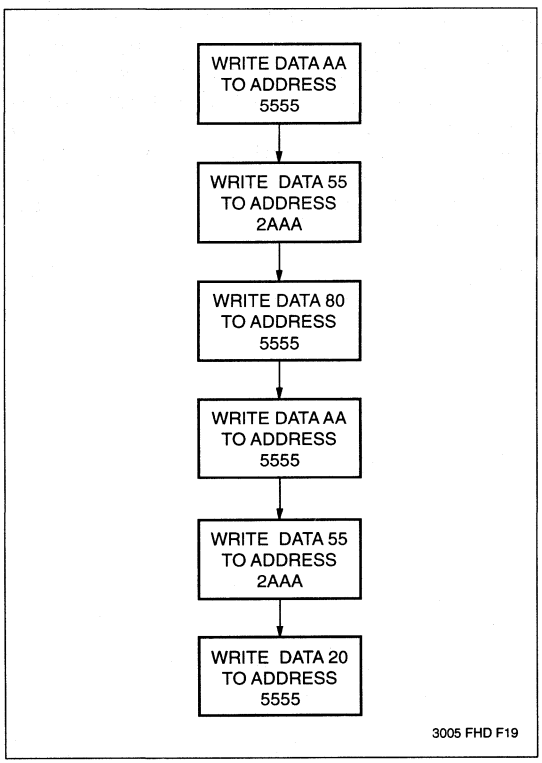
Figure 5a. Reset Software Data Protection Timing Sequence



NOTE: All other timings and control pins are per page write timing requirements.

3005 ILL F18

Figure 5b. Software Sequence to Deactivate Software Data Protection



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In the event the user wants to deactivate the software data protection feature for testing or reprogramming in an E²PROM programmer, the following six step algorithm will reset the internal protection circuit. After t_{WC}, the X28LC512/513 will be in standard operating mode.

Note: Once initiated, the sequence of write operations should not be interrupted.

SYSTEM CONSIDERATIONS

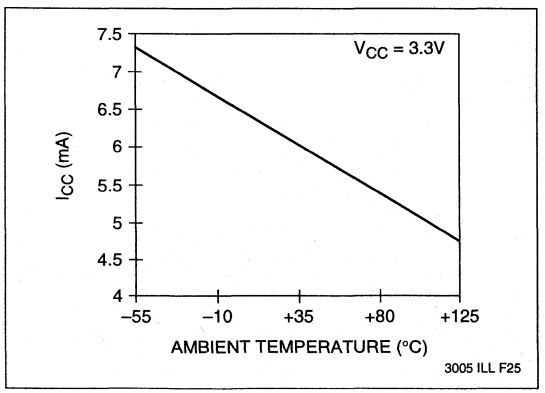
Because the X28LC512/513 is frequently used in large memory arrays it is provided with a two line control architecture for both read and write operations. Proper usage can provide the lowest possible power dissipation and eliminate the possibility of contention where multiple I/O pins share the same bus.

To gain the most benefit it is recommended that $\overline{CE}$ be decoded from the address bus and be used as the primary device selection input. Both $\overline{OE}$ and $\overline{WE}$ would then be common among all devices in the array. For a read operation this assures that all deselected devices are in their standby mode and that only the selected device(s) is outputting data on the bus.

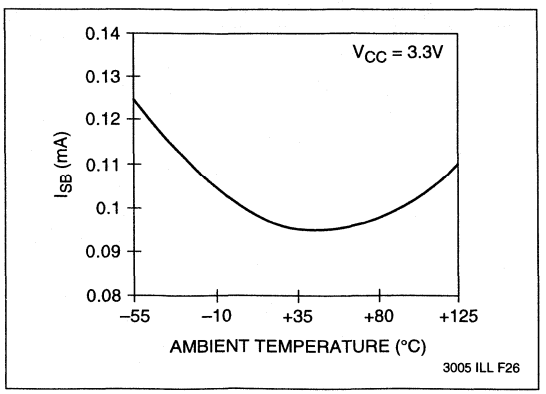
Because the X28LC512/513 has two power modes, standby and active, proper decoupling of the memory array is of prime concern. Enabling $\overline{CE}$ will cause transient current spikes. The magnitude of these spikes is dependent on the output capacitive loading of the I/Os. Therefore, the larger the array sharing a common bus, the larger the transient spikes. The voltage peaks associated with the current transients can be suppressed by the proper selection and placement of decoupling capacitors. As a minimum, it is recommended that a 0.1µF high frequency ceramic capacitor be used between V_{CC} and V_{SS} at each device. Depending on the size of the array, the value of the capacitor may have to be larger.

In addition, it is recommended that a 4.7µF electrolytic bulk capacitor be placed between V_{CC} and V_{SS} for each eight devices employed in the array. This bulk capacitor is employed to overcome the voltage droop caused by the inductive effects of the PC board traces.

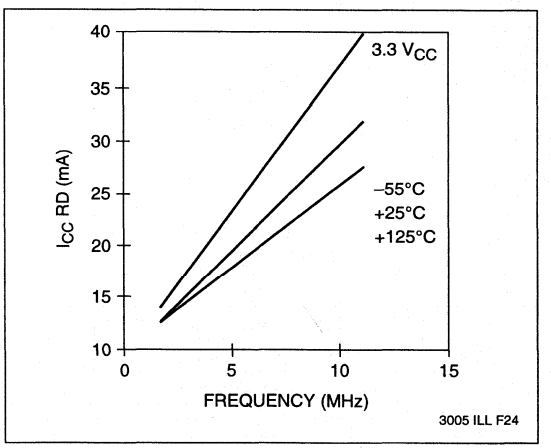
Active Supply Current vs. Ambient Temperature



Standby Supply Current vs. Ambient Temperature



I_{CC} (RD) by Temperature over Frequency



ABSOLUTE MAXIMUM RATINGS*

Temperature under Bias
- X28LC512/513 ..... −10°C to +85°C
- X28LC512I/X28LC513I ..... −65°C to +135°C

Storage Temperature ..... −65°C to +150°C

Voltage on any Pin with
- Respect to V_{SS} ..... −1V to +7V

D.C. Output Current 5mA

Lead Temperature
- (Soldering, 10 seconds) ..... 300°C

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMEND OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	+70°C
Industrial	−40°C	+85°C

3005 PGM T02

Supply Voltage	Limits
X28LC512/513	3.3V ±10%

3005 PGM T03.1

D.C. OPERATING CHARACTERISTICS (Over recommended operating conditions, unless otherwise specified.)

		Limits			
Symbol	Parameter	Min.	Max.	Units	Test Conditions
I_{CC}	V_{CC} Current (Active) (CMOS Inputs)		25	mA	$\overline{CE} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$, All I/O's = Open, Address Inputs = $0.1xV_{CC}/0.9xV_{CC}$ Levels @ f = 5MHz
I_{SB}	V_{CC} Current (Standby) (CMOS Inputs)		150	µA	$\overline{OE} = V_{IL}$, $\overline{CE} = V_{CC} - 0.3V$ All I/O's = Open, Other Inputs = V_{CC}
I_{LI}	Input Leakage Current		10	µA	$V_{IN} = V_{SS}$ to V_{CC}
I_{LO}	Output Leakage Current		10	µA	$V_{OUT} = V_{SS}$ to V_{CC}, $\overline{CE} = V_{IH}$
V_{IL}(1)	Input LOW Voltage	−1	0.6	V	
V_{IH}(1)	Input HIGH Voltage	2	V_{CC} + 0.5	V	
V_{OL}	Output LOW Voltage		0.4	V	I_{OL} = 1mA
V_{OH}	Output HIGH Voltage	2.4		V	I_{OH} = −200µA

3005 PGM T04.2

Notes: (1) V_{IL} min. and V_{IH} max. are for reference only and are not tested.

POWER-UP TIMING

Symbol	Parameter	Max.	Units
t_{PUR}(2)	Power-up to Read Operation	100	µs
t_{PUW}(2)	Power-up to Write Operation	5	ms

3005 PGM T05

CAPACITANCE T_A = +25°C, f = 1MHz, V_{CC} = 3.3V

Symbol	Parameter	Max.	Units	Test Conditions
$C_{I/O}$(2)	Input/Output Capacitance	10	pF	$V_{I/O}$ = 0V
C_{IN}(2)	Input Capacitance	10	pF	V_{IN} = 0V

3005 PGM T06.1

ENDURANCE AND DATA RETENTION

Parameter	Min.	Max.	Units
Endurance	10,000		Cycles per Byte
Data Retention	100		Years

3005 PGM T11

A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3V
Input Rise and Fall Times	10ns
Input and Output Timing Levels	1.5V

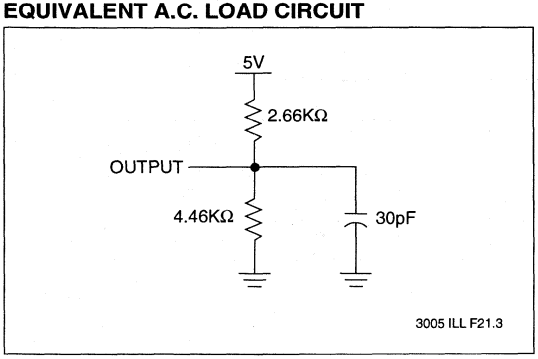
3856 PGM T07.1

MODE SELECTION

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O	Power
L	L	H	Read	D_{OUT}	Active
L	H	L	Write	D_{IN}	Active
H	X	X	Standby and Write Inhibit	High Z	Standby
X	L	X	Write Inhibit	—	—
X	X	H	Write Inhibit	—	—

3005 PGM T08

EQUIVALENT A.C. LOAD CIRCUIT



SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

Note: (2) This parameter is periodically sampled and not 100% tested.

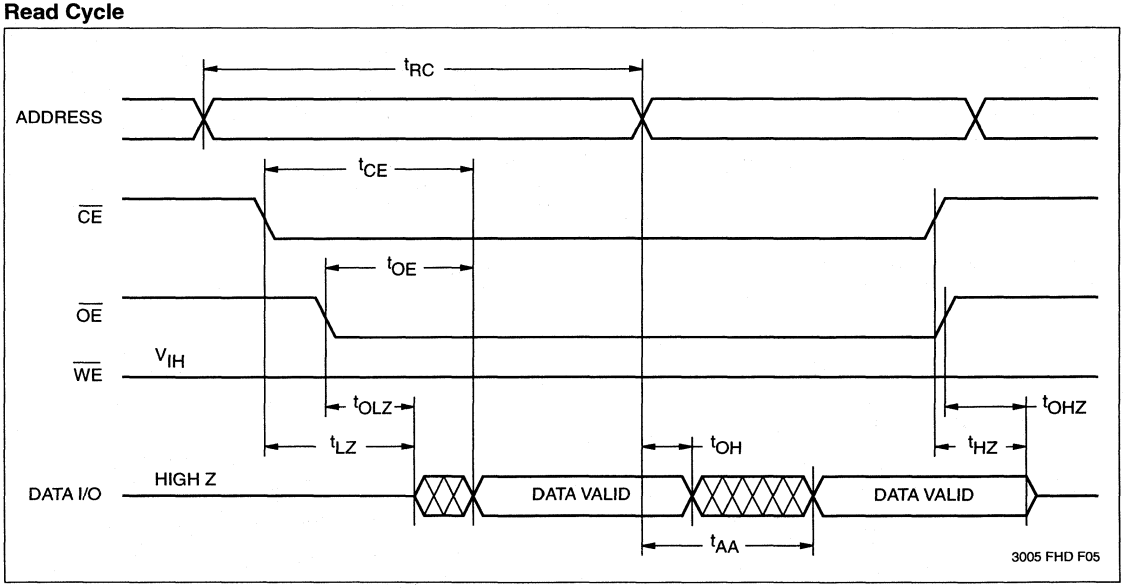
A.C. CHARACTERISTICS (Over the recommended operating conditions, unless otherwise specified.)

Read Cycle Limits

		X28LC512-15 X28LC513-15		X28LC512-20 X28LC513-20		X28LC512-25 X28LC513-25		
Symbol	**Parameter**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{RC}	Read Cycle Time	150		200		250		ns
t_{CE}	Chip Enable Access Time		150		200		250	ns
t_{AA}	Address Access Time		150		200		250	ns
t_{OE}	Output Enable Access Time		80		80		80	ns
t_{LZ}(3)	$\overline{CE}$ LOW to Active Output	0		0		0		ns
t_{OLZ}(3)	$\overline{OE}$ LOW to Active Output	0		0		0		ns
t_{HZ}(3)	$\overline{CE}$ HIGH to High Z Output		50		50		50	ns
t_{OHZ}(3)	$\overline{OE}$ HIGH to High Z Output		50		50		50	ns
t_{OH}	Output Hold from Address Change	0		0		0		ns

3005 PGM T09.2

Read Cycle



Notes: (3) t_{LZ} min., t_{HZ}, t_{OLZ} min., and tOHZ are periodically sampled and not 100% tested. t_{HZ} max. and t_{OHZ} max. are measured, with C_L = 5pF from the point when $\overline{CE}$ or $\overline{OE}$ return HIGH (whichever occurs first) to the time when the outputs are no longer driven.

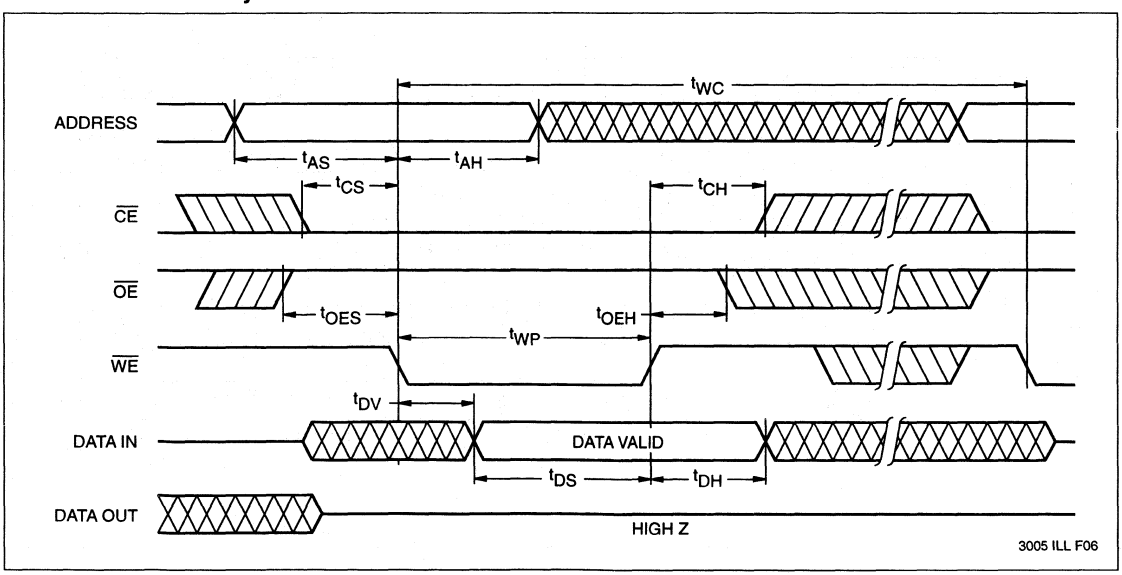
WRITE CYCLE LIMITS

Symbol	Parameter	Min.	Max.	Units
t_{WC}(4)	Write Cycle Time		5	ms
t_{AS}	Address Setup Time	0		ns
t_{AH}	Address Hold Time	50		ns
t_{CS}	Write Setup Time	0		ns
t_{CH}	Write Hold Time	0		ns
t_{CW}	$\overline{CE}$ Pulse Width	100		ns
t_{OES}	$\overline{OE}$ HIGH Setup Time	10		ns
t_{OEH}	$\overline{OE}$ HIGH Hold Time	10		ns
t_{WP}	$\overline{WE}$ Pulse Width	100		ns
t_{WPH}	$\overline{WE}$ HIGH Recovery	100		ns
t_{DV}	Data Valid		1	µs
t_{DS}	Data Setup	50		ns
t_{DH}	Data Hold	10		ns
t_{DW}	Delay to Next Write	10		µs
t_{BLC}	Byte Load Cycle	0.20	100	µs

3005 PGM T10.1

3

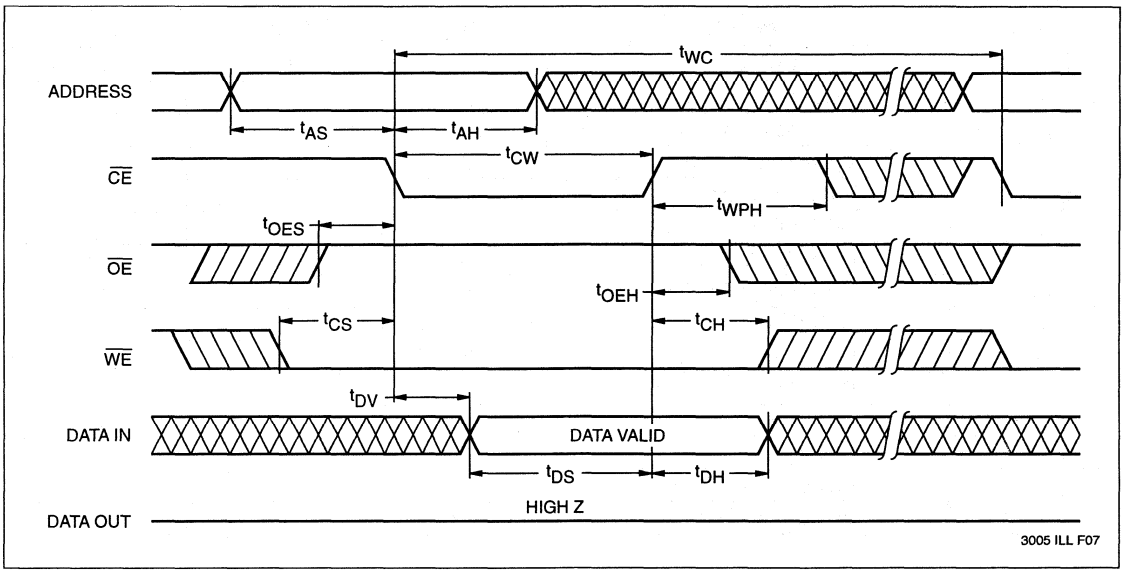
$\overline{WE}$ Controlled Write Cycle



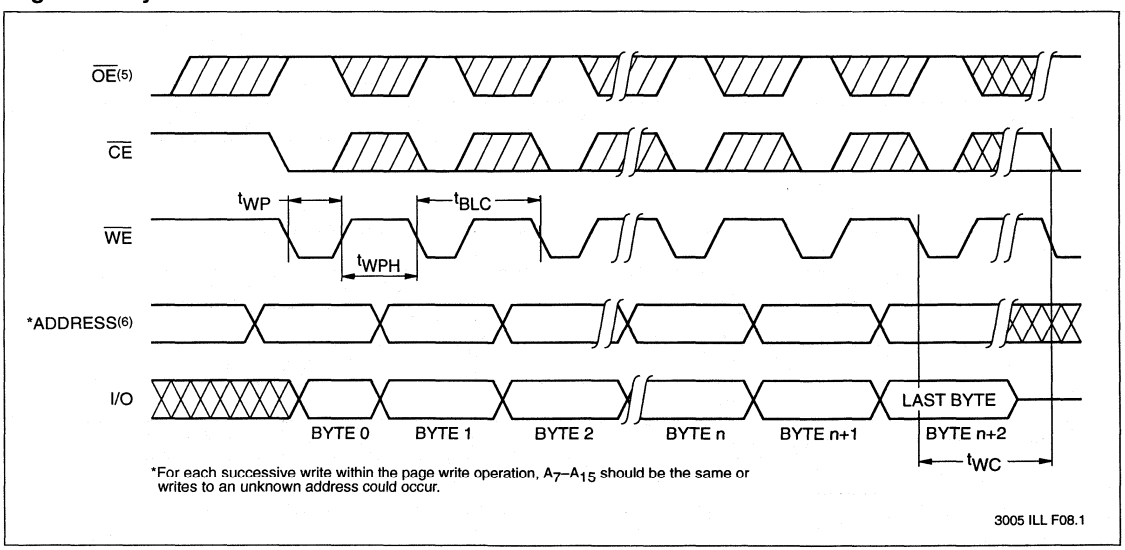
3005 ILL F06

Notes: (4) t_{WC} is the minimum cycle time to be allowed from the system perspective unless polling techniques are used. It is the maximum time the device requires to complete the internal write operation.

$\overline{CE}$ Controlled Write Cycle



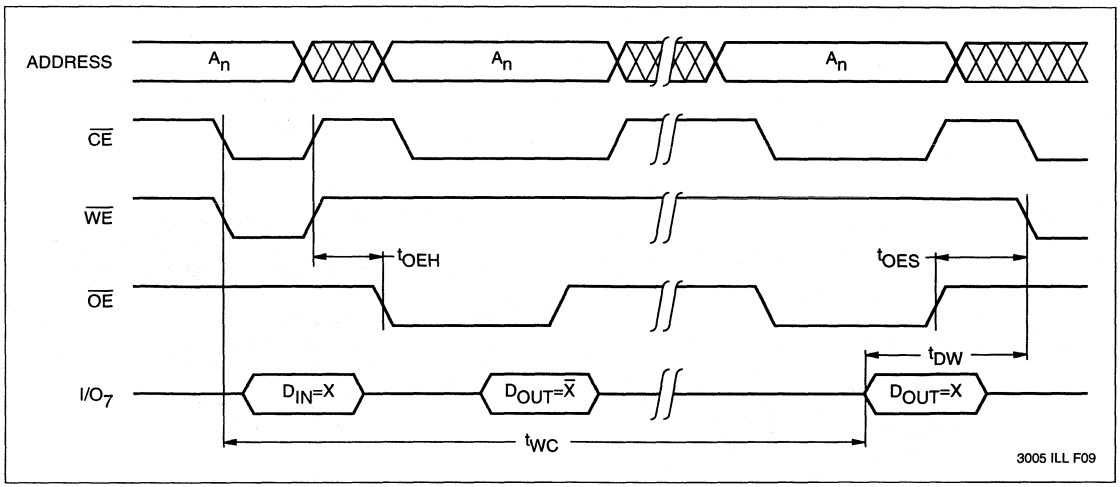
Page Write Cycle



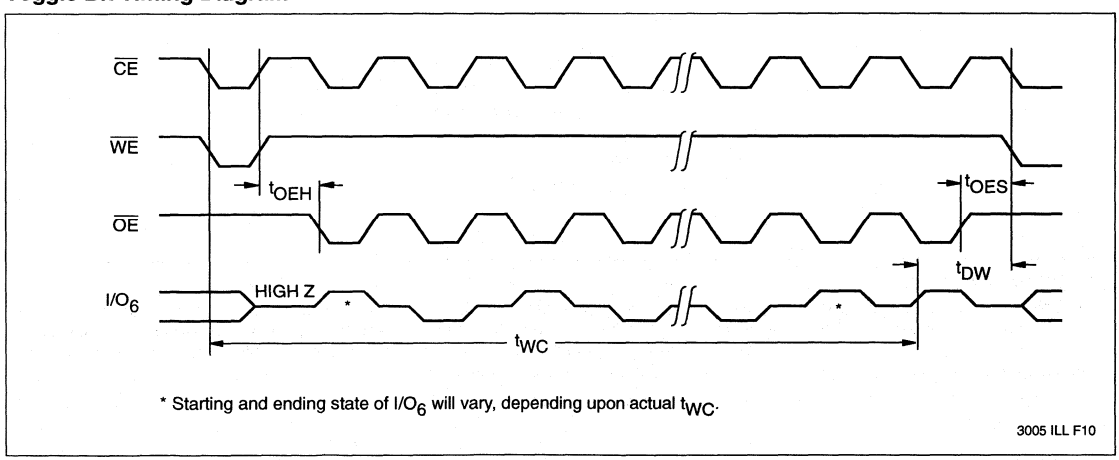
Notes: (5) Between successive byte writes within a page write operation, $\overline{OE}$ can be strobed LOW: e.g. this can be done with $\overline{CE}$ and $\overline{WE}$ HIGH to fetch data from another memory device within the system for the next write; or with $\overline{WE}$ HIGH and $\overline{CE}$ LOW effectively performing a polling operation.

(6) The timings shown above are unique to page write operations. Individual byte load operations within the page write must conform to either the $\overline{CE}$ or $\overline{WE}$ controlled write cycle timing.

$\overline{\text{DATA}}$ Polling Timing Diagram(7)

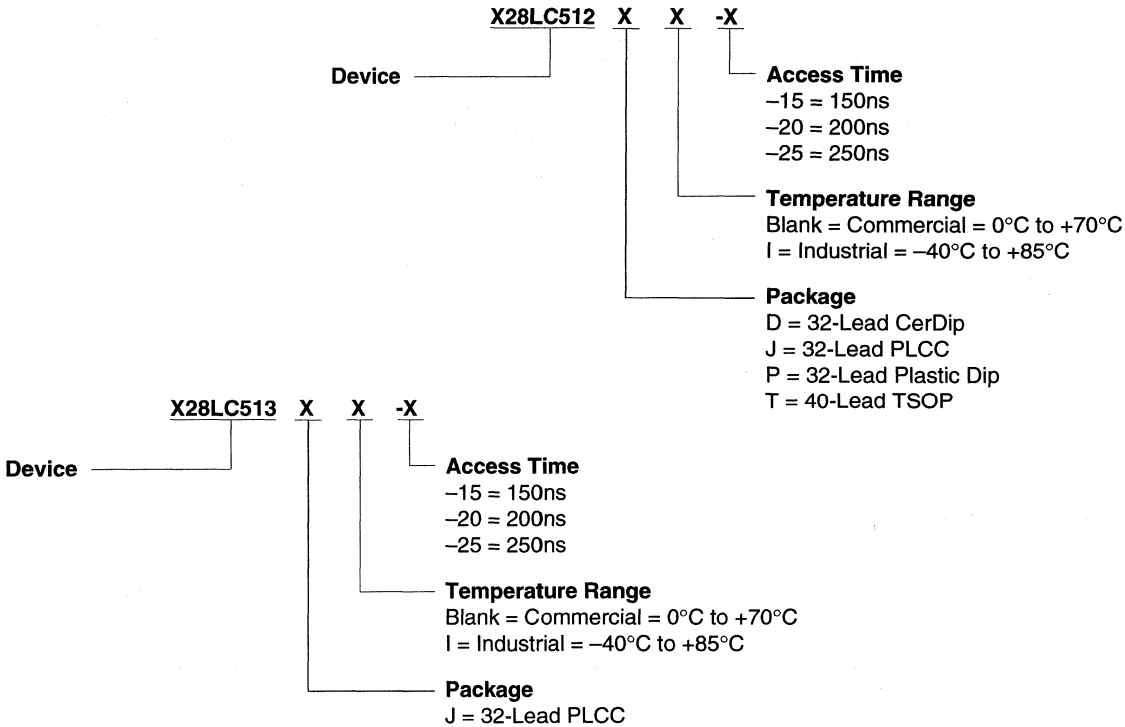


Toggle Bit Timing Diagram



Note: (7) Polling operations are by definition read cycles and are therefore subject to read cycle timings.

ORDERING INFORMATION



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US. PATENTS

Xicor products are covered by one or more of the following U.S. Patents: 4,263,664; 4,274,012; 4,300,212; 4,314,265; 4,326,134; 4,393,481; 4,404,475; 4,450,402; 4,486,769; 4,488,060; 4,520,461; 4,533,846; 4,599,706; 4,617,652; 4,668,932; 4,752,912; 4,829,482; 4,874,967; 4,883,976. Foreign patents and additional patents pending.

LIFE RELATED POLICY

In situations where semiconductor component failure may endanger life, system designers using this product should design the system with appropriate error detection and correction, redundancy and back-up features to prevent such an occurrence.

Xicor's products are not authorized for use as critical components in life support devices or systems.

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its satety or effectiveness.

5 Volt, Byte Alterable E²PROM

FEATURES

- Access Time: 120ns
- Simple Byte and Page Write
  - —Single 5V Supply
  - —No External High Voltages or V_{PP} Control Circuits
  - —Self-Timed
    - —No Erase Before Write
    - —No Complex Programming Algorithms
    - —No Overerase Problem
- Low Power CMOS:
  - —Active: 50mA
  - —Standby: 500µA
- Software Data Protection
  - —Protects Data Against System Level Inadvertant Writes
- High Speed Page Write Capability
- Highly Reliable Direct Write™ Cell
  - —Endurance: 100,000 Write Cycles
  - —Data Retention: 100 Years
- Early End of Write Detection
  - —$\overline{\text{DATA}}$ Polling
  - —Toggle Bit Polling

DESCRIPTION

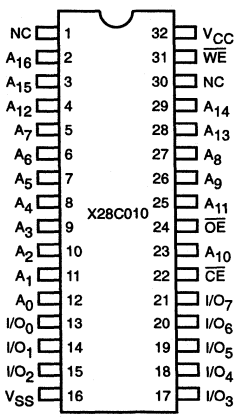
The Xicor X28C010 is a 128K x 8 E²PROM, fabricated with Xicor's proprietary, high performance, floating gate CMOS technology. Like all Xicor programmable nonvolatile memories the X28C010 is a 5V only device. The X28C010 features the JEDEC approved pinout for byte-wide memories, compatible with industry standard EPROMs.

The X28C010 supports a 256-byte page write operation, effectively providing a 19µs/byte write cycle and enabling the entire memory to be typically written in less than 2.5 seconds. The X28C010 also features $\overline{\text{DATA}}$ Polling and Toggle Bit Polling, system software support schemes used to indicate the early completion of a write cycle. In addition, the X28C010 supports Software Data Protection option.

Xicor E²PROMs are designed and tested for applications requiring extended endurance. Data retention is specified to be greater than 100 years.

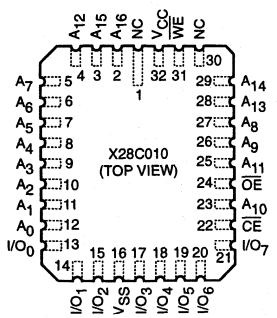
PIN CONFIGURATION

CERDIP
FLAT PACK
R (SOIC)



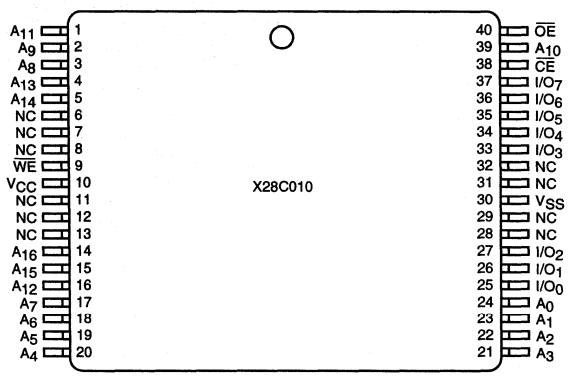
3858 FHD F02.1

PLCC
LCC



3858 FHD F03

TSOP



3858 ILL F21

PIN DESCRIPTIONS

Addresses (A_0–A_{16})

The Address inputs select an 8-bit memory location during a read or write operation.

Chip Enable ($\overline{CE}$)

The Chip Enable input must be LOW to enable all read/write operations. When $\overline{CE}$ is HIGH, power consumption is reduced.

Output Enable ($\overline{OE}$)

The Output Enable input controls the data output buffers and is used to initiate read operations.

Data In/Data Out (I/O_0–I/O_7)

Data is written to or read from the X28C010 through the I/O pins.

Write Enable ($\overline{WE}$)

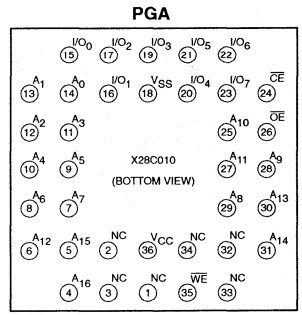
The Write Enable input controls the writing of data to the X28C010.

PIN NAMES

Symbol	Description
A_0–A_{16}	Address Inputs
I/O_0–I/O_7	Data Input/Output
$\overline{WE}$	Write Enable
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
V_{CC}	+5V
V_{SS}	Ground
NC	No Connect

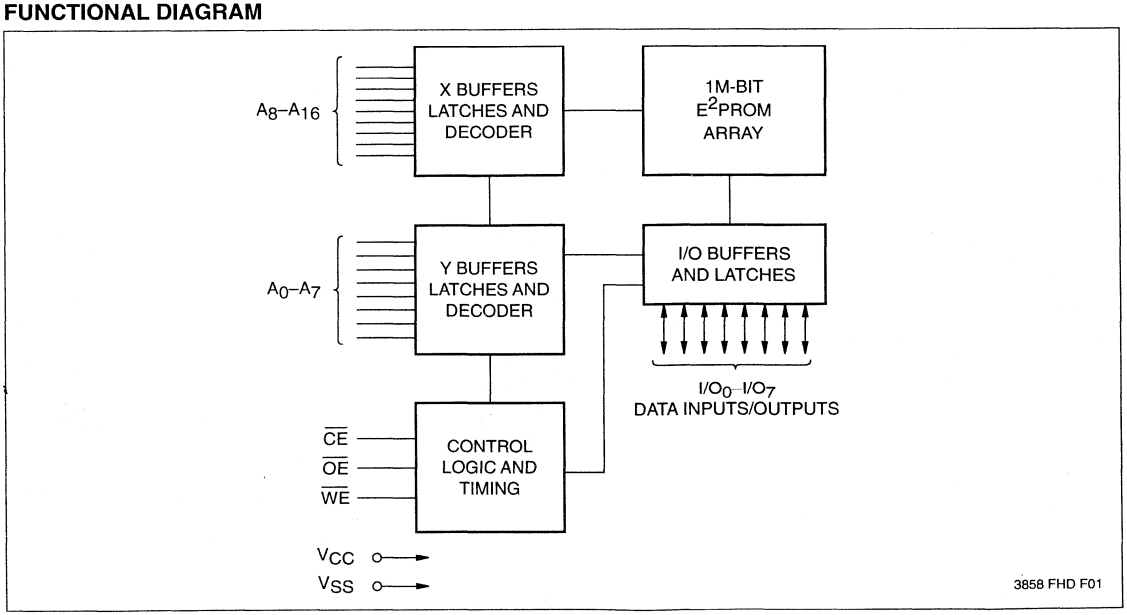
3858 PGM T01

PIN CONFIGURATION



3858 FHD F20

FUNCTIONAL DIAGRAM



3858 FHD F01

DEVICE OPERATION

Read

Read operations are initiated by both $\overline{OE}$ and $\overline{CE}$ LOW. The read operation is terminated by either $\overline{CE}$ or $\overline{OE}$ returning HIGH. This two line control architecture eliminates bus contention in a system environment. The data bus will be in a high impedance state when either $\overline{OE}$ or $\overline{CE}$ is HIGH.

Write

Write operations are initiated when both $\overline{CE}$ and $\overline{WE}$ are LOW and $\overline{OE}$ is HIGH. The X28C010 supports both a $\overline{CE}$ and $\overline{WE}$ controlled write cycle. That is, the address is latched by the falling edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs last. Similarly, the data is latched internally by the rising edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs first. A byte write operation, once initiated, will automatically continue to completion, typically within 5ms.

Page Write Operation

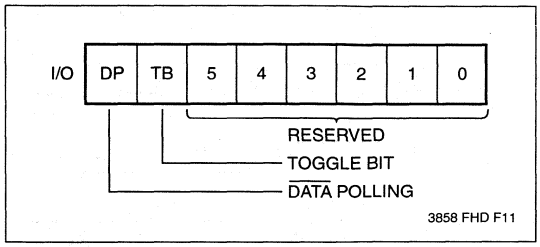
The page write feature of the X28C010 allows the entire memory to be written in 5 seconds. Page write allows two to two hundred fifty-six bytes of data to be consecutively written to the X28C010 prior to the commencement of the internal programming cycle. The host can fetch data from another device within the system during a page write operation (change the source address), but the page address (A_8 through A_{16}) for each subsequent valid write cycle to the part during this operation must be the same as the initial page address.

The page write mode can be initiated during any write operation. Following the initial byte write cycle, the host can write an additional one to two hundred fifty six bytes in the same manner as the first byte was written. Each successive byte load cycle, started by the $\overline{WE}$ HIGH to LOW transition, must begin within 100µs of the falling edge of the preceding $\overline{WE}$. If a subsequent $\overline{WE}$ HIGH to LOW transition is not detected within 100µs, the internal automatic programming cycle will commence. There is no page write window limitation. Effectively the page write window is infinitely wide, so long as the host continues to access the device within the byte load cycle time of 100µs.

Write Operation Status Bits

The X28C010 provides the user two write operation status bits. These can be used to optimize a system write cycle time. The status bits are mapped onto the I/O bus as shown in Figure 1.

Figure 1. Status Bit Assignment



$\overline{DATA}$ Polling (I/O_7)

The X28C010 features $\overline{DATA}$ Polling as a method to indicate to the host system that the byte write or page write cycle has completed. $\overline{DATA}$ Polling allows a simple bit test operation to determine the status of the X28C010, eliminating additional interrupt inputs or external hardware. During the internal programming cycle, any attempt to read the last byte written will produce the complement of that data on I/O_7 (i.e., write data = 0xxx xxxx, read data = 1xxx xxxx). Once the programming cycle is complete, I/O_7 will reflect true data. Note: If the X28C010 is in the protected state and an illegal write operation is attempted $\overline{DATA}$ Polling will not operate.

Toggle Bit (I/O_6)

The X28C010 also provides another method for determining when the internal write cycle is complete. During the internal programming cycle, I/O_6 will toggle from HIGH to LOW and LOW to HIGH on subsequent attempts to read the device. When the internal cycle is complete the toggling will cease and the device will be accessible for additional read or write operations.

$\overline{DATA}$ Polling I/O_7

Figure 2. $\overline{DATA}$ Polling Bus Sequence

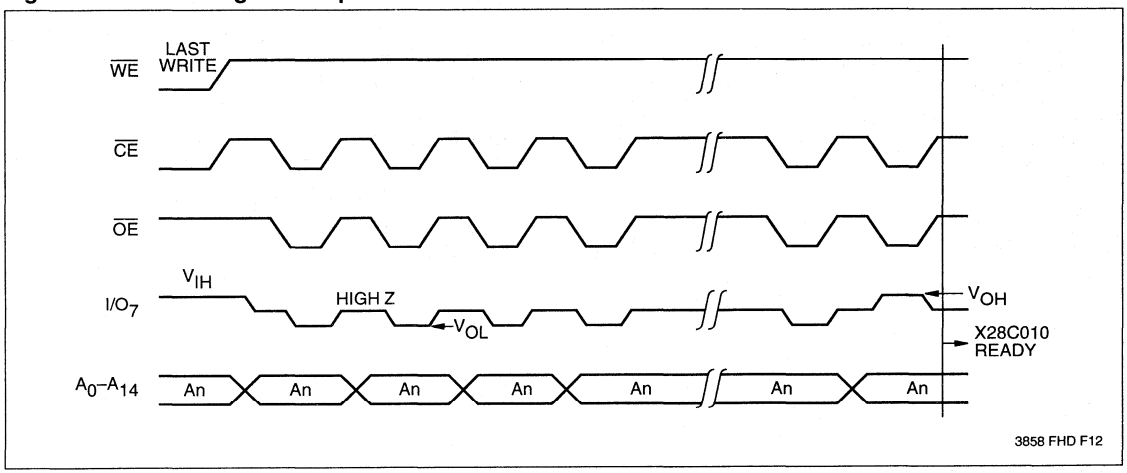
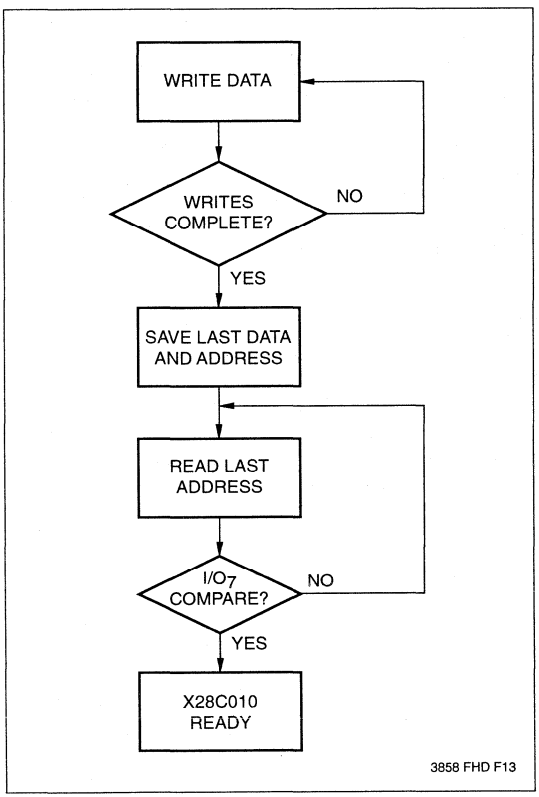


Figure 3. $\overline{DATA}$ Polling Software Flow



$\overline{DATA}$ Polling can effectively halve the time for writing to the X28C010. The timing diagram in Figure 2 illustrates the sequence of events on the bus. The software flow diagram in Figure 3 illustrates one method of implementing the routine.

The Toggle Bit I/O_6

Figure 4. Toggle Bit Bus Sequence

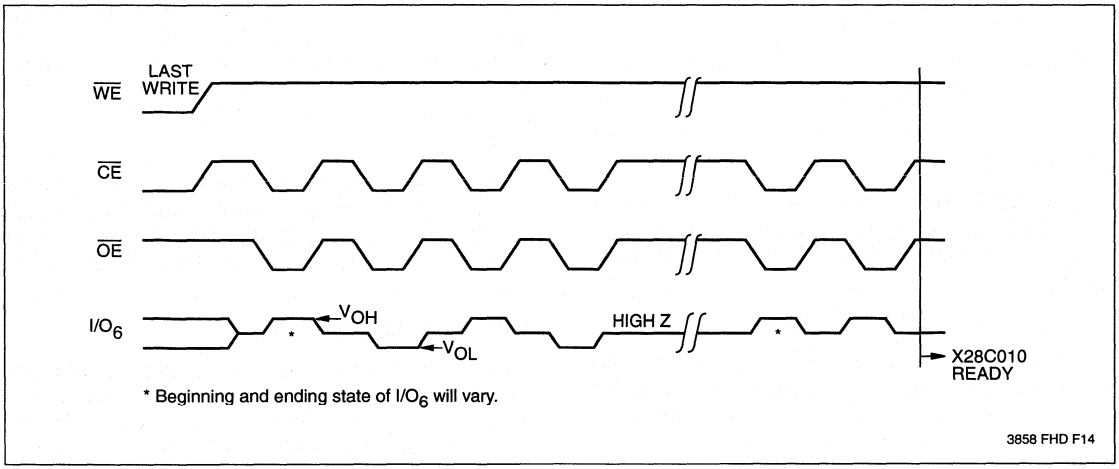
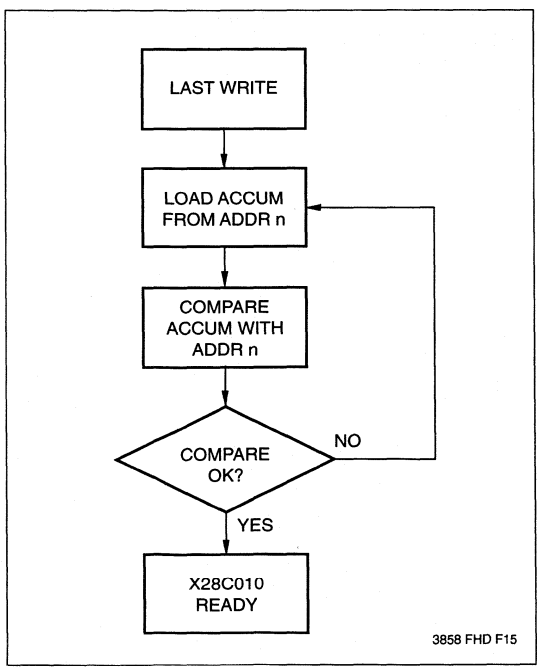


Figure 5. Toggle Bit Software Flow



The Toggle Bit can eliminate the software housekeeping chore of saving and fetching the last address and data written to a device in order to implement $\overline{DATA}$ Polling. This can be especially helpful in an array comprised of multiple X28C010 memories that is frequently updated. Toggle Bit Polling can also provide a method for status checking in multiprocessor applications. The timing diagram in Figure 4 illustrates the sequence of events on the bus. The software flow diagram in Figure 5 illustrates a method for polling the Toggle Bit.

HARDWARE DATA PROTECTION

The X28C010 provides three hardware features that protect nonvolatile data from inadvertent writes.

- Noise Protection—A $\overline{WE}$ pulse less than 10ns will not initiate a write cycle.
- Default V_{CC} Sense—All functions are inhibited when V_{CC} is ≤3.5V.
- Write inhibit—Holding either $\overline{OE}$ LOW, $\overline{WE}$ HIGH, or $\overline{CE}$ HIGH will prevent an inadvertent write cycle during power-up and power-down, maintaining data integrity.

SOFTWARE DATA PROTECTION

The X28C010 offers a software controlled data protection feature. The X28C010 is shipped from Xicor with the software data protection NOT ENABLED: that is the device will be in the standard operating mode. In this mode data should be protected during power-up/-down operations through the use of external circuits. The host would then have open read and write access of the device once V_{CC} was stable.

The X28C010 can be automatically protected during power-up and power-down without the need for external circuits by employing the software data protection feature. The internal software data protection circuit is enabled after the first write operation utilizing the software algorithm. This circuit is nonvolatile and will remain set for the life of the device unless the reset command is issued.

Once the software protection is enabled, the X28C010 is also protected from inadvertent and accidental writes in the powered-up state. That is, the software algorithm must be issued prior to writing additional data to the device.

SOFTWARE ALGORITHM

Selecting the software data protection mode requires the host system to precede data write operations by a series of three write operations to three specific addresses. Refer to Figures 6 and 7 for the sequence. The three byte sequence opens the page write window enabling the host to write from one to two hundred fifty-six bytes of data. Once the page load cycle has been completed, the device will automatically be returned to the data protected state.

Software Data Protection

Figure 6. Timing Sequence—Byte or Page Write

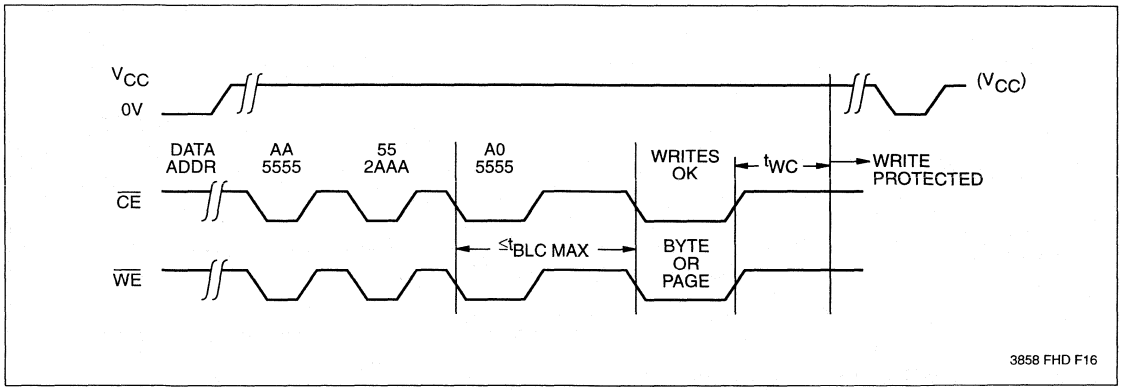
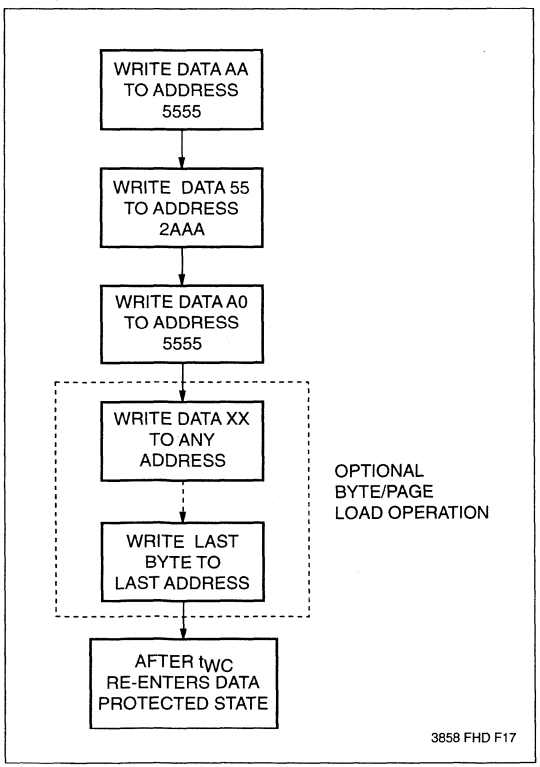


Figure 7. Write Sequence for Software Data Protection



Regardless of whether the device has previously been protected or not, once the software data protection algorithm is used and data has been written, the X28C010 will automatically disable further writes unless another command is issued to cancel it. If no further commands are issued the X28C010 will be write protected during power-down and after any subsequent power-up. The state of A_{15} and A_{16} while executing the algorithm is don't care.

Note: Once initiated, the sequence of write operations should not be interrupted.

Resetting Software Data Protection

Figure 8. Reset Software Data Protection Timing Sequence

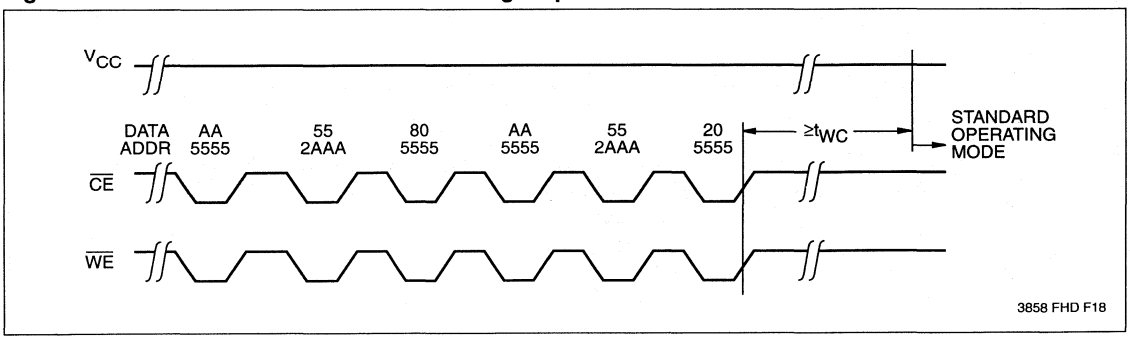
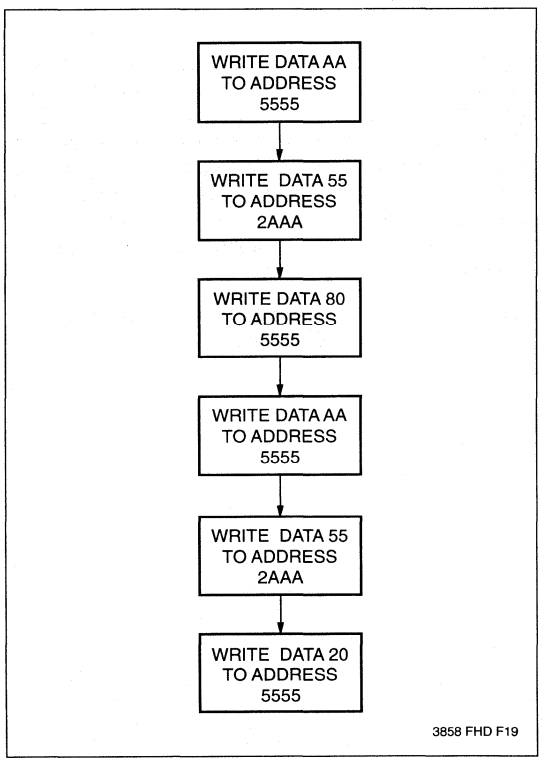


Figure 9. Software Sequence to Deactivate Software Data Protection



In the event the user wants to deactivate the software data protection feature for testing or reprogramming in an E²PROM programmer, the following six step algorithm will reset the internal protection circuit. After t_{WC}, the X28C010 will be in standard operating mode.

Note: Once initiated, the sequence of write operations should not be interrupted.

SYSTEM CONSIDERATIONS

Because the X28C010 is frequently used in large memory arrays it is provided with a two line control architecture for both read and write operations. Proper usage can provide the lowest possible power dissipation and eliminate the possibility of contention where multiple I/O pins share the same bus.

To gain the most benefit it is recommended that $\overline{CE}$ be decoded from the address bus and be used as the primary device selection input. Both $\overline{OE}$ and $\overline{WE}$ would then be common among all devices in the array. For a read operation this assures that all deselected devices are in their standby mode and that only the selected device(s) is outputting data on the bus.

Because the X28C010 has two power modes, standby and active, proper decoupling of the memory array is of prime concern. Enabling $\overline{CE}$ will cause transient current spikes. The magnitude of these spikes is dependent on the output capacitive loading of the I/Os. Therefore, the larger the array sharing a common bus, the larger the transient spikes. The voltage peaks associated with the current transients can be suppressed by the proper selection and placement of decoupling capacitors. As a minimum, it is recommended that a 0.1μF high frequency ceramic capacitor be used between V_{CC} and V_{SS} at each device. Depending on the size of the array, the value of the capacitor may have to be larger.

In addition, it is recommended that a 4.7μF electrolytic bulk capacitor be placed between V_{CC} and V_{SS} for each eight devices employed in the array. This bulk capacitor is employed to overcome the voltage droop caused by the inductive effects of the PC board traces.

ABSOLUTE MAXIMUM RATINGS*

Temperature under Bias
- X28C010 ..... −10°C to +85°C
- X28C010I ..... −65°C to +135°C
- X28C010M ..... −65°C to +135°C

Storage Temperature ..... −65°C to +150°C

Voltage on any Pin with
- Respect to V_{SS} ..... −1V to +7V

D.C. Output Current 5mA

Lead Temperature
- (Soldering, 10 seconds) ..... 300°C

***COMMENT**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMEND OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	+70°C
Industrial	−40°C	+85°C
Military	−55°C	+125°C

3858 PGM T02

Supply Voltage	Limits
X28C010	5V ±10%

3858 PGM T03

D.C. OPERATING CHARACTERISTICS (Over the recommended operating conditions, unless otherwise specified.)

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
I_{CC}	V_{CC} Current (Active) (TTL Inputs)		50	mA	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}, All I/O's = Open, Address Inputs = .4V/2.4V Levels @ f = 5MHz
I_{SB1}	V_{CC} Current (Standby) (TTL Inputs)		3	mA	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IL} All I/O's = Open, Other Inputs = V_{IH}
I_{SB2}	V_{CC} Current (Standby) (CMOS Inputs)		500	µA	$\overline{CE}$ = V_{CC} − 0.3V, $\overline{OE}$ = V_{IL} All I/O's = Open, Other Inputs = V_{CC}
I_{LI}	Input Leakage Current		10	µA	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output Leakage Current		10	µA	V_{OUT} = V_{SS} to V_{CC}, $\overline{CE}$ = V_{IH}
V_{IL}(1)	Input LOW Voltage	−1	0.8	V	
V_{IH}(1)	Input HIGH Voltage	2	V_{CC} + 1	V	
V_{OL}	Output LOW Voltage		0.4	V	I_{OL} = 2.1mA
V_{OH}	Output HIGH Voltage	2.4		V	I_{OH} = −400µA

3858 PGM T04.2

Notes: (1) V_{IL} min. and V_{IH} max. are for reference only and are not tested.

POWER-UP TIMING

Symbol	Parameter	Max.	Units
t_{PUR}(2)	Power-up to Read Operation	100	µs
t_{PUW}(2)	Power-up to Write Operation	5	ms

3858 PGM T05

CAPACITANCE T_A = +25°C, f = 1MHz, V_{CC} = 5V

Symbol	Parameter	Max.	Units	Test Conditions
$C_{I/O}$(2)	Input/Output Capacitance	10	pF	$V_{I/O}$ = 0V
C_{IN}(2)	Input Capacitance	10	pF	V_{IN} = 0V

3858 PGM T06

ENDURANCE AND DATA RETENTION

Parameter	Min.	Max.	Units
Endurance	10,000		Cycles Per Byte
Endurance	100,000		Cycles Per Page
Data Retention	100		Years

3858 PGM T07.1

A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3V
Input Rise and Fall Times	10ns
Input and Output Timing Levels	1.5V

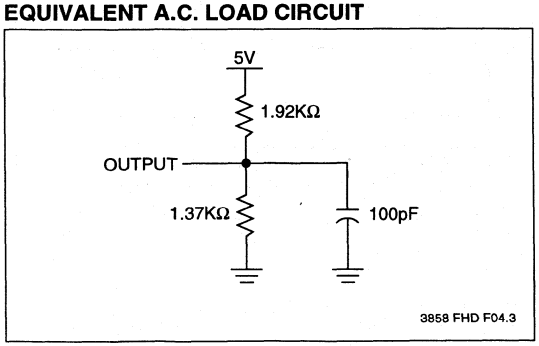
3858 PGM T05.1

MODE SELECTION

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O	Power
L	L	H	Read	D_{OUT}	Active
L	H	L	Write	D_{IN}	Active
H	X	X	Standby and Write Inhibit	High Z	Standby
X	L	X	Write Inhibit	—	—
X	X	H	Write Inhibit	—	—

3858 PGM T08

EQUIVALENT A.C. LOAD CIRCUIT



3858 FHD F04.3

SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

Note: (2) This parameter is periodically sampled and not 100% tested.

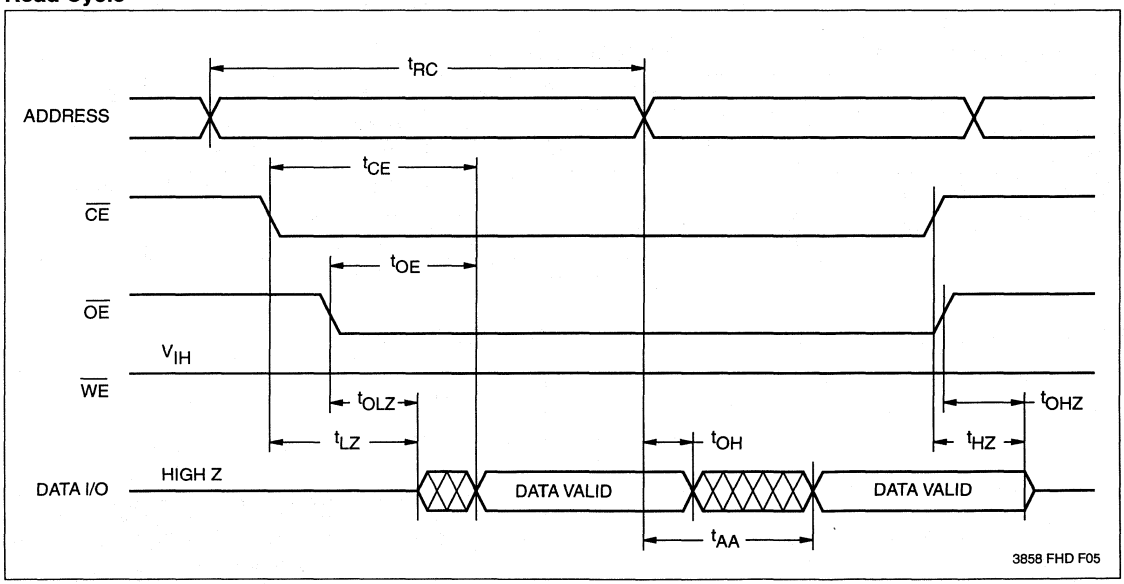
A.C. CHARACTERISTICS (Over the recommended operating conditions, unless otherwise specified.)

Read Cycle Limits

Symbol	Parameter	X28C010-12		X28C010-15		X28C010-20		X28C010-25		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	120		150		200		250		ns
t_{CE}	Chip Enable Access Time		120		150		200		250	ns
t_{AA}	Address Access Time		120		150		200		250	ns
t_{OE}	Output Enable Access Time		50		50		50		50	ns
t_{LZ}(3)	$\overline{CE}$ LOW to Active Output	0		0		0		0		ns
t_{OLZ}(3)	$\overline{OE}$ LOW to Active Output	0		0		0		0		ns
t_{HZ}(3)	$\overline{CE}$ HIGH to High Z Output		50		50		50		50	ns
t_{OHZ}(3)	$\overline{OE}$ HIGH to High Z Output		50		50		50		50	ns
t_{OH}	Output Hold from Address Change	0		0		0		0		ns

3858 PGM T09.1

Read Cycle



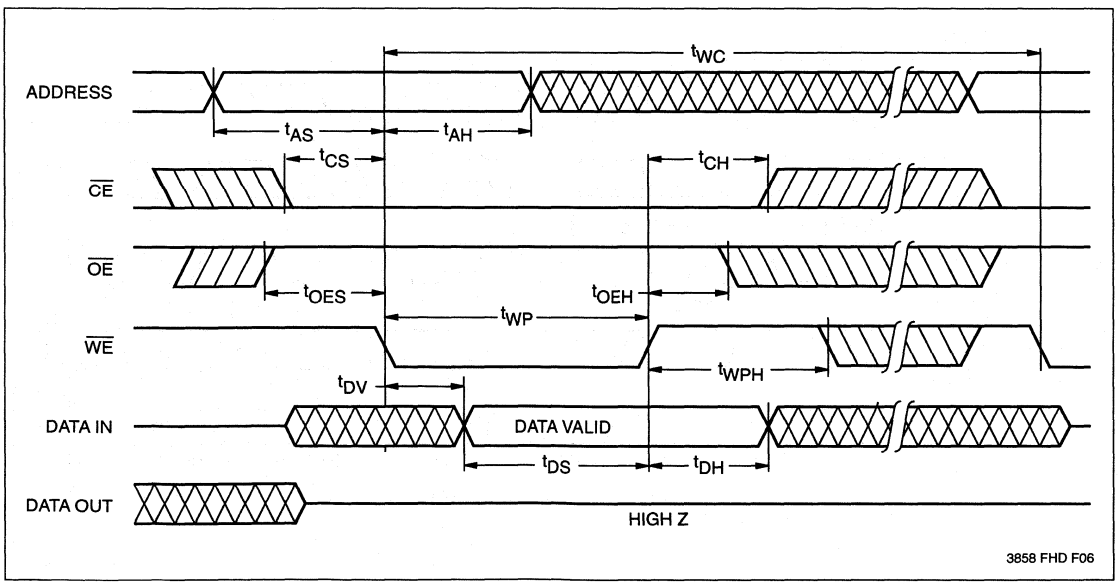
Note: (3) t_{LZ} min., t_{HZ}, t_{OLZ} min., and t_{OHZ} are periodically sampled and not 100% tested. t_{HZ} max. and t_{OHZ} max. are measured, with C_L = 5pF, from the point when $\overline{CE}$ or $\overline{OE}$ return HIGH (whichever occurs first) to the time when the outputs are no longer driven.

Write Cycle Limits

Symbol	Parameter	Min.	Max.	Units
t_{WC}(4)	Write Cycle Time		10	ms
t_{AS}	Address Setup Time	0		ns
t_{AH}	Address Hold Time	50		ns
t_{CS}	Write Setup Time	0		ns
t_{CH}	Write Hold Time	0		ns
t_{CW}	$\overline{CE}$ Pulse Width	100		ns
t_{OES}	$\overline{OE}$ HIGH Setup Time	10		ns
t_{OEH}	$\overline{OE}$ HIGH Hold Time	10		ns
t_{WP}	$\overline{WE}$ Pulse Width	100		ns
t_{WPH}	$\overline{WE}$ HIGH Recovery	100		ns
t_{DV}	Data Valid		1	µs
t_{DS}	Data Setup	50		ns
t_{DH}	Data Hold	10		ns
t_{DW}	Delay to Next Write	10		µs
t_{BLC}	Byte Load Cycle	0.2	100	µs

3858 PGM T10.1

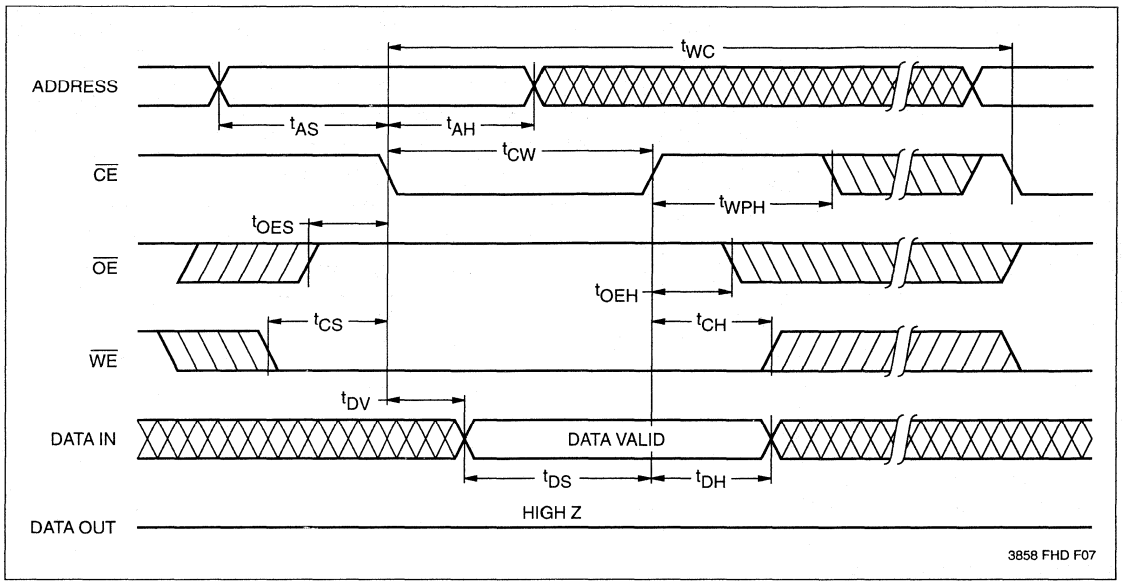
$\overline{WE}$ Controlled Write Cycle



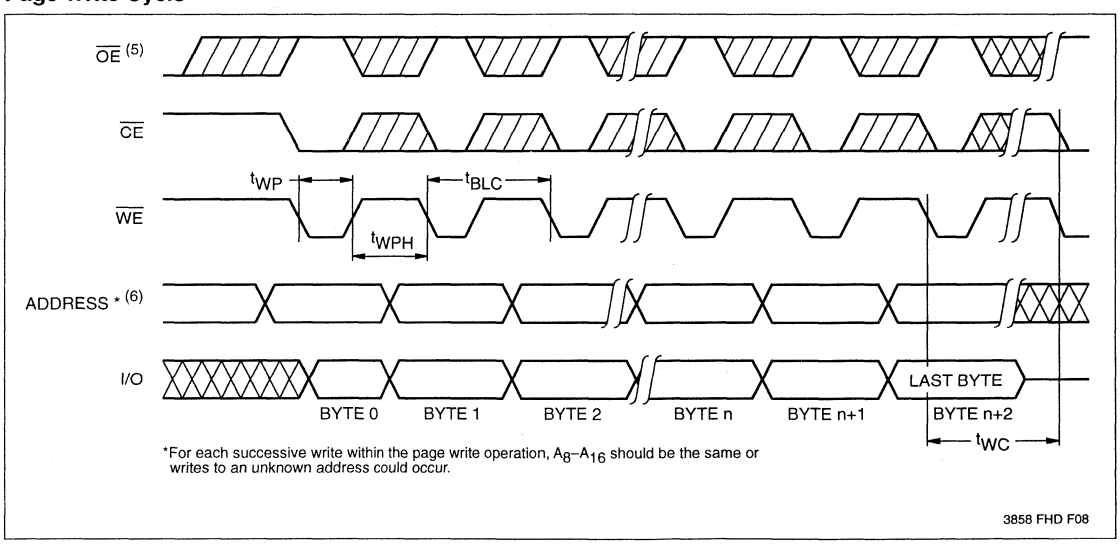
3858 FHD F06

Notes: (4) t_{WC} is the minimum cycle time to be allowed from the system perspective unless polling techniques are used. It is the maximum time the device requires to complete internal write operation.

$\overline{CE}$ Controlled Write Cycle



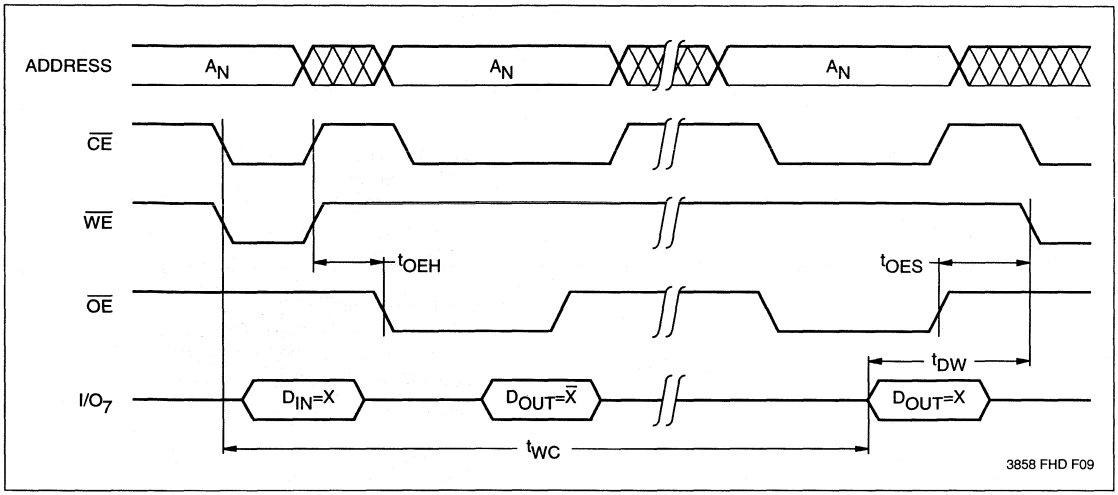
Page Write Cycle



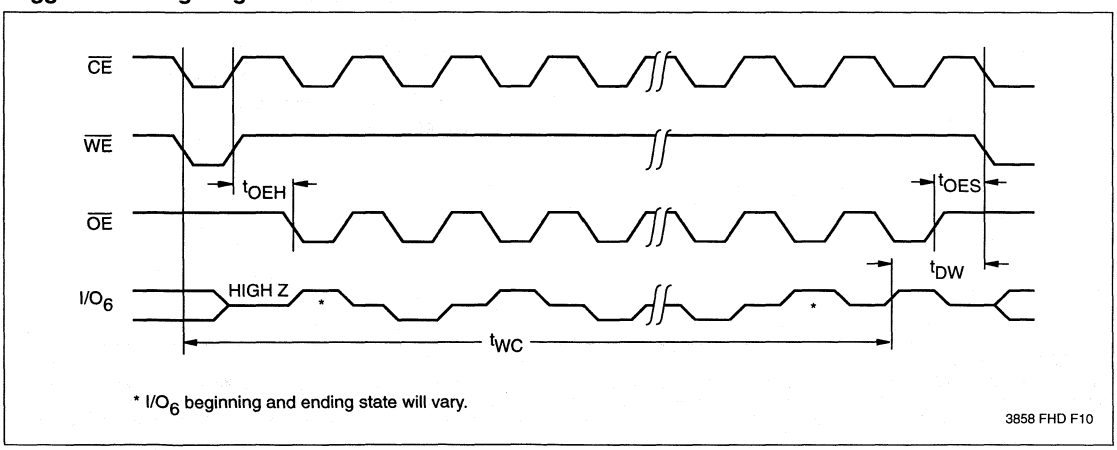
Notes: (5) Between successive byte writes within a page write operation, $\overline{OE}$ can be strobed LOW: e.g. this can be done with $\overline{CE}$ and $\overline{WE}$ HIGH to fetch data from another memory device within the system for the next write; or with $\overline{WE}$ HIGH and $\overline{CE}$ LOW effectively performing a polling operation.

(6) The timings shown above are unique to page write operations. Individual byte load operations within the page write must conform to either the $\overline{CE}$ or $\overline{WE}$ controlled write cycle timing.

$\overline{\text{DATA}}$ Polling Timing Diagram(7)

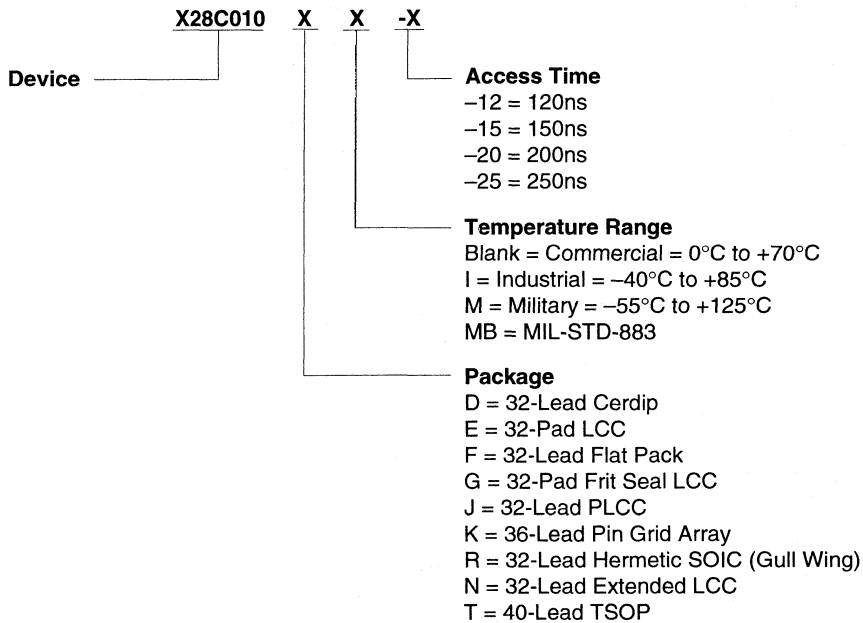


Toggle Bit Timing Diagram



Note: (7) Polling operations are by definition read cycles and are therefore subject to read cycle timings.

ORDERING INFORMATION



High Temperature, 5 Volt, Byte Alterable E²PROM

FEATURES

- **170°C Full Functionality**
- **Simple Byte and Page Write**
  - **—Single 5V Supply**
  - **—Self-Timed**
    - **—No Erase Before Write**
    - **—No Complex Programming Algorithms**
    - **—No Overerase Problem**
- **Highly Reliable Direct Write™ Cell**
  - **—Endurance: 10,000 Write Cycles**
  - **—Data Retention: 100 Years**
  - **—Higher Temperature Functionality is Possible by Operating in the Byte Mode.**

DESCRIPTION

The Xicor X28HT010 is a 128K x 8 E²PROM, fabricated with Xicor's proprietary, high performance, floating gate CMOS technology which provides Xicor products superior high temperature performance characteristics. Like all Xicor programmable non-volatile memories the X28HT010 is a 5V only device. The X28HT010 features the JEDEC approved pinout for byte-wide memories, compatible with industry standard EPROMs.

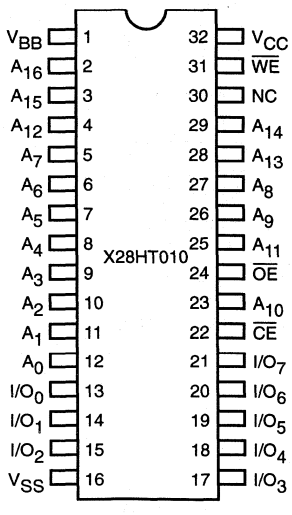
The X28HT010 supports a 256-byte page write operation, effectively providing a 19µs/byte write cycle and enabling the entire memory to be typically written in less than 2.5 seconds.

Xicor E²PROMs are designed and tested for applications requiring extended endurance. Data retention is specified to be greater than 100 years.

3

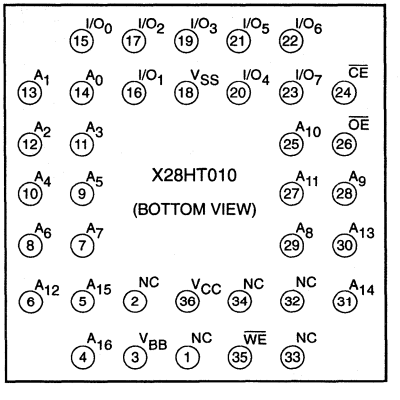
PIN CONFIGURATION

FLAT PACK
CERDIP



6613 FHD F02

PGA



6613 FHD F21

PIN DESCRIPTIONS

Addresses (A_0–A_{16})

The Address inputs select an 8-bit memory location during a read or write operation.

Chip Enable ($\overline{CE}$)

The Chip Enable input must be LOW to enable all read/write operations. When $\overline{CE}$ is HIGH, power consumption is reduced.

Output Enable ($\overline{OE}$)

The Output Enable input controls the data output buffers and is used to initiate read operations.

Data In/Data Out (I/O_0–I/O_7)

Data is written to or read from the X28HT010 through the I/O pins.

Write Enable ($\overline{WE}$)

The Write Enable input controls the writing of data to the X28HT010.

Back Bias Voltage (V_{BB})

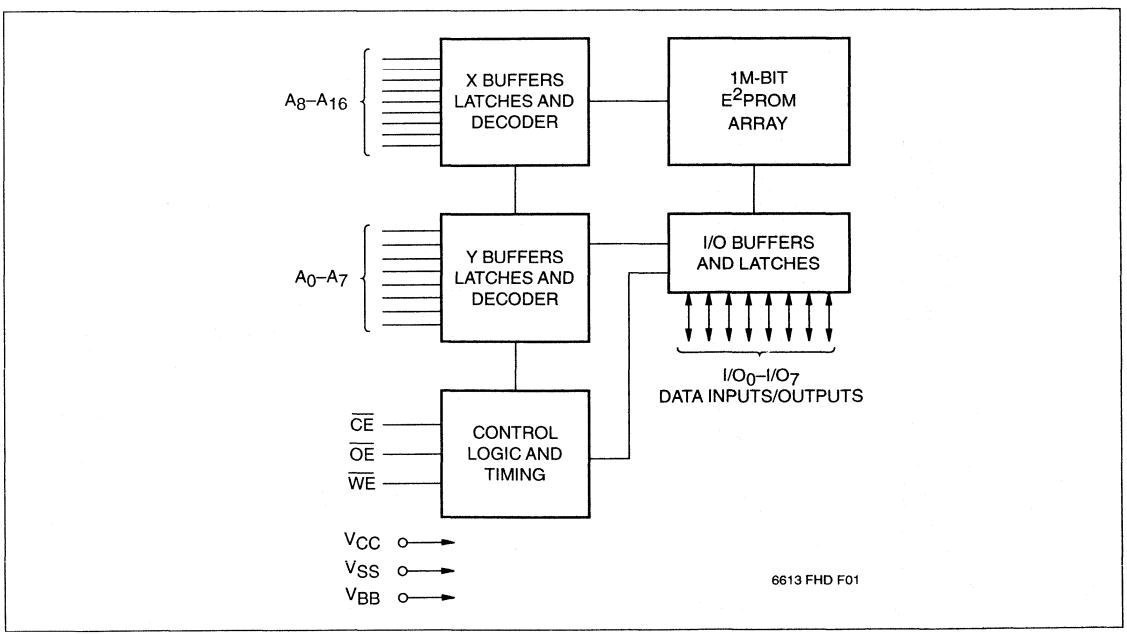
It is required to provide -3V on pin 1. This negative voltage improves higher temperature functionality.

PIN NAMES

Symbol	Description
A_0–A_{16}	Address Inputs
I/O_0–I/O_7	Data Input/Output
$\overline{WE}$	Write Enable
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
V_{BB}	–3V
V_{CC}	+5V
V_{SS}	Ground
NC	No Connect

6613 PGM T01

FUNCTIONAL DIAGRAM



DEVICE OPERATION

Read

Read operations are initiated by both $\overline{OE}$ and $\overline{CE}$ LOW. The read operation is terminated by either $\overline{CE}$ or $\overline{OE}$ returning HIGH. This two line control architecture eliminates bus contention in a system environment. The data bus will be in a high impedance state when either $\overline{OE}$ or $\overline{CE}$ is HIGH.

Write

Write operations are initiated when both $\overline{CE}$ and $\overline{WE}$ are LOW and $\overline{OE}$ is HIGH. The X28HT010 supports both a $\overline{CE}$ and $\overline{WE}$ controlled write cycle. That is, the address is latched by the falling edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs last. Similarly, the data is latched internally by the rising edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs first. A byte write operation, once initiated, will automatically continue to completion, typically within 5ms.

Page Write Operation

The page write feature of the X28HT010 allows the entire memory to be written in 5 seconds. Page write allows two to two hundred fifty-six bytes of data to be consecutively written to the X28HT010 prior to the commencement of the internal programming cycle. The host can fetch data from another device within the system during a page write operation (change the source address), but the page address (A_8 through A_{16}) for each subsequent valid write cycle to the part during this operation must be the same as the initial page address.

The page write mode can be initiated during any write operation. Following the initial byte write cycle, the host can write an additional one to two hundred fifty-six bytes in the same manner as the first byte was written. Each successive byte load cycle, started by the $\overline{WE}$ HIGH to LOW transition, must begin within 100µs of the falling edge of the preceding $\overline{WE}$. If a subsequent $\overline{WE}$ HIGH to LOW transition is not detected within 100µs, the internal automatic programming cycle will commence. There is no page write window limitation. Effectively the page write window is infinitely wide, so long as the host continues to access the device within the byte load cycle time of 100µs.

HARDWARE DATA PROTECTION

The X28HT010 provides three hardware features that protect nonvolatile data from inadvertent writes.

- Noise Protection—A $\overline{WE}$ pulse less than 10ns will not initiate a write cycle.
- Default V_{CC} Sense—All functions are inhibited when V_{CC} is ≤3.4V.
- Write inhibit—Holding either $\overline{OE}$ LOW, $\overline{WE}$ HIGH, or $\overline{CE}$ HIGH will prevent an inadvertent write cycle during power-up and power-down, maintaining data integrity.

SYSTEM CONSIDERATIONS

Because the X28HT010 is frequently used in large memory arrays it is provided with a two line control architecture for both read and write operations. Proper usage can provide the lowest possible power dissipation and eliminate the possibility of contention where multiple I/O pins share the same bus.

It has been demonstrated that markedly higher temperature performance can be obtained from this device if $\overline{CE}$ is left enabled throughout the read and write operation.

To gain the most benefit it is recommended that $\overline{CE}$ be decoded from the address bus and be used as the primary device selection input. Both $\overline{OE}$ and $\overline{WE}$ would then be common among all devices in the array. For a read operation this assures that all deselected devices are in their standby mode and that only the selected device(s) is outputting data on the bus.

Because the X28HT010 has two power modes, standby and active, proper decoupling of the memory array is of prime concern. Enabling $\overline{CE}$ will cause transient current spikes. The magnitude of these spikes is dependent on the output capacitive loading of the I/Os. Therefore, the larger the array sharing a common bus, the larger the transient spikes. The voltage peaks associated with the current transients can be suppressed by the proper selection and placement of decoupling capacitors. As a minimum, it is recommended that a 0.1µF high frequency ceramic capacitor be used between V_{CC} and V_{SS} at each device. Depending on the size of the array, the value of the capacitor may have to be larger.

In addition, it is recommended that a 4.7µF electrolytic bulk capacitor be placed between V_{CC} and V_{SS} for each eight devices employed in the array. This bulk capacitor is employed to overcome the voltage droop caused by the inductive effects of the PC board traces.

ABSOLUTE MAXIMUM RATINGS*

Temperature under Bias
X28HT010 ..... –55°C to +170°C
Voltage on any Pin with
Respect to V_{SS} ..... –1V to +7V
D.C. Output Current 5mA
Lead Temperature
(Soldering, 10 seconds) ..... 300°C

***COMMENT**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMEND OPERATING CONDITIONS

Temperature	Min.	Max.
High Temp.	–40°C	+170°C

6613 PGM T02.2

Supply Voltages	Limits
X28HT010	5V ±5%
Back Bias Voltage: v	3V ±10%

6613 PGM T03.1

D.C. OPERATING CHARACTERISTICS (Over the recommended operating conditions, unless otherwise specified.)

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
I_{CC}	V_{CC} Current (Active) (TTL Inputs)		50	mA	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}, All I/O's = Open, Address Inputs = .4V/2.4V Levels @ f = 5MHz
I_{SB1}	V_{CC} Current (Standby) (TTL Inputs)		3	mA	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IL} All I/O's = Open, Other Inputs = V_{IH}
I_{LI}	Input Leakage Current		20	µA	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output Leakage Current		20	µA	V_{OUT} = V_{SS} to V_{CC}, $\overline{CE}$ = V_{IH}
V_{IL}(1)	Input LOW Voltage	–1	0.6	V	
V_{IH}(1)	Input HIGH Voltage	2.2	V_{CC} + 1	V	
V_{OL}	Output LOW Voltage		0.5	V	I_{OL} = 1mA
V_{OH}	Output HIGH Voltage	2.6		V	I_{OH} = –400µA
I_{BB}	Back Bias Current		200	µA	V_{BB} = 3V ±10%

6613 PGM T04.2

Notes: (1) V_{IL} min. and V_{IH} max. are for reference only and are not tested.

POWER-UP TIMING

Symbol	Parameter	Max.	Units
t_{PUR}(2)	Power-up to Read Operation	100	µs
t_{PUW}(2)	Power-up to Write Operation	5	ms

6613 PGM T05

CAPACITANCE T_A = +25°C, f = 1MHz, V_{CC} = 5V

Symbol	Parameter	Max.	Units	Test Conditions
$C_{I/O}$(2)	Input/Output Capacitance	10	pF	$V_{I/O}$ = 0V
C_{IN}(2)	Input Capacitance	10	pF	V_{IN} = 0V

6613 PGM T06.1

3

ENDURANCE AND DATA RETENTION

Parameter	Min.	Max.	Units
Endurance	10,000		Cycles per Byte
Data Retention	100		Years

6613 PGM T07

A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3V
Input Rise and Fall Times	10ns
Input and Output Timing Levels	1.5V

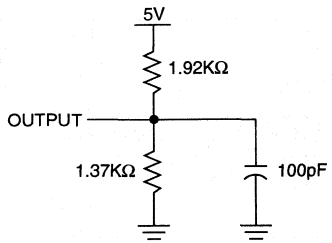
6613 PGM T08.1

MODE SELECTION

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O	Power
L	L	H	Read	D_{OUT}	Active
L	H	L	Write	D_{IN}	Active
H	X	X	Standby and Write Inhibit	High Z	Standby
X	L	X	Write Inhibit	—	—
X	X	H	Write Inhibit	—	—

6613 PGM T09

EQUIVALENT A.C. LOAD CIRCUIT



6613 FHD F04.3

SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

Note: (2) This parameter is periodically sampled and not 100% tested.

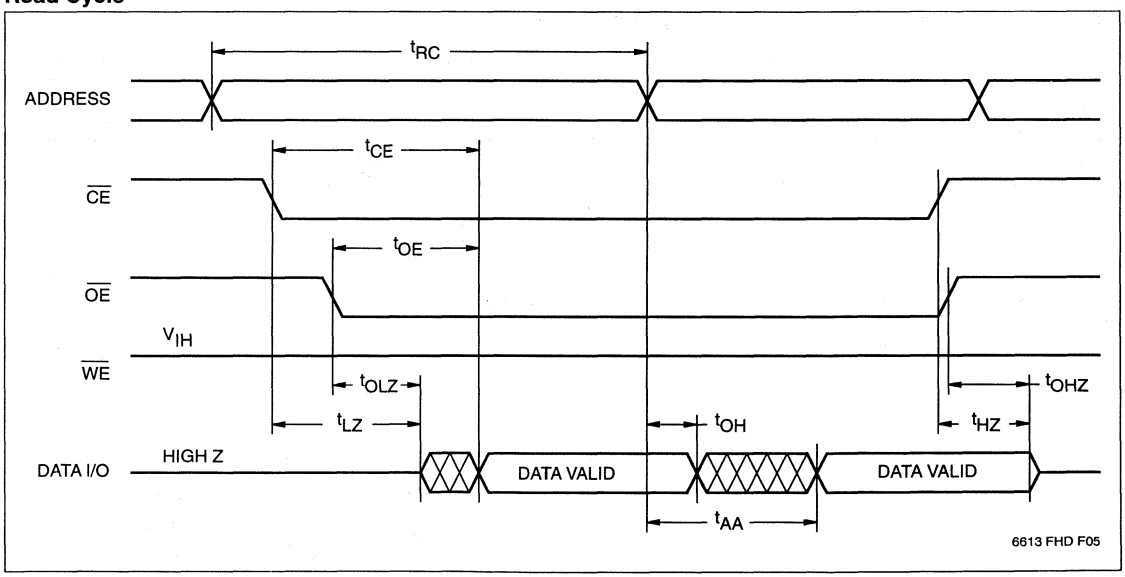
A.C. CHARACTERISTICS (Over the recommended operating conditions, unless otherwise specified.)

Read Cycle Limits

Symbol	Parameter	X28HT010-20		X28HT010-25		Units
		Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	200		250		ns
t_{CE}	Chip Enable Access Time		200		250	ns
t_{AA}	Address Access Time		200		250	ns
t_{OE}	Output Enable Access Time		50		50	ns
t_{LZ}(3)	$\overline{CE}$ LOW to Active Output	0		0		ns
t_{OLZ}(3)	$\overline{OE}$ LOW to Active Output	0		0		ns
t_{HZ}(3)	$\overline{CE}$ HIGH to High Z Output		50		50	ns
t_{OHZ}(3)	$\overline{OE}$ HIGH to High Z Output		50		50	ns
t_{OH}	Output Hold from Address Change		0		0	ns

6613 PGM T10.2

Read Cycle



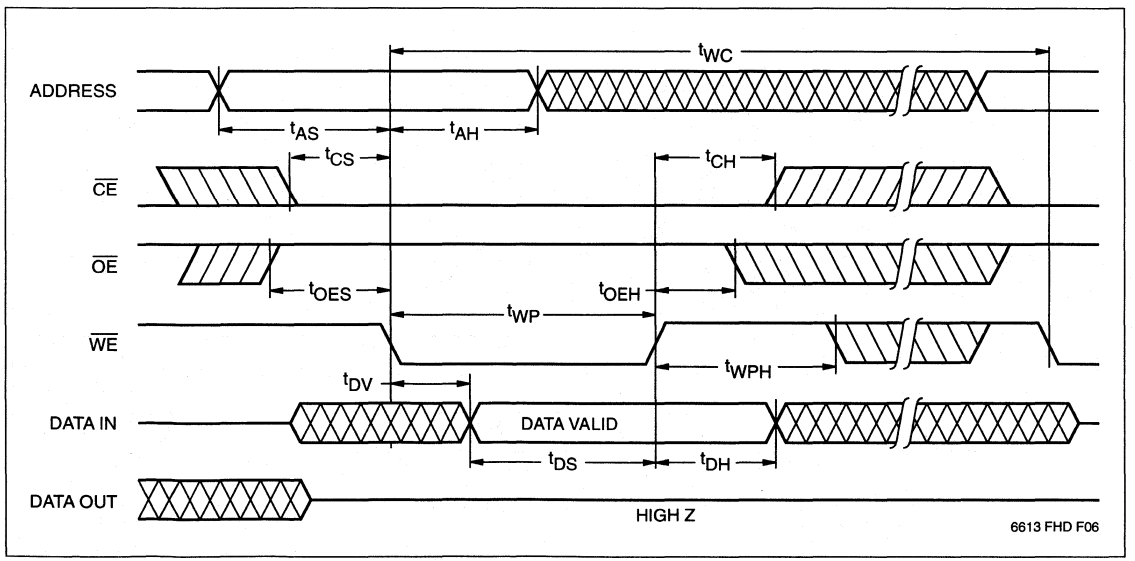
Note: (3) t_{LZ} min., t_{HZ}, t_{OLZ} min., and t_{OHZ} are periodically sampled and not 100% tested. t_{HZ} max. and t_{OHZ} max. are measured, with C_L = 5pF, from the point when $\overline{CE}$ or $\overline{OE}$ return HIGH (whichever occurs first) to the time when the outputs are no longer driven.

Write Cycle Limits

Symbol	Parameter	Min.	Max.	Units
t_{WC}(4)	Write Cycle Time		10	ms
t_{AS}	Address Setup Time	20		ns
t_{AH}	Address Hold Time	100		ns
t_{CS}	Write Setup Time	0		ns
t_{CH}	Write Hold Time	0		ns
t_{CW}	$\overline{CE}$ Pulse Width	200		ns
t_{OES}	$\overline{OE}$ HIGH Setup Time	10		ns
t_{OEH}	$\overline{OE}$ HIGH Hold Time	10		ns
t_{WP}	$\overline{WE}$ Pulse Width	200		ns
t_{WPH}	$\overline{WE}$ HIGH Recovery	200		ns
t_{DV}	Data Valid		1	µs
t_{DS}	Data Setup	100		ns
t_{DH}	Data Hold	25		ns
t_{DW}	Delay to Next Write	10		µs
t_{BLC}	Byte Load Cycle	0.4	100	µs

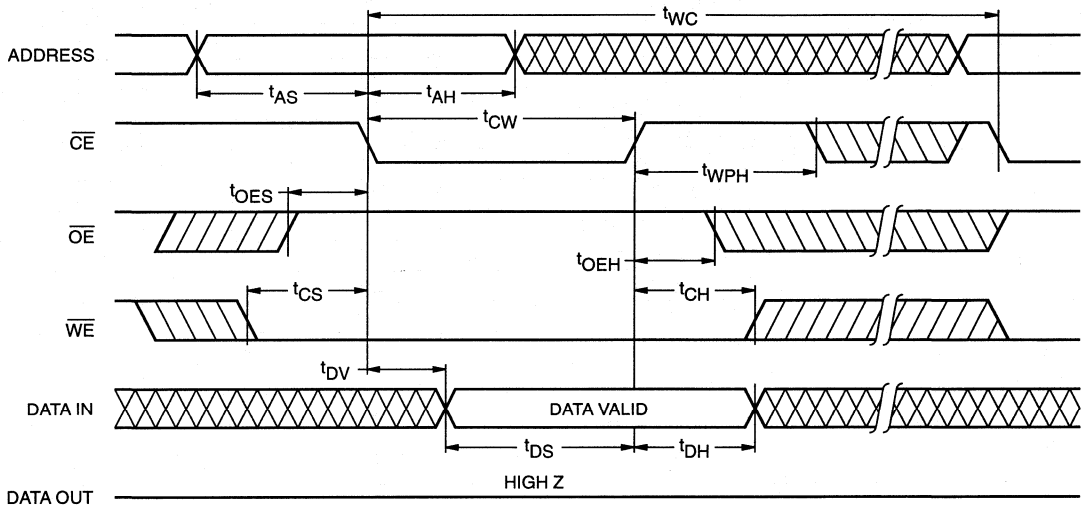
6613 PGM T11.1

$\overline{WE}$ Controlled Write Cycle

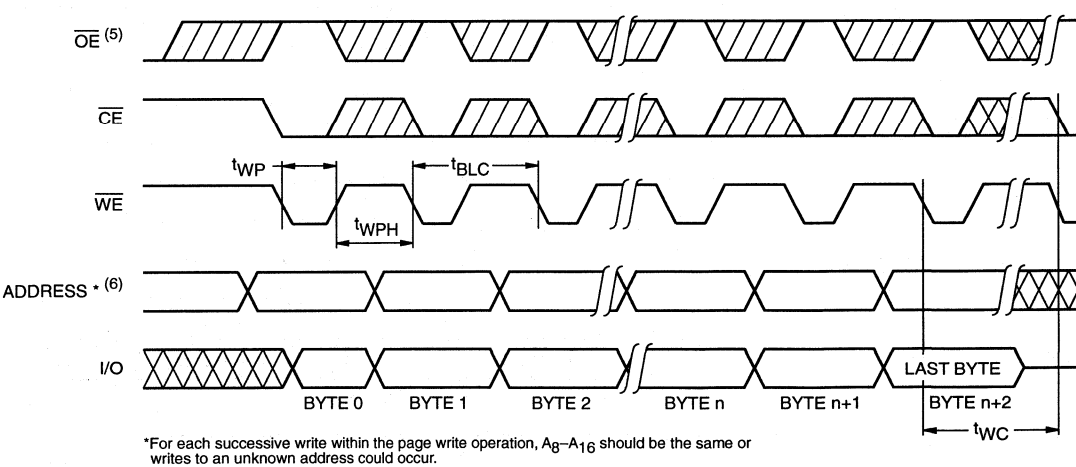


Notes: (4) t_{WC} is the minimum cycle time to be allowed from the system perspective unless polling techniques are used. It is the maximum time the device requires to complete internal write operation.

$\overline{CE}$ Controlled Write Cycle



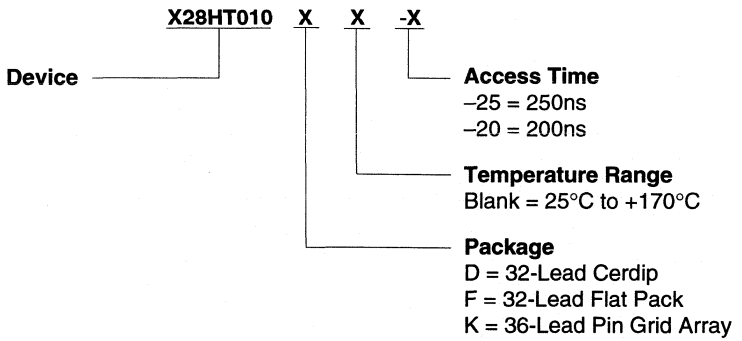
Page Write Cycle



Notes: (5) Between successive byte writes within a page write operation, $\overline{OE}$ can be strobed LOW: e.g. this can be done with $\overline{CE}$ and $\overline{WE}$ HIGH to fetch data from another memory device within the system for the next write; or with $\overline{WE}$ HIGH and $\overline{CE}$ LOW effectively performing a polling operation.

(6) The timings shown above are unique to page write operations. Individual byte load operations within the page write must conform to either the $\overline{CE}$ or $\overline{WE}$ controlled write cycle timing.

ORDERING INFORMATION



NOTES

Xicor®

3807-2.3 12/4/95 T12/C0/D0 NS

Terminal Voltage ±5V, 100 Taps

X9C102/103/104/503

E²POT™ Nonvolatile Digital Potentiometer

FEATURES

- **Compatible with X9102/103/104/503**
- **Low Power CMOS**
  - **—V_{CC} = 3V to 5.5V**
  - **—Active Current, 3mA Max**
  - **—Standby Current, 500μA Max**
- **99 Resistive Elements**
  - **—Temperature Compensated**
  - **—± 20% End to End Resistance Range**
- **100 Wiper Tap Points**
  - **—Wiper Positioned via Three-Wire Interface**
  - **—Similar to TTL Up/Down Counter**
  - **—Wiper Position Stored in Nonvolatile Memory and Recalled on Power-Up**
- **100 Year Wiper Position Data Retention**
- **X9C102 = 1KΩ**
- **X9C103 = 10KΩ**
- **X9C503 = 50KΩ**
- **X9C104 = 100KΩ**

DESCRIPTION

The Xicor X9C102/103/104/503 is a solid state nonvolatile potentiometer and is ideal for digitally controlled resistance trimming.

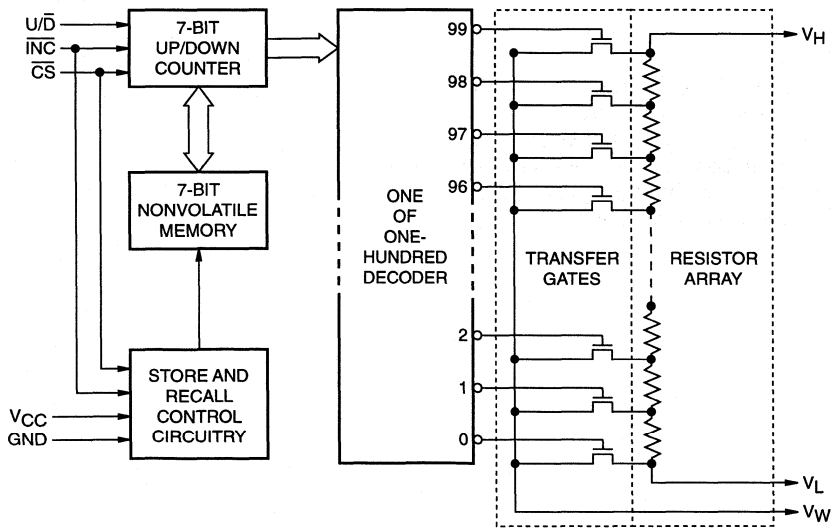
The X9C102/103/104/503 is a resistor array composed of 99 resistive elements. Between each element and at either end are tap points accessible to the wiper element. The position of the wiper element is controlled by the $\overline{CS}$, U/$\overline{D}$, and $\overline{INC}$ inputs. The position of the wiper can be stored in nonvolatile memory and then be recalled upon a subsequent power-up operation.

The resolution of the X9C102/103/104/503 is equal to the maximum resistance value divided by 99. As an example, for the X9C503 (50KΩ) each tap point represents 505Ω.

All Xicor nonvolatile memories are designed and tested for applications requiring extended endurance and data retention.

4

FUNCTIONAL DIAGRAM



3863 FHD F01

E²POT™ is a trademark of Xicor, Inc.

PIN DESCRIPTIONS

V_H and V_L

The high (V_H) and low (V_L) terminals of the X9C102/103/104/503 are equivalent to the fixed terminals of a mechanical potentiometer. The minimum voltage is –5V and the maximum is +5V. It should be noted that the terminology of V_L and V_H references the relative position of the terminal in relation to wiper movement direction selected by the U/$\overline{D}$ input and not the voltage potential on the terminal.

V_W

V_W is the wiper terminal, equivalent to the movable terminal of a mechanical potentiometer. The position of the wiper within the array is determined by the control inputs. The wiper terminal series resistance is typically 40Ω.

Up/Down (U/$\overline{D}$)

The U/$\overline{D}$ input controls the direction of the wiper movement and whether the counter is incremented or decremented.

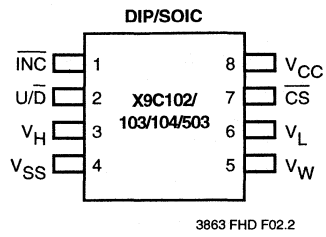
Increment ($\overline{INC}$)

The $\overline{INC}$ input is negative-edge triggered. Toggling $\overline{INC}$ will move the wiper and either increment or decrement the counter in the direction indicated by the logic level on the U/$\overline{D}$ input.

Chip Select ($\overline{CS}$)

The device is selected when the $\overline{CS}$ input is LOW. The current counter value is stored in nonvolatile memory when $\overline{CS}$ is returned HIGH while the $\overline{INC}$ input is also HIGH. After the store operation is complete the X9C102/103/104/503 will be placed in the low power standby mode until the device is selected once again.

PIN CONFIGURATION



3863 FHD F02.2

PIN NAMES

Symbol	Description
V_H	High Terminal
V_W	Wiper Terminal
V_L	Low Terminal
V_{SS}	Ground
V_{CC}	Supply Voltage
U/$\overline{D}$	Up/Down Input
$\overline{INC}$	Increment Input
$\overline{CS}$	Chip Select Input
NC	No Connect

3863 PGM T01

DEVICE OPERATION

There are three sections of the X9C102/103/104/503: the input control, counter and decode section; the nonvolatile memory; and the resistor array. The input control section operates just like an up/down counter. The output of this counter is decoded to turn on a single electronic switch connecting a point on the resistor array to the wiper output. Under the proper conditions the contents of the counter can be stored in nonvolatile memory and retained for future use. The resistor array is comprised of 99 individual resistors connected in series. At either end of the array and between each resistor is an electronic switch that transfers the potential at that point to the wiper.

The $\overline{INC}$, U/$\overline{D}$ and $\overline{CS}$ inputs control the movement of the wiper along the resistor array. With $\overline{CS}$ set LOW the X9C102/103/104/503 is selected and enabled to respond to the U/$\overline{D}$ and $\overline{INC}$ inputs. HIGH to LOW transitions on $\overline{INC}$ will increment or decrement (depending on the state of the U/$\overline{D}$ input) a seven-bit counter. The output of this counter is decoded to select one of one-hundred wiper positions along the resistive array.

The wiper, when at either fixed terminal, acts like its mechanical equivalent and does not move beyond the last position. That is, the counter does not wrap around when clocked to either extreme.

The value of the counter is stored in nonvolatile memory whenever $\overline{CS}$ transistions HIGH while the $\overline{INC}$ input is also HIGH.

When the X9C102/103/104/503 is powered-down, the last counter position stored will be maintained in the nonvolatile memory. When power is restored, the contents of the memory are recalled and the counter is reset to the value last stored.

OPERATION NOTES

The system may select the X9C102/103/104/503, move the wiper, and deselect the device without having to store the latest wiper, position in nonvolatile memory. The wiper movement is performed as described above; once the new position is reached, the system would the keep $\overline{INC}$ LOW while taking $\overline{CS}$ HIGH. The new wiper position would be maintained until changed by the system or until a power-down/up cycle recalled the previously stored data.

This would allow the system to always power-up to a preset value stored in nonvolatile memory; then during system operation minor adjustments could be made. The adjustments might be based on user preference: system parameter changes due to temperature drift, etc...

The state of U/$\overline{D}$ may be changed while $\overline{CS}$ remains LOW. This allows the host system to enable the X9C102/103/104/503 and then move the wiper up and down until the proper trim is attained.

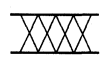
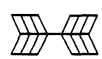
T_{IW}/R_{TOTAL}

The electronic switches on the X9C102/103/104/503 operate in a "make before break" mode when the wiper changes tap positions. If the wiper is moved several positions, multiple taps are connected to the wiper for t_{IW} ($\overline{INC}$ to V_W change). The R_{TOTAL} value for the device can temporarily be reduced by a significant amount if the wiper is moved several positions.

R_{TOTAL} with V_{CC} Removed

The end to end resistance of the array will fluctuate once V_{CC} is removed.

SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

ABSOLUTE MAXIMUM RATINGS*

Temperature under Bias ..... –65°C to +135°C
Storage Temperature ..... –65°C to +150°C
Voltage on $\overline{CS}$, $\overline{INC}$, U/$\overline{D}$ and V_{CC}
with Respect to V_{SS} ..... –1V to +7V
Voltage on V_H and V_L
Referenced to V_{SS} ..... –8V to +8V
$\Delta V = |V_H - V_L|$
X9C102 ..... 4V
X9C103, X9C503, and X9C104 ..... 10V
Lead Temperature (Soldering, 10 seconds) ... +300°C
Wiper Current ..... ±1mA

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ANALOG CHARACTERISTICS

Electrical Characteristics

End-to-End Resistance Tolerance ..... ±20%
Power Rating at 25°C
X9C102 ..... 16mW
X9C103, X9C503, and X9C104 ..... 10mW
Wiper Current ..... ±1mA Max.
Typical Wiper Resistance ..... 40Ω at 1mA
Typical Noise ..... < –120dB/√Hz Ref: 1V

Resolution

Resistance 1%

Linearity

Absolute Linearity(1) ..... ±1.0 MI(2)
Relative Linearity(3) ..... ±0.2 MI(2)

Temperature Coefficient

(–40°C to +85°C)
X9C102 ..... +600 ppm/°C Typical
X9C103, X9C503, X9C104 ..... +300 ppm/°C Typical
Ratiometric Temperature Coefficient ..... ±20 ppm

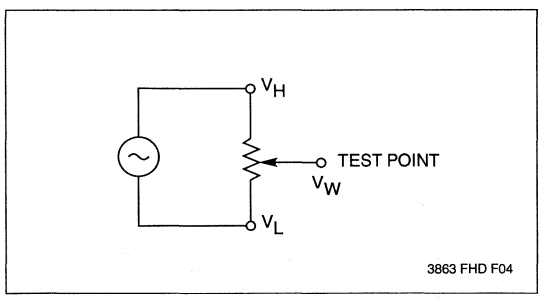
Wiper Adjustability

Unlimited Wiper Adjustment (Non-Store operation)
Wiper Position Store Operations 10,000
Data Changes

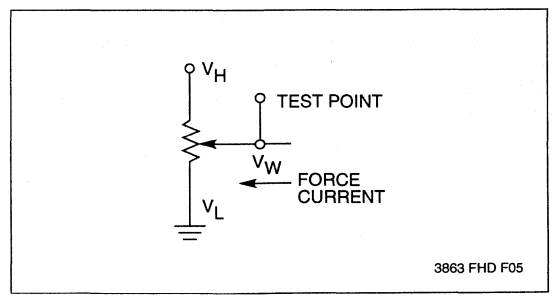
Physical Characteristics

Marking Includes
Manufacturer's Trademark
Resistance Value or Code
Date Code

Test Circuit #1



Test Circuit #2



Notes: (1) Absolute Linearity is utilized to determine actual wiper voltage versus expected voltage = ($V_{W(n)}$(actual) – $V_{W(n)}$(expected)) = ±1 MI Maximum.
(2) 1 MI = Minimum Increment = R_{TOT}/99.
(3) Relative Linearity is a measure of the error in step size between taps = $V_{W(n+1)} - [V_{W(n)} + MI] = +0.2$ MI.

RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	+70°C
Industrial	–40°C	+85°C
Military	–55°C	+125°C

3863 PGM T03.1

Supply Voltage	Limits
X9C102/103/104/503	5V ±10%
X9C102/103/104/503–3	3V to 5.5V

3863 PGM T04.2

D.C. OPERATING CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.(4)	Max.		
I_{CC}	V_{CC} Active Current		1	3	mA	$\overline{CS}$ = V_{IL}, U/$\overline{D}$ = V_{IL} or V_{IH} and $\overline{INC}$ = 0.4V to 2.4V @ max. t_{CYC}
I_{SB}	Standby Supply Current		200	500	µA	$\overline{CS}$ = V_{CC} – 0.3V, U/$\overline{D}$ and $\overline{INC}$ = V_{SS} or V_{CC} – 0.3V
I_{LI}	$\overline{CS}$, $\overline{INC}$, U/$\overline{D}$ Input Leakage Current			±10	µA	V_{IN} = V_{SS} to V_{CC}
V_{IH}	$\overline{CS}$, $\overline{INC}$, U/$\overline{D}$ Input HIGH Voltage	2		V_{CC} + 1	V	
V_{IL}	$\overline{CS}$, $\overline{INC}$, U/$\overline{D}$ Input LOW Voltage	–1		0.8	V	
R_W	Wiper Resistence		40	100	Ω	Max. Wiper Current ±1mA
V_H	VH Terminal Voltage	–5		+5	V	
V_L	VL Terminal Voltage	–5		+5	V	
C_{IN}(5)	$\overline{CS}$, $\overline{INC}$, U/$\overline{D}$ Input Capacitance			10	pF	V_{CC} = 5V, V_{IN} = V_{SS}, T_A = 25°C, f = 1MHz

3863 PGM T05.3

STANDARD PARTS

Part Number	Maximum Resistance	Wiper Increments	Minimum Resistance
X9C102	1KΩ	10.1Ω	40Ω
X9C103	10KΩ	101Ω	40Ω
X9C503	50KΩ	505Ω	40Ω
X9C104	100KΩ	1010Ω	40Ω

3863 PGM T08.1

Notes: (4) Typical values are for T_A = 25°C and nominal supply voltage.
(5) This parameter is periodically sampled and not 100% tested.

A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3V
Input Rise and Fall Times	10ns
Input Reference Levels	1.5V

3863 PGM T05.1

MODE SELECTION

$\overline{CS}$	$\overline{INC}$	U/$\overline{D}$	Mode
L	↓	H	Wiper Up
L	↓	L	Wiper Down
↑	H	X	Store Wiper Position
H	X	X	Standby Current
↑	L	X	No Store, Return to Standby

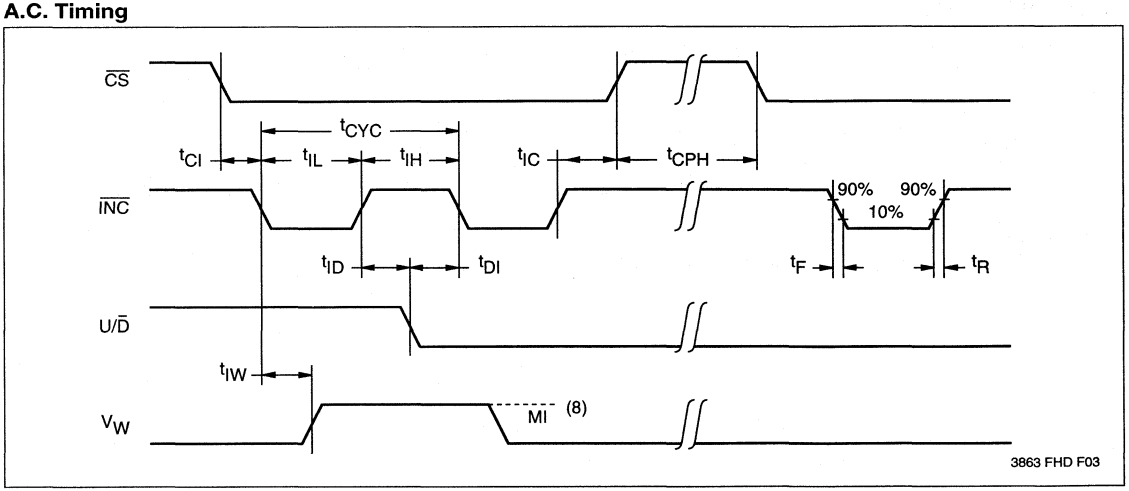
3863 PGM T06

A.C. OPERATING CHARACTERISTICS (Over recommended operating conditions unless otherwise specified)

Symbol	Parameter	Limits			Units
		Min.	Typ.(6)	Max.	
t_{CI}	$\overline{CS}$ to $\overline{INC}$ Setup	100			ns
t_{ID}	$\overline{INC}$ HIGH to U/$\overline{D}$ Change	100			ns
t_{DI}	U/$\overline{D}$ to $\overline{INC}$ Setup	2.9			µs
t_{IL}	$\overline{INC}$ LOW Period	1			µs
t_{IH}	$\overline{INC}$ HIGH Period	1			µs
t_{IC}	$\overline{INC}$ Inactive to $\overline{CS}$ Inactive	1			µs
t_{CPH}	$\overline{CS}$ Deselect Time	20			ms
t_{IW}	$\overline{INC}$ to Vw Change		100	500	µs
t_{CYC}	$\overline{INC}$ Cycle Time	4			µs
t_R, t_F(7)	$\overline{INC}$ Input Rise and Fall Time			500	µs
t_{PU}(7)	Power up to Wiper Stable			500	µs
t_R V_{CC}(7)	V_{CC} Power-up Rate	0.2		50	mV/µs

3863 PGM T07.3

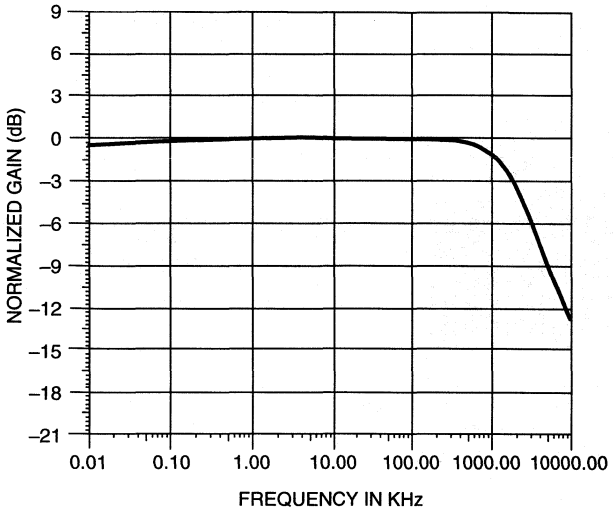
A.C. Timing



3863 FHD F03

Notes: (6) Typical values are for T_A = 25°C and nominal supply voltage.
(7) This parameter is periodically sampled and not 100% tested.
(8) MI in the A.C. timing diagram refers to the minimum incremental change in the V_W output due to a change in the wiper position.

Typical Frequency Response for X9C102

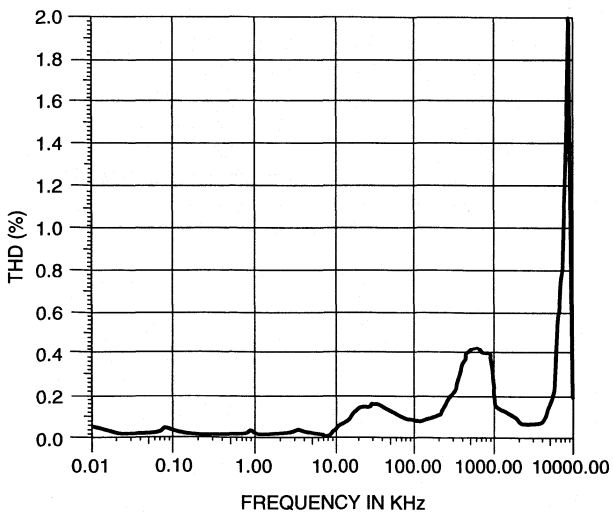


TEST CONDITIONS
V_{CC} = 5V
Temp. = 25°C
Wiper @ Tap 50
$V_H = 0.5V_{RMS}$
Normalized (0dB @ 1KHz)
Test Circuit #1

3863 FHD F06

4

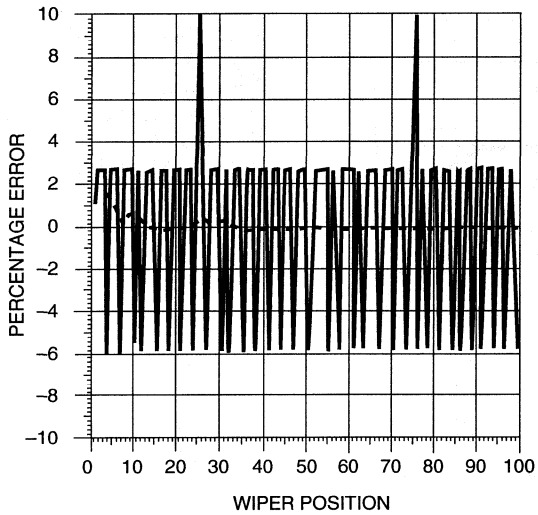
Typical Total Harmonic Distortion for X9C102



TEST CONDITIONS
V_{CC} = 5V
Temp. = 25°C
Wiper @ Tap 50
$V_H = 2V_{RMS}$
Test Circuit #1

3863 FHD F07

Typical Linearity for X9C102

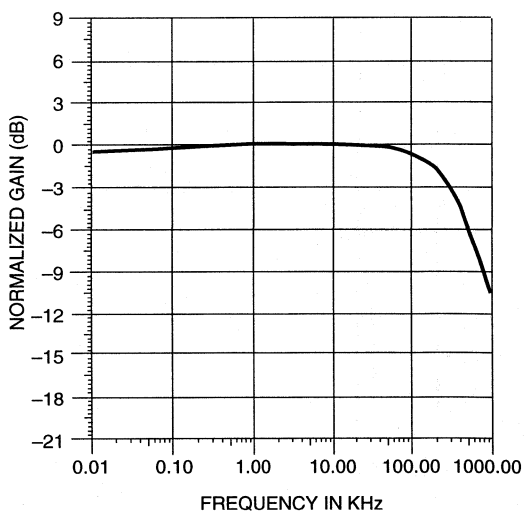


TEST CONDITIONS
V_{CC} = 5V
Temp. = 25°C
Test Circuit #2

KEY:
- - - - - - - = ABSOLUTE
——— = RELATIVE

3863 FHD F08

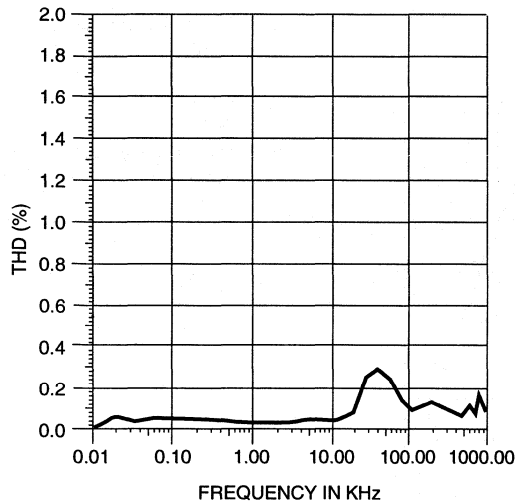
Typical Frequency Response for X9C103



TEST CONDITIONS
V_{CC} = 5V
Temp. = 25°C
Wiper @ Tap 50
$V_H = 0.5V_{RMS}$
Normalized (0dB @ 1KHz)
Test Circuit #1

3863 FHD F09

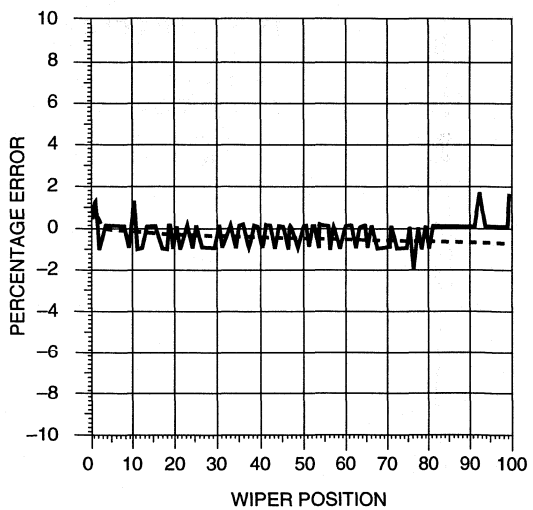
Typical Total Harmonic Distortion for X9C103



TEST CONDITIONS
V_{CC} = 5V
Temp. = 25°C
Wiper @ Tap 50
$V_H = 2V_{RMS}$
Test Circuit #1

3863 FHD F10

Typical Linearity for X9C103

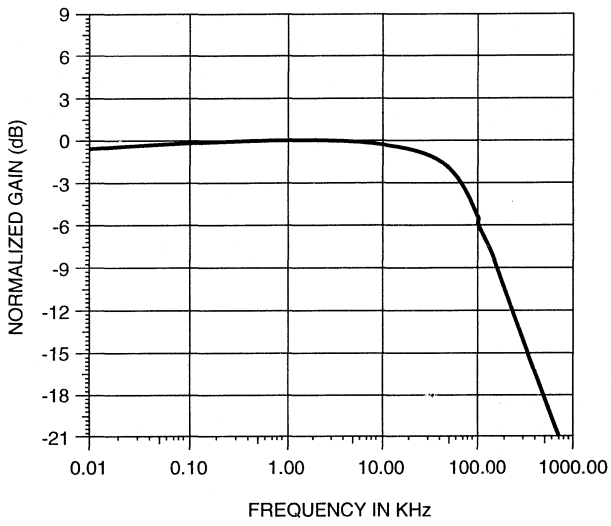


TEST CONDITIONS
V_{CC} = 5V
Temp. = 25°C
Test Circuit #2

KEY:
- - - - - - - = ABSOLUTE
——— = RELATIVE

3863 FHD F11

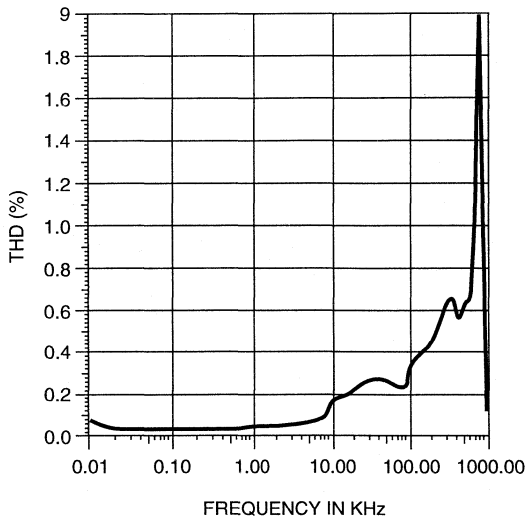
Typical Frequency Response for X9C503



TEST CONDITIONS
V_{CC} = 5V
Temp. = 25°C
Wiper @ Tap 50
$V_H = 0.5V_{RMS}$
Normalized (0dB @ 1 KHz)
Test Circuit #1

3863 FHD F12

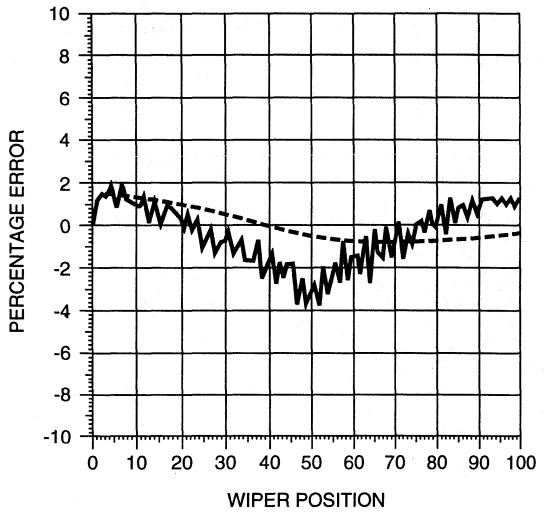
Typical Total Harmonic Distortion for X9C503



TEST CONDITIONS
V_{CC} = 5V
Temp. = 25°C
Wiper @ Tap 50
$V_H = 2V_{RMS}$
Test Circuit #1

3863 FHD F13

Typical Linearity for X9C503

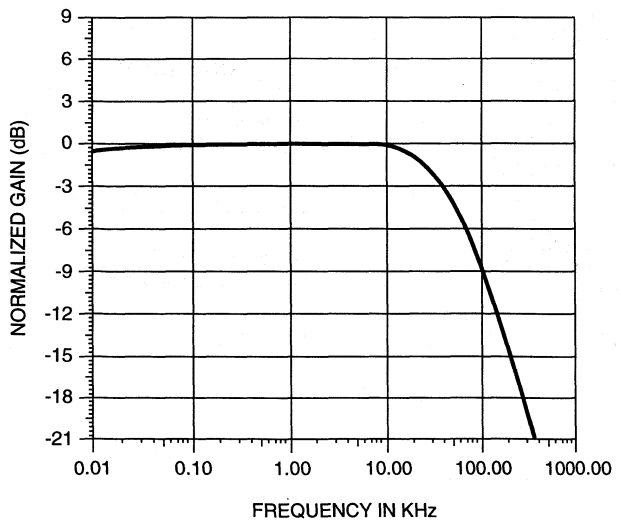


TEST CONDITIONS
V_{CC} = 5V
Temp. = 25°C
Test Circuit #2

KEY:
- - - - - - - = ABSOLUTE
——— = RELATIVE

3863 FHD F14

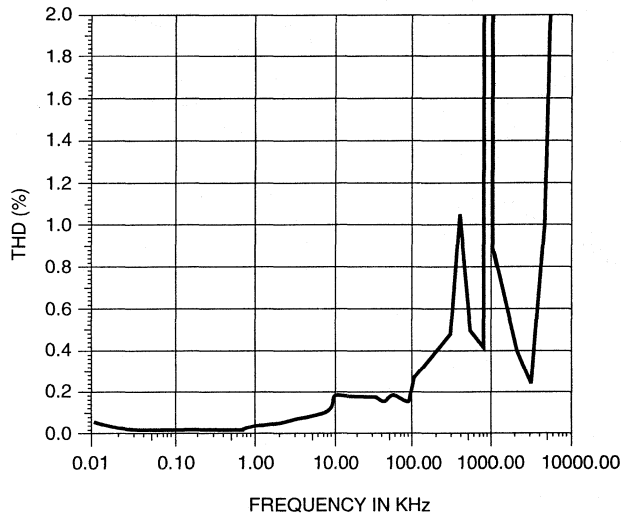
Typical Frequency Response for X9C104



TEST CONDITIONS
V_{CC} = 5V
Temp. = 25°C
Wiper @ Tap 50
$V_H = 0.5V_{RMS}$
Normalized (0dB @ 1 KHz)
Test Circuit #1

3863 FHD F15

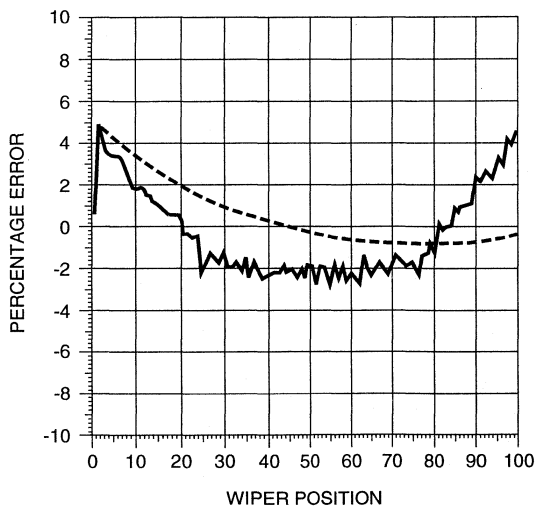
Typical Total Harmonic Distortion for X9C104



TEST CONDITIONS
V_{CC} = 5V
Temp. = 25°C
Wiper @ Tap 50
$V_H = 2V_{RMS}$
Test Circuit #1

3863 FHD F16

Typical Linearity for X9C104

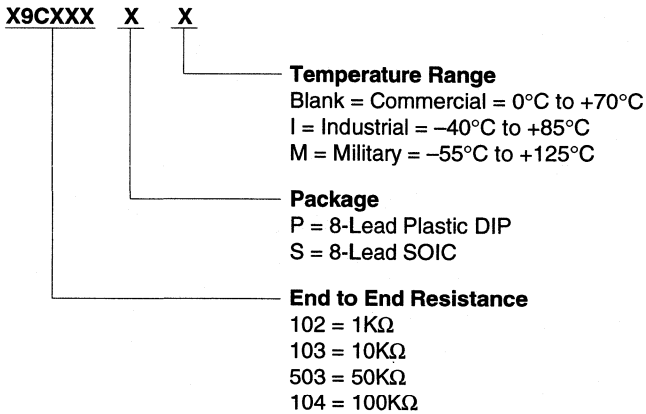


TEST CONDITIONS
V_{CC} = 5V
Temp. = 25°C
Test Circuit #2

KEY:
- - - - - - - = ABSOLUTE
——— = RELATIVE

3863 FHD F17

ORDERING INFORMATION



NOTES

Terminal Voltage 0V to +15V, 100 Taps

X9312

E²POT™ Nonvolatile Digital Potentiometer

FEATURES

- Compatible with X9C102/103/104/503
- Low Power CMOS
  - —Active Current, 3mA Max
  - —Standby Current, 1mA Max
- 99 Resistive Elements
  - —Temperature Compensated
  - —±20% End to End Resistance Range
  - — 0 to +15V Range
- 100 Wiper Tap Points
  - —Wiper Positioned via Three-Wire Interface
  - —Similar to TTL Up/Down Counter
  - —Wiper Position Stored in Nonvolatile Memory and Recalled on Power-Up
- 100 Year Wiper Position Data Retention
- X9312Z = 1KΩ
- X9312W = 10KΩ
- X9312U = 50KΩ
- X9312T = 100KΩ

DESCRIPTION

The Xicor X9312 is a solid state nonvolatile potentiometer and is ideal for digitally controlled resistance trimming.

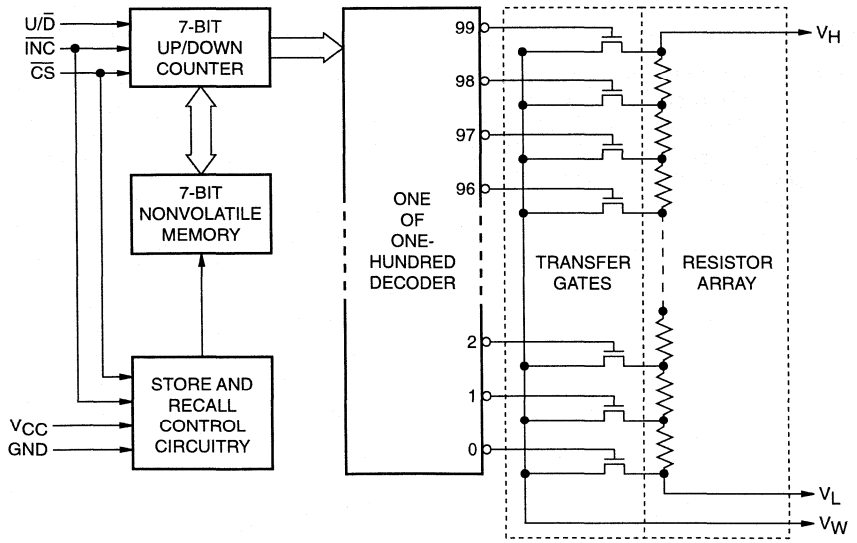
The X9312 is a resistor array composed of 99 resistive elements. Between each element and at either end are tap points accessible to the wiper element. The position of the wiper element is controlled by the $\overline{CS}$, U/$\overline{D}$, and $\overline{INC}$ inputs. The position of the wiper can be stored in nonvolatile memory and then be recalled upon a subsequent power-up operation.

The resolution of the X9312 is equal to the maximum resistance value divided by 99. As an example, for the X9312U (50KΩ) each tap point represents 505Ω.

All Xicor nonvolatile memories are designed and tested for applications requiring extended endurance and data retention.

4

FUNCTIONAL DIAGRAM



3865 FHD F01

E²POT™ is a trademark of Xicor, Inc.

PIN DESCRIPTIONS

V_H and V_L

The high (V_H) and low (V_L) terminals of the X9312 are equivalent to the fixed terminals of a mechanical potentiometer. The minimum voltage is 0V and the maximum is +15V. It should be noted that the terminology of V_L and V_H references the relative position of the terminal in relation to wiper movement direction selected by the U/$\overline{D}$ input and not the voltage potential on the terminal.

V_W

Vw is the wiper terminal, equivalent to the movable terminal of a mechanical potentiometer. The position of the wiper within the array is determined by the control inputs. The wiper terminal series resistance is typically 40Ω.

Up/Down (U/$\overline{D}$)

The U/$\overline{D}$ input controls the direction of the wiper movement and whether the counter is incremented or decremented.

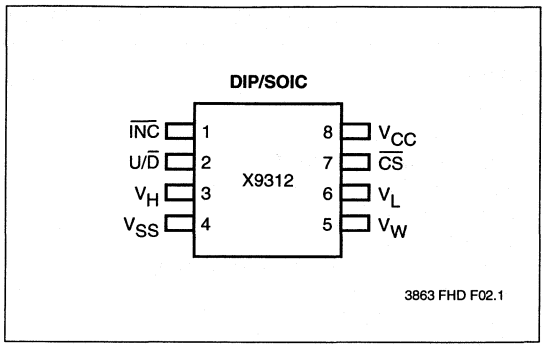
Increment ($\overline{INC}$)

The $\overline{INC}$ input is negative-edge triggered. Toggling $\overline{INC}$ will move the wiper and either increment or decrement the counter in the direction indicated by the logic level on the U/$\overline{D}$ input.

Chip Select ($\overline{CS}$)

The device is selected when the $\overline{CS}$ input is LOW. The current counter value is stored in nonvolatile memory when $\overline{CS}$ is returned HIGH while the $\overline{INC}$ input is also HIGH. After the store operation is complete the X9312 will be placed in the low power standby mode until the device is selected once again.

PIN CONFIGURATION



3863 FHD F02.1

PIN NAMES

Symbol	Description
V_H	High Terminal
V_W	Wiper Terminal
V_L	Low Terminal
V_{SS}	Ground
V_{CC}	Supply Voltage
U/$\overline{D}$	Up/Down Input
$\overline{INC}$	Increment Input
$\overline{CS}$	Chip Select Input

3865 PGM T01

DEVICE OPERATION

There are three sections of the X9312: the input control, counter and decode section; the nonvolatile memory; and the resistor array. The input control section operates just like an up/down counter. The output of this counter is decoded to turn on a single electronic switch connecting a point on the resistor array to the wiper output. Under the proper conditions the contents of the counter can be stored in nonvolatile memory and retained for future use. The resistor array is comprised of 99 individual resistors connected in series. At either end of the array and between each resistor is an electronic switch that transfers the potential at that point to the wiper.

The $\overline{INC}$, U/$\overline{D}$ and $\overline{CS}$ inputs control the movement of the wiper along the resistor array. With $\overline{CS}$ set LOW the X9312 is selected and enabled to respond to the U/D and $\overline{INC}$ inputs. HIGH to LOW transitions on $\overline{INC}$ will increment or decrement (depending on the state of the U/$\overline{D}$ input) a seven bit counter. The output of this counter is decoded to select one of one-hundred wiper positions along the resistive array.

The wiper, when at either fixed terminal, acts like its mechanical equivalent and does not move beyond the last position. That is, the counter does not wrap around when clocked to either extreme.

The value of the counter is stored in nonvolatile memory whenever $\overline{CS}$ transistions HIGH while the $\overline{INC}$ input is also HIGH.

When the X9312 is powered-down, the last counter position stored will be maintained in the nonvolatile memory. When power is restored, the contents of the memory are recalled and the counter is reset to the value last stored.

Operation Notes

The system may select the X9312, move the wiper and deselect the device without having to store the latest wiper position in nonvolatile memory. The wiper movement is performed as described above; once the new position is reached, the system would the keep $\overline{INC}$ LOW while taking $\overline{CS}$ HIGH. The new wiper position would be maintained until changed by the system or until a power-up/down cycle recalled the previously stored data.

This would allow the system to always power-up to a preset value stored in nonvolatile memory; then during system operation minor adjustments could be made. The adjustments might be based on user preference, system parameter changes due to temperature drift, etc...

The state of U/$\overline{D}$ may be changed while $\overline{CS}$ remains LOW. This allows the host system to enable the X9312 and then move the wiper up and down until the proper trim is attained.

T_{IW}/R_{TOTAL}

The electronic switches on the X9312 operate in a "make before break" mode when the wiper changes tap positions. If the wiper is moved several positions multiple taps are connected to the wiper for t_{IW} ($\overline{INC}$ to V_W change). The R_{TOTAL} value for the device can temporarily be reduced by a significant amount if the wiper is moved several positions.

R_{TOTAL} with V_{CC} Removed

The end to end resistance of the array will fluctuate once V_{CC} is removed.

SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

ABSOLUTE MAXIMUM RATINGS*

Temperature under Bias ..... –65°C to +135°C
Storage Temperature ..... –65°C to +150°C
Voltage on $\overline{CS}$, $\overline{INC}$, U/$\overline{D}$ and V_{CC}
with Respect to V_{SS} ..... –1V to +7V
Voltage on V_H and V_L Referenced to V_{SS}
$\Delta V = |V_H - V_L|$
X9312Z, X9312W, X9312U, and X9312T 15V
Lead Temperature (Soldering 10 seconds) ..... 300°C
Wiper Current ..... ±1mA

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ANALOG CHARACTERISTICS

Electrical Characteristics

End-to-End Resistance Tolerance ..... ±20%
Power Rating at 25°C
X9312Z, ... 225mW
X9312W, X9312U, and X9312T 25mW
Wiper Current ..... ±1mA Max.
Typical Wiper Resistance ..... 40Ω at 1mA
Typical Noise ..... < –120dB/√Hz Ref: 1V

Resolution

Resistance 1%

Linearity

Absolute Linearity(1) ..... ±1.0 MI(2)
Relative Linearity(3) ..... ±0.2 MI(2)

Temperature Coefficient

(–40°C to +85°C)
X9312W, X9312U and
X9312T ..... +300 ppm/°C Typical
Ratiometric Temperature Coefficient ..... ±20 ppm

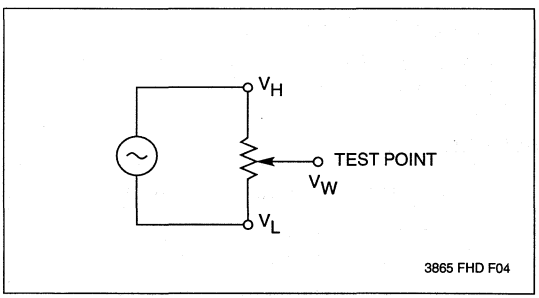
Wiper Adjustability

Unlimited Wiper Adjustment (Non-Store operation)
Wiper Position Store Operations 10,000
Data Changes

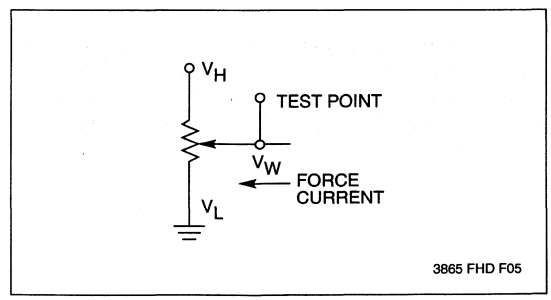
Physical Characteristics

Marking Includes
Manufacturer's Trademark
Resistance Value or Code
Date Code

Test Circuit #1



Test Circuit #2



Notes: (1) Absolute Linearity is utilized to determine actual wiper voltage versus expected voltage
= ($V_{w(n)}$(actual) – $V_{w(n)}$(expected)) = ±1 MI Maximum.
(2) 1 MI = Minimum Increment = R_{TOT}/99.
(3) Relative Linearity is a measure of the error in step size between taps = $V_{W(n+1)} - [V_{w(n)} + MI] = +0.2$ MI.

RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	+70°C
Industrial	–40°C	+85°C
Military	–55°C	+125°C

3865 PGM T03.1

Supply Voltage	Limits
X9312	5V ±10%

3865 PGM T04.1

D.C. OPERATING CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.(4)	Max.		
I_{CC}	V_{CC} Active Current		1	3	mA	$\overline{CS}$ = V_{IL}, U/$\overline{D}$ = V_{IL} or V_{IH} and $\overline{INC}$ = 0.4V/2.4V @ max. t_{CYC}
I_{SB}	Standby Supply Current		500	1000	µA	$\overline{CS}$ = V_{CC} – 0.3V, U/$\overline{D}$ and $\overline{INC}$ = V_{SS} or V_{CC} – 0.3V
I_{LI}	$\overline{CS}$, $\overline{INC}$, U/$\overline{D}$ Input Leakage Current			±10	µA	V_{IN} = V_{SS} to V_{CC}
V_{IH}	$\overline{CS}$, $\overline{INC}$, U/$\overline{D}$ Input HIGH Voltage	2		V_{CC} + 1	V	
V_{IL}	$\overline{CS}$, $\overline{INC}$, U/$\overline{D}$ Input LOW Voltage	–1		0.8	V	
R_W	Wiper Resistence		40	100	Ω	Max. Wiper Current ±1mA
V_{VH}	VH Terminal Voltage	0		15	V	
V_{VL}	VL Terminal Voltage	0		15	V	
C_{IN}(5)	$\overline{CS}$, $\overline{INC}$, U/$\overline{D}$ Input Capacitance			10	pF	V_{CC} = 5V, V_{IN} = V_{SS}, T_A = 25°C, f = 1MHz

3865 PGM T05.3

STANDARD PARTS

Part Number	Maximum Resistance	Wiper Increments	Minimum Resistance
X9312Z	1KΩ	10.1Ω	40Ω
X9312W	10KΩ	101Ω	40Ω
X9312U	50KΩ	505Ω	40Ω
X9312T	100KΩ	1010Ω	40Ω

3865 PGM T08.1

Notes: (4) Typical values are for T_A = 25°C and nominal supply voltage.
(5) This parameter is periodically sampled and not 100% tested.

A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3V
Input Rise and Fall Times	10ns
Input Reference Levels	1.5V

3865 PGM T05.1

MODE SELECTION

$\overline{CS}$	$\overline{INC}$	U/$\overline{D}$	Mode
L	↘	H	Wiper Up
L	↘	L	Wiper Down
∫	H	X	Store Wiper Position
H	X	X	Standby
∫	L	X	No Store, Return to Standby

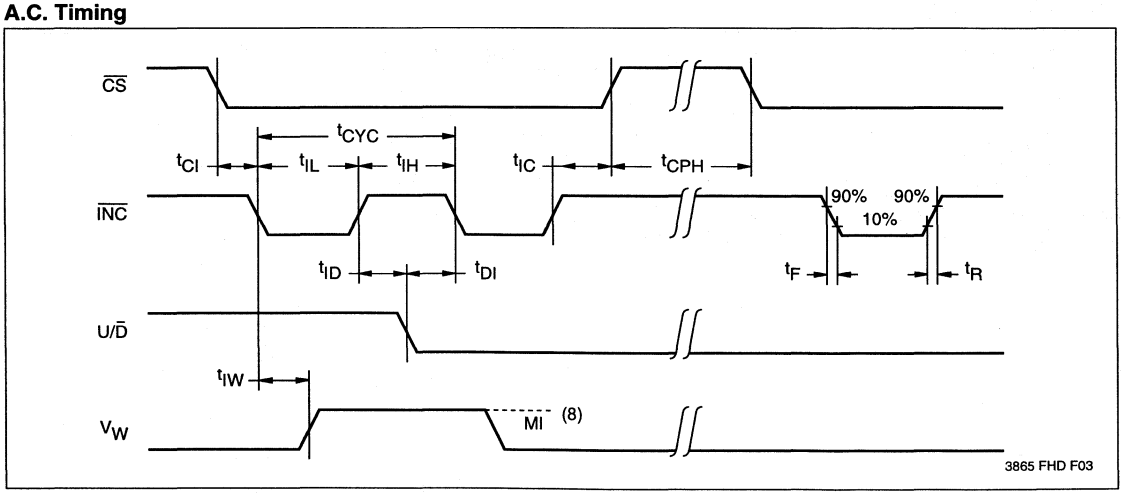
3865 PGM T06

A.C. OPERATING CHARACTERISTICS (Over recommended operating conditions unless otherwise specified)

Symbol	Parameter	Limits			Units
		Min.	Typ.(6)	Max.	
t_{CI}	$\overline{CS}$ to $\overline{INC}$ Setup	100			ns
t_{ID}	$\overline{INC}$ HIGH to U/$\overline{D}$ Change	100			ns
t_{DI}	U/$\overline{D}$ to $\overline{INC}$ Setup	1			µs
t_{IL}	$\overline{INC}$ LOW Period	1			µs
t_{IH}	$\overline{INC}$ HIGH Period	1			µs
t_{IC}	$\overline{INC}$ Inactive to $\overline{CS}$ Inactive	1			µs
t_{CPH}	$\overline{CS}$ Deselect Time	20			ms
t_{IW}	$\overline{INC}$ to Vw Change		100	500	µs
t_{CYC}	$\overline{INC}$ Cycle Time	4			µs
t_R, t_F(7)	$\overline{INC}$ Input Rise and Fall Time			500	µs
t_{PU}(7)	Power up to Wiper Stable			500	µs
t_R V_{CC}(7)	V_{CC} Power-up Rate	0.2		50	mV/µs

3865 PGM T07.4

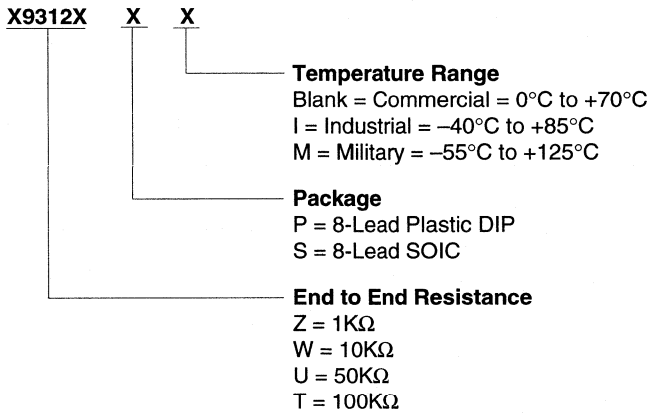
A.C. Timing



3865 FHD F03

Notes: (6) Typical values are for T_A = 25°C and nominal supply voltage.
(7) This parameter is periodically sampled and not 100% tested.
(8) MI in the A.C. timing diagram refers to the minimum incremental change in the V_W output due to a change in the wiper position.

ORDERING INFORMATION



NOTES

Terminal Voltage ±5V, 32 Taps

X9313

E²POT™ Nonvolatile Digital Potentiometer

FEATURES

- **Low Power CMOS**
  - **—V_{CC} = 3V to 5.5V**
  - **—Active Current, 3mA Max**
  - **—Standby Current, 500µA Max**
- **31 Resistive Elements**
  - **—Temperature Compensated**
  - **—±20% End to End Resistance Range**
  - **— –5V to +5V Range**
- **32 Wiper Tap Points**
  - **—Wiper Positioned via Three-Wire Interface**
  - **—Similar to TTL Up/Down Counter**
  - **—Wiper Position Stored in Nonvolatile Memory and Recalled on Power-Up**
- **100 Year Wiper Position Data Retention**
- **X9313Z = 1KΩ**
- **X9313W = 10KΩ**
- **Packages**
  - **—8-Pin DIP**
  - **—8-Lead SOIC**

DESCRIPTION

The Xicor X9313 is a solid state nonvolatile potentiometer and is ideal for digitally controlled resistance trimming.

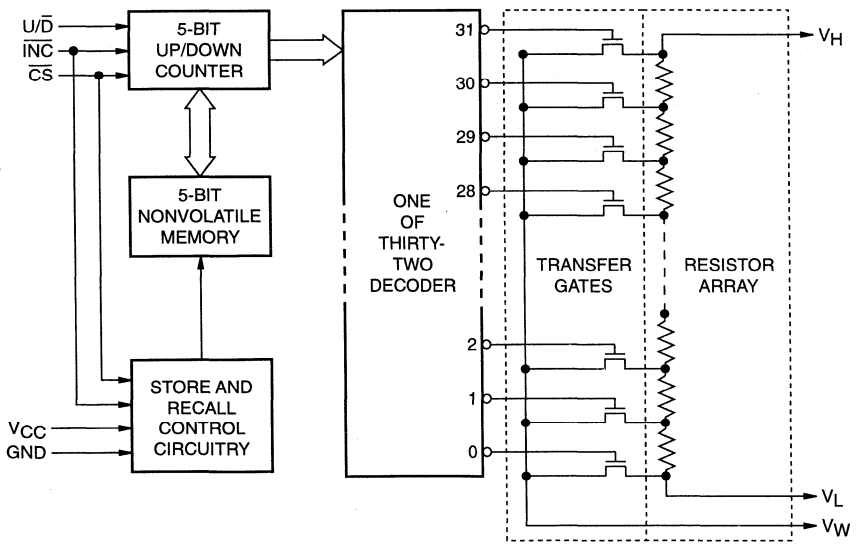
The X9313 is a resistor array composed of 31 resistive elements. Between each element and at either end are tap points accessible to the wiper element. The position of the wiper element is controlled by the $\overline{CS}$, U/$\overline{D}$, and $\overline{INC}$ inputs. The position of the wiper can be stored in nonvolatile memory and then be recalled upon a subsequent power-up operation.

The resolution of the X9313 is equal to the maximum resistance value divided by 31. As an example, for the X9313W (10KΩ) each tap point represents 323Ω.

All Xicor nonvolatile memories are designed and tested for applications requiring extended endurance and data retention.

4

FUNCTIONAL DIAGRAM



3866 FHD F01

E²POT™ is a trademark of Xicor, Inc.

PIN DESCRIPTIONS

V_H and V_L

The high (V_H) and low (V_L) terminals of the X9313 are equivalent to the fixed terminals of a mechanical potentiometer. The minimum voltage is –5V and the maximum is +5V. It should be noted that the terminology of V_L and V_H references the relative position of the terminal in relation to wiper movement direction selected by the U/$\overline{D}$ input and not the voltage potential on the terminal.

V_W

Vw is the wiper terminal, equivalent to the movable terminal of a mechanical potentiometer. The position of the wiper within the array is determined by the control inputs. The wiper terminal series resistance is typically 40Ω.

Up/Down (U/$\overline{D}$)

The U/$\overline{D}$ input controls the direction of the wiper movement and whether the counter is incremented or decremented.

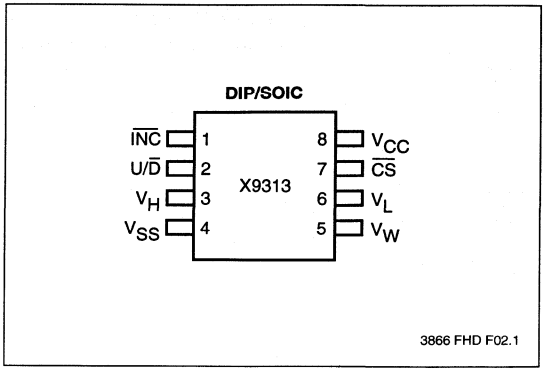
Increment ($\overline{INC}$)

The $\overline{INC}$ input is negative-edge triggered. Toggling $\overline{INC}$ will move the wiper and either increment or decrement the counter in the direction indicated by the logic level on the U/$\overline{D}$ input.

Chip Select ($\overline{CS}$)

The device is selected when the $\overline{CS}$ input is LOW. The current counter value is stored in nonvolatile memory when $\overline{CS}$ is returned HIGH while the $\overline{INC}$ input is also HIGH. After the store operation is complete the X9313 will be placed in the low power standby mode until the device is selected once again.

PIN CONFIGURATION



PIN NAMES

Symbol	Description
V_H	High Terminal
V_W	Wiper Terminal
V_L	Low Terminal
V_{SS}	Ground
V_{CC}	Supply Voltage
U/$\overline{D}$	Up/Down Input
$\overline{INC}$	Increment Input
$\overline{CS}$	Chip Select Input

3866 PGM T01

DEVICE OPERATION

There are three sections of the X9313: the input control, counter and decode section; the nonvolatile memory; and the resistor array. The input control section operates just like an up/down counter. The output of this counter is decoded to turn on a single electronic switch connecting a point on the resistor array to the wiper output. Under the proper conditions the contents of the counter can be stored in nonvolatile memory and retained for future use. The resistor array is comprised of 31 individual resistors connected in series. At either end of the array and between each resistor is an electronic switch that transfers the potential at that point to the wiper.

The $\overline{INC}$, U/$\overline{D}$ and $\overline{CS}$ inputs control the movement of the wiper along the resistor array. With $\overline{CS}$ set LOW the X9313 is selected and enabled to respond to the U/$\overline{D}$ and $\overline{INC}$ inputs. HIGH to LOW transitions on $\overline{INC}$ will increment or decrement (depending on the state of the U/$\overline{D}$ input) a seven bit counter. The output of this counter is decoded to select one of thirty two wiper positions along the resistive array.

The wiper, when at either fixed terminal, acts like its mechanical equivalent and does not move beyond the last position. That is, the counter does not wrap around when clocked to either extreme.

The value of the counter is stored in nonvolatile memory whenever $\overline{CS}$ transistions HIGH while the $\overline{INC}$ input is also HIGH.

When the X9313 is powered-down, the last counter position stored will be maintained in the nonvolatile memory. When power is restored, the contents of the memory are recalled and the counter is reset to the value last stored.

Operation Notes

The system may select the X9313, move the wiper and deselect the device without having to store the latest wiper position in nonvolatile memory. The wiper movement is performed as described above; once the new position is reached, the system would the keep $\overline{INC}$ LOW while taking $\overline{CS}$ HIGH. The new wiper position would be maintained until changed by the system or until a power-up/down cycle recalled the previously stored data.

This would allow the system to always power-up to a preset value stored in nonvolatile memory; then during system operation minor adjustments could be made. The adjustments might be based on user preference, system parameter changes due to temperature drift, etc...

The state of U/$\overline{D}$ may be changed while $\overline{CS}$ remains LOW. This allows the host system to enable the X9313 and then move the wiper up and down until the proper trim is attained.

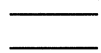
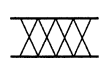
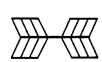
T_{IW}/R_{TOTAL}

The electronic switches on the X9313 operate in a "make before break" mode when the wiper changes tap positions. If the wiper is moved several positions multiple taps are connected to the wiper for t_{IW} ($\overline{INC}$ to V_W change). The R_{TOTAL} value for the device can temporarily be reduced by a significant amount if the wiper is moved several positions.

R_{TOTAL} with V_{CC} Removed

The end to end resistance of the array will fluctuate once V_{CC} is removed.

SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

ABSOLUTE MAXIMUM RATINGS*

Temperature under Bias ..... –65°C to +135°C
Storage Temperature ..... –65°C to +150°C
Voltage on $\overline{CS}$, $\overline{INC}$, U/$\overline{D}$ and V_{CC}
with Respect to V_{SS} ..... –1V to +7V
Voltage on V_H and V_L Referenced to V_{SS}
$\Delta V = |V_H - V_L|$
X9313Z 4V
X9313W, X9313U, X9313T 10V
Lead Temperature (Soldering 10 seconds) ..... 300°C
Wiper Current ..... ±1mA

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ANALOG CHARACTERISTICS

Electrical Characteristics

End-to-End Resistance Tolerance ..... ±20%
Power Rating at 25°C
X9313Z 16mW
X9313W 10mW
Wiper Current ..... ±1mA Max.
Typical Wiper Resistance ..... 40Ω at 1mA
Typical Noise ..... < –120dB/√Hz Ref: 1V

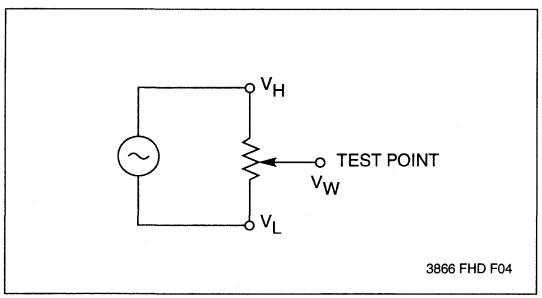
Resolution

Resistance 3%

Linearity

Absolute Linearity(1) ..... ±1.0 MI(2)
Relative Linearity(3) ..... ±0.2 MI(2)

Test Circuit #1



Temperature Coefficient

(–40°C to +85°C)
X9313Z ..... +600 ppm/°C Typical
X9313W, X9313U, X9313T ..... +300 ppm/°C Typical
Ratiometric Temperature Coefficient ..... ±20 ppm

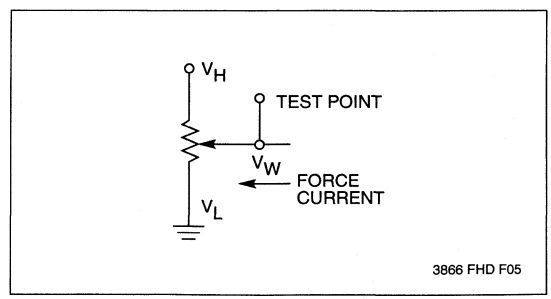
Wiper Adjustability

Unlimited Wiper Adjustment (Non-Store operation)
Wiper Position Store Operations ..... 10,000 Data Changes

Physical Characteristics

Marking Includes
Manufacturer's Trademark
Resistance Value or Code
Date Code

Test Circuit #2



Notes: (1) Absolute Linearity is utilized to determine actual wiper voltage versus expected voltage = ($V_{w(n)}$(actual) – $V_{w(n)}$(expected)) = ±1 MI Maximum.
(2) 1 MI = Minimum Increment = R_{TOT}/31.
(3) Relative Linearity is a measure of the error in step size between taps = $V_{W(n+1)} - [V_{w(n)} + MI] = +0.2$ MI.

RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	+70°C
Industrial	–40°C	+85°C
Military	–55°C	+125°C

3866 PGM T03.1

Supply Voltage	Limits
X9313	5V ±10%
X9313-3	3V to 5.5V

3866 PGM T04.1

D.C. OPERATING CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.(4)	Max.		
I_{CC}	V_{CC} Active Current		1	3	mA	$\overline{CS}$ = V_{IL}, U/$\overline{D}$ = V_{IL} or V_{IH} and $\overline{INC}$ = 0.4V/2.4V @ max. t_{CYC}
I_{SB}	Standby Supply Current		200	500	µA	$\overline{CS}$ = V_{CC} – 0.3V, U/$\overline{D}$ and $\overline{INC}$ = V_{SS} or V_{CC} – 0.3V
I_{LI}	$\overline{CS}$, $\overline{INC}$, U/$\overline{D}$ Input Leakage Current			±10	µA	V_{IN} = V_{SS} to V_{CC}
V_{IH}	$\overline{CS}$, $\overline{INC}$, U/$\overline{D}$ Input HIGH Voltage	2		V_{CC} + 1	V	
V_{IL}	$\overline{CS}$, $\overline{INC}$, U/$\overline{D}$ Input LOW Voltage	–1		0.8	V	
R_W	Wiper Resistence		40	100	Ω	Max. Wiper Current ±1mA
V_{VH}	VH Terminal Voltage	–5		+5	V	
V_{VL}	VL Terminal Voltage	–5		+5	V	
C_{IN}(5)	$\overline{CS}$, $\overline{INC}$, U/$\overline{D}$ Input Capacitance			10	pF	V_{CC} = 5V, V_{IN} = V_{SS}, T_A = 25°C, f = 1MHz

3866 PGM T05.3

STANDARD PARTS

Part Number	Maximum Resistance	Wiper Increments	Minimum Resistance
X9313Z	1KΩ	32.3Ω	40Ω
X9313W	10KΩ	323Ω	40Ω
X9313U	50KΩ	2381Ω	40Ω
X9313T	100KΩ	3226Ω	40Ω

3866 PGM T08.1

Notes: (4) Typical values are for T_A = 25°C and nominal supply voltage.
(5) This parameter is periodically sampled and not 100% tested.

A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3V
Input Rise and Fall Times	10ns
Input Reference Levels	1.5V

3866 PGM T05.1

MODE SELECTION

$\overline{CS}$	$\overline{INC}$	U/$\overline{D}$	Mode
L	↓	H	Wiper Up
L	↓	L	Wiper Down
↑	H	X	Store Wiper Position
H	X	X	Standby
↑	L	X	No Store, Return to Standby

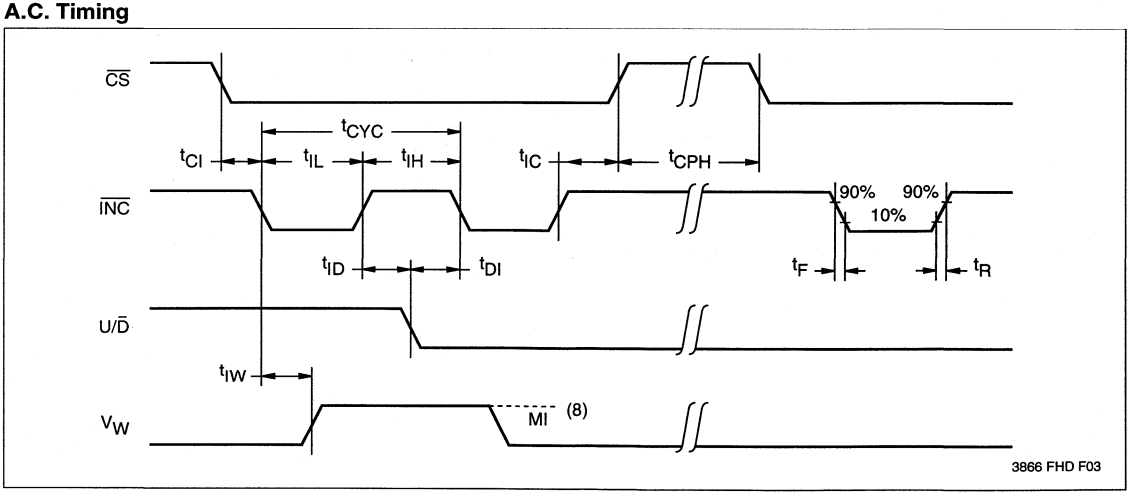
3866 PGM T06

A.C. OPERATING CHARACTERISTICS (Over recommended operating conditions unless otherwise specified)

Symbol	Parameter	Limits			Units
		Min.	Typ.(6)	Max.	
t_{CI}	$\overline{CS}$ to $\overline{INC}$ Setup	100			ns
t_{ID}	$\overline{INC}$ HIGH to U/$\overline{D}$ Change	100			ns
t_{DI}	U/$\overline{D}$ to $\overline{INC}$ Setup	2.9			µs
t_{IL}	$\overline{INC}$ LOW Period	1			µs
t_{IH}	$\overline{INC}$ HIGH Period	1			µs
t_{IC}	$\overline{INC}$ Inactive to $\overline{CS}$ Inactive	1			µs
t_{CPH}	$\overline{CS}$ Deselect Time	20			ms
t_{IW}	$\overline{INC}$ to Vw Change		100	500	µs
t_{CYC}	$\overline{INC}$ Cycle Time	4			µs
t_R, t_F(7)	$\overline{INC}$ Input Rise and Fall Time			500	µs
t_{PU}(7)	Power up to Wiper Stable			500	µs
t_R V_{CC}(7)	V_{CC} Power-up Rate	0.2		50	mV/µs

3866 PGM T07.3

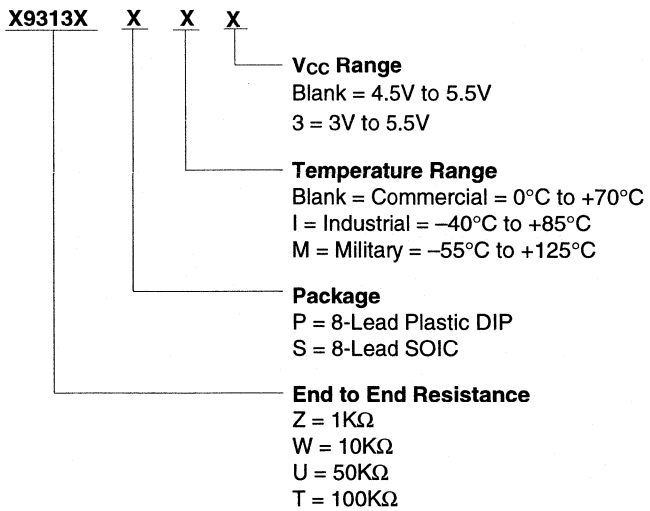
A.C. Timing



3866 FHD F03

Notes: (6) Typical values are for T_A = 25°C and nominal supply voltage.
(7) This parameter is periodically sampled and not 100% tested.
(8) MI in the A.C. timing diagram refers to the minimum incremental change in the V_W output due to a change in the wiper position.

ORDERING INFORMATION



NOTES

Terminal Voltage ±5V, 32 Taps, Log Taper

X9314

E²POT™ Nonvolatile Digital Potentiometer

FEATURES

- Low Power CMOS
  - —V_{CC} = 3V to 5.5V
  - —Active Current, 3mA Max
  - —Standby Current, 500µA Max
- 31 Resistive Elements
  - —Temperature Compensated
  - —±20% End to End Resistance Range
  - — –5V to +5V Range
- 32 Wiper Tap Points
  - —Wiper Positioned via Three-Wire Interface
  - —Similar to TTL Up/Down Counter
  - —Wiper Position Stored in Nonvolatile Memory and Recalled on Power-Up
- 100 Year Wiper Position Data Retention
- X9314W = 10KΩ
- Packages
  - —8-Pin DIP
  - —8-Lead SOIC

DESCRIPTION

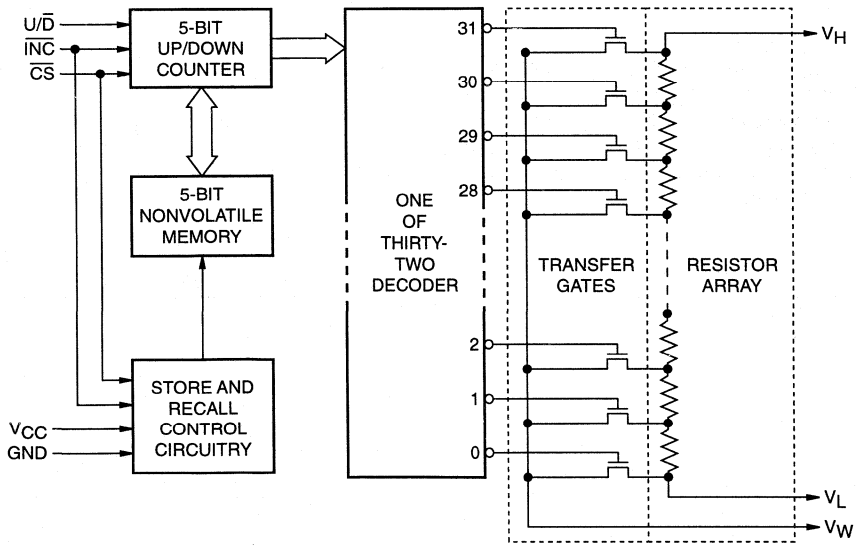
The Xicor X9314 is a solid state nonvolatile potentiometer and is ideal for digitally controlled resistance trimming.

The X9314 is a resistor array composed of 31 resistive elements. Between each element and at either end are tap points accessible to the wiper element. The position of the wiper element is controlled by the $\overline{CS}$, U/$\overline{D}$, and $\overline{INC}$ inputs. The position of the wiper can be stored in nonvolatile memory and then be recalled upon a subsequent power-up operation.

All Xicor nonvolatile Digitally Controlled Potentiometers are designed and tested for applications requiring extended endurance and data retention.

4

FUNCTIONAL DIAGRAM



6427 FHD F01

E²POT™ is a trademark of Xicor, Inc.

PIN DESCRIPTIONS

V_H and V_L

The high (V_H) and low (V_L) terminals of the X9314 are equivalent to the fixed terminals of a mechanical potentiometer. The minimum voltage is –5V and the maximum is +5V. It should be noted that the terminology of V_L and V_H references the relative position of the terminal in relation to wiper movement direction selected by the U/$\overline{D}$ input and not the voltage potential on the terminal.

V_W

Vw is the wiper terminal, equivalent to the movable terminal of a mechanical potentiometer. The position of the wiper within the array is determined by the control inputs. The wiper terminal series resistance is typically 40Ω.

Up/Down (U/$\overline{D}$)

The U/$\overline{D}$ input controls the direction of the wiper movement and whether the counter is incremented or decremented.

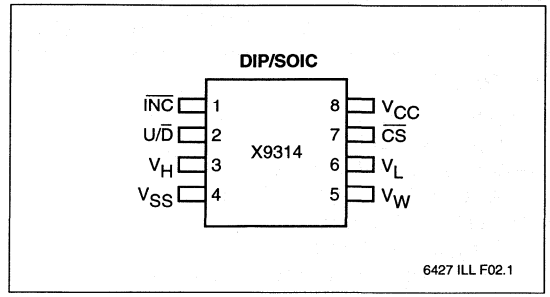
Increment ($\overline{INC}$)

The $\overline{INC}$ input is negative-edge triggered. Toggling $\overline{INC}$ will move the wiper and either increment or decrement the counter in the direction indicated by the logic level on the U/$\overline{D}$ input.

Chip Select ($\overline{CS}$)

The device is selected when the $\overline{CS}$ input is LOW. The current counter value is stored in nonvolatile memory when $\overline{CS}$ is returned HIGH while the $\overline{INC}$ input is also HIGH. After the store operation is complete the X9314 will be placed in the low power standby mode until the device is selected once again.

PIN CONFIGURATION

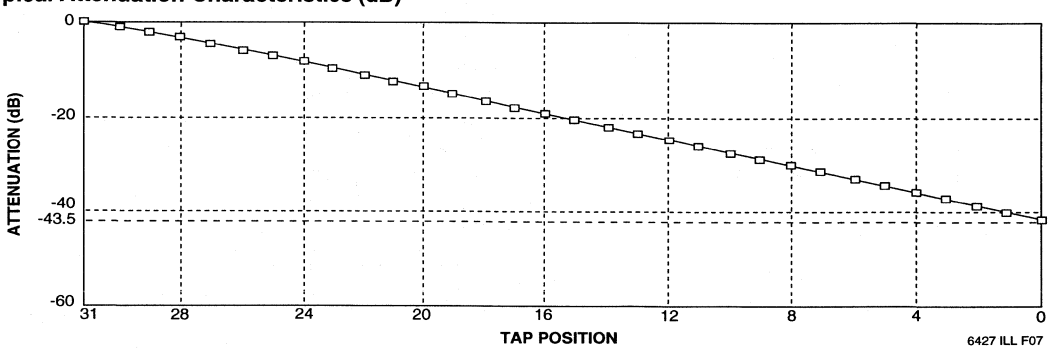


PIN NAMES

Symbol	Description
V_H	High Terminal
V_W	Wiper Terminal
V_L	Low Terminal
V_{SS}	Ground
V_{CC}	Supply Voltage
U/$\overline{D}$	Up/Down Input
$\overline{INC}$	Increment Input
$\overline{CS}$	Chip Select Input

6427 PGM T01

Typical Attenuation Characteristics (dB)



DEVICE OPERATION

There are three sections of the X9314: the input control, counter and decode section; the nonvolatile memory; and the resistor array. The input control section operates just like an up/down counter. The output of this counter is decoded to turn on a single electronic switch connecting a point on the resistor array to the wiper output. Under the proper conditions the contents of the counter can be stored in nonvolatile memory and retained for future use. The resistor array is comprised of 31 individual resistors connected in series. At either end of the array and between each resistor is an electronic switch that transfers the potential at that point to the wiper.

The $\overline{INC}$, U/$\overline{D}$ and $\overline{CS}$ inputs control the movement of the wiper along the resistor array. With $\overline{CS}$ set LOW the X9314 is selected and enabled to respond to the U/$\overline{D}$ and $\overline{INC}$ inputs. HIGH to LOW transitions on $\overline{INC}$ will increment or decrement (depending on the state of the U/$\overline{D}$ input) a five bit counter. The output of this counter is decoded to select one of thirty-two wiper positions along the resistive array.

The wiper, when at either fixed terminal, acts like its mechanical equivalent and does not move beyond the last position. That is, the counter does not wrap around when clocked to either extreme.

The value of the counter is stored in nonvolatile memory whenever $\overline{CS}$ transistions HIGH while the $\overline{INC}$ input is also HIGH.

When the X9314 is powered-down, the last counter position stored will be maintained in the nonvolatile memory. When power is restored, the contents of the memory are recalled and the counter is reset to the value last stored.

SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

Operation Notes

The system may select the X9314, move the wiper and deselect the device without having to store the latest wiper position in nonvolatile memory. The wiper movement is performed as described above; once the new position is reached, the system would keep the $\overline{INC}$ LOW while taking $\overline{CS}$ HIGH. The new wiper position would be maintained until changed by the system or until a power-up/down cycle recalled the previously stored data.

This would allow the system to always power-up to a preset value stored in nonvolatile memory; then during system operation minor adjustments could be made. The adjustments might be based on user preference, system parameter changes due to temperature drift, etc...

The state of U/$\overline{D}$ may be changed while $\overline{CS}$ remains LOW. This allows the host system to enable the X9314 and then move the wiper up and down until the proper trim is attained.

T_{IW}/R_{TOTAL}

The electronic switches on the X9314 operate in a "make before break" mode when the wiper changes tap positions. If the wiper is moved several positions multiple taps are connected to the wiper for t_{IW} ($\overline{INC}$ to V_W change). The R_{TOTAL} value for the device can temporarily be reduced by a significant amount if the wiper is moved several positions.

R_{TOTAL} with V_{CC} Removed

The end to end resistance of the array will fluctuate once V_{CC} is removed.

ABSOLUTE MAXIMUM RATINGS*

Temperature under Bias ..... –65°C to +135°C
Storage Temperature ..... –65°C to +150°C
Voltage on $\overline{CS}$, $\overline{INC}$, U/$\overline{D}$ and V_{CC}
with Respect to V_{SS} ..... –1V to +7V
Voltage on V_H and V_L
Referenced to V_{SS} ..... –8V to +8V
$\Delta V = |V_H - V_L|$
X9314W 10V
Lead Temperature (Soldering 10 seconds) ..... 300°C
Wiper Current ..... ±1mA

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ANALOG CHARACTERISTICS

Electrical Characteristics

End-to-End Resistance Tolerance ..... ±20%
Power Rating at 25°C
X9314W 10mW
Wiper Current ..... ±1mA Max.
Typical Wiper Resistance ..... 40Ω at 1mA
Typical Noise ..... < –120dB/√Hz Ref: 1V

Relative Variation

Relative variation is a measure of the error in step size between taps = $\log(V_{w(n)}) - \log(V_{w(n-1)}) = 0.07 \pm 0.003$ for tap n = 2 – 31

Temperature Coefficient

(–40°C to +85°C)
X9314W ..... +600 ppm/°C Typical
Ratiometric Temperature Coefficient ..... ±20 ppm

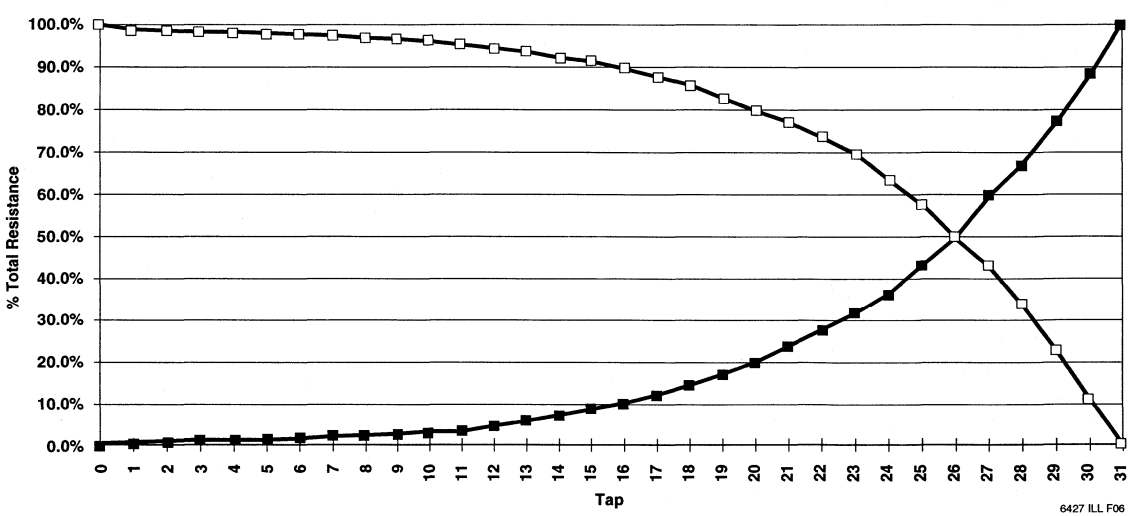
Wiper Adjustability

Unlimited Wiper Adjustment (Non-Store operation)
Wiper Position Store Operations 100,000
Data Changes

Physical Characteristics

Marking Includes
Manufacturer's Trademark
Resistance Value or Code
Date Code

Typical Electrical Taper



RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	+70°C
Industrial	–40°C	+85°C
Military	–55°C	+125°C

6427 PGM T03.1

Supply Voltage	Limits
X9314	5V ±10%
X9314-3	3V to 5.5V

6427 PGM T04.1

D.C. OPERATING CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.(4)	Max.		
I_{CC}	V_{CC} Active Current		1	3	mA	$\overline{CS}$ = V_{IL}, U/$\overline{D}$ = V_{IL} or V_{IH} and $\overline{INC}$ = 0.4V/2.4V @ max. t_{CYC}
I_{SB}	Standby Supply Current			500	µA	$\overline{CS}$ = V_{CC} – 0.3V, U/$\overline{D}$ and $\overline{INC}$ = V_{SS} or V_{CC} – 0.3V
I_{LI}	$\overline{CS}$, $\overline{INC}$, U/$\overline{D}$ Input Leakage Current			±10	µA	V_{IN} = V_{SS} to V_{CC}
V_{IH}	$\overline{CS}$, $\overline{INC}$, U/$\overline{D}$ Input HIGH Voltage	2		V_{CC} + 1	V	
V_{IL}	$\overline{CS}$, $\overline{INC}$, U/$\overline{D}$ Input LOW Voltage	–1		0.8	V	
R_W	Wiper Resistance		40	100	Ω	Max. Wiper Current ±1mA
V_{VH}	VH Terminal Voltage	–5		+5	V	
V_{VL}	VL Terminal Voltage	–5		+5	V	
C_{IN}(5)	$\overline{CS}$, $\overline{INC}$, U/$\overline{D}$ Input Capacitance			10	pF	V_{CC} = 5V, V_{IN} = V_{SS}, T_A = 25°C, f = 1MHz

6427 PGM T05.3

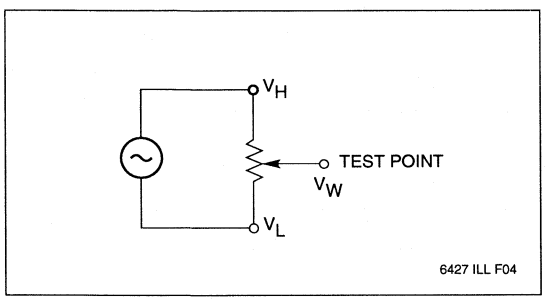
STANDARD PARTS

Part Number	Maximum Resistance	Wiper Increments	Minimum Resistance
X9314W	10KΩ	Log Taper	40Ω

6427 PGM T08.1

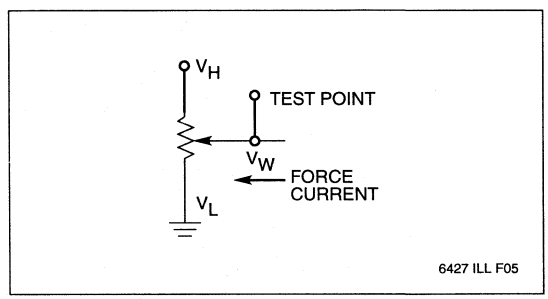
Notes: (4) Typical values are for T_A = 25°C and nominal supply voltage.
(5) This parameter is periodically sampled and not 100% tested.

Test Circuit #1



6427 ILL F04

Test Circuit #2



6427 ILL F05

A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3V
Input Rise and Fall Times	10ns
Input Reference Levels	1.5V

6427 PGM T05.1

MODE SELECTION

$\overline{CS}$	$\overline{INC}$	U/$\overline{D}$	Mode
L	↓	H	Wiper Up
L	↓	L	Wiper Down
↑	H	X	Store Wiper Position
H	X	X	Standby
↑	L	X	No Store, Return to Standby

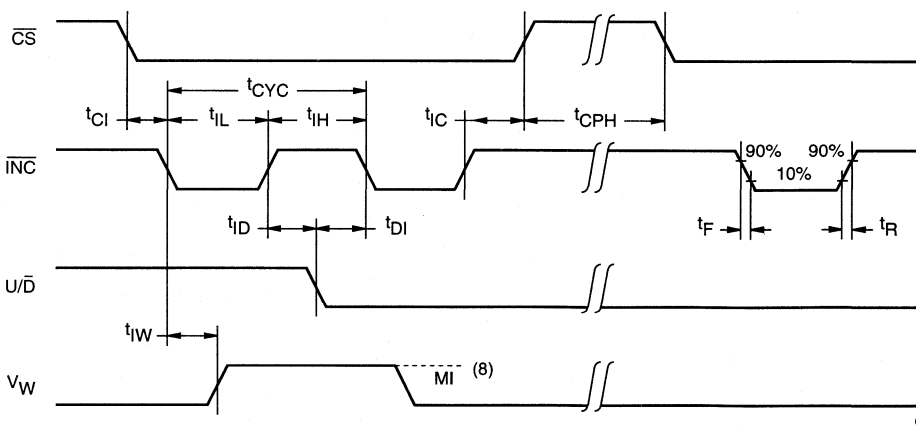
6427 PGM T06

A.C. OPERATING CHARACTERISTICS (Over recommended operating conditions unless otherwise specified)

Symbol	Parameter	Limits			Units
		Min.	Typ.(6)	Max.	
t_{CI}	$\overline{CS}$ to $\overline{INC}$ Setup	100			ns
t_{ID}	$\overline{INC}$ HIGH to U/$\overline{D}$ Change	100			ns
t_{DI}	U/$\overline{D}$ to $\overline{INC}$ Setup	2.9			µs
t_{IL}	$\overline{INC}$ LOW Period	1			µs
t_{IH}	$\overline{INC}$ HIGH Period	1			µs
t_{IC}	$\overline{INC}$ Inactive to $\overline{CS}$ Inactive	1			µs
t_{CPH}	$\overline{CS}$ Deselect Time	20			ms
t_{IW}	$\overline{INC}$ to Vw Change		100	500	µs
t_{CYC}	$\overline{INC}$ Cycle Time	4			µs
t_R, t_F(7)	$\overline{INC}$ Input Rise and Fall Time			500	µs
t_{PU}(7)	Power up to Wiper Stable			500	µs
t_R V_{CC}	V_{CC} Power-up Rate	0.2		50	mV/µs

6427 PGM T07.3

A.C. Timing

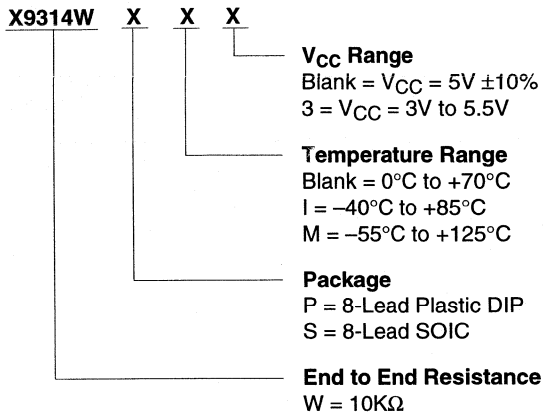


6427 FHD F03

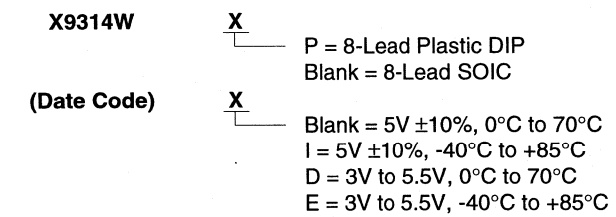
Notes: (6) Typical values are for T_A = 25°C and nominal supply voltage.
(7) This parameter is periodically sampled and not 100% tested.
(8) MI in the A.C. timing diagram refers to the minimum incremental change in the V_W output due to a change in the wiper position.

ORDERING INFORMATION

X9314 E²POT 10K Ohms, Log Taper



Part Mark Convention



NOTES

Terminal Voltage ±5V, 32 Taps

X9511

PushPot™ Potentiometer (Push Button Controlled)

FEATURES

- Push Button Controlled
- Low Power CMOS
  - —Active Current, 3mA Max
  - —Standby Current, 200μA Max
- 31 Resistive Elements
  - —Temperature Compensated
  - —±20% End to End Resistance Range
  - —–5V to +5V Range
- 32 Wiper Tap Points
  - —Wiper Positioned via Two Push Button Inputs
  - —Slow & Fast Scan Modes
  - —AUTOSTORE® Option
  - —Manual Store Option
  - —Wiper Position Stored in Nonvolatile Memory and Recalled on Power-Up
- 100 Year Wiper Position Data Retention
- X9511Z = 1KΩ
- X9511W = 10KΩ
- Packages
  - —8-Lead SOIC
  - —8-Pin DIP

DESCRIPTION

The Xicor X9511 is a push button controlled, potentiometer and is ideal for push button controlled resistance trimming.

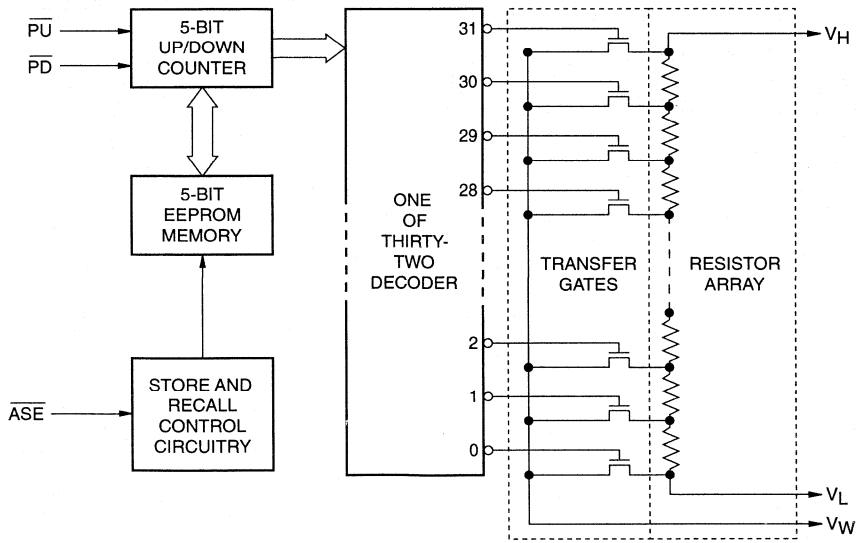
The X9511 is a resistor array composed of 31 resistive elements. Between each element and at either end are tap points accessible to the wiper element. The position of the wiper element is controlled by the $\overline{PU}$ and $\overline{PD}$ inputs. The position of the wiper can be automatically stored in E^2 memory and then be recalled upon a subsequent power-on operation.

The resolution of the X9511 is equal to the maximum resistance value divided by 31. As an example, for the X9511W (10KΩ) each tap point represents 323Ω.

All Xicor nonvolatile products are designed and tested for applications requiring extended endurance and data retention.

4

FUNCTIONAL DIAGRAM



3067 ILL F01.1

AUTOSTORE is a registered trademark of Xicor, Inc.
E^2POT™ and PushPot™ are trademarks of Xicor, Inc.

PIN DESCRIPTIONS

V_H and V_L

The high (V_H) and low (V_L) terminals of the X9511 are equivalent to the fixed terminals of a mechanical potentiometer. The minimum voltage is –5V and the maximum is +5V. It should be noted that the terminology of V_L and V_H references the relative position of the terminal in relation to wiper movement direction selected by the $\overline{PU}$ and $\overline{PD}$ inputs and not the voltage potential on the terminal.

$\overline{PU}$

The debounced $\overline{PU}$ input is for incrementing the wiper position. An on-chip pull-up holds the $\overline{PU}$ input HIGH. A switch closure to ground or a LOW logic level will, after a debounce time, move the wiper to the next adjacent higher tap position.

$\overline{PD}$

The debounced $\overline{PD}$ input is for decrementing the wiper position. An on-chip pull-up holds the $\overline{PD}$ input HIGH. A switch closure to ground or a LOW logic level will, after a debounce time, move the wiper to the next adjacent lower tap position.

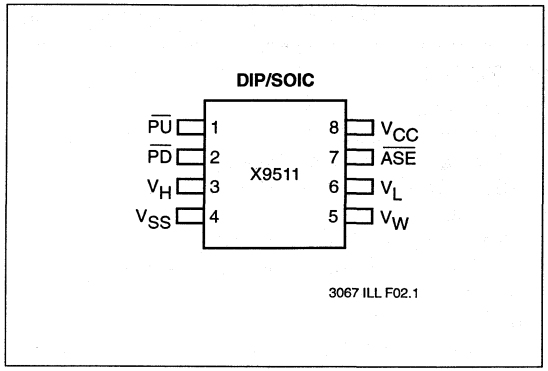
$\overline{ASE}$

The debounced $\overline{ASE}$ (AUTOSTORE enable) pin can be in one of two states:

V_{IL} – AUTOSTORE is enabled. When V_{CC} powers-down an automatic store cycle takes place.

V_{IH} – AUTOSTORE is disabled. A LOW to HIGH will initiate a manual store operation. This is for a user who wishes to connect a push button switch to this pin. For every valid push, the X9511 will store the current wiper position to the E^2PROM.

PIN CONFIGURATION



PIN NAMES

Symbol	Description
V_H	High Terminal
V_W	Wiper Terminal
V_L	Low Terminal
V_{SS}	Ground
V_{CC}	Supply Voltage
$\overline{PU}$	Push Up Input
$\overline{PD}$	Push Down Input
$\overline{ASE}$	AUTOSTORE Enable Input

3067 PGM T01.1

DEVICE OPERATION

There are three sections of the X9511: the input control, counter and decode section; the E²PROM memory; and the resistor array. The input control section operates just like an up/down counter. The output of this counter is decoded to turn on a single electronic switch connecting a point on the resistor array to the wiper output. Under the proper conditions the contents of the counter can be stored in E²PROM memory and retained for future use. The resistor array is comprised of 31 individual resistors connected in series. At either end of the array and between each resistor is an electronic switch that transfers the potential at that point to the wiper.

The X9511 is designed to interface directly to two push button switches for effectively moving the wiper up or down. The $\overline{PU}$ and $\overline{PD}$ inputs increment or decrement a 5-bit counter respectively. The output of this counter is decoded to select one of the thirty-two wiper positions along the resistive array. The wiper increment input, $\overline{PU}$ and the wiper decrement input, $\overline{PD}$ are both connected to an internal pull-up so that they normally remain HIGH. When pulled LOW by an external push button switch or a logic LOW level input, the wiper will be switched to the next adjacent tap position.

Internal debounce circuitry prevents inadvertent switching of the wiper position if $\overline{PU}$ or $\overline{PD}$ remain LOW for less than 40ms, typical. Each of the buttons can be pushed either once for a single increment/decrement or continuously for a multiple increments/decrements. The number of increments/decrements of the wiper position depend on how long the button is being pushed. When making a continuous push, after the first second, the increment/decrement speed increases. For the first second the device will be in the slow scan mode. Then if the button is held for longer than 1 second the device will go into the fast scan mode. As soon as the button is released the X9511 will return to a standby condition.

The wiper, when at either fixed terminal, acts like its mechanical equivalent and does not move beyond the last position. That is, the counter does not wrap around when clocked to either extreme.

AUTOSTORE

The value of the counter is stored in E²PROM memory whenever the chip senses a power-down of V_{CC} while $\overline{ASE}$ is enabled (held LOW). When power is restored, the content of the memory is recalled and the counter reset to the last value stored.

If AUTOSTORE is to be implemented, $\overline{ASE}$ is typically hard wired to V_{SS}. If $\overline{ASE}$ is held HIGH during power-up and then taken LOW, the wiper will not respond to the $\overline{PU}$ or $\overline{PD}$ inputs until $\overline{ASE}$ is brought HIGH and held HIGH.

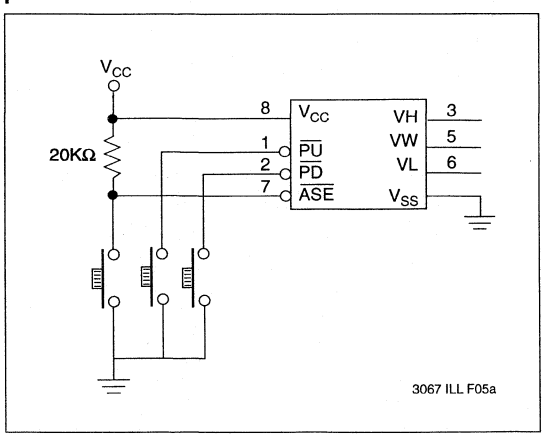
Manual (Push Button) Store

When $\overline{ASE}$ is not enabled (held HIGH) a push button switch may be used to pull $\overline{ASE}$ LOW and released to perform a manual store of the wiper position.

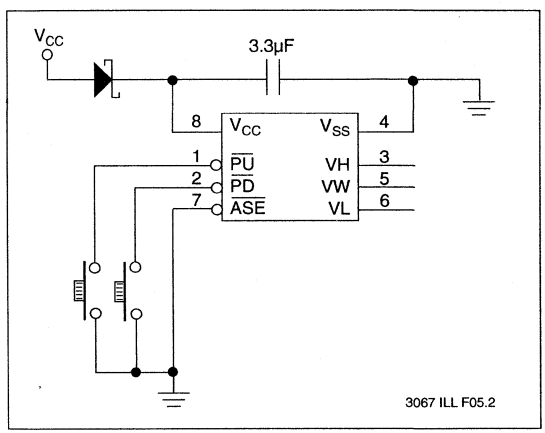
R_{TOTAL} with V_{CC} Removed

The end to end resistance of the array will fluctuate once V_{CC} is removed.

Typical circuit with $\overline{ASE}$ store pin controlled by push button switch



Typical circuit with $\overline{ASE}$ store pin used in AUTOSTORE mode



ABSOLUTE MAXIMUM RATINGS*

Temperature under Bias ..... –65°C to +135°C
Storage Temperature ..... –65°C to +150°C
Voltage on $\overline{PU}$, $\overline{PD}$, and V_{CC}
with Respect to V_{SS} ..... –1V to +7V
Voltage on V_H and V_L
Referenced to V_{SS} ..... –8V to +8V
$\Delta V = |V_H - V_L|$
X9511Z 4V
X9511W 10V
Lead Temperature (Soldering 10 seconds) ..... 300°C
Wiper Current ..... ±1mA

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ANALOG CHARACTERISTICS

Electrical Characteristics

End-to-End Resistance Tolerance ..... ±20%
Power Rating at 25°C
X9511Z 16mW
X9511W 10mW
Wiper Current ..... ±1mA Max.
Typical Wiper Resistance ..... 40Ω at 1mA
Typical Noise ..... < –120dB/$\sqrt{}$Hz Ref: 1V

Resolution

Resistance 3%

Linearity

Absolute Linearity(1) ..... ±1.0 MI(2)
Relative Linearity(3) ..... ±0.2 MI(2)

Temperature Coefficient

–40°C to +85°C
X9511Z ..... +600 ppm/°C Typical
X9511W ..... +300 ppm/°C Typical
Ratiometric Temperature Coefficient ..... ±20 ppm

Wiper Adjustability

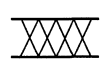
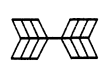
Unlimited Wiper Adjustment (Non-Store operation)
Wiper Position Store Operations ..... 100,000 Data Changes

Physical Characteristics

Marking Includes
Manufacturer's Trademark
Resistance Value or Code
Date Code

Notes: (1) Absolute Linearity is utilized to determine actual wiper voltage versus expected voltage = ($V_{w(n)}$(actual) – $V_{w(n)}$(expected)) = ±1 MI Maximum.
(2) 1 MI = Minimum Increment = R_{TOT}/31.
(3) Relative Linearity is a measure of the error in step size between taps = $V_{W(n+1)} - [V_{w(n)} + MI] = +0.2$ MI.

SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	+70°C
Industrial	–40°C	+85°C
Military	–55°C	+125°C

3067 PGM T03

Supply Voltage	Limits
X9511	5V ±10%

3067 PGM T04.1

D.C. OPERATING CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.(4)	Max.		
I_{CC}	V_{CC} Active Current		1	3	mA	$\overline{PU}$ or $\overline{PD}$ held at V_{IL} the other at V_{IH}
I_{SB}	Standby Supply Current		100	200	µA	$\overline{PU} = \overline{PD} = V_{IH}$
I_{LI}	$\overline{PU}$, $\overline{PD}$, $\overline{ASE}$ Input Leakage Current			10	µA	$V_{IN} = V_{SS}$ to V_{CC}
V_{IH}	$\overline{PU}$, $\overline{PD}$, $\overline{ASE}$ Input HIGH Voltage	2		$V_{CC} + 1$	V	
V_{IL}	$\overline{PU}$, $\overline{PD}$, $\overline{ASE}$ Input LOW Voltage	–1		0.8	V	
R_W	Wiper Resistence		40	100	Ω	Max. Wiper Current ±1mA
V_{VH}	VH Terminal Voltage	–5		+5	V	
V_{VL}	VL Terminal Voltage	–5		+5	V	
C_{IN}(5)	$\overline{ASE}$, $\overline{PU}$, $\overline{PD}$ Input Capacitance			10	pF	V_{CC} = 5V, V_{IN} = 0V, T_A = 25°C, f = 1MHz

3067 PGM T05.4

STANDARD PARTS

Part Number	Maximum Resistance	Wiper Increments	Minimum Resistance
X9511Z	1KΩ	32.3Ω	40Ω
X9511W	10KΩ	323Ω	40Ω

3067 PGM T08.1

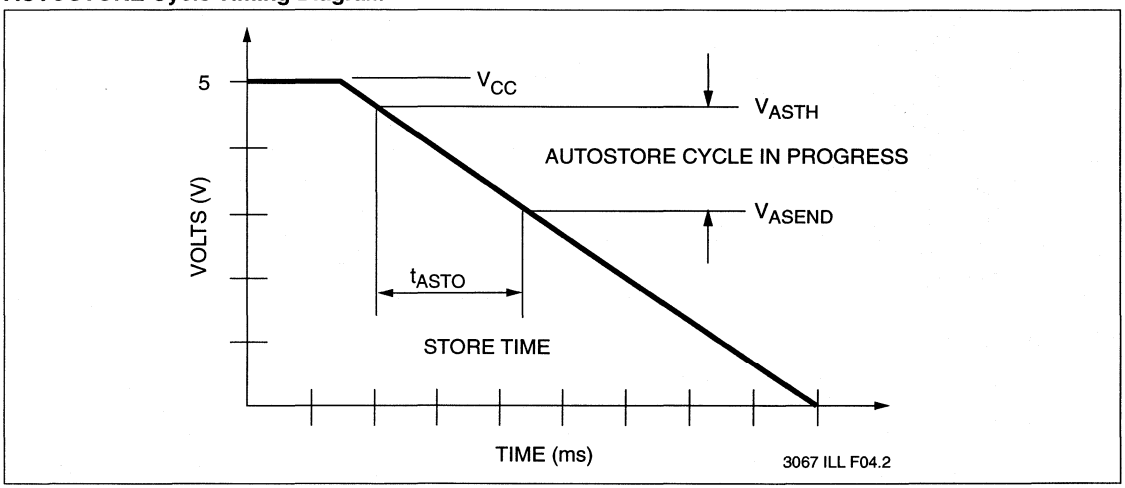
Notes: (4) Typical values are for T_A = 25°C and nominal supply voltage.
(5) This parameter is periodically sampled and not 100% tested.

A.C. OPERATING CHARACTERISTICS (Over recommended operating conditions unless otherwise specified)

Symbol	Parameter	Limits			Units
		Min.	Typ.(6)	Max.	
t_{GAP}	Time Between Two Separate Push Button Events	0			µs
t_{DB}	Debounce Time		30	60	ms
$t_{S\ SLOW}$	After Debounce to Wiper Change on a Slow Mode	100	250	375	ms
$t_{S\ FAST}$(7)	Wiper Change on a Fast Mode	25	50	75	ms
t_{PU}(7)	Power Up to Wiper Stable			500	µs
$t_R\ V_{cc}$(7)	V_{CC} Power-up Rate	0.2		50	mV/µs
t_{ASTO}(7)	AUTOSTORE Cycle Time	2			ms
V_{ASTH}(7)	AUTOSTORE Threshold Voltage		4		V
V_{ASEND}(7)	AUTOSTORE Cycle End Voltage		3.5		V

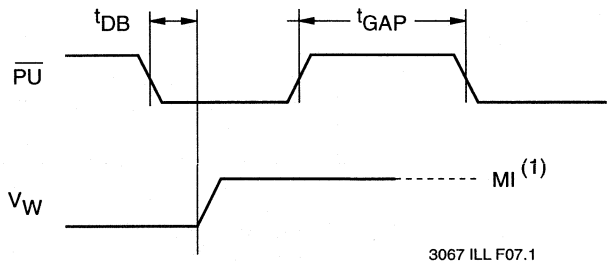
3067 PGM T07.3

AUTOSTORE Cycle Timing Diagram



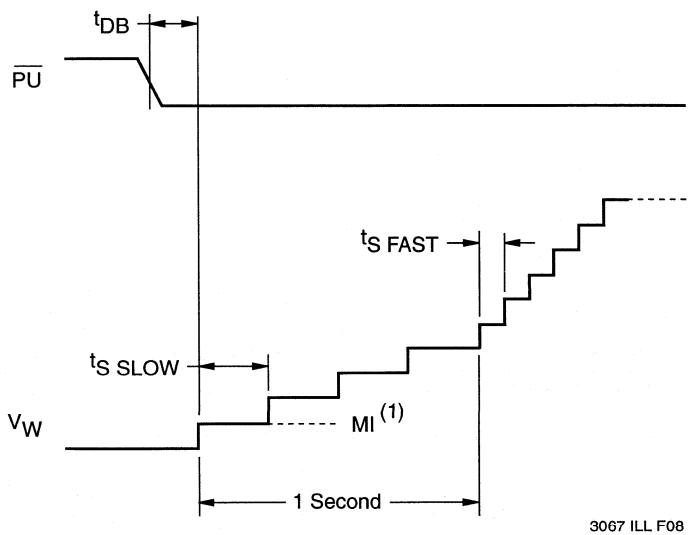
Notes: V_{ASTH} – AUTOSTORE threshold voltage
V_{ASEND} – AUTOSTORE cycle end voltage
t_{ASTO} – AUTOSTORE cycle time
(6) Typical values are for T_A = 25°C and nominal supply voltage.
(7) This parameter is periodically sampled and not 100% tested.

Slow Mode Timing



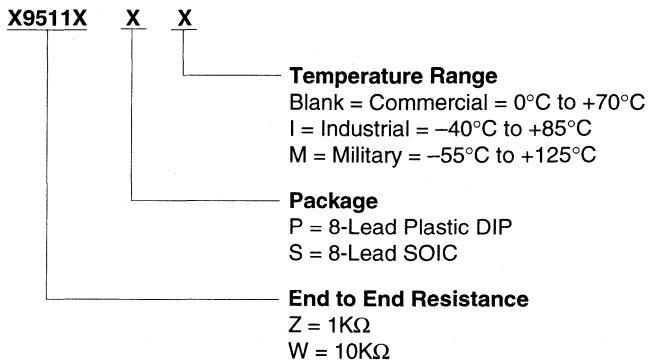
Notes: (1) MI in the A.C. timing diagram refers to the minimum incremental change in the wiper voltage.

Fast Mode Timing



Notes: (1) MI in the A.C. timing diagram refers to the minimum incremental change in the wiper voltage.

ORDERING INFORMATION



Terminal Voltage ±5V, 32 Taps, Log Taper

X9514

PushPot™ Potentiometer (Push Button Controlled)

FEATURES

- Push Button Controlled
- Low Power CMOS
  - —Active Current, 3mA Max
  - —Standby Current, 200µA Max
- 31 Resistive Elements
  - —Temperature Compensated
  - —±20% End to End Resistance Range
  - — –5V to +5V Range
- 32 Wiper Tap Points
  - —Logarithmic Taper
  - —Wiper Positioned via Two Push Button Inputs
  - —Slow & Fast Scan Modes
  - —AUTOSTORE® Option
  - —Manual Store Option
  - —Wiper Position Stored in Nonvolatile Memory and Recalled on Power-Up
- 100 Year Wiper Position Data Retention
- X9514W = 10KΩ
- Packages
  - —8-Pin DIP
  - —8-Lead SOIC

DESCRIPTION

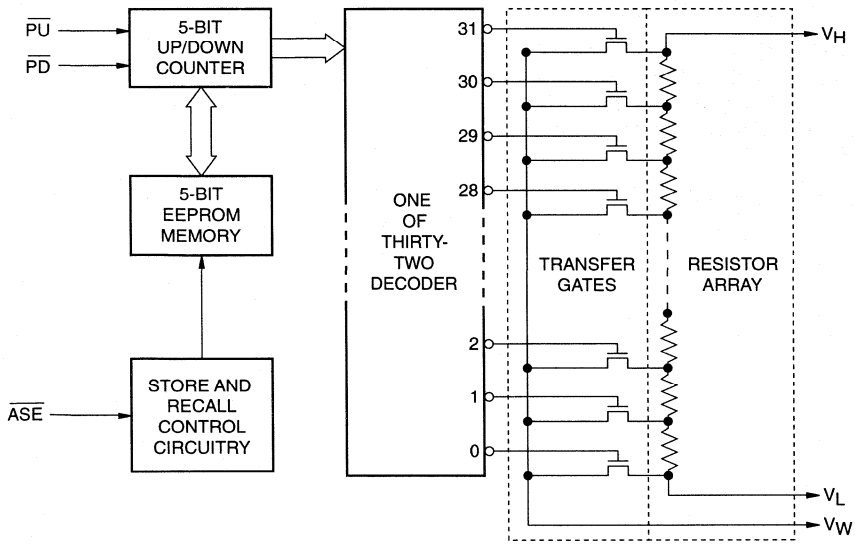
The Xicor X9514 is a push button controlled, logarithmic taper potentiometer and is ideal for push button controlled resistance trimming.

The X9514 is a resistor array composed of 31 resistive elements. Between each element and at either end are tap points accessible to the wiper element. The position of the wiper element is controlled by the $\overline{PU}$ and $\overline{PD}$ inputs. The position of the wiper can be automatically stored in E^2 memory and then be recalled upon a subsequent power-on operation.

All Xicor nonvolatile products are designed and tested for applications requiring extended endurance and data retention.

4

FUNCTIONAL DIAGRAM



6487 ILL F01.1

AUTOSTORE is a registered trademark of Xicor, Inc.
E^2POT™ and PushPot™ are trademarks of Xicor, Inc.

PIN DESCRIPTIONS

V_H and V_L

The high (V_H) and low (V_L) terminals of the X9514 are equivalent to the fixed terminals of a mechanical potentiometer. The minimum voltage is –5V and the maximum is +5V. It should be noted that the terminology of V_L and V_H references the relative position of the terminal in relation to wiper movement direction selected by the $\overline{PU}$ and $\overline{PD}$ inputs and not the voltage potential on the terminal.

$\overline{PU}$

The debounced $\overline{PU}$ input is for incrementing the wiper position. An on-chip pull-up holds the $\overline{PU}$ input HIGH. A switch closure to ground or a LOW logic level will, after a debounce time, move the wiper to the next adjacent higher tap position.

$\overline{PD}$

The debounced $\overline{PD}$ input is for decrementing the wiper position. An on-chip pull-up holds the $\overline{PD}$ input HIGH. A switch closure to ground or a LOW logic level will, after a debounce time, move the wiper to the next adjacent lower tap position.

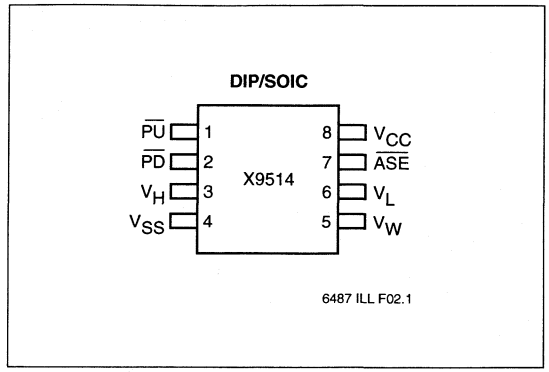
$\overline{ASE}$

The debounced $\overline{ASE}$ (AUTOSTORE enable) pin can be in one of two states:

V_{IL} – AUTOSTORE is enabled. When V_{CC} powers-down an automatic store cycle takes place.

V_{IH} – AUTOSTORE is disabled. A LOW to HIGH will initiate a manual store operation. This is for a user who wishes to connect a push button switch to this pin. For every valid push, the X9514 will store the current wiper position to the E²PROM.

PIN CONFIGURATION

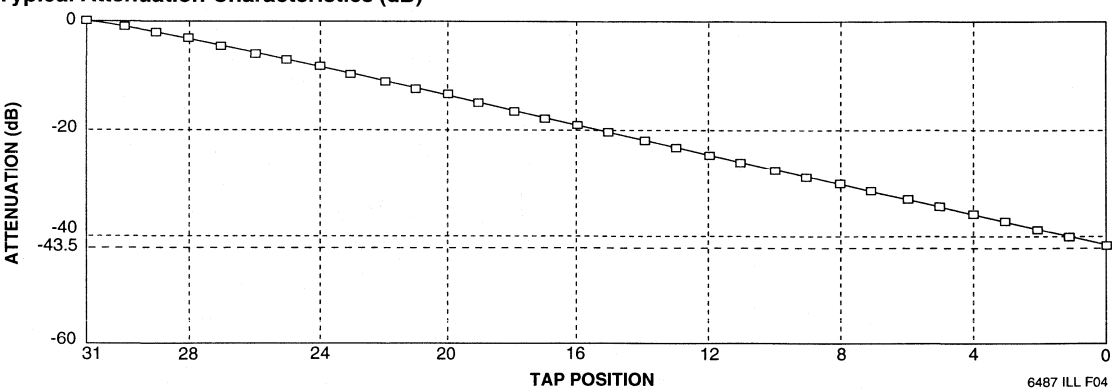


PIN NAMES

Symbol	Description
V_H	High Terminal
V_W	Wiper Terminal
V_L	Low Terminal
V_{SS}	Ground
V_{CC}	Supply Voltage
$\overline{PU}$	Push Up Input
$\overline{PD}$	Push Down Input
$\overline{ASE}$	AUTOSTORE Enable Input

6487 PGM T01.1

Typical Attenuation Characteristics (dB)



DEVICE OPERATION

There are three sections of the X9514: the input control, counter and decode section; the E²PROM memory; and the resistor array. The input control section operates just like an up/down counter. The output of this counter is decoded to turn on a single electronic switch connecting a point on the resistor array to the wiper output. Under the proper conditions the contents of the counter can be stored in E²PROM memory and retained for future use. The resistor array is comprised of 31 individual resistors connected in series. At either end of the array and between each resistor is an electronic switch that transfers the potential at that point to the wiper.

The X9514 is designed to interface directly to two push button switches for effectively moving the wiper up or down. The $\overline{PU}$ and $\overline{PD}$ inputs increment or decrement a 5-bit counter respectively. The output of this counter is decoded to select one of the thirty-two wiper positions along the resistive array. The wiper increment input, $\overline{PU}$ and the wiper decrement input, $\overline{PD}$ are both connected to an internal pull-up so that they normally remain HIGH. When pulled LOW by an external push button switch or a logic LOW level input, the wiper will be switched to the next adjacent tap position.

Internal debounce circuitry prevents inadvertent switching of the wiper position if $\overline{PU}$ or $\overline{PD}$ remain LOW for less than 40ms, typical. Each of the buttons can be pushed either once for a single increment/decrement or continuously for a multiple increments/decrements. The number of increments/decrements of the wiper position depend on how long the button is being pushed. When making a continuous push, after the first second, the increment/decrement speed increases. For the first second the device will be in the slow scan mode. Then if the button is held for longer than 1 second the device will be in the fast scan mode. As soon as the button is released the X9514 will return to a standby condition.

The wiper, when at either fixed terminal, acts like its mechanical equivalent and does not move beyond the last position. That is, the counter does not wrap around when clocked to either extreme.

AUTOSTORE

The value of the counter is stored in E²PROM memory whenever the chip senses a powers-down of V_{CC} while $\overline{ASE}$ is enabled (held LOW). When power is restored, the content of the memory is recalled and the counter reset to the last value stored.

If AUTOSTORE is to be implemented, $\overline{ASE}$ is typically hard wired to V_{SS}. If $\overline{ASE}$ is held HIGH during power up and then taken LOW, the wiper will not respond to the $\overline{PU}$ or $\overline{PD}$ inputs until $\overline{ASE}$ is brought HIGH and held HIGH.

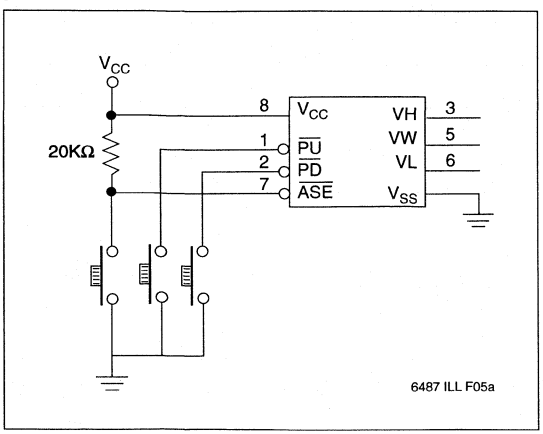
Manual (Push Button) Store

When $\overline{ASE}$ is not enabled (held HIGH) a push button switch may be used to pull $\overline{ASE}$ LOW and released to perform a manual store of the wiper position.

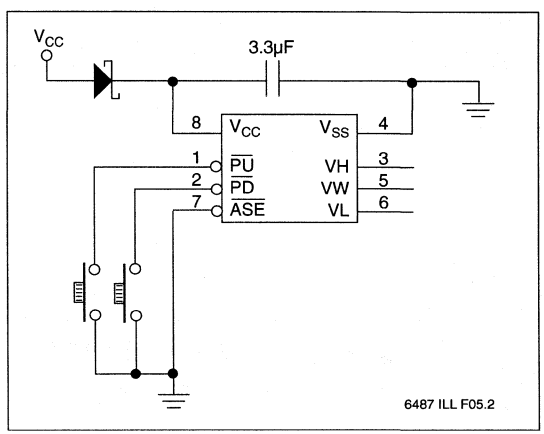
R_{TOTAL} with V_{CC} Removed

The end to end resistance of the array will fluctuate once V_{CC} is removed.

Typical circuit with $\overline{ASE}$ store pin controlled by push button switch



Typical circuit with $\overline{ASE}$ store pin used in AUTOSTORE mode



ABSOLUTE MAXIMUM RATINGS*

Temperature under Bias ..... –65°C to +135°C
Storage Temperature ..... –65°C to +150°C
Voltage on $\overline{PU}$, $\overline{PD}$, $\overline{ASE}$ and V_{CC}
with Respect to V_{SS} ..... –1V to +7V
Voltage on V_H and V_L Referenced to V_{SS}
$\Delta V = |V_H - V_L|$ 10V
Lead Temperature (Soldering 10 seconds) ..... 300°C
Wiper Current ..... ±1mA

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ANALOG CHARACTERISTICS

Electrical Characteristics

End-to-End Resistance Tolerance ..... ±20%
Power Rating at 25°C
X9514W 10mW
Wiper Current ..... ±1mA Max.
Typical Wiper Resistance ..... 40Ω at 1mA
Typical Noise ..... < –120dB/√Hz Ref: 1V

Relative Variation

Relative variation is a measure of the error in step size between taps = $\log(V_{w(n)}) - \log(V_{w(n-1)}) = 0.08 \pm 0.05$ for tap n = 2 – 31

Temperature Coefficient

(–40°C to +85°C)
X9514W ..... +600 ppm/°C Typical
Ratiometric Temperature Coefficient ..... ±20 ppm

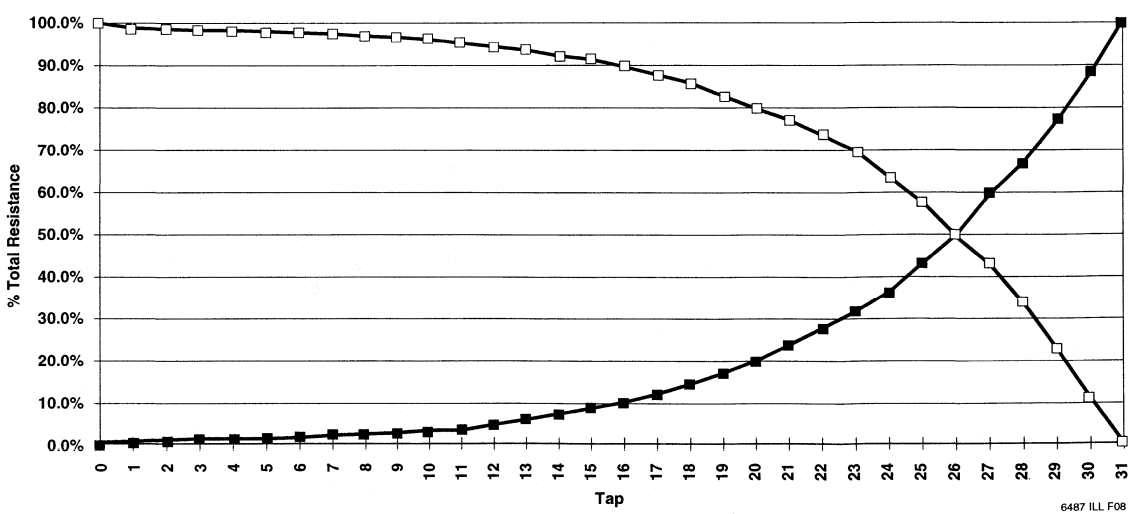
Wiper Adjustability

Unlimited Wiper Adjustment (Non-Store operation)
Wiper Position Store Operations 100,000
Data Changes

Physical Characteristics

Marking Includes
Manufacturer's Trademark
Resistance Value or Code
Date Code

Typical Electrical Taper



RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	+70°C
Industrial	–40°C	+85°C
Military	–55°C	+125°C

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Supply Voltage	Limits
X9514	5V ±10%

6487 PGM T04.1

D.C. OPERATING CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.(4)	Max.		
I_{CC}	V_{CC} Active Current		1	3	mA	$\overline{PU}$ or $\overline{PD}$ held at V_{IL} the others at V_{IH}
I_{SB}	Standby Supply Current			200	µA	$\overline{PU} = \overline{PD} = V_H$
I_{LI}	$\overline{ASE}$, $\overline{PU}$, $\overline{PD}$ Input Leakage Current			10	µA	$V_{IN} = V_{SS}$ to V_{CC}
V_{IH}	$\overline{ASE}$, $\overline{PU}$, $\overline{PD}$ Input HIGH Voltage	2		$V_{CC} + 1$	V	
V_{IL}	$\overline{ASE}$, $\overline{PU}$, $\overline{PD}$ Input LOW Voltage	–1		0.8	V	
R_W	Wiper Resistance		40	100	Ω	Max. Wiper Current ±1mA
V_{VH}	VH Terminal Voltage	–5		+5	V	
V_{VL}	VL Terminal Voltage	–5		+5	V	
C_{IN}(5)	$\overline{ASE}$, $\overline{PU}$, $\overline{PD}$ Input Capacitance			10	pF	V_{CC} = 5V, V_{IN} = 0V, T_A = 25°C, f = 1MHz

6487 PGM T05.4

STANDARD PARTS

Part Number	Maximum Resistance	Wiper Increments	Minimum Resistance
X9514W	10KΩ	Log Taper	40Ω

6487 PGM T08.1

Notes: (4) Typical values are for T_A = 25°C and nominal supply voltage.
(5) This parameter is periodically sampled and not 100% tested.

SYMBOL TABLE

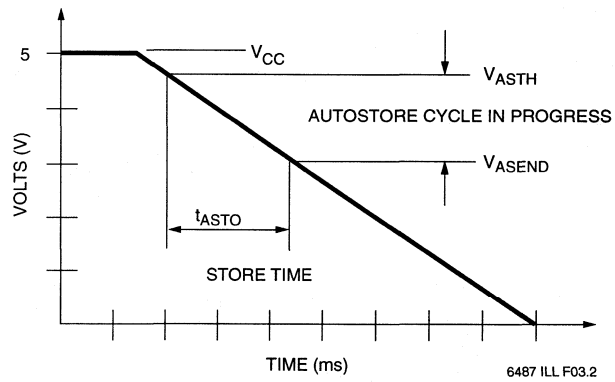
WAVEFORM	INPUTS	OUTPUTS
———	Must be steady	Will be steady
⫽⫽⫽	May change from LOW to HIGH	Will change from LOW to HIGH
⫽⫽⫽	May change from HIGH to LOW	Will change from HIGH to LOW
⨯⨯⨯	Don't Care: Changes Allowed	Changing: State Not Known
⫽⫽⫽	N/A	Center Line is High Impedance

A.C. OPERATING CHARACTERISTICS (Over recommended operating conditions unless otherwise specified)

Symbol	Parameter	Limits			Units
		Min.	Typ.(6)	Max.	
t_{GAP}	Time Between Two Separate Push Button Events	0			µs
t_{DB}	Debounce Time			60	ms
$t_{S\ SLOW}$	After Debounce to Wiper Change on a Slow Mode	100	250	375	ms
$t_{S\ FAST}$(7)	Wiper Change on a Scan Mode	25	50	75	ms
t_{PU}(7)	Power Up to Wiper Stable			500	µs
$t_R\ V_{CC}$(7)	V_{CC} Power-up Rate	0.2		50	mV/µs
t_{ASTO}(7)	AUTOSTORE Cycle Time	2			ms
V_{ASTH}(7)	AUTOSTORE Threshold Voltage		4		V
V_{ASEND}(7)	AUTOSTORE Cycle End Voltage		3.5		V

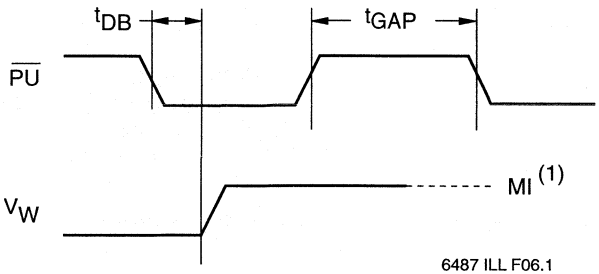
6487 PGM T07.3

AUTOSTORE Cycle Timing Diagram



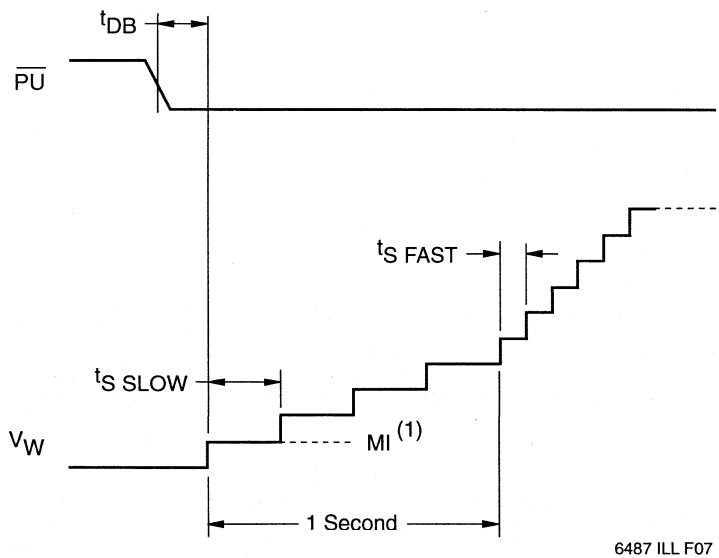
Notes: V_{ASTH} – AUTOSTORE threshold voltage
V_{ASEND} – AUTOSTORE cycle end voltage
t_{ASTO} – AUTOSTORE cycle time
(6) Typical values are for T_A = 25°C and nominal supply voltage.
(7) This parameter is periodically sampled and not 100% tested.

Slow Mode Timing



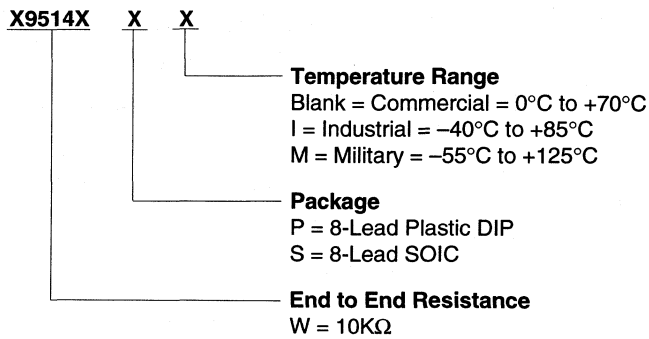
Notes: (1) MI in the A.C. timing diagram refers to the minimum incremental change in the wiper voltage.

Fast Mode Timing



Notes: (1) MI in the A.C. timing diagram refers to the minimum incremental change in the wiper voltage.

ORDERING INFORMATION



Terminal Voltage ±5V, 64 Taps

X9221

Dual E²POT™ Nonvolatile Digital Potentiometer

FEATURES

- Two E²POTs in One Package
- Two-Wire Serial Interface
- Register Oriented Format
  - —Directly Write Wiper Position
  - —Read Wiper Position
  - —Store as Many as Four Positions per Pot
- Instruction Format
  - —Quick Transfer of Register Contents to Resistor Array
- Low Power CMOS
- Direct Write Cell
  - —Endurance - 100,000 Writes per Register
  - —Register Data Retention - 100 years
- 8 Bytes of E²PROM memory
- 3 Resistor Array Values
  - —2KΩ to 50KΩ Mask Programmable
- Resolution: 64 Taps each Pot
- 20-Pin Plastic DIP and 20-Lead SOIC Packages

DESCRIPTION

The X9221 integrates two nonvolatile E²POT™ digitally controlled potentiometers on a monolithic CMOS microcircuit.

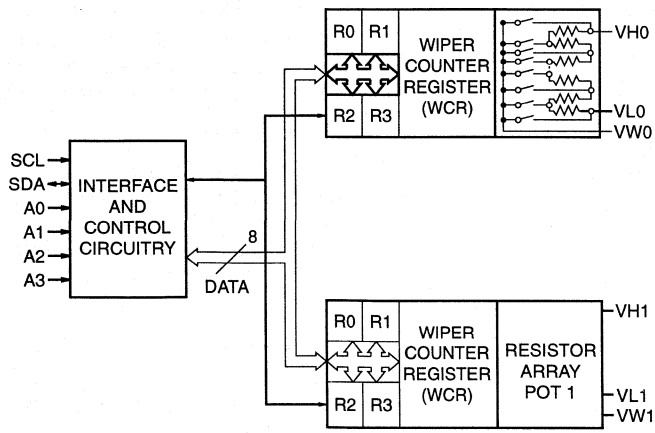
The X9221 contains two resistor arrays, each composed of 63 resistive elements. Between each element and at either end are tap points accessible to the wiper elements. The position of the wiper element on the array is controlled by the user through the two-wire serial bus interface.

Each resistor array has associated with it a wiper counter register and four 8-bit data registers that can be directly written and read by the user. The contents of the wiper counter register control the position of the wiper on the resistor array.

The data register may be read or written by the user. The contents of the data registers can be transferred to the wiper counter register to position the wiper. The current wiper position can be transferred to any one of its associated data registers.

4

FUNCTIONAL DIAGRAM



3079 ILL F07.1

PIN DESCRIPTIONS

Host Interface Pins

Serial Clock (SCL)

The SCL input is used to clock data into and out of the X9221.

Serial Data (SDA)

SDA is a bidirectional pin used to transfer data into and out of the device. It is an open drain output and may be wire-ORed with any number of open drain or open collector outputs. An open drain output requires the use of a pull-up resistor. For selecting typical values, refer to the guidelines for calculating typical values on the bus pull-up resistors graph.

Address

The Address inputs are used to set the least significant 4 bits of the 8-bit slave address. A match in the slave address serial data stream must be made with the Address input in order to initiate communication with the X9221

Potentiometer Pins

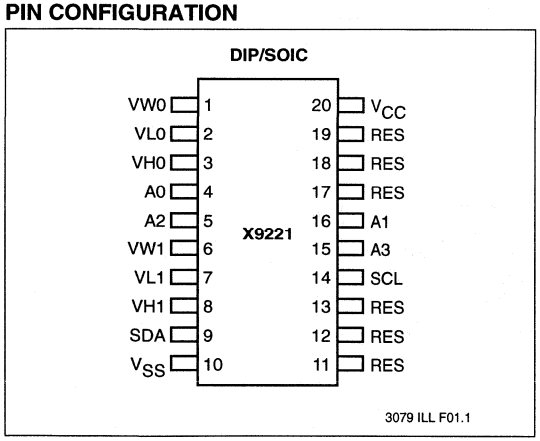
V_H (V_{H0} – V_{H1}), V_L (V_{L0} – V_{L1})

The VH and VL inputs are equivalent to the terminal connections on either end of a mechanical potentiometer.

V_W (V_{W0} – V_{W1})

The wiper outputs are equivalent to the wiper output of a mechanical potentiometer.

PIN CONFIGURATION



PIN NAMES

Symbol	Description
SCL	Serial Clock
SDA	Serial Data
A0–A3	Address
V_{H0}–V_{H1}, V_{L0}–V_{L1}	Potentiometers (terminal equivalent)
V_{W0}–V_{W1}	Potentiometers (wiper equivalent)
RES	Reserved (Do not connect)

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PRINCIPLES OF OPERATION

The X9221 is a highly integrated microcircuit incorporating two resistor arrays, their associated registers and counters and the serial interface logic providing direct communication between the host and the E²POT potentiometers.

Serial Interface

The X9221 supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is a master and the device being controlled is the slave. The master will always initiate data transfers and provide the clock for both transmit and receive operations. Therefore, the X9221 will be considered a slave device in all applications.

Clock and Data Conventions

Data states on the SDA line can change only during SCL LOW periods (t_{LOW}). SDA state changes during SCL HIGH are reserved for indicating start and stop conditions.

Start Condition

All commands to the X9221 are preceded by the start condition, which is a HIGH to LOW transition of SDA while SCL is HIGH (t_{HIGH}). The X9221 continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition is met.

Stop Condition

All communications must be terminated by a stop condition, which is a LOW to HIGH transition of SDA while SCL is HIGH.

Acknowledge

Acknowledge is a software convention used to provide a positive handshake between the master and slave devices on the bus to indicate the successful receipt of data. The transmitting device, either the master or the slave, will release the SDA bus after transmitting eight bits. The master generates a ninth clock cycle and during this period the receiver pulls the SDA line LOW to acknowledge that it successfully received the eight bits of data. See Figure 7.

The X9221 will respond with an acknowledge after recognition of a start condition and its slave address and once again after successful receipt of the command byte. If the command is followed by a data byte the X9221 will respond with a final acknowledge.

Array Description

The X9221 is comprised of two resistor arrays. Each array contains 63 discrete resistive segments that are connected in series. The physical ends of each array are equivalent to the fixed terminals of a mechanical potentiometer (V_H and V_L inputs).

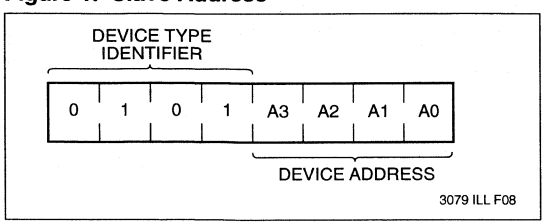
At both ends of each array and between each resistor segment is a FET switch connected to the wiper (V_W) output. Within each individual array only one switch may be turned on at a time. These switches are controlled by the Wiper Counter Register (WCR). The six least significant bits of the WCR are decoded to select, and enable, one of sixty-four switches.

The WCR may be written directly, or it can be changed by transferring the contents of one of four associated data registers into the WCR. These data registers and the WCR can be read and written by the host system.

Device Addressing

Following a start condition the master must output the address of the slave it is accessing. The most significant four bits of the slave address are the device type identifier (refer to Figure 1 below). For the X9221 this is fixed as 0101[B].

Figure 1. Slave Address

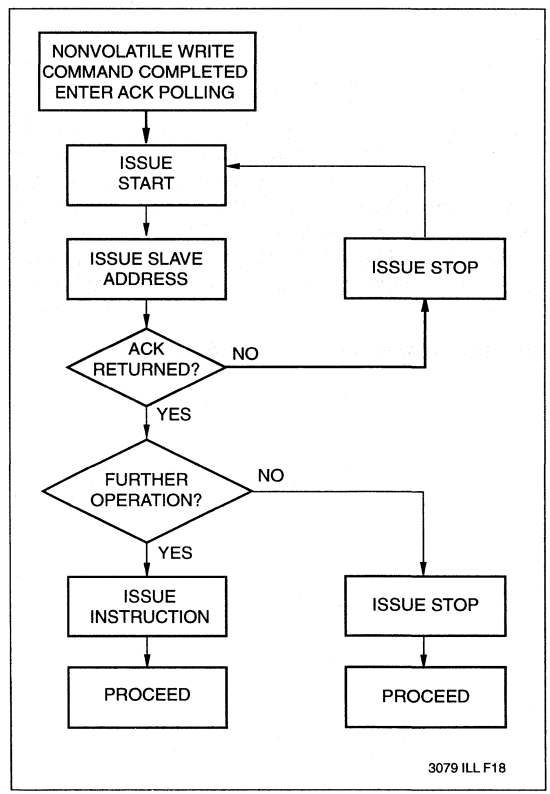


The next four bits of the slave address are the device address. The physical device address is defined by the state of the A0-A3 inputs. The X9221 compares the serial data stream with the address input state; a successful compare of all four address bits is required for the X9221 to respond with an acknowledge.

Acknowledge Polling

The disabling of the inputs, during the internal nonvolatile write operation, can be used to take advantage of the typical 5ms E²PROM write cycle time. Once the stop condition is issued to indicate the end of the nonvolatile write command the X9221 initiates the internal write cycle. ACK polling can be initiated immediately. This involves issuing the start condition followed by the device slave address. If the X9221 is still busy with the write operation no ACK will be returned. If the X9221 has completed the write operation an ACK will be returned and the master can then proceed with the next operation.

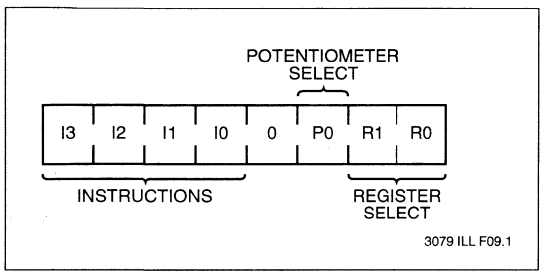
Flow 1. ACK Polling Sequence



Instruction Structure

The next byte sent to the X9221 contains the instruction and register pointer information. The four most significant bits are the instruction. The next four bits point to one of two pots and when applicable they point to one of four associated registers. The format is shown below in Figure 2.

Figure 2. Instruction Byte Format



The four high order bits define the instruction. The sixth bit (P0) selects which one of the two potentiometers is to be affected by the instruction. The last two bits (R1 and R0) select one of the four registers that is to be acted upon when a register oriented instruction is issued.

Four of the nine instructions end with the transmission of the instruction byte. The basic sequence is illustrated in Figure 3. These two-byte instructions exchange data between the WCR and one of the data registers. A transfer from a data register to a WCR is essentially a write to a static RAM. The response of the wiper to this action will be delayed t_{STPWV}. A transfer from WCR's current wiper position to a data register is a write to nonvolatile memory and takes a minimum of t_{WR} to complete. The transfer can occur between either potentiometer and their associated registers or it may occur between both of the potentiometers and one of their associated registers.

Four instructions require a three-byte sequence to complete. These instructions transfer data between the host and the X9221; either between the host and one of the data registers or directly between the host and the WCR. These instructions are: Read WCR, read the current wiper position of the selected pot; Write WCR, change current wiper position of the selected pot; Read Data Register, read the contents of the selected nonvolatile register; Write Data Register, write a new value to the selected data register. The sequence of operations is shown in Figure 4.

The Increment/Decrement command is different from the other commands. Once the command is issued and the X9221 has responded with an acknowledge, the master can clock the selected wiper up and/or down in one segment steps; thereby, providing a fine tuning capability to the host. For each SCL clock pulse (t_{HIGH}) while SDA is HIGH, the selected wiper will move one resistor segment towards the V_H terminal. Similarly, for each SCL clock pulse while SDA is LOW, the selected wiper will move one resistor segment towards the V_L terminal. A detailed illustration of the sequence and timing for this operation are shown in Figures 5 and 6 respectively.

Figure 3. Two-Byte Command Sequence

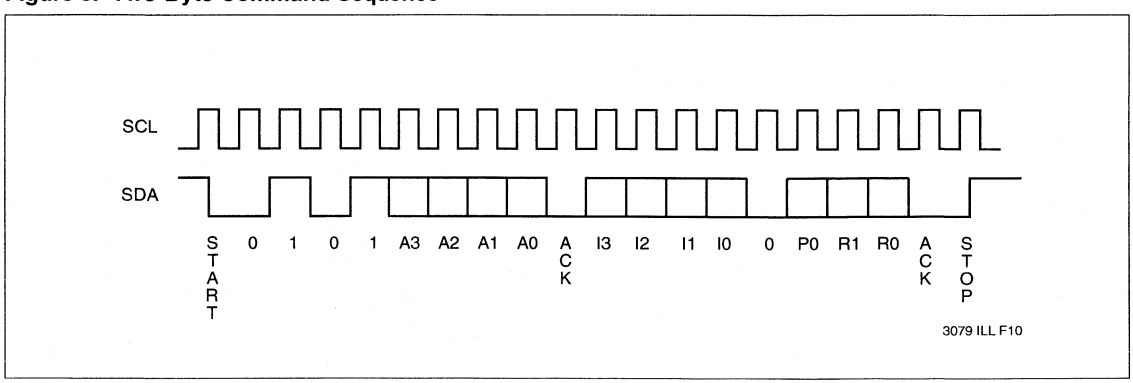


Figure 4. Three-Byte Command Sequence

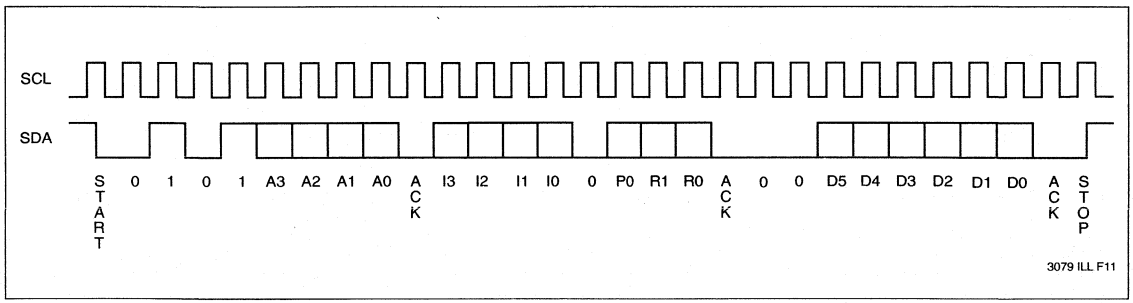


Figure 5. Increment/Decrement Command Sequence

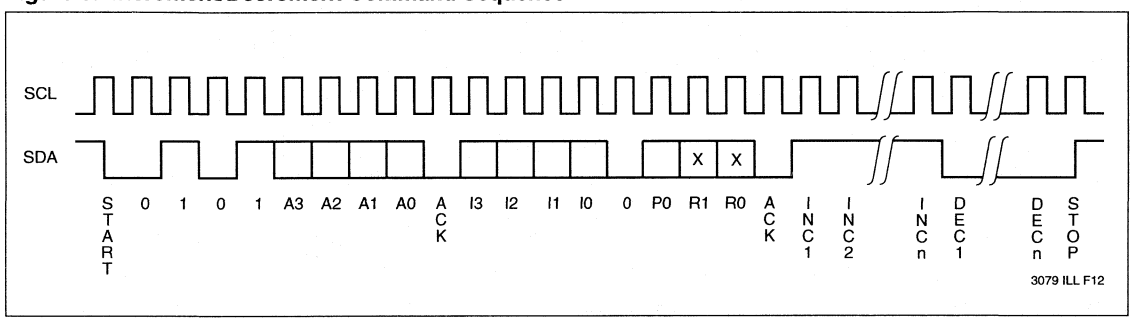


Figure 6. Increment/Decrement Timing Limits

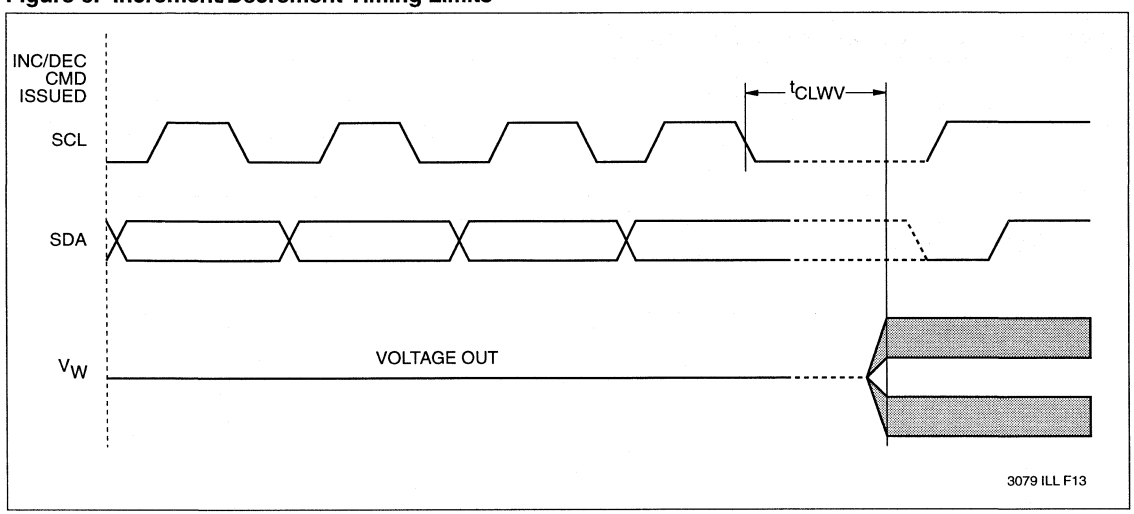


Table 1. Instruction Set

Instruction	Instruction Format								Operation
	I_3	I_2	I_1	I_0	0	P_0	R_1	R_0	
Read WCR	1	0	0	1	0	1/0	N/A(7)	N/A	Read the contents of the Wiper Counter Register pointed to by P_0
Write WCR	1	0	1	0	0	1/0	N/A	N/A	Write new value to the Wiper Counter Register pointed to by P_0
Read Data Register	1	0	1	1	0	1/0	1/0	1/0	Read the contents of the Register pointed to by P_0 and R_1–R_0
Write Data Register	1	1	0	0	0	1/0	1/0	1/0	Write new value to the Register pointed to by P_0 and R_1–R_0
XFR Data Register to WCR	1	1	0	1	0	1/0	1/0	1/0	Transfer the contents of the Register pointed to by P_0 and R_1–R_0 to its associated WCR
XFR WCR to Data Register	1	1	1	0	0	1/0	1/0	1/0	Transfer the contents of the WCR pointed to by P_0 to the Register pointed to by R_1–R_0
Global XFR Data Register to WCR	0	0	0	1	N/A	N/A	1/0	1/0	Transfer the contents of all four Data Registers pointed to by R_1–R_0 to their respective WCR
Global XFR WCR to Data Register	1	0	0	0	N/A	N/A	1/0	1/0	Transfer the contents of all WCRs to their respective data Registers pointed to by R_1–R_0
Increment/Decrement Wiper	0	0	1	0	0	1/0	N/A	N/A	Enable Increment/decrement of the WCR pointed to by P_0

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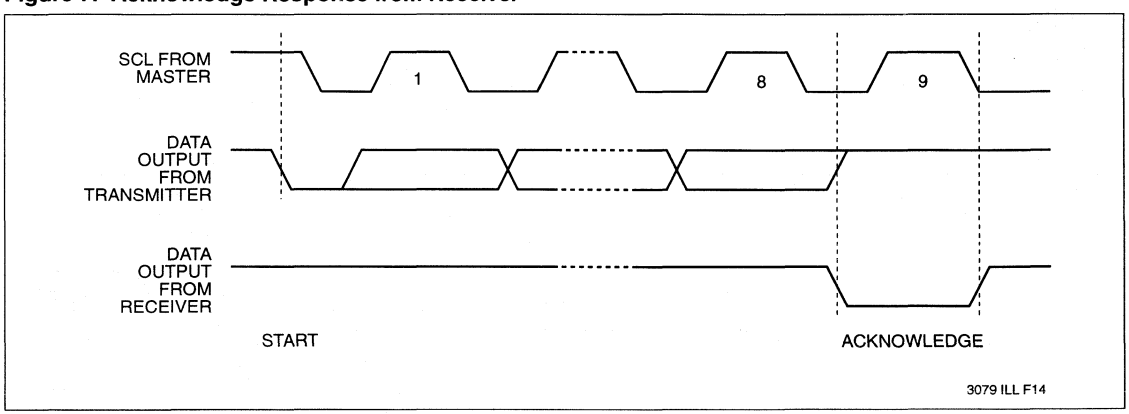
Notes: (7) N/A = Not applicable or don't care; that is, a data register is not involved in the operation and need not be addressed (typical)

Figure 7. Acknowledge Response from Receiver



DETAILED OPERATION

Both E²POT potentiometers share the serial interface and share a common architecture. Each potentiometer is comprised of a resistor array, a wiper counter register and four data registers. A detailed discussion of the register organization and array operation follows.

Wiper Counter Register

The X9221 contains two wiper counter registers (WCR), one for each E²POT potentiometer. The WCR can be envisioned as a 6-bit parallel and serial load counter with its outputs decoded to select one of sixty-four switches along its resistor array. The contents of the WCR can be altered in four ways: it may be written directly by the host via the Write WCR instruction (serial load); it may be written indirectly by transferring the contents of one of four associated data registers via the XFR Data Register instruction (parallel load); it can be modified one step at a time by the Increment/ Decrement instruction; finally, it is loaded with the contents of its data register zero (R0) upon power-up.

The WCR is a volatile register; that is, its contents are lost when the X9221 is powered-down. Although the register is automatically loaded with the value in R0 upon power-up, it should be noted this may be different from the value present at power-down.

Data Registers

Each potentiometer has four nonvolatile data registers. These can be read or written directly by the host and data can be transferred between any of the four data registers and the WCR. It should be noted all operations changing data in one of these registers is a nonvolatile operation and will take a maximum of 10ms.

If the application does not require storage of multiple settings for the potentiometer, these registers can be used as regular memory locations that could possibly store system parameters or user preference data.

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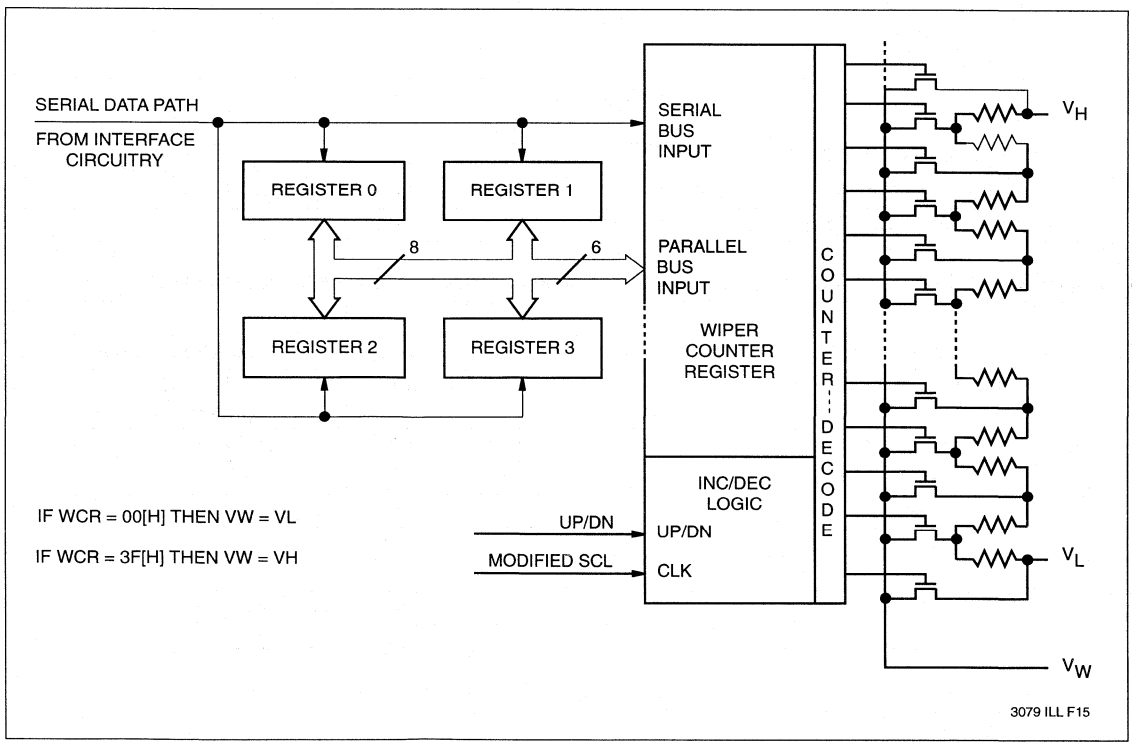
Figure 8. Detailed Potentiometer Block Diagram



ABSOLUTE MAXIMUM RATINGS*

Temperature under Bias ..... –65°C to +135°C
Storage Temperature ..... –65°C to +150°C
Voltage on SCK, SCL or any Address Input with Respect to V_{SS} ..... –1V to +7V
Voltage on any V_H or V_L Referenced to V_{SS} ..... ±8V
$\Delta V = |V_H - V_L|$ 16V
Lead Temperature (Soldering, 10 seconds) ..... 300°C

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	+70°C
Industrial	–40°C	+85°C
Military	–55°C	+125°C

3079 PGM T02

Supply Voltage	Limits
X9221	5V ±10%

3079 PGM T03.1

ANALOG CHARACTERISTICS (Over recommended operating conditions unless otherwise stated.)

Symbol	Parameter	Limits				Test Conditions
		Min.	Typ.	Max.	Units	
R_{TOTAL}	End to End Resistance	–20		+20	%	
	Power Rating			50	mW	25°C, each pot
I_W	Wiper Current	–1		+1	mA	
R_W	Wiper Resistance		40	100	Ω	Wiper Current = ± 1mA
V_{TERM}	Voltage on any V_H or or V_L Pin	–5		+5	V	
	Noise		≤120		dB/$\sqrt{Hz}$	Ref: 1V
	Resolution			1.6	%	
	Absolute Linearity (1)	–1		+1	MI(3)	$V_{w(n)(actual)} - V_{w(n)(expected)}$
	Relative Linearity (2)	–0.2		+0.2	MI(3)	$V_{w(n+1)} - [V_{w(n)} + MI]$
	Temperature Coefficient		±300		ppm/°C	

3079 PGM T04.2

D.C. OPERATING CHARACTERISTICS (Over recommended operating conditions unless otherwise stated.)

Symbol	Parameter	Limits				Test Conditions
		Min.	Typ.	Max.	Units	
I_{CC}	Supply Current (Active)			3	mA	f_{SCL} = 100KHz, SDA = Open, Other Inputs = V_{SS}
I_{SB}	V_{CC} Current (Standby)		200	500	µA	SCL=SDA=V_{CC}, Addr.= V_{SS}
I_{LI}	Input Leakage Current			10	µA	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output Leakage Current			10	µA	V_{OUT} = V_{SS} to V_{CC}
V_{IH}	Input HIGH Voltage	2		V_{CC} + 1	V	
V_{IL}	Input LOW Voltage	–1		0.8	V	
V_{OL}	Output LOW Voltage			0.4	V	I_{OL} = 3mA

3079 PGM T05.3

Notes: (1) Absolute Linearity is utilized to determine actual wiper voltage versus expected voltage as determined by wiper position when used as a potentiometer.
(2) Relative Linearity is utilized to determine the actual change in voltage between two successive tap positions when used as a potentiometer. It is a measure of the error in step size.
(3) MI = RTOT/63 or $(V_H - V_L)/63$, single pot

ENDURANCE AND DATA RETENTION

Parameter	Min.	Units
Minimum Endurance	100,000	Data Changes per Register
Data Retention	100	Years

3079 PGM T06.2

CAPACITANCE

Symbol	Parameter	Max.	Units	Test Conditions
$C_{I/O}$(5)	Input/Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}(5)	Input Capacitance (A0, A1, A2, A3 and SCL)	6	pF	V_{IN} = 0V

3079 PGM T07

POWER-UP TIMING

Symbol	Parameter	Max.	Units
t_{PUR}(6)	Power-up to Initiation of Read Operation	1	ms
t_{PUW}(6)	Power-up to Initiation of Write Operation	5	ms

3079 PGM T08

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A.C. CONDITIONS OF TEST

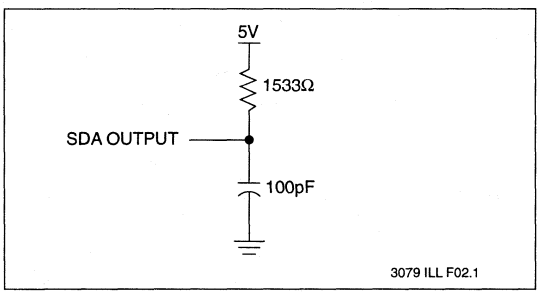
Input Pulse Levels	V_{CC} x 0.1 to V_{CC} x 0.9
Input Rise and Fall Times	10ns
Input and Output Timing Levels	V_{CC} x 0.5

3079 PGM T09

Notes: (5) This parameter is periodically sampled and not 100% tested.

(6) t_{PUR} and t_{PUW} are the delays required from the time VCC is stable until the specified operation can be initiated. These parameters are periodically sampled and not 100% tested.

EQUIVALENT A.C. TEST CIRCUIT



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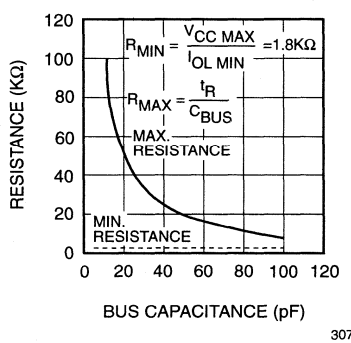
SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

Guidelines for Calculating Typical Values of Bus Pull-Up Resistors



3079 ILL F17

A.C. CHARACTERISTICS (Over recommended operating conditions unless otherwise stated)

Symbol	Parameter	Limits		Units	Reference Figure
		Min.	Max.		
f_{SCL}	SCL Clock Frequency	0	100	KHz	10
t_{LOW}	Clock LOW Period	4700		ns	10
t_{HIGH}	Clock HIGH Period	4000		ns	10
t_R	SCL and SDA Rise Time		1000	ns	10
t_F	SCL and SDA Fall Time		300	ns	10
Ti	Noise Suppression Time Constant (Glitch Filter)		100	ns	10
$t_{SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	4700		ns	10 & 12
$t_{HD:STA}$	Start Condition Hold Time	4000		ns	10 & 12
$t_{SU:DAT}$	Data in Setup Time	250		ns	10
$t_{HD:DAT}$	Data in Hold Time	0		ns	10
t_{AA}	SCL LOW to SDA Data Out Valid	300	3500	ns	11
t_{DH}	Data Out Hold Time	300		ns	11
$t_{SU:STO}$	Stop Condition Setup Time	4700		ns	10 & 12
t_{BUF}	Bus Free Time Prior to New Transmission	4700		ns	10
t_{WR}	Write Cycle Time (Nonvolatile Write Operation)		10	ms	13
t_{STPWV}	Wiper Response Time From Stop Generation		1000	µs	13
t_{CLWV}	Wiper Response From SCL LOW		500	µs	6
$t_R V_{CC}$	V_{CC} Power-up Rate	0.2	50	mV/µs	

3079 PGM T10.3

Figure 10. Input Bus Timing

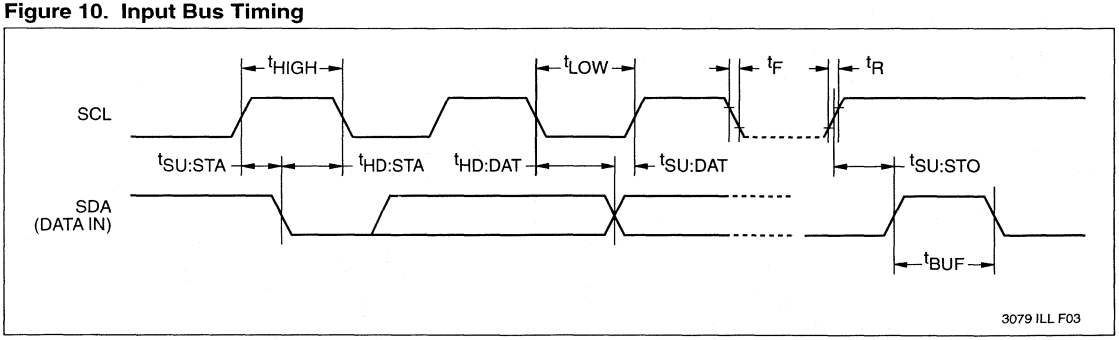


Figure 11. Output Bus Timing

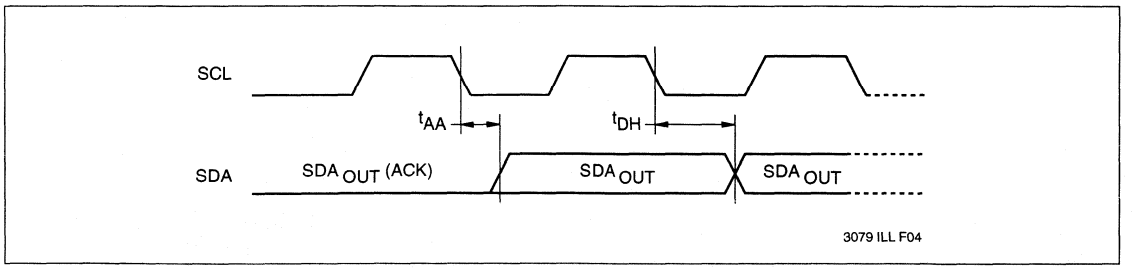


Figure 12. Start Stop Timing

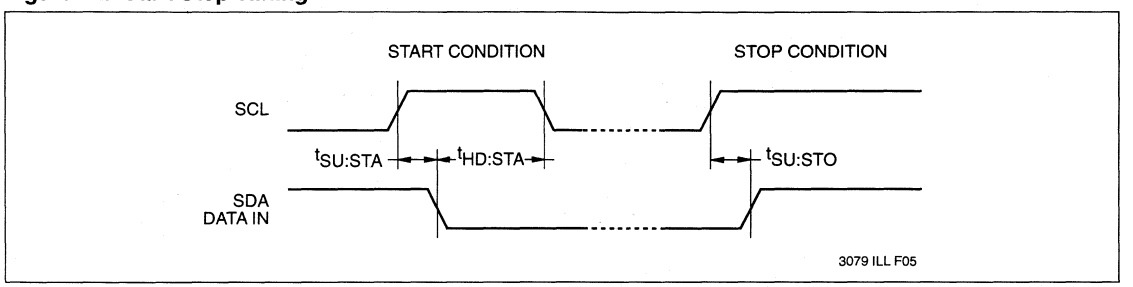
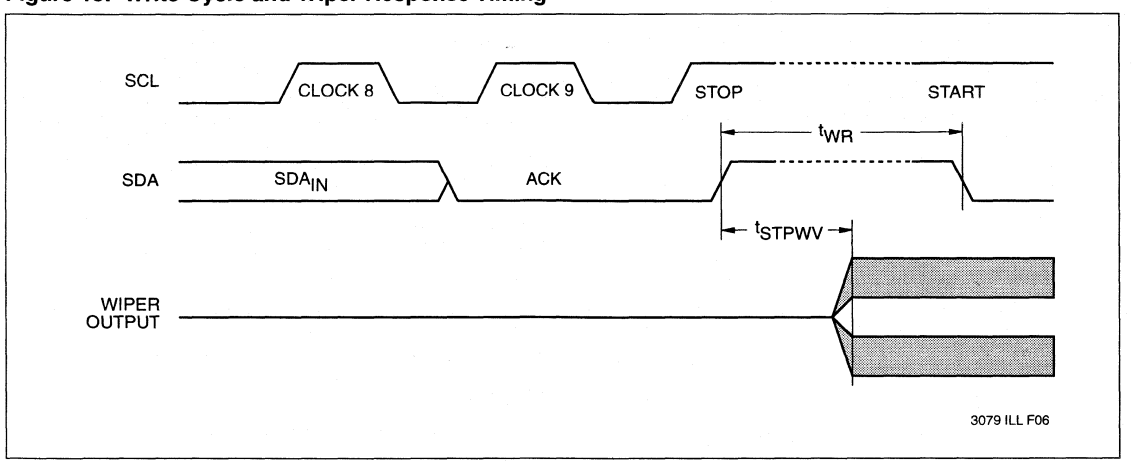
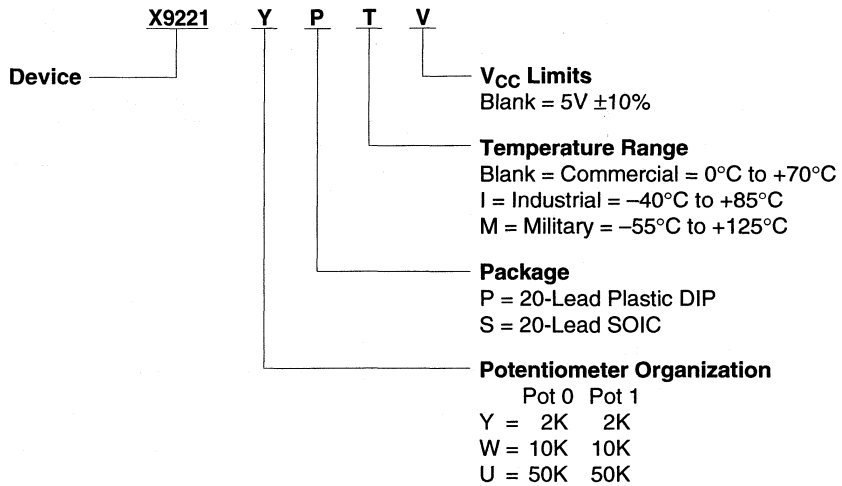


Figure 13. Write Cycle and Wiper Response Timing



ORDERING INFORMATION



NOTES

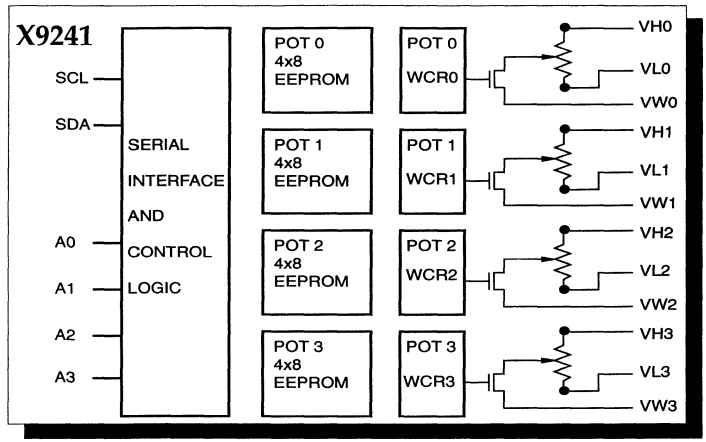
Xicor® #2

Design Engineers Bulletin

New Product and Applications Information for Design Engineers

Xicor's New X9241 Quad Potentiometer Allows Factory Automation of 64 Potentiometer Adjustments via a Digital Two Wire Serial Bus

For complex systems requiring multiple adjustment capability, Xicor offers the new X9241, Quad E²POT. In addition to retaining wiper positions without power, the X9241 offers a two-wire serial interface for controlling the potentiometers independently or simultaneously using microprocessor control commands. A user programmable address allows up to 16 devices to be software controlled via the common two wire serial bus.



Quad E²POT Development System

PC based system automates production adjustments of system potentiometers

The XK9241 can be used in a production environment to optimize the settings of the E²POT.

Faster analog circuit checkout and calibration is made possible by Xicor's new XK9241W Quad E²POT Development System. This system consists of an X9241 evaluation board, interface cables and software which allows a design engineer to control all functions of the Xicor X9241 Quad E²POT from a menu driven system on a IBM PC Compatible computer. The XK9241W Development System allows the design engineer to place the X9241 in a target analog system and perform all adjustments and configuration needed to recognize the features and benefits of the Quad E²POT.

The XK9241 PC based development system can also be used in production environments to automate potentiometer adjustments for initial system calibration.

The XK9241 supports all versions of the X9241 family. It can simultaneously control up to 16 different Quad E²POTs on the same two-wire bus to effectively allow adjustment of 64 individual E²POTs. Orders for the XK9241W can be placed with any authorized Xicor distributor.

Terminal Voltage ±5V, 64 Taps

X9241

Quad E²POT™ Nonvolatile Digital Potentiometer

FEATURES

- Four E²POTs in One Package
- Two-Wire Serial Interface
- Register Oriented Format
  - —Directly Write Wiper Position
  - —Read Wiper Position
  - —Store as Many as Four Positions per Pot
- Instruction Format
  - —Quick Transfer of Register Contents to Resistor Array
  - —Cascade Resistor Arrays
- Low Power CMOS
- Direct Write Cell
  - —Endurance - 100,000 Data Changes per Register
  - —Register Data Retention - 100 years
- 16 Bytes of E²PROM memory
- 3 Resistor Array Values
  - —2KΩ to 50KΩ Mask Programmable
  - —Cascadable For Values of 500Ω to 200KΩ
- Resolution: 64 Taps each Pot
- 20-Pin Plastic DIP, 20-Lead TSSOP and 20-Lead SOIC Packages

DESCRIPTION

The X9241 integrates four nonvolatile E²POT digitally controlled potentiometers on a monolithic CMOS microcircuit.

The X9241 contains four resistor arrays, each composed of 63 resistive elements. Between each element and at either end are tap points accessible to the wiper elements. The position of the wiper element on the array is controlled by the user through the two-wire serial bus interface.

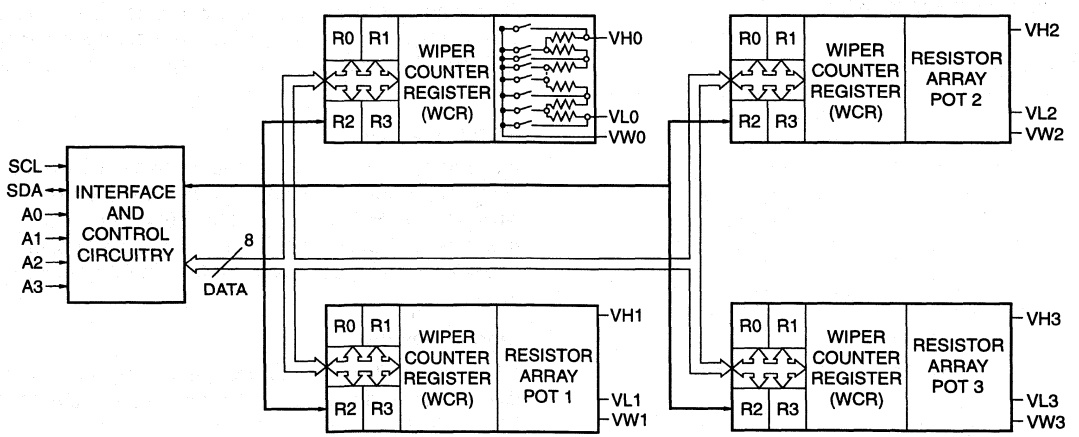
Each resistor array has associated with it a wiper counter register and four 8-bit data registers that can be directly written and read by the user. The contents of the wiper counter register control the position of the wiper on the resistor array.

The data register may be read or written by the user. The contents of the data registers can be transferred to the wiper counter register to position the wiper. The current wiper position can be transferred to any one of its associated data registers.

The arrays may be cascaded to form resistive elements with 127, 190 or 253 taps.

4

FUNCTIONAL DIAGRAM



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PIN DESCRIPTIONS

Host Interface Pins

Serial Clock (SCL)

The SCL input is used to clock data into and out of the X9241.

Serial Data (SDA)

SDA is a bidirectional pin used to transfer data into and out of the device. It is an open drain output and may be wire-ORed with any number of open drain or open collector outputs. An open drain output requires the use of a pull-up resistor. For selecting typical values, refer to the guidelines for calculating typical values on the bus pull-up resistors graph.

Address

The Address inputs are used to set the least significant 4 bits of the 8-bit slave address. A match in the slave address serial data stream must be made with the Address input in order to initiate communication with the X9241.

Potentiometer Pins

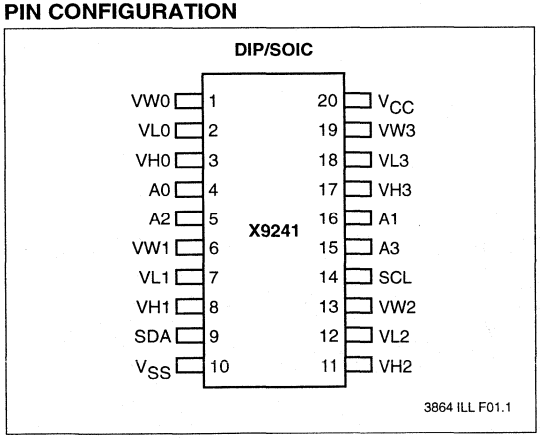
V_H (V_{H0} – V_{H3}), V_L (V_{L0} – V_{L3})

The VH and VL inputs are equivalent to the terminal connections on either end of a mechanical potentiometer.

V_W (V_{W0} – V_{W3})

The wiper outputs are equivalent to the wiper output of a mechanical potentiometer.

PIN CONFIGURATION



PIN NAMES

Symbol	Description
SCL	Serial Clock
SDA	Serial Data
A0–A3	Address
V_{H0}–V_{H3}, V_{L0}–V_{L3}	Potentiometers (terminal equivalent)
V_{W0}–V_{W3}	Potentiometers (wiper equivalent)

3864 PGM T01

PRINCIPLES OF OPERATION

The X9241 is a highly integrated microcircuit incorporating four resistor arrays, their associated registers and counters and the serial interface logic providing direct communication between the host and the E²POT potentiometers.

Serial Interface

The X9241 supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is a master and the device being controlled is the slave. The master will always initiate data transfers and provide the clock for both transmit and receive operations. Therefore, the X9241 will be considered a slave device in all applications.

Clock and Data Conventions

Data states on the SDA line can change only during SCL LOW periods (t_{LOW}). SDA state changes during SCL HIGH are reserved for indicating start and stop conditions.

Start Condition

All commands to the X9241 are preceded by the start condition, which is a HIGH to LOW transition of SDA while SCL is HIGH (t_{HIGH}). The X9241 continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition is met.

Stop Condition

All communications must be terminated by a stop condition, which is a LOW to HIGH transition of SDA while SCL is HIGH.

Acknowledge

Acknowledge is a software convention used to provide a positive handshake between the master and slave devices on the bus to indicate the successful receipt of data. The transmitting device, either the master or the slave, will release the SDA bus after transmitting eight bits. The master generates a ninth clock cycle and during this period the receiver pulls the SDA line LOW to acknowledge that it successfully received the eight bits of data. See Figure 7.

The X9241 will respond with an acknowledge after recognition of a start condition and its slave address and once again after successful receipt of the command byte. If the command is followed by a data byte the X9241 will respond with a final acknowledge.

Array Description

The X9241 is comprised of four resistor arrays. Each array contains 63 discrete resistive segments that are connected in series. The physical ends of each array are equivalent to the fixed terminals of a mechanical potentiometer (V_H and V_L inputs).

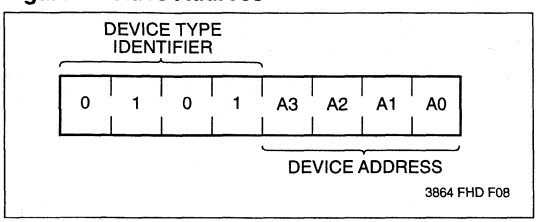
At both ends of each array and between each resistor segment is a FET switch connected to the wiper (V_W) output. Within each individual array only one switch may be turned on at a time. These switches are controlled by the Wiper Counter Register (WCR). The six least significant bits of the WCR are decoded to select, and enable, one of sixty-four switches.

The WCR may be written directly, or it can be changed by transferring the contents of one of four associated data registers into the WCR. These data registers and the WCR can be read and written by the host system.

Device Addressing

Following a start condition the master must output the address of the slave it is accessing. The most significant four bits of the slave address are the device type identifier (refer to Figure 1 below). For the X9241 this is fixed as 0101[B].

Figure 1. Slave Address

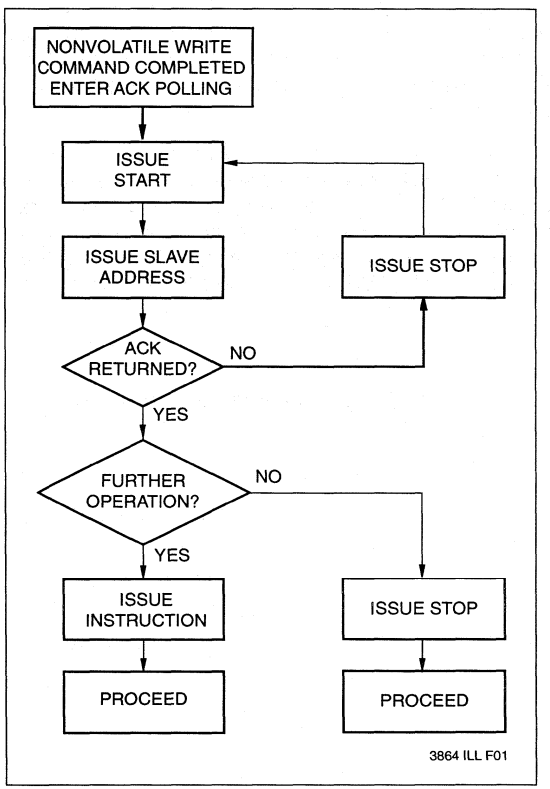


The next four bits of the slave address are the device address. The physical device address is defined by the state of the A0-A3 inputs. The X9241 compares the serial data stream with the address input state; a successful compare of all four address bits is required for the X9241 to respond with an acknowledge.

Acknowledge Polling

The disabling of the inputs, during the internal nonvolatile write operation, can be used to take advantage of the typical 5ms E²PROM write cycle time. Once the stop condition is issued to indicate the end of the nonvolatile write command the X9241 initiates the internal write cycle. ACK polling can be initiated immediately. This involves issuing the start condition followed by the device slave address. If the X9241 is still busy with the write operation no ACK will be returned. If the X9241 has completed the write operation an ACK will be returned and the master can then proceed with the next operation.

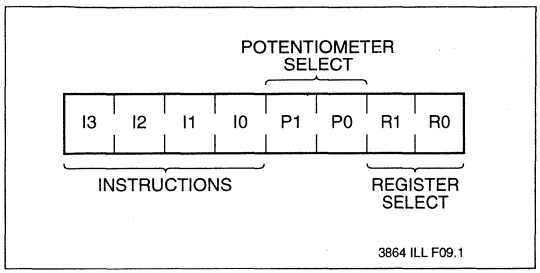
Flow 1. ACK Polling Sequence



Instruction Structure

The next byte sent to the X9241 contains the instruction and register pointer information. The four most significant bits are the instruction. The next four bits point to one of four pots and when applicable they point to one of four associated registers. The format is shown below in Figure 2.

Figure 2. Instruction Byte Format



The four high order bits define the instruction. The next two bits (P1 and P0) select which one of the four potentiometers is to be affected by the instruction. The last two bits (R1 and R0) select one of the four registers that is to be acted upon when a register oriented instruction is issued.

Four of the nine instructions end with the transmission of the instruction byte. The basic sequence is illustrated in Figure 3. These two-byte instructions exchange data between the WCR and one of the data registers. A transfer from a data register to a WCR is essentially a write to a static RAM. The response of the wiper to this action will be delayed t_{STPWV}. A transfer from WCR current wiper position, to a data register is a write to nonvolatile memory and takes a minimum of t_{WR} to complete. The transfer can occur between one of the four potentiometers and one of its associated registers; or it may occur globally, wherein the transfer occurs between all four of the potentiometers and one of their associated registers.

Four instructions require a three-byte sequence to complete. These instructions transfer data between the host and the X9241; either between the host and one of the data registers or directly between the host and the WCR. These instructions are: Read WCR, read the current wiper position of the selected pot; Write WCR, change current wiper position of the selected pot; Read Data Register, read the contents of the selected nonvolatile register; Write Data Register, write a new value to the selected data register. The sequence of operations is shown in Figure 4.

The Increment/Decrement command is different from the other commands. Once the command is issued and the X9241 has responded with an acknowledge, the master can clock the selected wiper up and/or down in one segment steps; thereby, providing a fine tuning capability to the host. For each SCL clock pulse (t_{HIGH}) while SDA is HIGH, the selected wiper will move one resistor segment towards the V_H terminal. Similarly, for each SCL clock pulse while SDA is LOW, the selected wiper will move one resistor segment towards the V_L terminal. A detailed illustration of the sequence and timing for this operation are shown in Figures 5 and 6 respectively.

Figure 3. Two-Byte Command Sequence

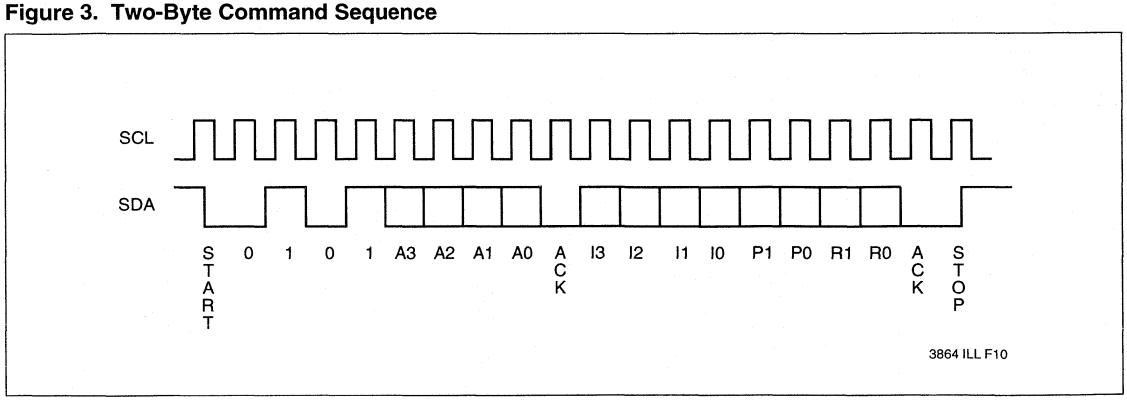


Figure 4. Three-Byte Command Sequence

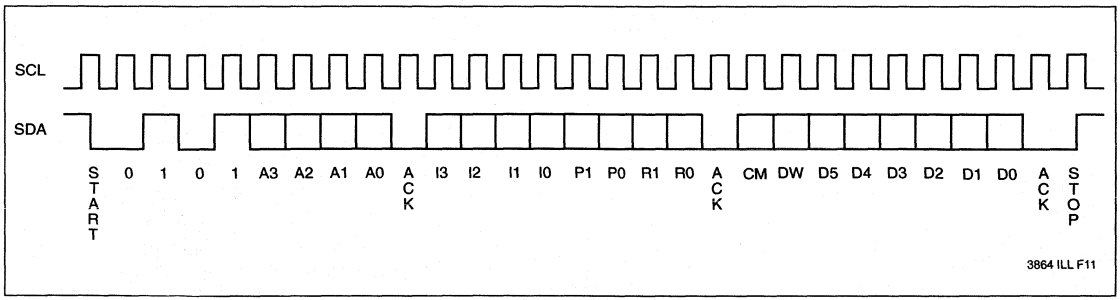


Figure 5. Increment/Decrement Command Sequence

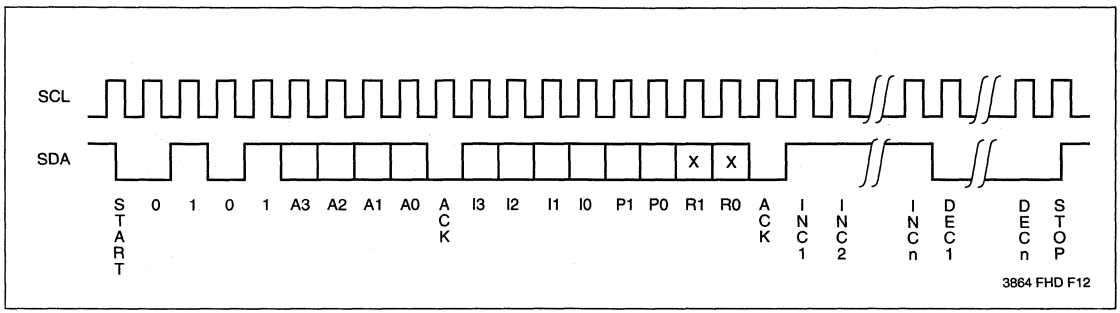


Figure 6. Increment/Decrement Timing Limits

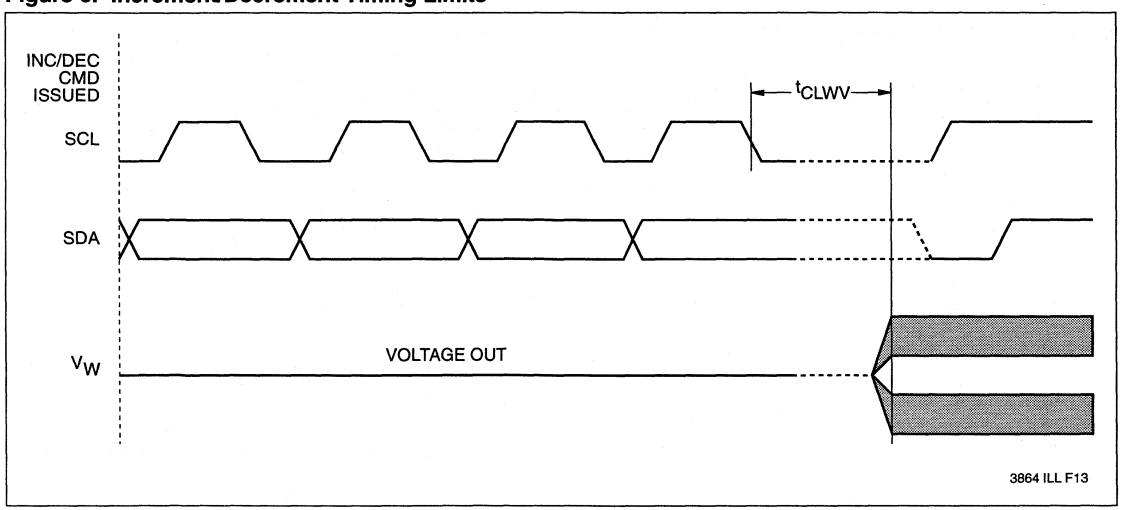


Table 1. Instruction Set

Instruction	Instruction Format								Operation
	I_3	I_2	I_1	I_0	P_1	P_0	R_1	R_0	
Read WCR	1	0	0	1	1/0(7)	1/0	N/A(8)	N/A	Read the contents of the Wiper Counter Register pointed to by P_1–P_0
Write WCR	1	0	1	0	1/0	1/0	N/A	N/A	Write new value to the Wiper Counter Register pointed to by P_1–P_0
Read Data Register	1	0	1	1	1/0	1/0	1/0	1/0	Read the contents of the Register pointed to by P_1–P_0 and R_1–R_0
Write Data Register	1	1	0	0	1/0	1/0	1/0	1/0	Write new value to the Register pointed to by P_1–P_0 and R_1–R_0
XFR Data Register to WCR	1	1	0	1	1/0	1/0	1/0	1/0	Transfer the contents of the Register pointed to by P_1–P_0 and R_1–R_0 to its associated WCR
XFR WCR to Data Register	1	1	1	0	1/0	1/0	1/0	1/0	Transfer the contents of the WCR pointed to by P_1–P_0 to the Register pointed to by R_1–R_0
Global XFR Data Register to WCR	0	0	0	1	N/A	N/A	1/0	1/0	Transfer the contents of all four Data Registers pointed to by R_1–R_0 to their respective WCR
Global XFR WCR to Data Register	1	0	0	0	N/A	N/A	1/0	1/0	Transfer the contents of all WCRs to their respective data Registers pointed to by R_1–R_0
Increment/Decrement Wiper	0	0	1	0	1/0	1/0	N/A	N/A	Enable Increment/decrement of the WCR pointed to by P_1–P_0

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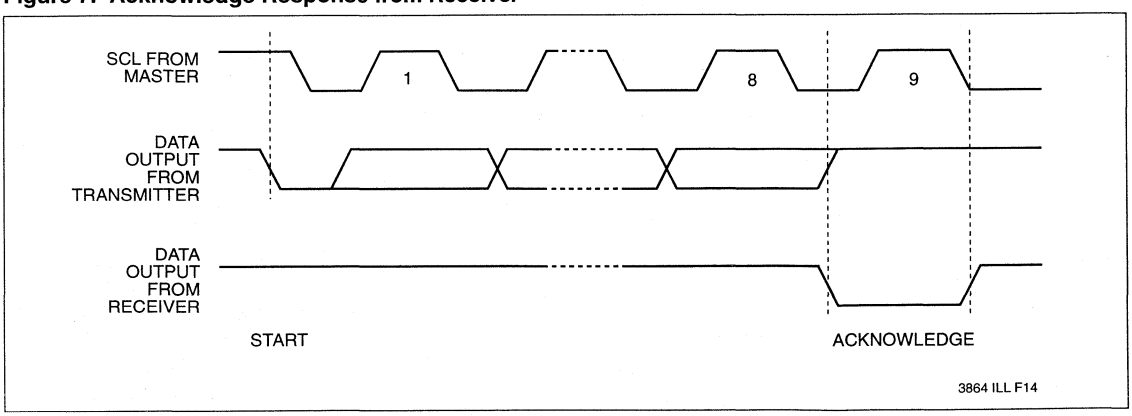
Notes: (7) 1/0 = data is one or zero
(8) N/A = Not applicable or don't care; that is, a data register is not involved in the operation and need not be addressed (typical)

Figure 7. Acknowledge Response from Receiver



DETAILED OPERATION

All four E²POT potentiometers share the serial interface and share a common architecture. Each potentiometer is comprised of a resistor array, a wiper counter register and four data registers. A detailed discussion of the register organization and array operation follows.

Wiper Counter Register

The X9241 contains four wiper counter registers (WCR), one for each E²POT potentiometer. The WCR can be envisioned as a 6-bit parallel and serial load counter with its outputs decoded to select one of sixty-four switches along its resistor array. The contents of the WCR can be altered in four ways: it may be written directly by the host via the Write WCR instruction (serial load); it may be written indirectly by transferring the contents of one of four associated data registers via the XFR Data Register instruction (parallel load); it can be modified one step at a time by the Increment/ Decrement instruction; finally, it is loaded with the contents of its data register zero (R0) upon power-up.

The WCR is a volatile register; that is, its contents are lost when the X9241 is powered-down. Although the register is automatically loaded with the value in R0 upon power-up, it should be noted this may be different from the value present at power-down.

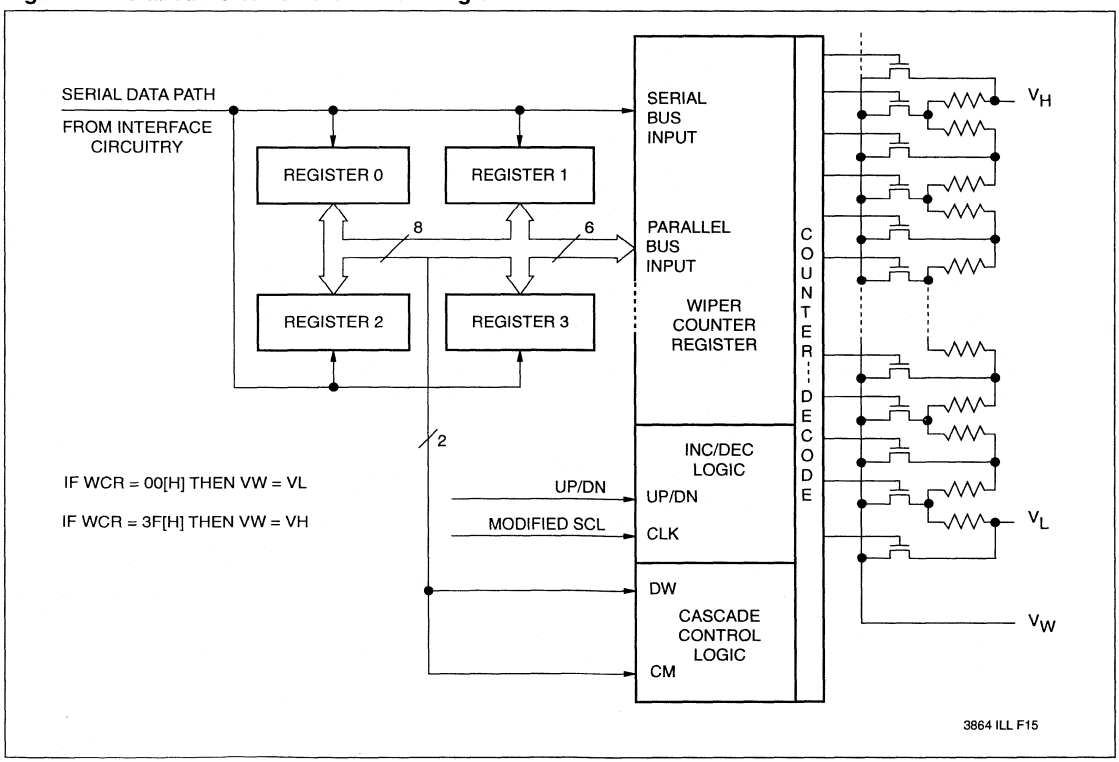
Data Registers

Each potentiometer has four nonvolatile data registers. These can be read or written directly by the host and data can be transferred between any of the four data registers and the WCR. It should be noted all operations changing data in one of these registers is a nonvolatile operation and will take a maximum of 10ms.

If the application does not require storage of multiple settings for the potentiometer, these registers can be used as regular memory locations that could possibly store system parameters or user preference data.

4

Figure 8. Detailed Potentiometer Block Diagram



Cascade Mode

The X9241 provides a mechanism for cascading the arrays. That is, the sixty-three resistor elements of one array may be cascaded (linked) with the resistor elements of an adjacent array.

Cascade Control Bits

The data byte, for the three-byte commands, contains 6 bits (LSBs) for defining the wiper position plus two high order bits, CM (Cascade Mode) and DW (Disable Wiper).

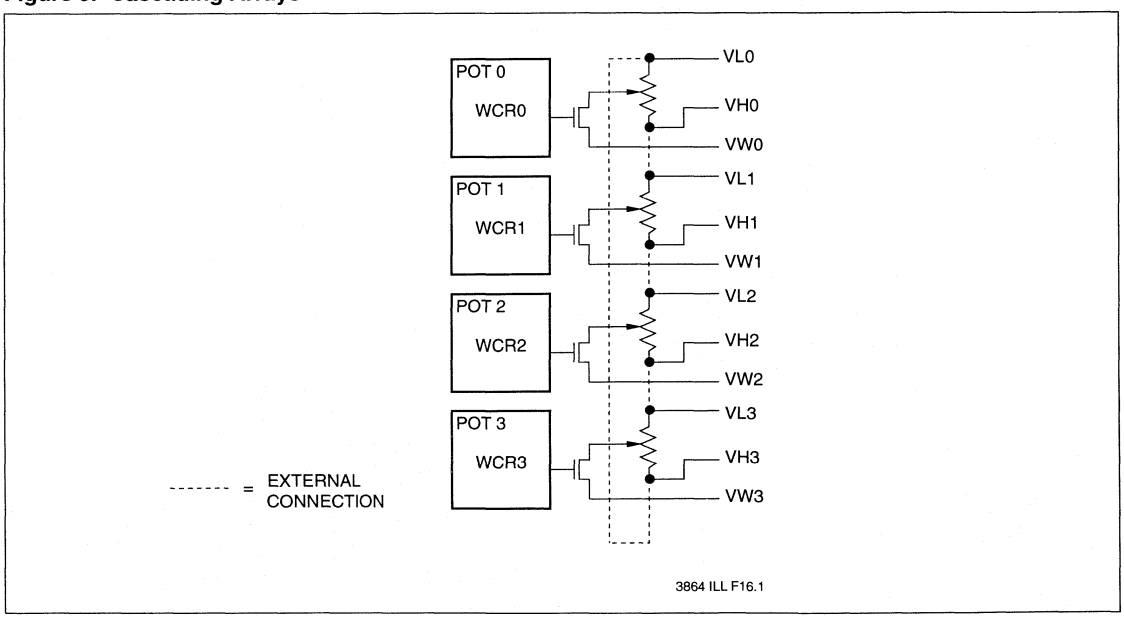
The state of CM enables or disables (normal operation) cascade mode. When the CM bit of the WCR is set to "0" the potentiometer is in the normal operation mode. When the CM bit of the WCR is set to "1" the potentiometer is cascaded with its adjacent higher order potentiometer. For example; if bit 7 of WCR2 is set to "1", pot 2 will be cascaded to pot 3.

The state of DW enables or disables the wiper. When the DW bit of the WCR is set to "0" the wiper is enabled; when set to "1" the wiper is disabled. If the wiper is disabled, the wiper terminal will be electrically isolated and float.

When operating in cascade mode VH, VL and the wiper terminals of the cascaded arrays must be electrically connected externally. All but one of the wipers must be disabled. The user can alter the wiper position by writing directly to the WCR or indirectly by transferring the contents of the data registers to the WCR or by using the Increment/Decrement command.

When using the Increment/Decrement command the wiper position will automatically transition between arrays. The current position of the wiper can be determined by reading the WCR registers; if the DW bit is "0", the wiper in that array is active. If the current wiper position is to be maintained, a global XFR WCR to Data Register command must be issued before power-down.

Figure 9. Cascading Arrays



ABSOLUTE MAXIMUM RATINGS*

Temperature under Bias ..... –65°C to +135°C
Storage Temperature ..... –65°C to +150°C
Voltage on SCK, SCL or any Address Input with Respect to V_{SS} ..... –1V to +7V
Voltage on any V_H or V_L Referenced to V_{SS} ..... ±8V
$\Delta V = |V_H - V_L|$ 16V
Lead Temperature (Soldering, 10 seconds) ..... 300°C

***COMMENT**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	+70°C
Industrial	–40°C	+85°C
Military	–55°C	+125°C

3864 PGM T03

Supply Voltage	Limits
X9241	5V ±10%

3864 PGM T04.1

ANALOG CHARACTERISTICS (Over recommended operating conditions unless otherwise stated.)

Symbol	Parameter	Limits				Test Conditions
		Min.	Typ.	Max.	Units	
R_{TOTAL}	End to End Resistance	–20		+20	%	
	Power Rating			50	mW	25°C, each pot
I_W	Wiper Current	–1		+1	mA	
R_W	Wiper Resistance		40	100	Ω	Wiper Current = ± 1mA
V_{TERM}	Voltage on any V_H or or V_L Pin	–5		+5	V	
	Noise		≤120		dB/$\sqrt{Hz}$	Ref: 1V
	Resolution (4)		1.6	0.4	%	
	Absolute Linearity (1)	–1		+1	MI(3)	$V_{w(n)(actual)} - V_{w(n)(expected)}$
	Relative Linearity (2)	–0.2		+0.2	MI(3)	$V_{w(n+1)} - [V_{w(n)} + MI]$
	Temperature Coefficient		±300		ppm/°C	

3864 PGM T05.2

D.C. OPERATING CHARACTERISTICS (Over recommended operating conditions unless otherwise stated.)

Symbol	Parameter	Limits				Test Conditions
		Min.	Typ.	Max.	Units	
I_{CC}	Supply Current (Active)			3	mA	f_{SCL} = 100KHz, SDA = Open, Other Inputs = V_{SS}
I_{SB}	V_{CC} Current (Standby)		200	500	µA	SCL=SDA=V_{CC}, Addr. = V_{SS}
I_{LI}	Input Leakage Current			10	µA	$V_{IN} = V_{SS}$ to V_{CC}
I_{LO}	Output Leakage Current			10	µA	$V_{OUT} = V_{SS}$ to V_{CC}
V_{IH}	Input HIGH Voltage	2		V_{CC} + 1	V	
V_{IL}	Input LOW Voltage	–1		0.8	V	
V_{OL}	Output LOW Voltage			0.4	V	I_{OL} = 3mA

3864 PGM T06.3

Notes: (1) Absolute Linearity is utilized to determine actual wiper voltage versus expected voltage as determined by wiper position when used as a potentiometer.
(2) Relative Linearity is utilized to determine the actual change in voltage between two successive tap positions when used as a potentiometer. It is a measure of the error in step size.
(3) MI = RTOT/63 or $(V_H - V_L)/63$, single pot
(4) Max. = all four arrays cascaded together, Typical = individual array resolutions.

ENDURANCE AND DATA RETENTION

Parameter	Min.	Units
Minimum Endurance	100,000	Data Changes per Register
Data Retention	100	Years

3864 PGM T07.2

CAPACITANCE

Symbol	Parameter	Max.	Units	Test Conditions
$C_{I/O}$(5)	Input/Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}(5)	Input Capacitance (A0, A1, A2, A3 and SCL)	6	pF	V_{IN} = 0V

3864 PGM T08

POWER-UP TIMING

Symbol	Parameter	Max.	Units
t_{PUR}(6)	Power-up to Initiation of Read Operation	1	ms
t_{PUW}(6)	Power-up to Initiation of Write Operation	5	ms

3864 PGM T09

A.C. CONDITIONS OF TEST

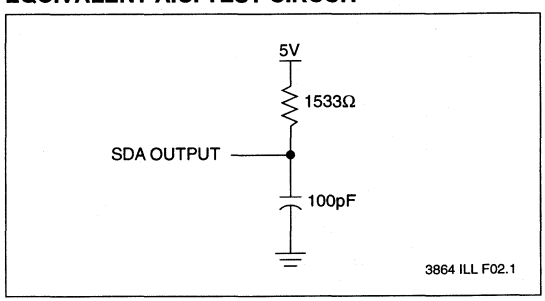
Input Pulse Levels	V_{CC} x 0.1 to V_{CC} x 0.9
Input Rise and Fall Times	10ns
Input and Output Timing Levels	V_{CC} x 0.5

3864 PGM T10

Notes: (5) This parameter is periodically sampled and not 100% tested.

(6) t_{PUR} and t_{PUW} are the delays required from the time VCC is stable until the specified operation can be initiated. These parameters are periodically sampled and not 100% tested.

EQUIVALENT A.C. TEST CIRCUIT

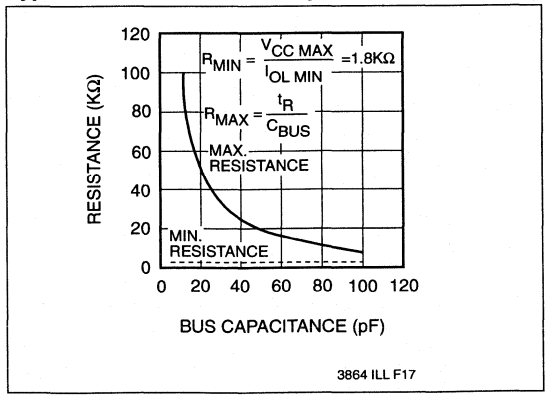


3864 ILL F02.1

SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

Guidelines for Calculating Typical Values of Bus Pull-Up Resistors



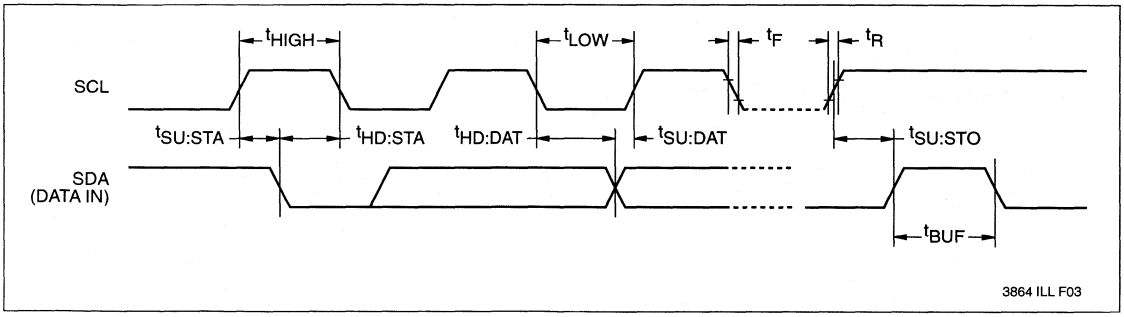
3864 ILL F17

A.C. CHARACTERISTICS (Over recommended operating conditions unless otherwise stated)

Symbol	Parameter	Limits		Units	Reference Figure
		Min.	Max.		
f_{SCL}	SCL Clock Frequency	0	100	KHz	10
t_{LOW}	Clock LOW Period	4700		ns	10
t_{HIGH}	Clock HIGH Period	4000		ns	10
t_R	SCL and SDA Rise Time		1000	ns	10
t_F	SCL and SDA Fall Time		300	ns	10
Ti	Noise Suppression Time Constant (Glitch Filter)		100	ns	10
$t_{SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	4700		ns	10 & 12
$t_{HD:STA}$	Start Condition Hold Time	4000		ns	10 & 12
$t_{SU:DAT}$	Data in Setup Time	250		ns	10
$t_{HD:DAT}$	Data in Hold Time	0		ns	10
t_{AA}	SCL LOW to SDA Data Out Valid	300	3500	ns	11
t_{DH}	Data Out Hold Time	300		ns	11
$t_{SU:STO}$	Stop Condition Setup Time	4700		ns	10 & 12
t_{BUF}	Bus Free Time Prior to New Transmission	4700		ns	10
t_{WR}	Write Cycle Time (Nonvolatile Write Operation)		10	ms	13
t_{STPWV}	Wiper Response Time From Stop Generation		500	μs	13
t_{CLWV}	Wiper Response From SCL LOW		1000	μs	6
$t_R V_{CC}$	V_{CC} Power-up Rate	0.2	50	mV/μs	

3864 PGM T11.3

Figure 10. Input Bus Timing



3864 ILL F03

Figure 11. Output Bus Timing

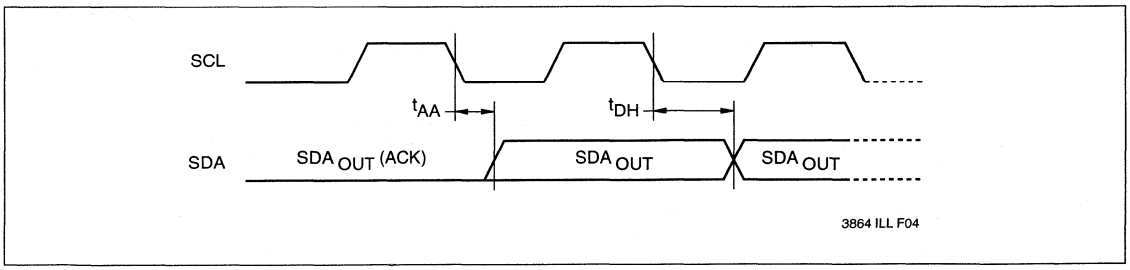


Figure 12. Start Stop Timing

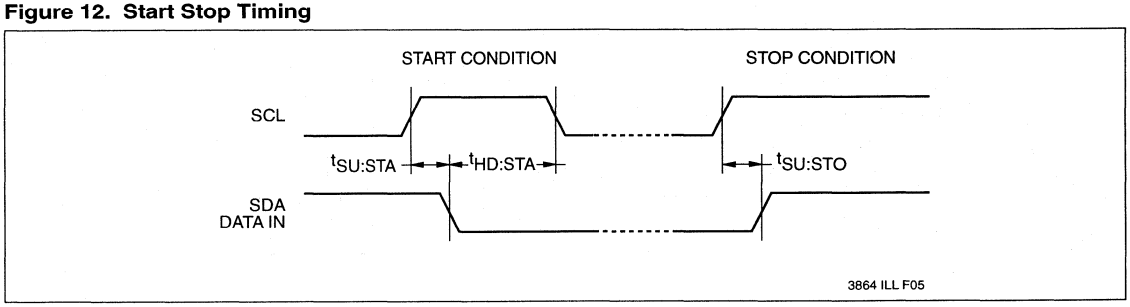
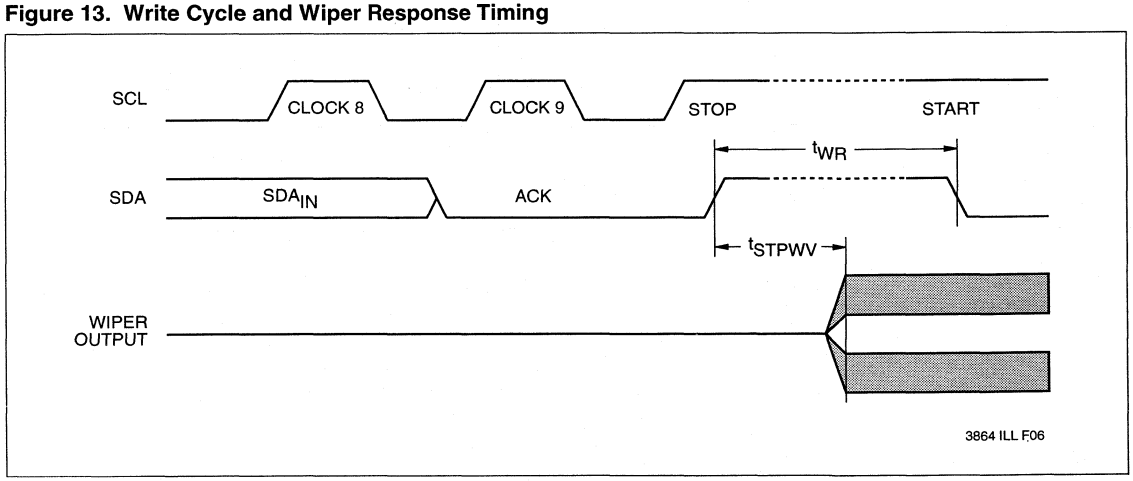
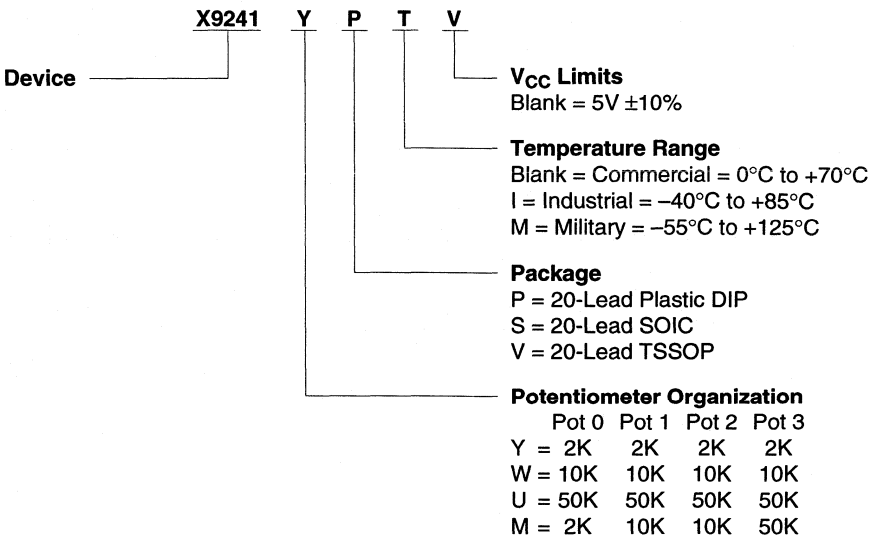


Figure 13. Write Cycle and Wiper Response Timing



ORDERING INFORMATION



4

NOTES

Xicor®

3807-2.3 12/4/95 T12/C0/D0 NS

64K X68C64 8192 x 8 Bit

E² Micro-Peripheral

FEATURES

- CONCURRENT READ WRITE™
  - —Dual Plane Architecture
    - —Isolates Read/Write Functions Between Planes
    - —Allows Continuous Execution of Code From One Plane While Writing in the Other Plane
- Multiplexed Address/Data Bus
  - —Direct Interface to Popular 8-bit Microcontrollers, e.g., Motorola M6801/03, M68HC11 Family
- High Performance CMOS
  - —Fast Access Time, 120ns
  - —Low Power
    - —60mA Maximum Active
    - —500μA Maximum Standby
- Software Data Protection
- Block Protect Register
  - —Individually Set Write Lock Out in 1K Blocks
- Toggle Bit Polling
  - —Early End of Write Detection
- Page Mode Write
  - —Allows up to 32 Bytes to be Written in One Write Cycle
- High Reliability
  - —Endurance: 100,000 Write Cycles
  - —Data Retention: 100 Years

DESCRIPTION

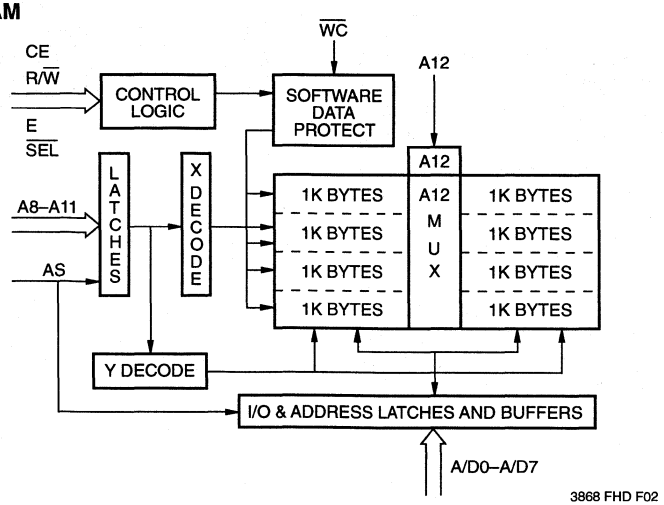
The X68C64 is an 8K x 8 E²PROM fabricated with advanced CMOS Textured Poly Floating Gate Technology. The X68C64 features a Multiplexed Address and Data bus allowing a direct interface to a variety of popular single-chip microcontrollers operating in expanded multiplexed mode without the need for additional interface circuitry.

The X68C64 is internally configured as two independent 4K x 8 memory arrays. This feature provides the ability to perform nonvolatile memory updates in one array and continue operation out of code stored in the other array; effectively eliminating the need for an auxiliary memory device for code storage.

To write to the X68C64, a three-byte command sequence must precede the byte(s) being written. The X68C64 also provides a second generation software data protection scheme called Block Protect. Block Protect can provide write lockout of the entire device or selected 1K blocks. There are eight 1K x 8 blocks that can be write protected individually in any combination required by the user. Block Protect, in addition to Write Control input, allows the different segments of the memory to have varying degrees of alterability in normal system operation.

5

FUNCTIONAL DIAGRAM



CONCURRENT READ WRITE™ is a trademark of Xicor, Inc.

PIN DESCRIPTIONS

Address/Data (A/D_0–A/D_7)

Multiplexed low-order addresses and data. The addresses flow into the device while AS is HIGH. After AS transitions from a HIGH to LOW the addresses are latched. Once the addresses are latched these pins input data or output data depending on E, R/$\overline{W}$, and CE.

Addresses (A_8–A_{12})

High order addresses flow into the device when AS is HIGH and are latched when AS goes LOW.

Chip Enable (CE)

The Chip Enable input must be HIGH to enable all read/write operations. When CE is LOW and AS is LOW, the X68C64 is placed in the low power standby mode.

Enable (E)

When used with a MC6801 or MC6803, the E input is tied directly to the E output of the microcontroller.

Read/Write (R/$\overline{W}$)

When used with a MC6801 or MC6803, the R/$\overline{W}$ input is tied directly to the R/$\overline{W}$ output of the microcontroller.

Address Strobe (AS)

Addresses flow through the latches to address decoders when AS is HIGH and are latched when AS transitions from a HIGH to LOW.

Device Select ($\overline{SEL}$)

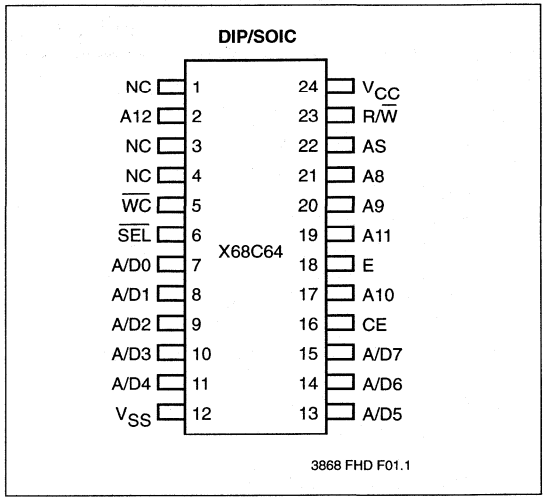
Must be connected to V_{SS}.

Write Control ($\overline{WC}$)

The Write Control allows external circuitry to abort a page load cycle once it has been initiated. This input is useful in applications in which a power failure or processor RESET could interrupt a page load cycle. In this case, the microcontroller might drive all signals HIGH, causing bad data to be latched into the E^2PROM. If the Write Control input is driven HIGH (before t_{TBLC} Max) after Read/Write (R/$\overline{W}$) goes HIGH, the write cycle will be aborted.

When $\overline{WC}$ is LOW (tied to V_{SS}) the X68C64 will be enabled to perform write operations. When $\overline{WC}$ is HIGH normal read operations may be performed, but all attempts to write to the device will be disabled.

PIN CONFIGURATION



PIN NAMES

Symbol	Description
AS	Address Strobe
A/D_0–A/D_7	Address Inputs/Data I/O
A_8–A_{12}	Address Inputs
E	Enable Input
R/$\overline{W}$	Read/Write Input
CE	Chip Enable
$\overline{WC}$	Write Control
$\overline{SEL}$	Device Select—Connect to V_{SS}
V_{SS}	Ground
V_{CC}	Supply Voltage
NC	No Connect

3868 PGM T01.1

PRINCIPLES OF OPERATION

The X68C64 is a highly integrated peripheral device for a wide variety of single-chip microcontrollers. The X68C64 provides 8K bytes of E²PROM which can be used either for Program Storage, Data Storage, or a combination of both in systems based upon Von Neumann (68XX) architectures. The X68C64 incorporates the interface circuitry normally needed to decode the control signals and demultiplex the Address/Data bus to provide a "Seamless" interface.

The interface inputs on the X68C64 are configured such that it is possible to directly connect them to the proper interface signals of the appropriate single-chip microcontroller.

The X68C64 is internally organized as two independent planes of 4K bytes of memory with the A_{12} input selecting which of the two planes of memory are to be accessed. While the processor is executing code out of one plane, write operations can take place in the other plane, allowing the processor to continue execution of code out of the X68C64 during a byte or page write to the device.

The X68C64 also features an advanced implementation of the Software Data Protection scheme, called Block Protect, which allows the device to be broken into 8 independent sections of 1K bytes. Each of these sections can be independently enabled for write operations; thereby allowing certain sections of the device to be secured so that updates can only occur in a controlled environment (e.g. in an automotive application, only at an authorized service center). The desired set-up configuration is stored in a nonvolatile register, ensuring the configuration data will be maintained after the device is powered down.

The X68C64 also features a Write Control input ($\overline{WC}$), which serves as an external control over the completion of a previously initiated page load cycle.

The X68C64 also features the industry standard E²PROM characteristics such a byte or page mode write and Toggle Bit Polling.

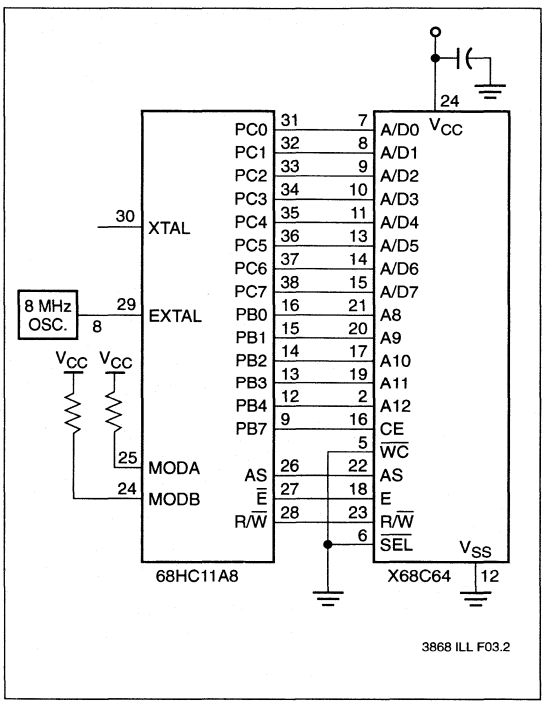
DEVICE OPERATION

Motorola 68XX operation requires the microcontroller's AS, E, and R/$\overline{W}$ outputs tied to the X68C64 AS, E, and R/$\overline{W}$ inputs respectively.

The falling edge of AS will latch the addresses for both a read and write operation. The state of R/$\overline{W}$ output determines the operation to be performed, with the E signal acting as a data strobe.

If R/$\overline{W}$ is HIGH and CE HIGH (read operation), data will be output on A/D_0–A/D_7 after E transitions HIGH. If R/$\overline{W}$ is LOW and CE is HIGH (write operation), data presented at A/D_0–A/D_7 will be strobed into the X68C64 on the HIGH to LOW transition of E.

Typical Application



MODE SELECTION

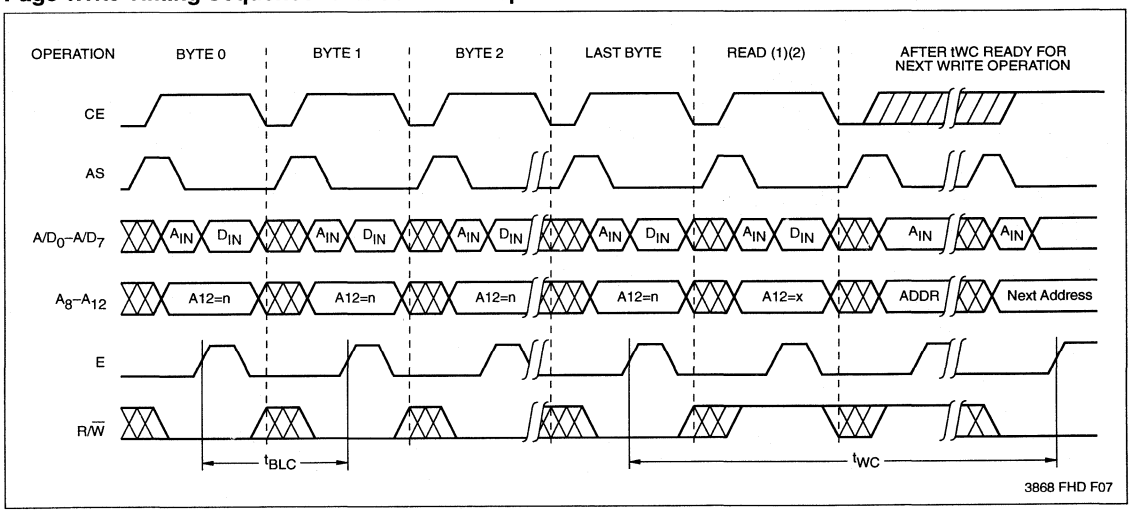
CE	E	R/$\overline{W}$	Mode	I/O	Power
V_{SS}	X	X	Standby	High Z	Standby (CMOS)
LOW	X	X	Standby	High Z	Standby (TTL)
HIGH	HIGH	HIGH	Read	D_{OUT}	Active
HIGH	⌝⌞	LOW	Write	D_{IN}	Active

3868 PGM T02.1

PAGE WRITE OPERATION

Regardless of the microcontroller employed, the X68C64 supports page mode write operations. This allows the microcontroller to write from one to thirty-two bytes of data to the X68C64. Each individual write within a page write operation must conform to the byte write timing requirements. The rising edge of E starts a timer delaying the internal programming cycle 100µs. Therefore, each successive write operation must begin within 100µs of the last byte written. The following waveforms illustrate the sequence and timing requirements.

Page Write Timing Sequence for E Controlled Operation

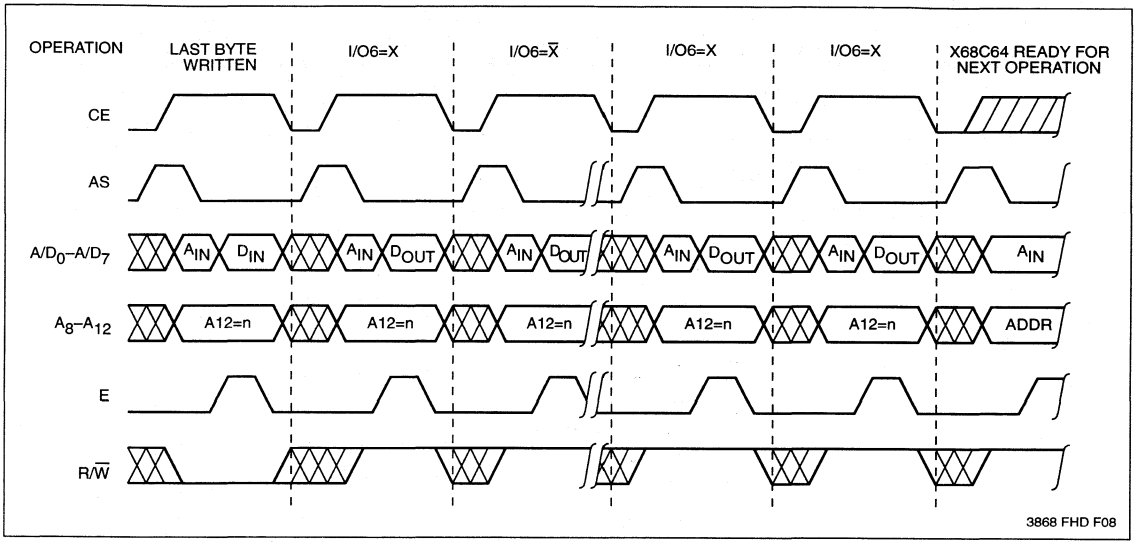


Notes: (1) For each successive write within a page write cycle A_5–A_{12} must be the same.
(2) Although it is not illustrated, the microcontroller may interleave read operations between the individual byte writes within the page write operation. Two responses are possible.
a. Reading from the same plane being written (A_{12} of Read = A_{12} of Write) is effectively a Toggle Bit Polling operation.
b. Reading from the opposite plane being written (A_{12} of Read ≠ A_{12} of Write) true data will be returned, facilitating the use of a single memory component as both program and data storage.

Toggle Bit Polling

Because the X68C64 typical nonvolatile write cycle time is less than the specified 5ms, Toggle Bit Polling has been provided to determine the early completion of write. During the internal programming cycle, I/O_6 will toggle from HIGH to LOW and LOW to HIGH on subsequent attempts to read the device. When the internal cycle is complete, the toggling will cease and the device will be accessible for additional read or write operations. Due to the dual plane architecture, reads for polling must occur in the plane that is being written; that is, the state of A_{12} during a write must match the state of A_{12} during Toggle Bit Polling.

Toggle Bit Polling E Control



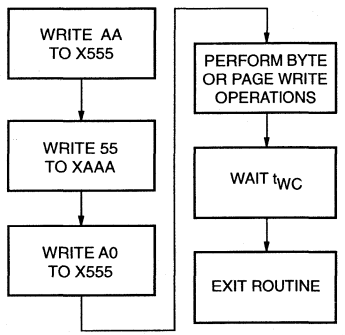
SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

DATA PROTECTION

The X68C64 provides two levels of data protection through software control. There is a global software data protection feature similar to the industry standard for E²PROMs and a new Block Protect write lockout protection providing a secondary level of data security.

Writing with SDP



$X = A_{12}$:

A_{12} = 1 IF DATA TO BE WRITTEN IS WITHIN ADDRESS 1000 TO 1FFF.

A_{12} = 0 IF DATA TO BE WRITTEN IS WITHIN ADDRESS 0000 TO 0FFF.

3868 FHD F09

Software Data Protection

Software Data Protection (SDP) is employed to protect the entire array against inadvertent writes. To write to the X68C64, a three-byte command sequence must precede the byte(s) being written.

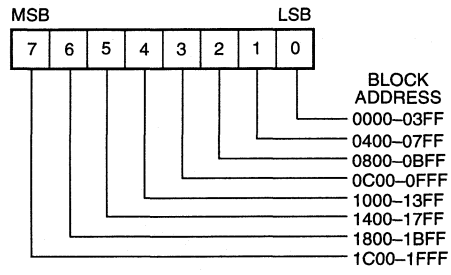
All write operations, both the command sequence and any data write operations, must conform to the page write timing requirements.

Block Protect Write Lockout

The X68C64 provides a secondary level of data security referred to as Block Protect write lockout. This is accessed through an extension of the SDP command sequence. Block Protect allows the user to lockout writes to any 1K x 8 blocks of memory. Unlike SDP which prevents inadvertent writes, but still allows easy system access to writing the memory, Block Protect will lockout all attempts unless it is specifically disabled by the host. This could be used to set a higher level of protection in a system where a portion of the memory is used for Program Storage and another portion is used as Data Storage.

Setting write lockout is accomplished by writing a five-byte command sequence, opening access to the Block Protect Register (BPR). After the fifth byte is written, the user writes to the BPR, selecting which blocks to protect or unprotect. All write operations, both the command sequence and writing the data to the BPR, must conform to the page write timing requirements.

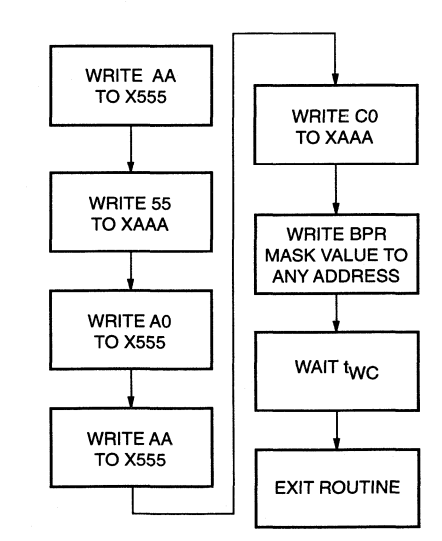
Block Protect Register Format



1 = Protect, 0 = Unprotect Block Specified

3868 FHD F11

Setting BPR Command Sequence



$X = A_{12}$:

A_{12} = 1 IF PROGRAM BEING EXECUTED IS WITHIN 0000 TO 0FFF.

A_{12} = 0 IF PROGRAM BEING EXECUTED RESIDES WITHIN 1000 TO 1FFF.

3868 FHD F12

ABSOLUTE MAXIMUM RATINGS*

Temperature under Bias ..... –65°C to +135°C
Storage Temperature ..... –65°C to +150°C
Voltage on any Pin with
Respect to V_{SS} ..... –1V to +7V
D.C. Output Current 5mA
Lead Temperature
(Soldering, 10 seconds) ..... 300°C

***COMMENT**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	+70°C
Industrial	–40°C	+85°C
Military	–55°C	+125°C

3868 PGM T03.1

Supply Voltage	Limits
X68C64	5V ±10%

3868 PGM T04.1

D.C. OPERATING CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
I_{CC}	V_{CC} Current (Active)		60	mA	CE = V_{IL}, All I/O's = Open, Other Inputs = V_{CC}, AS = V_{IH}
$I_{SB1(CMOS)}$	V_{CC} Current (Standby)		500	µA	CE = V_{SS}, All I/O's = Open,Other Inputs = V_{CC} – 0.3V, AS = V_{SS}
$I_{SB2(TTL)}$	V_{CC} Current (Standby)		6	mA	CE = V_{IH}, All I/O's = Open, Other Inputs = V_{IH}, AS = V_{IL}
I_{LI}	Input Leakage Current		10	µA	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output Leakage Current		10	µA	V_{OUT} = V_{SS} to V_{CC}, E = V_{IL}
V_{IL}(1)	Input LOW Voltage	–1	0.8	V	
V_{IH}(1)	Input HIGH Voltage	2	V_{CC} + 0.5	V	
V_{OL}	Output LOW Voltage		0.4	V	I_{OL} = 2.1mA
V_{OH}	Output HIGH Voltage	2.4		V	I_{OH} = –400µA

3868 PGM T05.1

CAPACITANCE T_A = +25°C, f = 1MHz, V_{CC} = 5V

Symbol	Test	Max.	Units	Conditions
$C_{I/O}$(2)	Input/Output Capacitance	10	pF	$V_{I/O}$ = 0V
C_{IN}(2)	Input Capacitance	6	pF	V_{IN} = 0V

3868 PGM T06

POWER-UP TIMING

Symbol	Parameter	Max.	Units
t_{PUR}(2)	Power-Up to Read	1	ms
t_{PUW}(2)	Power-Up to Write	5	ms

3868 PGM T07

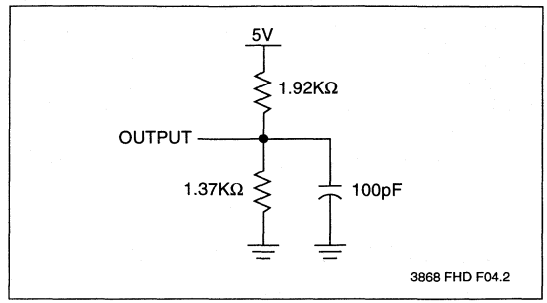
Notes: (1) V_{IL} min. and V_{IH} max. are for reference only and are not tested.
(2) This parameter is periodically sampled and not 100% tested.

A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3V
Input Rise and Fall Times	10ns
Input and Output Timing Levels	1.5V

3868 PGM T08.1

TEST CIRCUIT



3868 FHD F04.2

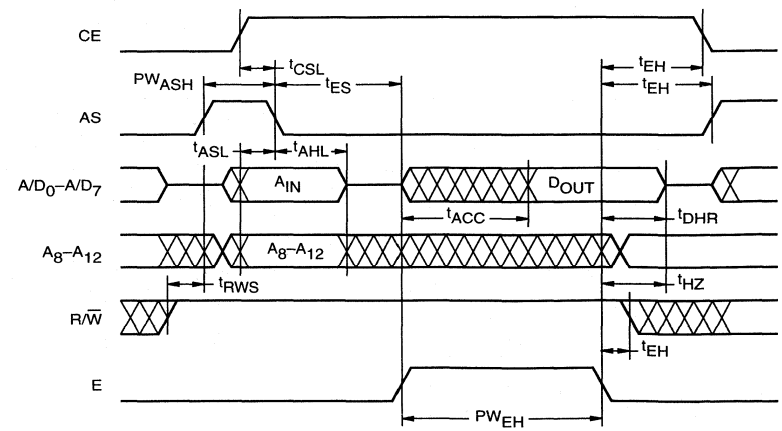
A.C. CHARACTERISTICS (Over the recommended operating conditions unless otherwise specified.)

E Controlled Read Cycle

Symbol	Parameter	Min.	Max.	Units
PW_{ASH}	Address Strobe Pulse Width	80		ns
t_{ASL}	Address Setup Time	20		ns
t_{AHL}	Address Hold Time	30		ns
t_{ACC}	Data Access Time		120	ns
t_{DHR}	Data Hold Time	0		ns
t_{CSL}	CE Setup Time	7		ns
PW_{EH}	E Pulse Width	150		ns
t_{ES}	Enable Setup Time	30		ns
t_{EH}	E Hold Time	20		ns
t_{RWS}	R/$\overline{W}$ Setup Time	20		ns
t_{HZ}(3)	E LOW to High Z Output		50	ns
t_{LZ}(3)	E HIGH to Low Z Output	0		ns

3868 PGM T09.1

E Controlled Read Cycle



3868 FHD F05

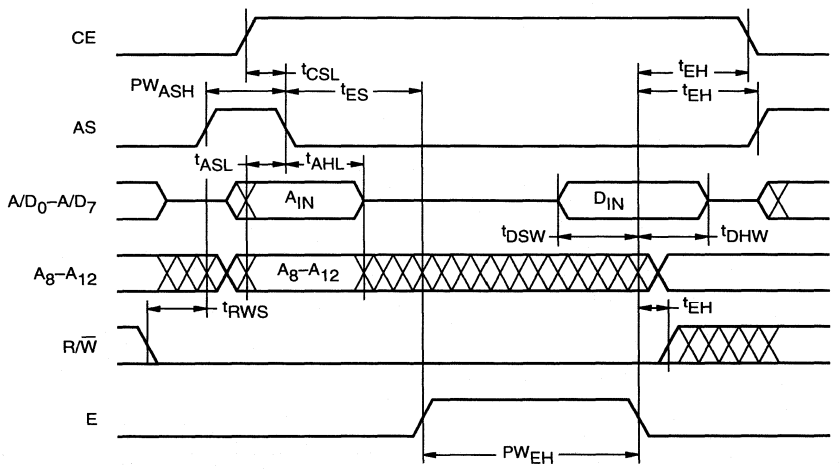
Note: (3) This parameter is periodically sampled and not 100% tested.

E Controlled Write Cycle

Symbol	Parameter	Min.	Max.	Units
PW_{ASH}	Address Strobe Pulse Width	80		ns
t_{ASL}	Address Setup Time	20		ns
t_{AHL}	Address Hold Time	30		ns
t_{DSW}	Data Setup Time	50		ns
t_{DHW}	Data Hold Time	30		ns
t_{CSL}	CE Setup Time	7		ns
PW_{EH}	E Pulse Width	120		ns
t_{WC}	Write Cycle Time		5	ms
t_{ES}	Enable Setup Time	30		ns
t_{RWS}	R/$\overline{W}$ Setup Time	20		ns
t_{EH}	E Hold Time	20		ns
t_{BLC}	Byte Load Time (Page Write)	0.5	100	µs

3868 PGM T10

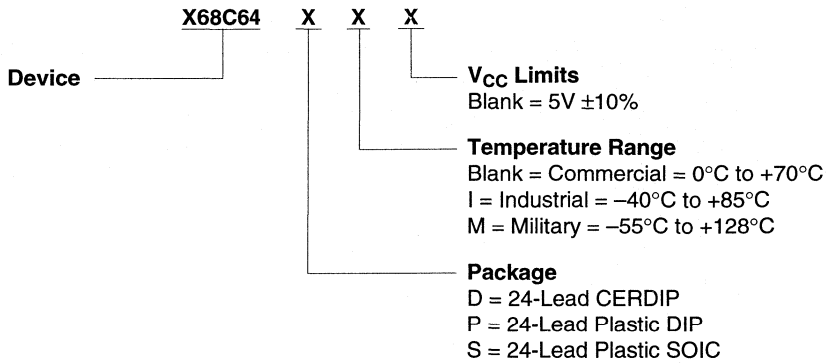
E Controlled Write Cycle



3868 FHD F06

Note: (4) t_{WC} is the minimum cycle time to be allowed from the system perspective unless polling techniques are used. It is the maximum time the device requires to automatically complete the internal write operation.

ORDERING INFORMATION



APPLICATION NOTES AND DEVELOPMENT SYSTEM
AVAILABLE
AN62 • AN64 • AN66 • AN68 • AN74 • XK68

68HC11 Microcontroller Family Compatible

64K X68C64 SLIC® E^2 8192 x 8 Bit

E^2 Micro-Peripheral

FEATURES

SLIC (SELF LOADING INTEGRATED CODE) FIRMWARE

- **Automatically Downloads User's Software into 68HC11 Based Systems**
- **Features Load, Verify, and Block Protection Capabilities**
- **Transfers Baud Rate 9600 at 8MHz**
- **Concurrent Read Write™**
  - **—Dual Plane Architecture**
    - **—Isolates Read/Write Functions Between Planes**
    - **—Allows Continuous Execution of Code From One Plane While Writing in the Other Plane**
- **Multiplexed Address/Data Bus**
  - **—Direct Interface to Popular 68HC11 Family**
- **Block Protect Register**
  - **—Individually Set Write Lock Out in 1K Blocks**
- **Toggle Bit Polling**
  - **—Early End of Write Detection**
- **Page Mode Write**
  - **—Allows up to 32 Bytes to be Written in One Write Cycle**

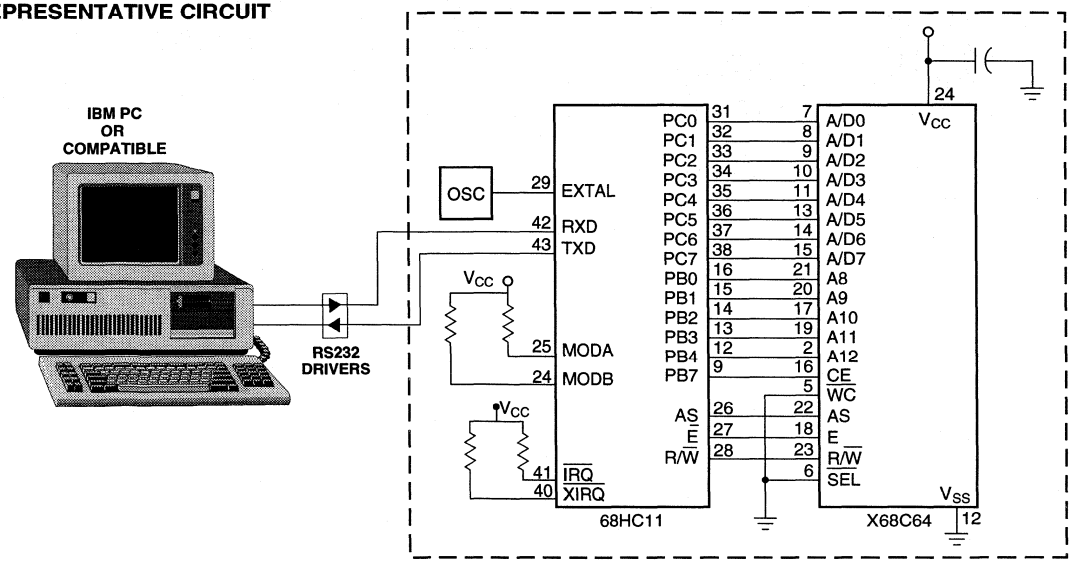
DESCRIPTION

The X68C64 SLIC E^2 is a highly integrated E^2 Microcontroller peripheral which combines the functionality of the X68C64 component with pre-loaded software routines allowing any embedded system using it to upgrade and download software via the serial port. This self-loading integrated code eliminates the need to initially program the firmware into a memory device at the time of initial manufacture. The SLIC E^2 routines also greatly facilitate the loading of subsequent versions of the firmware into the system.

The SLIC E^2 routines consist of approximately 500 bytes of instructions for the 68HC11 which will initialize the microcontroller and its on-board UART and upload the user's software through the UART. The baud rate for the transfer is 9600 based on a crystal frequency of 8MHz. Data transfer is accomplished using a proprietary format called XCOM. Xicor also has developed a program for IBM PCs and compatibles called XSLIC, which will translate an Intel HEX or Motorola S-record format file into XCOM format and download the program to a X68C64 SLIC E^2.

5

REPRESENTATIVE CIRCUIT



2134 ILL F01.2

SLIC® E^2 and CONCURRENT READ WRITE™ are trademarks of Xicor, Inc.

The X68C64 component is an 8K x 8 E^2PROM fabricated with advanced CMOS Textured Poly Floating Gate Technology. The X68C64 features a Multiplexed Address and Data bus allowing direct interface to a variety of popular single-chip microcontrollers operating in expanded multiplexed mode without the need for additional interface circuitry.

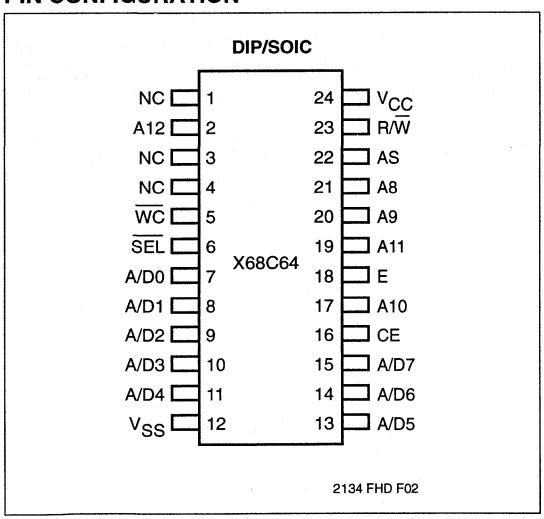
The X68C64 is internally configured as two independent 4K x 8 memory arrays. This feature provides the ability to perform nonvolatile memory updates in one array and continue operation out of code stored in the other array; effectively eliminating the need for an auxiliary memory device for code storage.

To write to the X68C64 SLIC E^2, a three-byte command sequence must precede the byte(s) being written. This sequence called Software Data Protection prevents the loss of data or program information due to inadvertant write cycles during power-up or power-down. The X68C64 SLIC E^2 also provides a second generation software data protection scheme called Block Protect.

Block Protect can provide write lockout of the entire device or selected 1K blocks. There are eight 1K x 8 blocks that can be write protected individually in any combination required by the user. Block Protect, in additional to Write Control input, allows the different segments of the memory to have varying degrees of alterability in normal system operation.

For further information on the X68C64 hardware interface, consult the X68C64 Data Sheet.

PIN CONFIGURATION

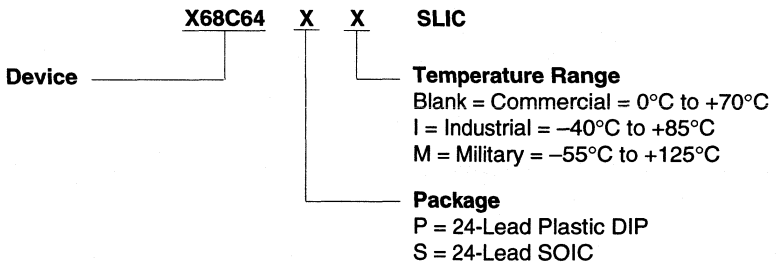


PIN NAMES

Symbol	Description
AS	Address Strobe
A/D_0–A/D_7	Address Inputs/Data I/O
A_8–A_{12}	Address Inputs
E	Enable Input
R/$\overline{W}$	Read/Write Input
$\overline{CE}$	Chip Enable
$\overline{WC}$	Write Control
$\overline{SEL}$	Device Select—Connect to V_{SS}
V_{SS}	Ground
V_{CC}	Supply Voltage

2134 PGM T01

ORDERING INFORMATION



5

NOTES

X68C75 SLIC® E² Microperipheral

Port Expander and E² Memory

FEATURES

- Highly Integrated Microcontroller Peripheral
  - —8K x 8 E² Memory
  - —2 x 8 General Purpose Bidirectional I/O Ports
  - —16 x 8 General Purpose Registers
  - —Integerated Interrupt Controller Module
  - —Internal Programmable Address Decoding
- Self Loading Integrated Code (SLIC)
  - —On-Chip BIOS and Boot Loader
  - —IBM/PC Based Interface Software(XSLIC)
- Concurrent Read During Write
  - —Dual Plane Architecture
- Isolates Read/Write Functions Between Planes
- Allows Continuous Execution Of Code From One Plane While Writing In The Other Plane
- Multiplexed Address/Data Bus
  - —Direct Interface to Popular 68HC11 Family of Microcontrollers
- Software Data Protection
  - —Protect Entire Array During Power-up/-down
- Block Lock™ Data Protection
  - —Set Write Lockout in 1K Blocks
- Toggle Bit Polling
- High Performance CMOS
  - —Fast Access Time, 120ns
  - —Low Power
    - 60mA Active
    - 100µA Standby
- PDIP, PLCC, and TQFP Packaging Available

DESCRIPTION

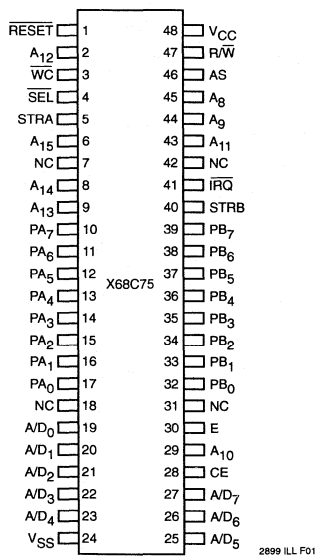
The X68C75 is a highly integrated peripheral for the 68HC11 family of microcontrollers. The device integrates 8K-bytes of 5V byte-alterable nonvolatile memory, 2 bidirectional 8-bit ports, 16 general purpose registers, programmable internal address decoding and a multiplexed address and data bus.

The 5V byte-alterable nonvolatile memory can be used as program storage, data storage, or a combination of both. The memory array is separated into two 4K-byte sections which allows read accesses to one section while a write operation is taking place in the other section. The nonvolatile memory also features Software Data Protection to protect the contents during power transitions, and an advanced Block Protect register which allows individual blocks of the memory to be configured as read-only or read/write.

5

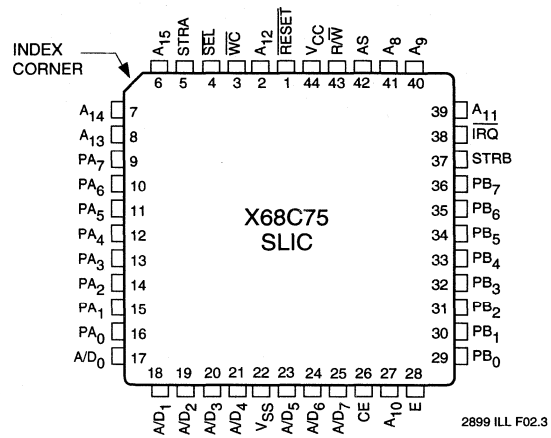
PIN CONFIGURATIONS

DIP



2899 ILL F01

PLCC
TQFP



2899 ILL F02.3

Concurrent Read During Write, Block Lock, and SLIC® E² are registered trademarks of Xicor, Inc.

Each bidirectional port consists of 8 general purpose I/O lines and 1 data strobe line. The ports also feature a configurable interrupt request output.

Access to the X68C75 is accomplished through the multiplexed address/data bus of the 68HC11 type controllers. An internal programmable address decoder maps the internal memory and register locations into the desired address space.

ARCHITECTURAL OVERVIEW

The X68C75 incorporates the interface circuitry normally needed to decode the control signals and demultiplex the address/data bus to provide a "seamless" interface.

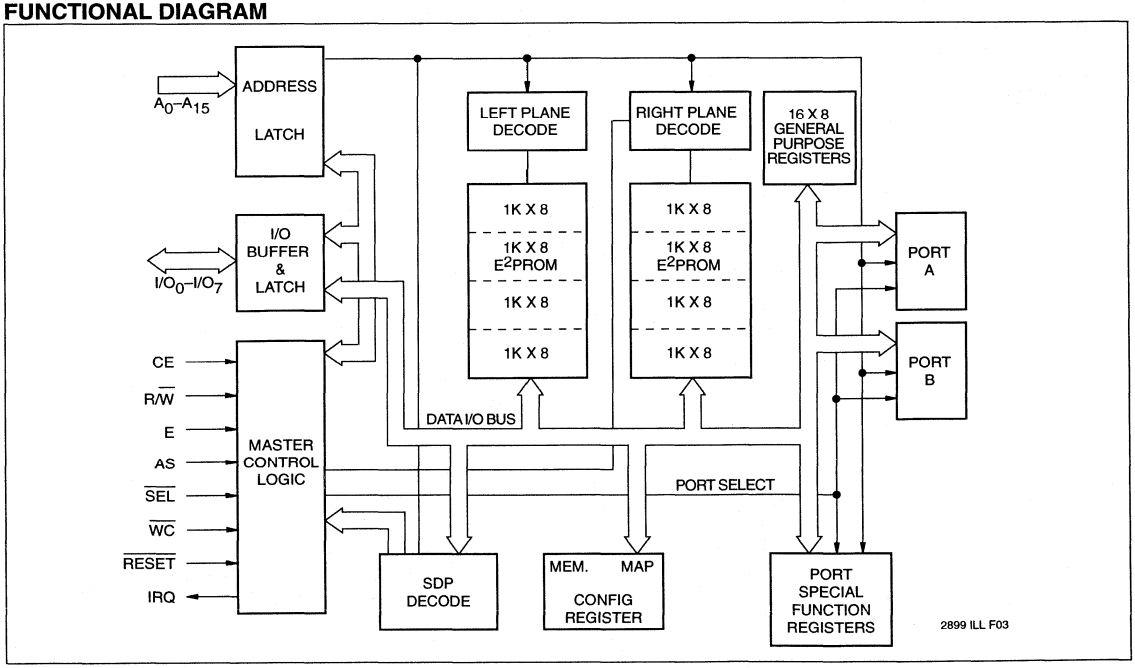
The control inputs on the X68C75 are configured such that it is possible to directly connect them to the proper interface signals of the 68HC11 microcontroller. The reading of data from the chip is controlled by the R/$\overline{W}$ and E clock signals.

Reading and writing of the nonvolatile memory array is analogous to RAM operation. During a write operation to either the nonvolatile memory or the control registers, the falling edge of AS latches the address present on the address bus into the X68C75, and the falling edge of E clock latches the data to be written.

The nonvolatile memory of the X68C75 is internally organized as two independent arrays of 4K-bytes with the A12 input selecting which of the two planes of memory is to be accessed. While the processor is executing code out of one plane, write operations can take place in the other plane; allowing the processor to continue execution of code out of the X68C75 during a byte or page write to the device. This feature is called Concurrent Read During Write.

The X68C75 also features an advanced implementation of the Software Data Protection scheme, called Block Protect, which allows the nonvolatile memory array to be treated as 8 independent sections of 1K-bytes. Each of these sections can be independently enabled for write operations. This allows segmentation of the memory contents into writable and non-writable sections, thereby, allowing certain sections of the device to be secured so that updates can only occur in a controlled environment. (e.g. in an automotive application, only at an authorized service center). The Block Protect configuration is stored in a nonvolatile register, ensuring that the configuration data will be maintained after the device is powered-down.

FUNCTIONAL DIAGRAM



The X68C75 write control input, serves as an external control over the completion of a previously initiated page load cycle.

The X68C75 also features the industry standard 5V E² memory characteristics such as byte or page mode write and Toggle Bit Polling.

Read

A HIGH to LOW transition on AS latches the address; the data will be output on the AD pins when E clock and R/$\overline{W}$ are HIGH (t_{ACC}).

Write

A write is performed by latching the address on the falling edge of AS. The R/$\overline{W}$ signal LOW while E clock is HIGH initiates a write cycle. The valid data must be present on AD_0-AD_7 prior to an E clock HIGH to LOW transition. The data will be latched into the X68C75 on the falling edge of E clock.

Page Write Operation

The X68C75 supports page mode write operations. This allows the microcontroller to write from one to thirty-two bytes of data to the X68C75. Each individual write within a page write operation must conform to the byte write timing requirements. The rising edge of E clock starts a timer delaying the internal programming cycle 100µs, therefore, each successive write operation must begin within 100µs of the last byte written. The waveform on page 19 illustrates the sequence and timing requirements.

Toggle Bit Polling

Because the X68C75 typical write timing is less than the specified 5ms, Toggle Bit Polling has been provided to

PIN DESCRIPTIONS

PIN NAME	I/O	DESCRIPTION
A_{15}–A_8	I	Non-multiplexed high-order Address line inputs for the upper byte of the address. The addresses are latched when AS makes a HIGH to LOW transition.
AD_7–AD_0	I/O	Multiplexed lower-order Address and DATA lines. The addresses are latched when AS makes a HIGH to LOW transition.
AS	I	Address Strobe input is used to latch the addresses present on the address lines A_{15}–A_8 and AD_7–AD_0 into the device. The addresses are latched when AS transitions from HIGH to LOW.
CE	I	The device select (CE) is an active HIGH input. This signal has to be asserted prior to AS HIGH to LOW transition in order to generate a valid internal device select signal. Holding this pin LOW and AS LOW will place the device in standby mode. The ports stay active at all times.
E	I	The E clock is the bus frequency clock input, and is used as a data timing reference signal. When the E clock is LOW, the addresses are latched by HIGH to LOW transition on the AS pin. The E clock HIGH cycle is used for data transfers.
$\overline{IRQ}$	O	The $\overline{IRQ}$ is an open-drain output. It can be configured to signal latching of new data into the ports, and completion of an E² memory write cycle.
PA_7–PA_0	I/O	The I/O lines of port A. The output driver can be configured as either CMOS or open-drain using the AWO bit in CR. The I/O direction bit (DIRA) in CR is used to select the port A I/O mode.
PB_7–PB_0	I/O	The I/O lines of port B. The output driver can be configured as either CMOS or open-drain using the BWO bit in CR. The I/O direction bit (DIRB) in CR is used to select the port B I/O mode.
R/$\overline{W}$	I	The R/$\overline{W}$ signal indicates the direction of data transfers. During phase 2 (HIGH cycle) of the E clock, the R/$\overline{W}$ is HIGH for a read, and LOW for a write cycle.
$\overline{RESET}$	I	$\overline{RESET}$ is used to initialize the internal static registers and has no effect on the E² memory operations. The default active level is LOW, but it can be reconfigured in EEM register.
$\overline{SEL}$	I	The $\overline{SEL}$ input should be LOW for the device to be selected. This input is normaly tied to V_{SS}.
STRA, STRB	I/O	The STRA controls port A and STRB controls port B. When ports are configured as inputs, a valid transition on their strobe pins will latch into their Port Data Register the data present at the port input pins. Writing to an output port Data Register generates a pulse of fixed duration on its corresponding strobe pin. The output data presented at the output pins stay valid until the next data is written to the output port data register.
$\overline{WC}$	I	$\overline{WC}$ input has to be held LOW during a write cycle. It can be permanently tied HIGH in order to disable writes to the E² memory. Taking the $\overline{WC}$ HIGH prior to t_{BLC} (100µs; the time delay from the last write cycle to the start of internal programming cycle) will inhibit the write operation.

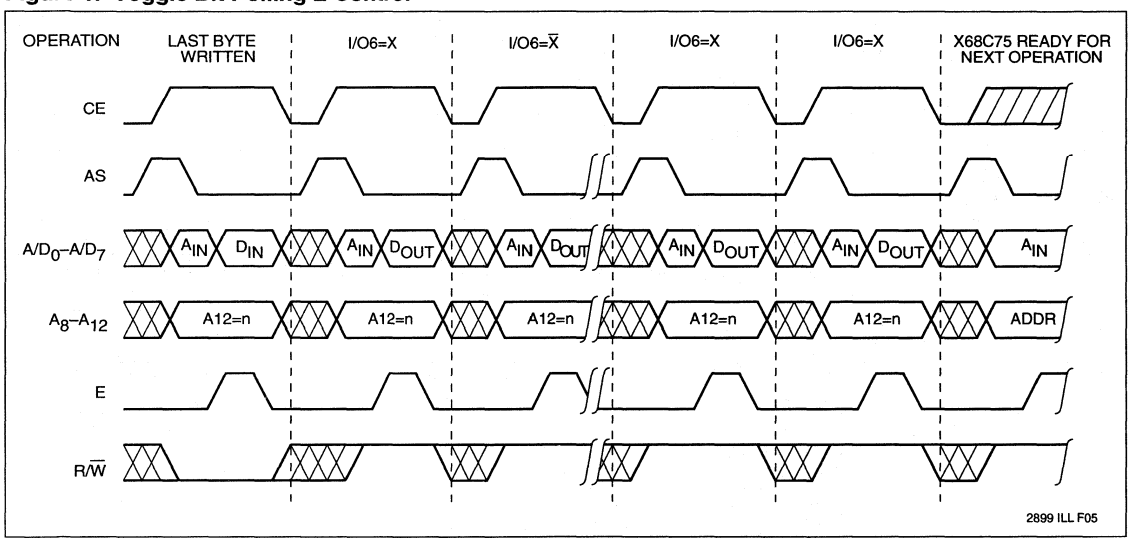
2899 PGM T01.1

determine the early completion of a write cycle. During the internal programming cycle, I/O_6 will toggle from "1" to "0" and "0" to "1" on subsequent attempts to read from the memory plane that is being updated. When the internal cycle is complete, the toggling will cease and the device will be accessible for additional read or write operations. Due to the dual plane architecture, reads for polling must occur from the plane that was written; that is, the state of A_{12} during a write must match the state of A_{12} during polling.

DATA PROTECTION

The X68C75 provides two levels of data protection through software control. There is a global software data protection feature similar to the industry standard for E²PROMs and a new Block Lock Protect write lockout protection providing a secondary level data security option.

Figure 1. Toggle Bit Polling E Control



Software Data Protection

Software Data Protection (SDP) can be employed to protect the entire array against inadvertent writes during power-up/power-down operations. The X68C75 is shipped from the factory with SDP enabled. With SDP enabled, inadvertent attempts to write to the X68C75 will be blocked.

The system can still write data, but only when the write operation (page or byte) is preceded by the three-byte command sequence. All write operations, both the command sequence and any data write operations must conform to the page write timing requirements.

Writing with SDP Enabled

The SDP mode is also enabled anytime one of the nonvolatile configuration registers are modified. These include writing to EE map, SFR map, and BPR.

Block Lock Protect Write Lockout

The X68C75 provides a second level of data security referred to as Block Lock Protect write lockout (or Block Protection). This is accessed through an extension of the SDP command sequence. Block Protect allows the user to lockout writes to 1K x 8 blocks of memory. Unlike SDP which prevents inadvertent writes, but still allows easy system access to writing the memory, Block Protect will lockout all attempts unless it is specifically disabled by issuing the deactivation sequence. This feature can be used to set a higher level of protection in a system where a portion of the memory is used to store the system kernel and protect it from the application programs residing in the other blocks.

Setting write lockout is accomplished by writing a five-byte command sequence opening access to the Block Protect Register (BPR). After the fifth byte is written, the user writes to the BPR, selecting which blocks to protect or unprotect. All write operations, both the command sequence and writing the data to the BPR, must conform to the page write timing requirements. It should be noted that accessing the BPR automatically sets the upper level SDP. If for some reason the user does not want SDP enabled, they may reset it using the normal reset

Figure 2.

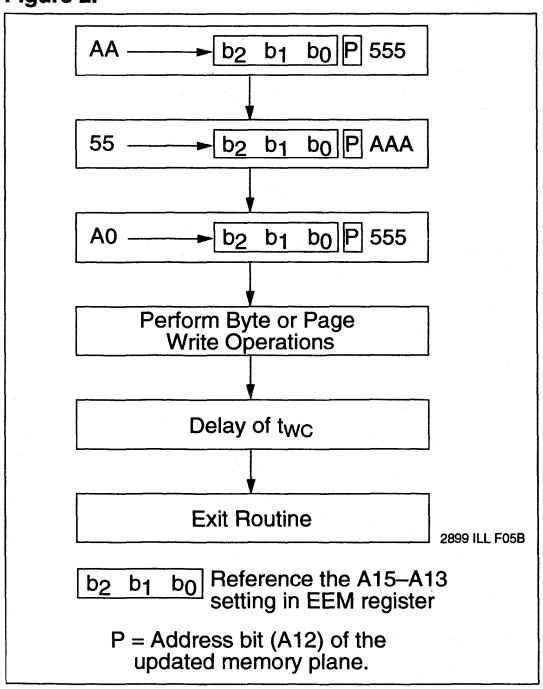


Figure 3. Sequence to Deactivate Software Data Protection

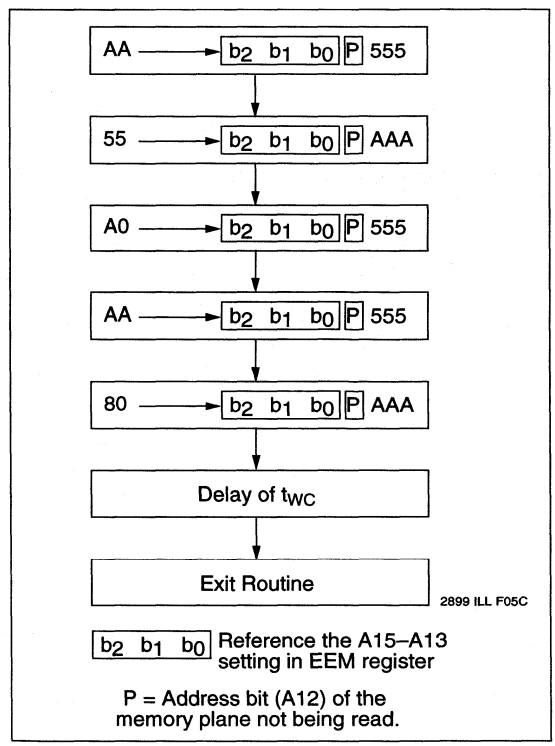
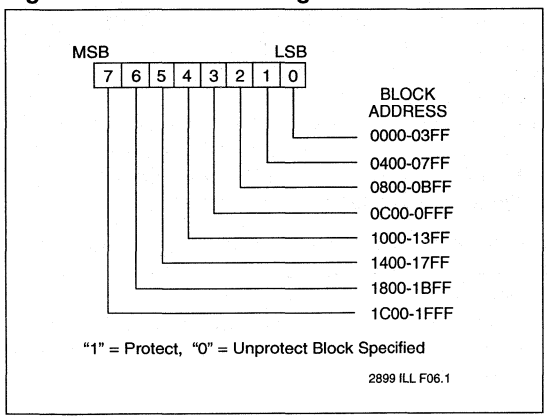


Figure 4. Block Protect Register Format



The BPR format and block map are illustrated above. The command sequence is illustrated to the right.

Figure 5. Setting BPR Command Sequence

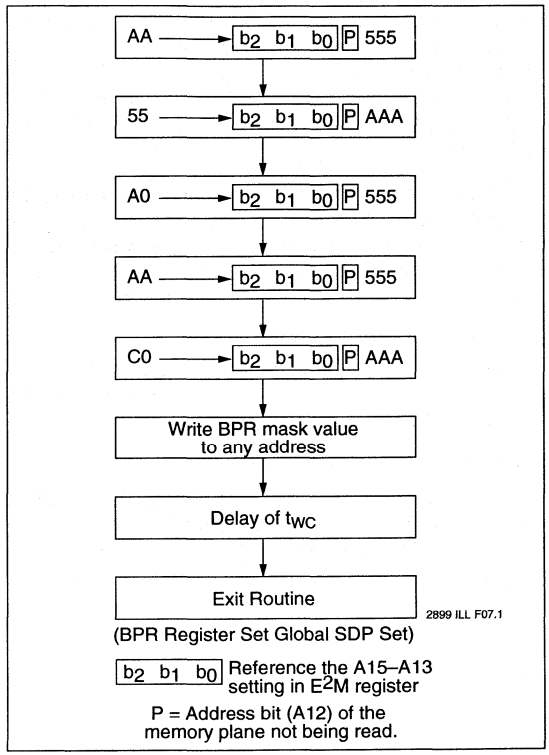


Figure 6. Microcontroller Map

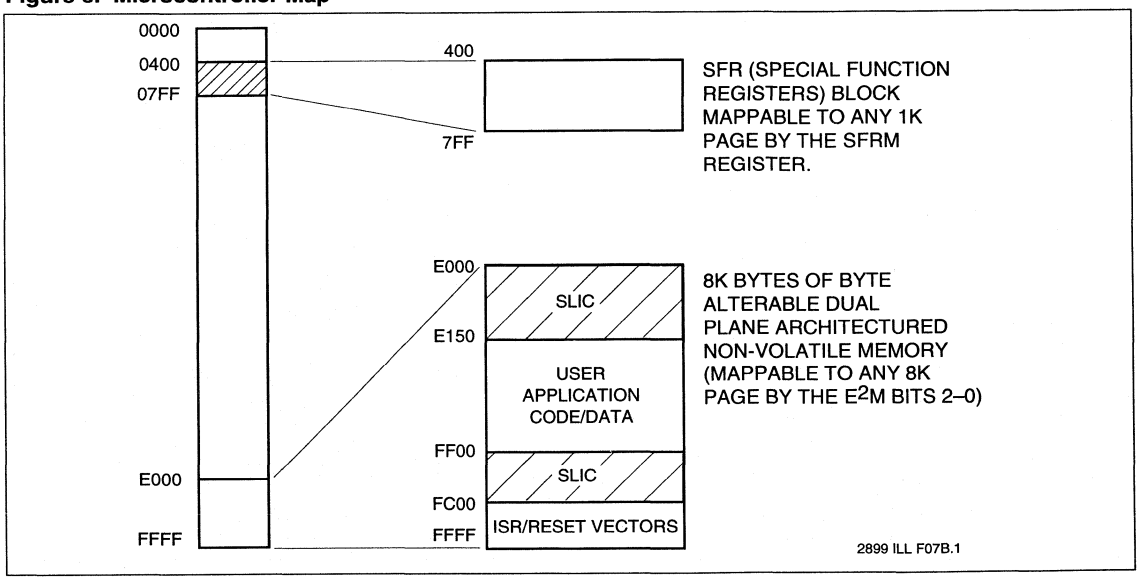
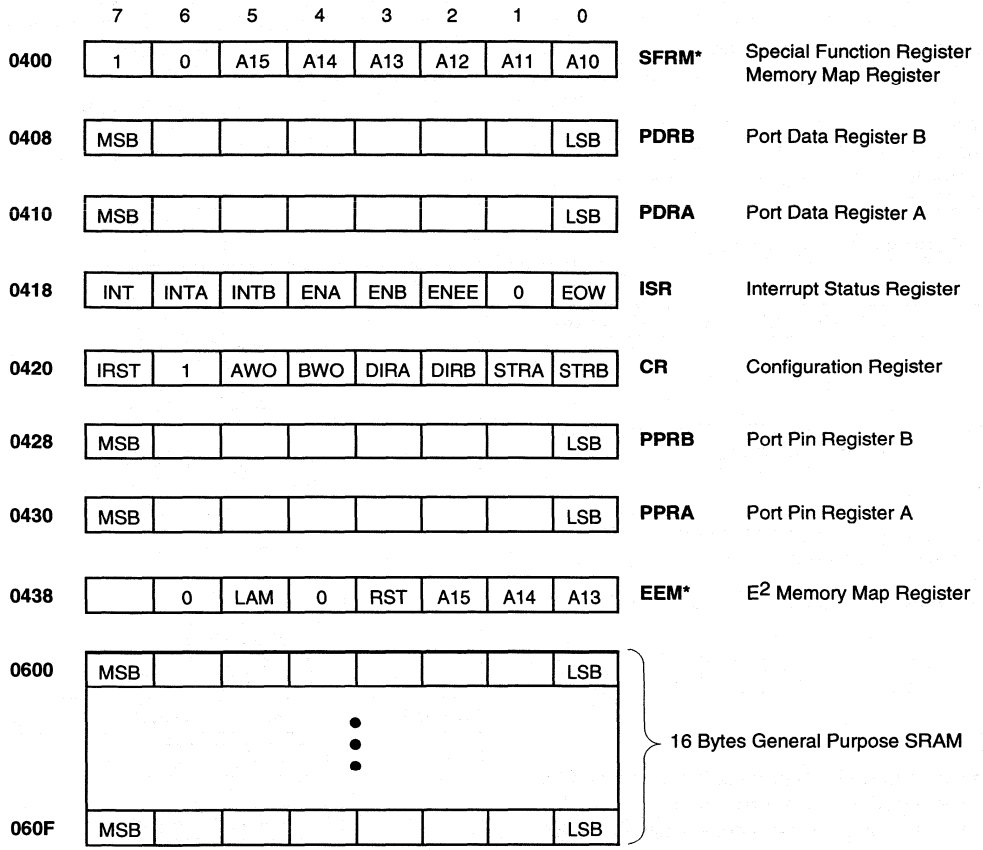


Figure 7. On-Chip Registers



NOTE: * The value returned by reading these registers is the complement of the actual data. These registers are nonvolatile and a special SDP sequence is used to alter their contents. All the other registers are initialized by a valid reset input signal and when the device is power cycled.

2899 ILL F07.3C

5

Programmable Address Decoding

The X68C75 features an internal programmable address decoder which allows the nonvolatile memory array and the internal registers to be mapped in various locations of the 64K-byte memory map. The register set is mappable into a 1K-byte block, while the nonvolatile memory array is mappable into an 8K-byte block. The mapping is controlled by two nonvolatile configuration registers, the SFR Map Register and the E² Memory Map Register. Their bits are mapped as follows:

SFR Map Register (SFRM) Default = 81

7	6	5	4	3	2	1	0
1	0	A15	A14	A13	A12	A11	A10

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A15-A10

A15-A10 are upper address bits for the 1K-byte page where the SFR memory is mapped.

BITS 7:6

Setting these two bits to any combination other than "10" will interfere with device proper operation.

E² Memory Map Register (EEM) Default = 07

7	6	5	4	3	2	1	0
0	0	LAM	0	RST	A15	A14	A13

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A15-A13

Modifying these three bits changes the location of the program memory within the address map.The A15-A13 correspond to the upper three address bits of the 8K-byte page where program memory will be mapped.

RST

The RST bit controls the polarity of the RESET input pin.

"0" = RESET is Active LOW
"1" = RESET is Active HIGH

LAM

Port B can be configured as either a general purpose I/O port (normal I/O mode), or latched address mode (LAM). The LAM option programs port B to output the demultiplexed low order byte of the address latched into the X68C75 by AS. The LAM bit selects between these two modes.

"0" = Port B is an I/O Port
"1" = Port B outputs low address byte (A7-A0)

Setting the Mapping Registers

The mapping registers are written using a modified version of the Software Data Protection sequence. All timings must adhere to the normal Software Data Protection sequence.

Figure 8. Setting the SFR Map Register

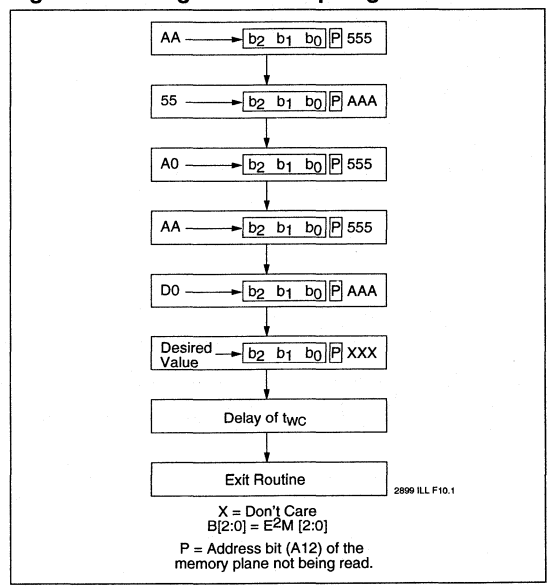
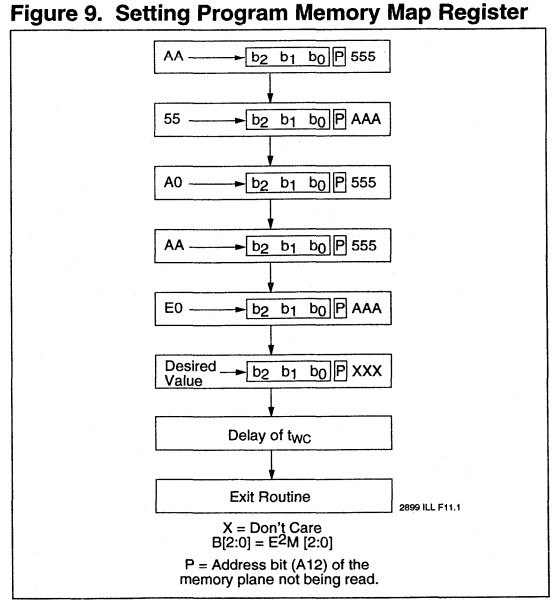


Figure 9. Setting Program Memory Map Register



The complemented contents of the SFR map register and the E² memory map register can be read by the microcontroller at their corresponding SFR addresses. The physical memory location of these registers can be derived by adding the following offset to the SFR base address:

SFR Map Register	00H
E² Memory Map Register	38H

If the regions specified in the map registers overlap, only the SFR will be accessible.

Interrupt Status Register (ISR)

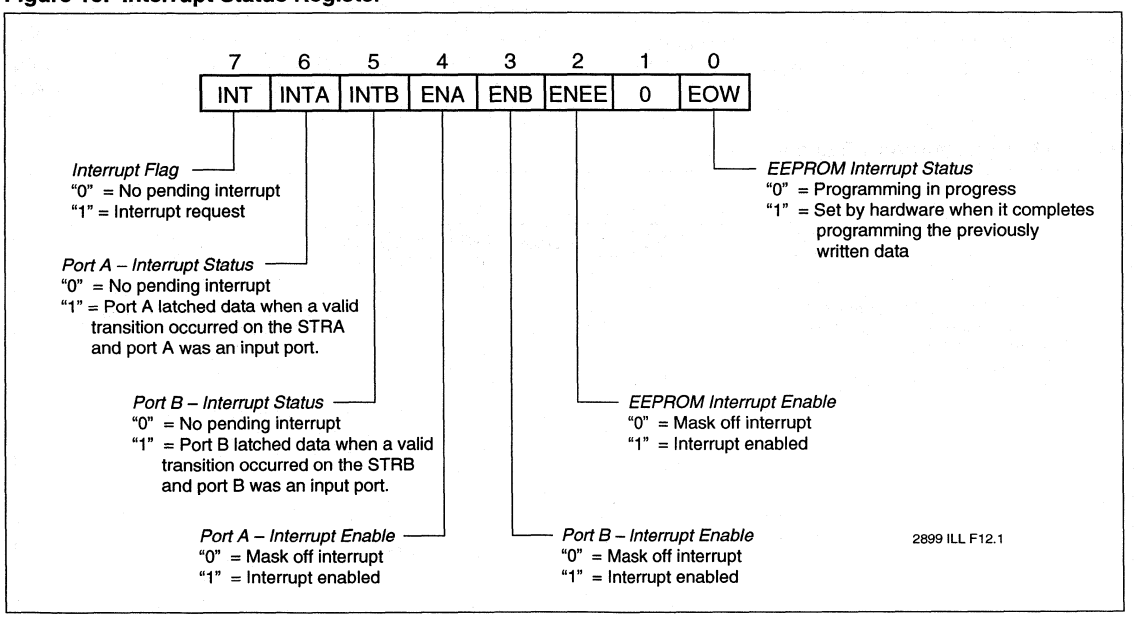
The Interrupt Status Register is a volatile register used to configure the interrupt condition for the I/O ports as well as to determine the interrupt status of the ports. The X68C75 ports can generate an interrupt to the microcontroller upon the proper transition (as specified in the configuration register) on either STRA or STRB pins when the corresponding I/O port is configured as an input.

The INT flag is set when any of input strobes are toggled provided that their corresponding interrupt enable bits (ENA, ENB) are set. The INT flag is cleared when latched data is read (PDR) or pending interrupt status flag (INTA, INTB) in ISR is forced to "0" by the interrupt service routine. Interrupt service routine should examine the interrupt status flags (INTA, INTB) and identify the source of pending interrupt.

The E² memory interrupt status flag (EOW) is another means to detect the early completion of a write cycle. When ENEE is enabled, the hardware will set the EOW flag, and interrupt the microcontroller at the end of an internal programming cycle. Toggle Bit Polling can be replaced by the EOW hardware interrupt, which reduces the software overhead. The EOW flag should be cleared by software. The interrupt status register bits are mapped as follows.

5

Figure 10. Interrupt Status Register



Configuration Register (CR)

The Configuration Register is a volatile register used to configure the operation of the I/O ports. The configuration register allows the microcontroller to designate whether each of the two ports is an input or output, what type of output drive is to be used, and specifies the polarity of the two strobe lines, STRA and STRB. The bit map of configuration register is shown below.

The IRST bit in the configuration register controls the method used to clear the port interrupt request flags (INTA, INTB). The interrupts are reset by either reading the interrupt source or writing to the interrupt status register. The interrupt must be disabled prior to changing strobe polarity bits (STPA, STPB), or port direction bits (DIRA, DIRB) in CR. Otherwise, any attempt to modify the status of these bits may cause an interrupt to occur.

Port Data Registers (PDR)

The PDRA/PDRB are byte-wide latches which hold port data. When a port is configured as an output, the outputs of its PDR latch are connected to the port pins. Writing to PDR generates a pulse on the port strobe pin and latches the data. If a port is configured as an input, the inputs of its PDR latch are connected to the port pins. External data is latched into PDR on the positive edge of its clock. The port strobe input and strobe polarity bit (STPA, STPB) are XORed to generate the PDR input clock.

Port Pin Registers (PPR)

The read-only Port Pin Registers are used for reading the current status of the external I/O port pins. Accessing the PPR causes the values on the port pins to be placed on the data bus.

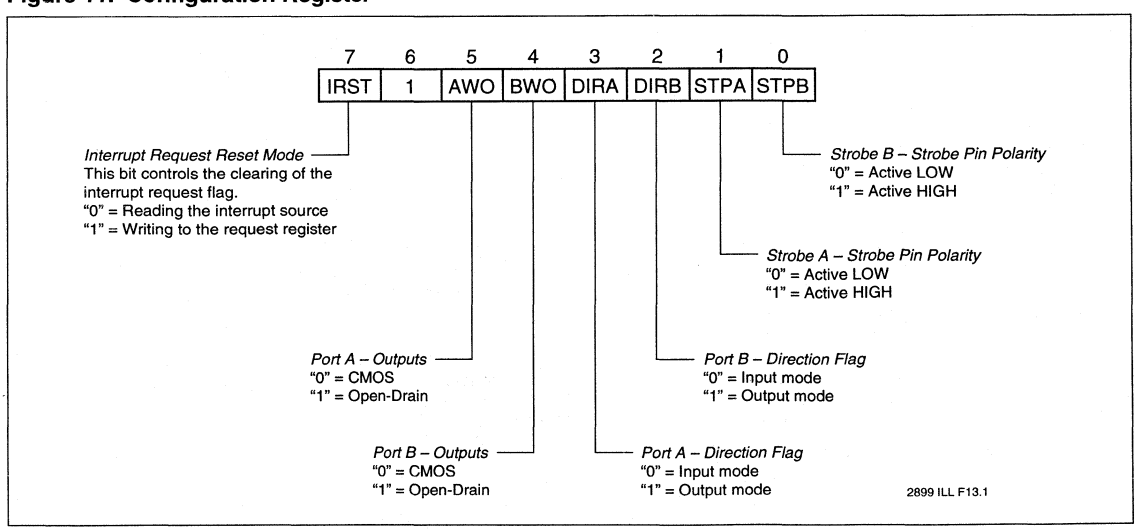
The port direction control bits in configuration register set the direction for the entire port and no control mechanism is provided to program the direction of individual pins. However, the ports have a flexible architecture which allows operating I/O ports in bidirectional mode using the PPR read feature.

A port can be operated in input/output mode by configuring it as an open-drain output port. The port wire-OR bit (AWO, or BW) and its port data direction bit (DIRA, or DIRB) in CR, should be set to "1". The PDR bits which correspond to the port pins assigned as inputs should be programmed to "1". For monitoring the status of the input pins, the PPR can be read. In this application the port strobe pin and the PDR latch are in output mode. In open-drain mode, there are weak internal pull-ups on the port pins, however external pull-ups must be used for proper switching of the I/O lines.

Static RAM Block

There are 16 bytes of volatile static RAM registers mapped to the SFR region. They reside in the 200H-20FH area offset from the SFR base address. Accessing these registers has to be done through external RAM operations for both writes and reads.

Figure 11. Configuration Register



PRINCIPLES OF OPERATION

I/O Ports Operation

The expansion ports are accessible to the software using their assigned memory mapped addresses. Each port occupies two addresses in the SFR plane, the Port Data Register and Port Pin Register. These registers and their location in the 1K-byte register memory space is shown on page 7.

The ports can be configured as either inputs or outputs, the DIRA and DIRB bits in the configuration register are used to select between the modes. The input signal on the strobe pin, when the corresponding port is configured as an input, is fed to the clock input of the port latch. These are transparent latches and the trailing edge of the strobe pulse is used to latch the data present on the input pins. The strobe signal polarity is configurable using the STPA and STPB bits in the configuration register.

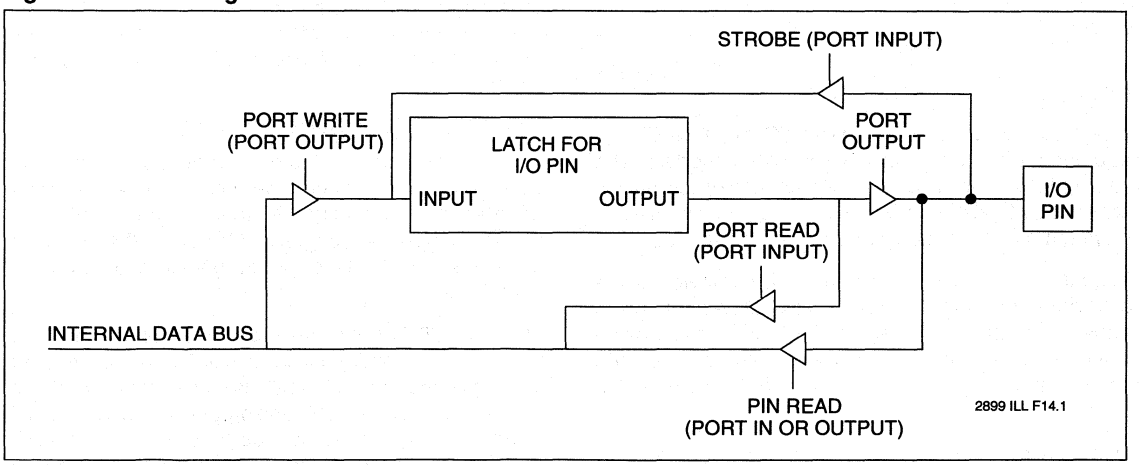
Writing to the port data register of an output port will generate a pulse of fixed duration on its strobe pin. The data also simultaneously arrives at the port output pins. The latched data stays there until new data is written to the port data register. The strobe pulse shape is controlled by the state of the STPA and STPB bits in configuration register. A "1" forces the valid transition on the corresponding strobe pin as active HIGH (⎍⎍), and a "0" sets it to active LOW (⎍⎍) .

When an external strobe signal is applied to an input port, the latching of input data is followed by the setting of the interrupt flags. The INTA and INTB interrupt flags are used by ports A and B respectively, and are set along with the INT interrupt flag at the end of strobe pulse input. External interrupt ($\overline{IRQ}$) is generated if the interrupt enable flags (ENA, and ENB) are set by the software. The former enables the port A interrupt and the latter the port B interrupt.

The port output drivers can be either CMOS or open-drain. The wire-OR bits (AWO, BWO) in the configuration register are used to make the selection. When the bits are "0" the CMOS drivers are enabled . Setting these bits will enable the open-drain output drivers. Small pull-up resistors should be used on the pins of open-drain outputs.

5

Figure 12. Block Diagram of the I/O Ports



IRQ

The $\overline{IRQ}$ pin is an active LOW open-drain output. In embedded systems applications, this signal is connected to the microcontroller interrupt input pin through either a direct connection or via an interrupt controller.

Table 1 depicts the three sources of interrupts and their associated flags. Under normal conditions, the INT and port interrupt flags are set, if the port which is configured as an input has its strobe line toggled. If the port interrupt enable flag is set, or gets set while the INT flag is set, then the $\overline{IRQ}$ signal is asserted. The $\overline{IRQ}$ stays valid as long as the interrupt flags are not cleared by the software or the hardware.

Another interrupt source is the End Of Write flag (EOW) which is set by the hardware at the end of every internal programming cycle. The interrupt from this source is controlled by the ENEE bit in ISR. If ENEE is enabled, then EOW can generate an external interrupt. The interrupt is cleared by setting EOW to "0".

Table 1. X68C75 Interrupt Sources

Interrupt Source	Interrupt Enable	Status Flag	INT Flag
PORT A	ENA	INTA	"1"
PORT B	ENB	INTB	"1"
EOW	ENEE	EOW	—

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PORTS A & B INTERRUPTS

The X68C75 features two 8-bit I/O ports which are equipped with a configurable interrupt module. The interrupts are used to signal the reception of new data at an input port data latch. When a port is configured as an output, it can no longer generate any interrupts.

The input port interrupt mechanism is controlled by the external strobe pins (STRA, STRB). Detecting a valid transition on the pins will set the interrupt flags and latch in the input data. The external interrupts from the ports can be masked off using interrupt enable bits(ENA and ENB) in ISR.

Once an external interrupt is asserted, clearing the interrupt flags will cause the $\overline{IRQ}$ signal to return to its idle state. There are two ways of resetting the interrupt flags. The selection is made using the IRST bit in the configuration register. If IRST is set, then the interrupt flags are cleared by writing "0" to the bit positions corresponding to the interrupt flags (INTA, INTB) in ISR. When the IRST bit is cleared, reading the PDR automatically clears the interrupt flags.

SOFTWARE CONTROLLED PORT OPERATIONS

The individual clock signals, that control the PDR input latches and load the external data present on the port pins, are generated by XORing the strobe polarity bit and the strobe input of the port. The strobe polarity bits (STPA, STPB) in CR can be used to program the active edge of the strobe inputs. However, if the external strobe input is permanently tied to V_{SS} or V_{CC}, then the strobe polarity bit controls the PDR input latch clock signal.

When a port strobe and its polarity bit have identical logic levels, the corresponding PDR latch is active and any change in the port inputs will show up at the PDR latch outputs. Holding the strobe input at current levels and changing the strobe polarity bit value will generate a positive transition on the PDR clock signal, causing the latch outputs to reflect the previous logic state of the port pins. The clock transition sets the interrupt flags, and if the interrupts have been enabled, then an external interrupt signal will be asserted.

This feature allows the port input operation by permanently tying the STRx inputs to V_{CC} or V_{SS}, and using the STPx bits in CR to control PDR latches. Another advantage of this feature are software generated interrupts. Since the clocking of the PDR latch causes the corresponding port INTx flags to be set, by enabling the interrupts the microcontroller is forced to execute the interrupt service routine responsible to service the newly latched data.

END OF WRITE (EOW) INTERRUPT

The internal programming cycle requires several milliseconds for either a single byte write or a page write. The updated memory plane is inaccessible while the programming is in progress. However, the opposite plane is still available for program fetch and data read operations.

The X68C75 has two means of signaling end of an internal programming cycle. In the Toggle Bit Polling technique, the last written byte is successively read. Bit 6 of read data toggles while the programming cycle is still in progress. The software has to continually monitor device responses and determine if it can again access the plane.

In the other method, at the end of an internal programming cycle, the hardware sets the EOW flag. The software can either poll this flag or enable the interrupts by setting the ENEE bit in ISR. Effective use of EOW is made by clearing it prior to initiating a write operation. If

the interrupt is enabled, an external interrupt will be asserted at the completion of the internal write cycle. The interrupt is cleared by setting EOW to "0".

USING A PORT IN BIDIRECTIONAL MODE

In order to use a port in bidirectional mode, it has to be configured as an open drain output port. Small pull-up resistors are required on all port output pins. Bit positions in the port data register corresponding to port inputs should contain "1". The inputs are then read by accessing PPR. Data is not latched into the device, so the inputs must stay valid throughout the read cycle. The port strobe pin is configured as an output and cannot be used as port latch clock input.

SLIC FUNCTIONS (68HC11 Specific SLIC)

The resident SLIC E² has designated memory spaces allocated for its use. The user's application code should avoid using these areas as part of its code segment, otherwise it will overwrite the SLIC E². Version 3.0 of the X68C75 SLIC E² occupies 192 bytes in the upper memory bank, FF00-FFC0H, and 336 bytes in the lower bank's address range E000-E14FH. Prior to downloading code, assemble and link the source files using the above address information. Use memory space taken up by the SLIC E² as a run-time data storage, if there is no further need to modify the X68C75 SLIC E² content.

The current version of the SLIC E² configures the 68HC11 serial port to the variable baud rate mode. It sets a timer prescalar value for a system clock rate of 8MHz. For other clock rates, the end user must recalculate timer 1 reload value for 9600 baud rate and write it into the X68C75 location E024H. The XSLIC software, a PC based communication driver, automates changing of the default parameters when using its SETUP option menu. The boot-firmware (SLIC) residing on the X68C75 contains a lookup table which can be accessed from the subroutine (EXEC_FUNC), located at location E120H. Two bytes are used per table entry. The EXEC_FUNC input requirements are as follows:

B = Contains a function number from the following function table.

The table entry at location (E14E-E14FH) is reserved for user's application code. This function will be executed on power-up if the SLIC receives any characters other than those for the RESET (ASCII 'R'), or ID (ASCII 'X') commands. This table entry can be changed to point to other code responsible for power-up initialization. This method is preferred to changing the reset vector, since the SLIC code can still be invoked upon power-up.

Other functions available through the EXEC_FUNC calls are as follows:

Figure 13.

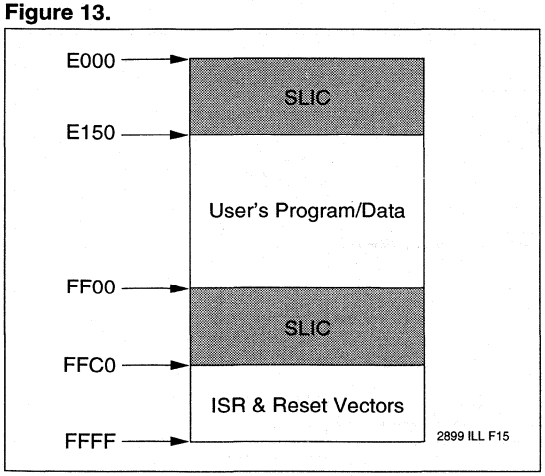

Table 2.

FUNCTION NO.	DESCRIPTION
0 - PROC_PROG	Download and program a page
1 - PROC_BPR	Program BPR
2 - RESET	Start execution from location 0000H
3 - PROC_VER	Download and verify a page
4 - DUMMY	Command not recognized
5 - INIT_UART	Initialize UART parameters to default
6 - PROG_PG	Program a page
7 - SEND_CHAR	Send a character to the UART
8 - GET_CHAR	Read a character from the RAM receive buffer (40H-5FH)
9 - SDP_HI_PLANE	Generate SDP off sequence for upper plane
10- SDP_LO_PLANE	Generate SDP off sequence for lower plane
11- USER_CODE	Execute user's code

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For detailed information about the listed functions, including their input requirements, refer to the SLIC software specification document.

APPLICATION EXAMPLES

This section gives examples of most widely used embedded systems architectures using the X68C75 and 68HC11 microcontroller. However, keep in mind that other microcontrollers are also supported by the X68C75 and/or other SLIC devices that Xicor manufactures.

Example 1

In this system, the X68C75 is the only parallel device residing on the multiplexed address and data bus. There may be other peripherals on the system board which are controlled by the ports on the X68C75. This configuration maps the EEM to a memory address in the range of E000-FFFFH. The SFRM can be mapped to any of the 64 x 1K pages within the memory space.

Example 2

Applications requiring more than 8K bytes of program memory space can be implemented using the basic system architecture depicted in example 1 along with an additional memory device such as the X28C256. Since this device requires non-multiplexed address/data buses, the X68C75 LAM feature is used to output the low order address byte. The SFRM can be mapped to any 64x1K page, but the X28C256 should be mapped to the low memory address space and out of the E²M address range (E000-FFFFH). This technique may also be used for other external byte wide memories such as SRAMs or EPROMs.

Figure 14. Example 1

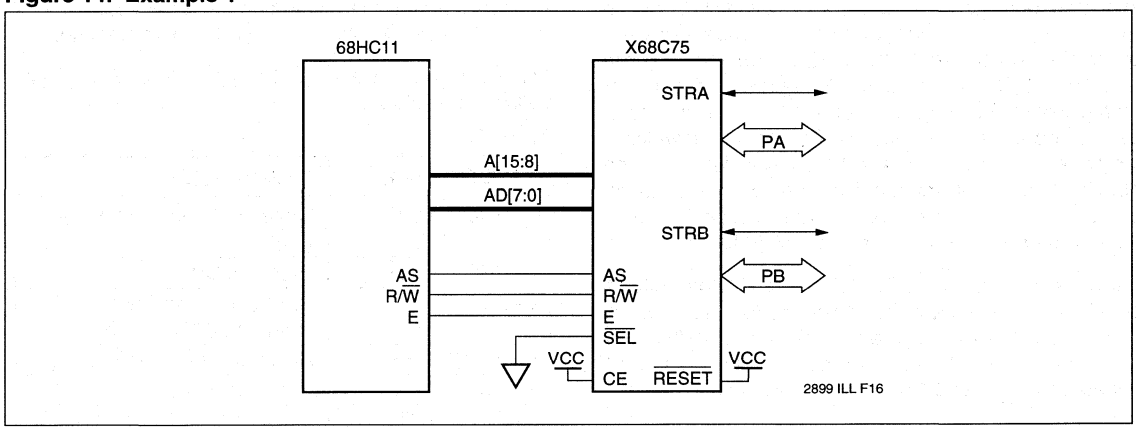
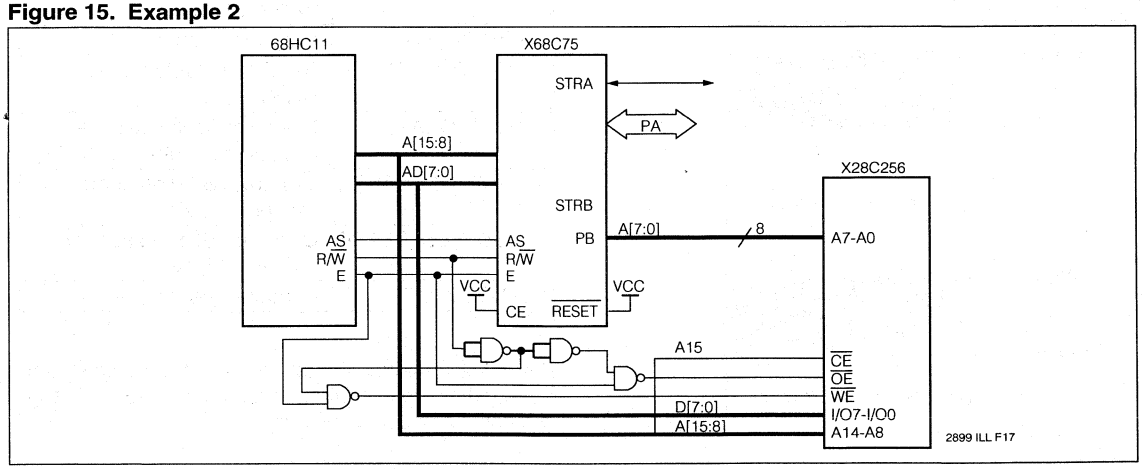


Figure 15. Example 2



Example 3

If an application requires larger program memory storage and both extra ports, then example 2 does not meet this requirement. Since the LAM feature uses port B to output the non-multiplexed address, then port B cannot be also used as general purpose I/O. The solution to this problem is to use X88C64, which interfaces to a multiplexed bus and takes an active LOW $\overline{CE}$ input. Example 3 maps the X88C64 to the bottom 8K program memory space in the range of 0000-1FFFH. This approach provides a total of 16K-bytes of program memory. Using the same approach, two additional X88C64 devices can be added and A13-A14 can be used as their $\overline{CE}$ inputs, for a total of 32K-bytes of program memory. Ports A and B are still available to handle any general purpose I/O functions.

Example 4

For those applications using extensive I/O, up to 128 I/O pins are obtained by placing 8 of the X68C75 devices on the same bus. This approach gives a total of 64K-bytes of program memory space, and 128 I/O pins. Note that the SFRM can overlap the E²M address space, however, only the SFR resources are accessible and the associated E² memory location are not available.

Figure 16. Example 3

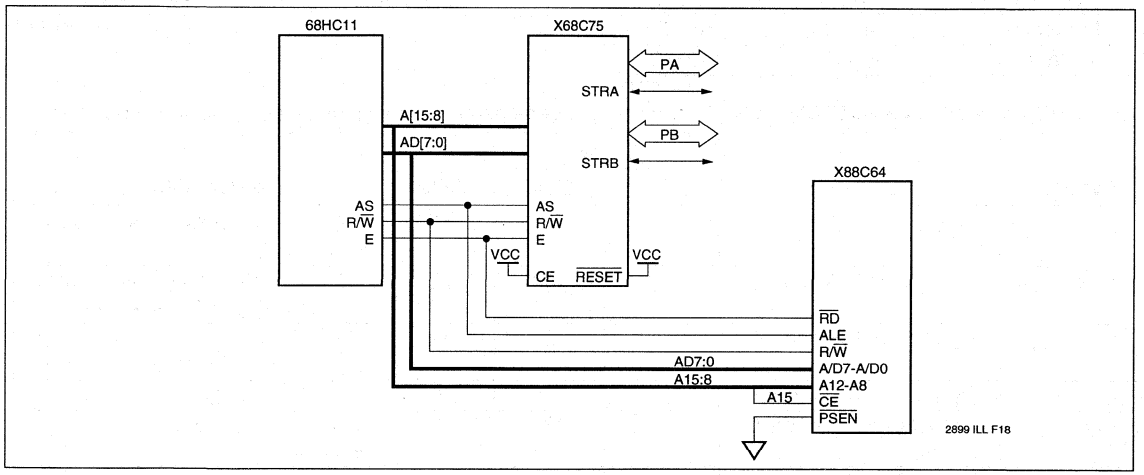
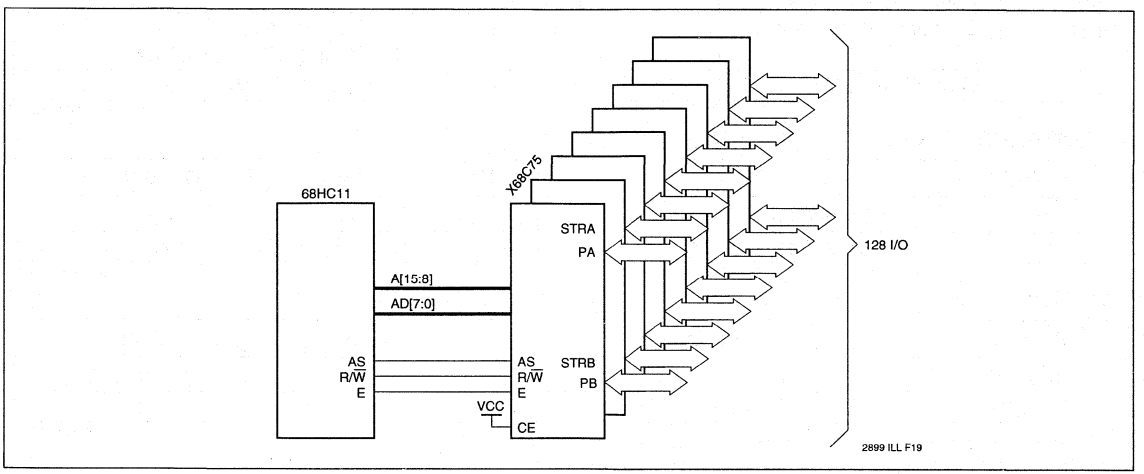


Figure 17. Example 4



ABSOLUTE MAXIMUM RATINGS*

Temperature under Bias ..... –65°C to +135°C
Storage Temperature ..... –65°C to +150°C
Voltage on any Pin with
Respect to V_{SS} ..... –1V to +7V
D.C. Output Current 5mA
Lead Temperature
(Soldering, 10 seconds) ..... 300°C

***COMMENT**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	+70°C
Industrial	–40°C	+85°C
Military	–55°C	+125°C

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Supply Voltage	Limits
X68C75	5V ±10%

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D.C. OPERATING CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
I_{CC}	V_{CC} Current (Active)		60	mA	CE = V_{IH}, All I/O's = Open, Other Inputs = V_{CC}
$I_{SB1(CMOS)}$	V_{CC} Current (Standby)		100	µA	CE = V_{IL}, All I/O's = Open, Other Inputs = V_{CC}–0.3V, AS = V_{IL}
$I_{SB2(TTL)}$	V_{CC} Current (Standby)		2	mA	CE = V_{IL}, All I/O's = Open, Other Inputs = V_{IH}, AS = V_{IL}
I_{LI}	Input Leakage Current		10	µA	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output Leakage Current		10	µA	V_{OUT} = V_{SS} to V_{CC}, E = V_{IL}
V_{IL}(3)	Input LOW Voltage	–1	0.8	V	
V_{IH}(3)	Input HIGH Voltage	2	V_{CC} + 0.5	V	
V_{OL}	Output LOW Voltage		0.4	V	I_{OL} = 2.1mA, Ports (A,B) I_{OL} = 20mA
V_{OH}	Output HIGH Voltage	2.4		V	I_{OH} = –400µA

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CAPACITANCE T_A = +25°C, f = 1MHz, V_{CC} = 5V

Symbol	Test	Max.	Units	Conditions
$C_{I/O}$(4)	Input/Output Capacitance	10	pF	$V_{I/O}$ = 0V
C_{IN}(4)	Input Capacitance	6	pF	V_{IN} = 0V

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POWER-UP TIMING

Symbol	Parameter	Max.	Units
t_{PUR}(4)	Power-Up to Read	1	ms
t_{PUW}(4)	Power-Up to Write	5	ms

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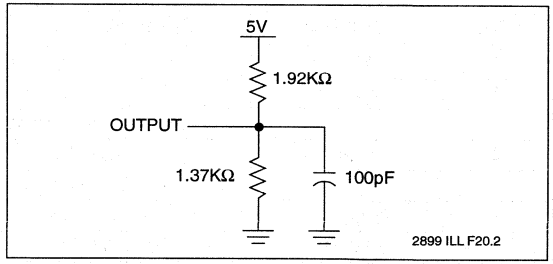
Notes: (3) V_{IL} min. and V_{IH} max. are for reference only and are not tested.
(4) This parameter is periodically sampled and not 100% tested.

A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3V
Input Rise and Fall Times	10ns
Input and Output Timing Levels	1.5V

2899 PGM T09.1

EQUIVALENT A.C. TEST CIRCUIT



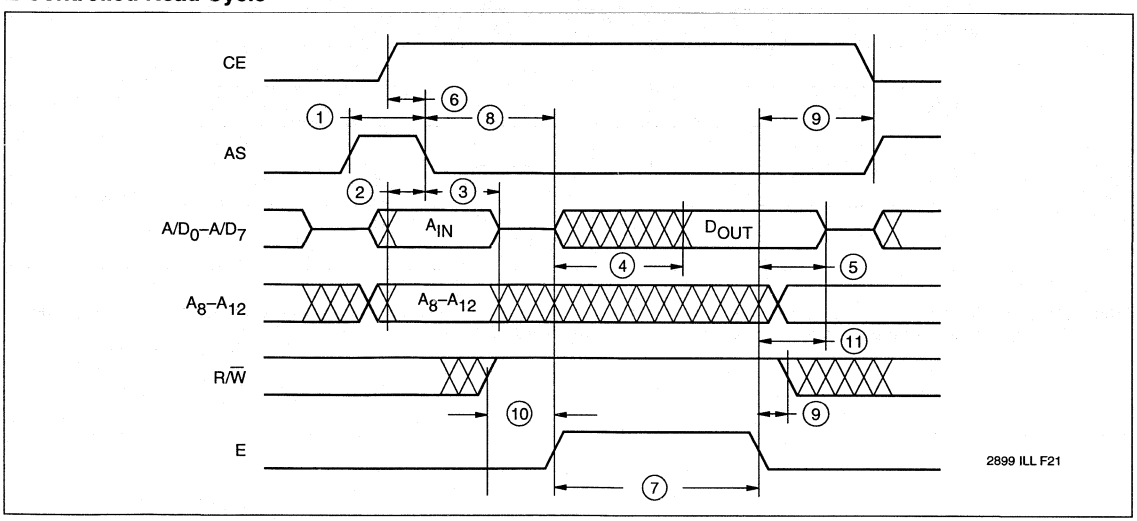
A.C. CHARACTERISTICS (Over the recommended operating conditions unless otherwise specified.)

E Controlled Read Cycle

No.	Symbol	Parameter	Min.	Max.	Units
1	PW_{ASH}	Address Strobe Pulse Width	80		ns
2	t_{ASL}	Address Setup Time	20		ns
3	t_{AHL}	Address Hold Time	30		ns
4	t_{ACC}	Data Access Time		120	ns
5	t_{DHR}	Data Hold Time	0		ns
6	t_{CSL}	CE Setup Time	7		ns
7	PW_{EH}	E Pulse Width	150		ns
8	t_{ES}	Enable Setup Time	30		ns
9	t_{EH}	E Hold Time	20		ns
10	t_{RWS}	R/$\overline{W}$ Setup Time	20		ns
11	t_{HZ}(5)	E LOW to High Z Output		50	ns

2899 PGM T10.1

E Controlled Read Cycle



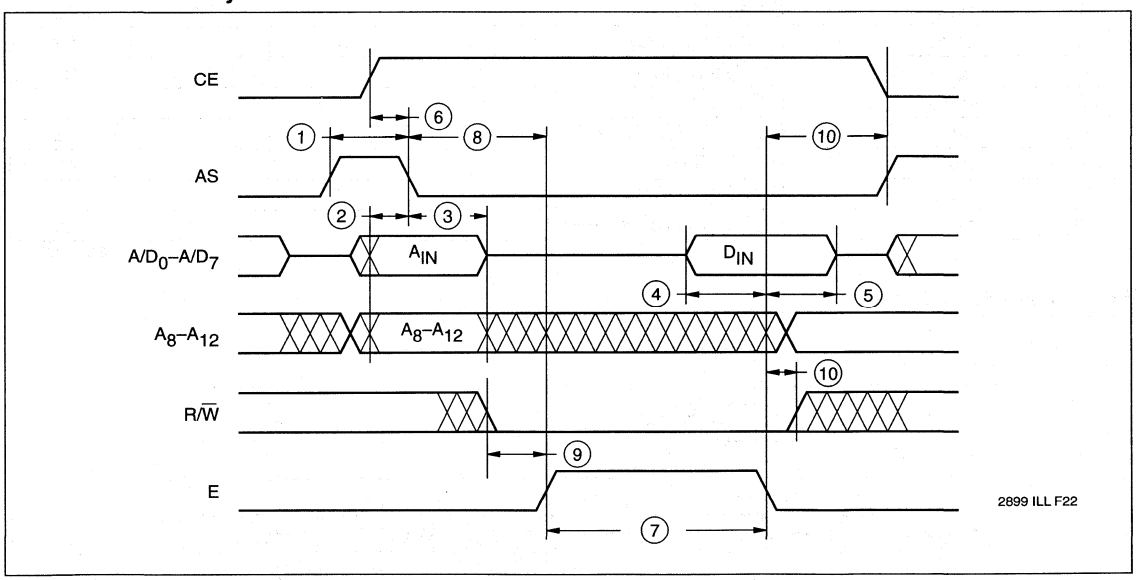
Note: (5) This parameter is periodically sampled and not 100% tested.

E Controlled Write Cycle

No.	Symbol	Parameter	Min.	Max.	Units
1	PW_{ASH}	Address Strobe Pulse Width	80		ns
2	t_{ASL}	Address Setup Time	20		ns
3	t_{AHL}	Address Hold Time	30		ns
4	t_{DSW}	Data Setup Time	50		ns
5	t_{DHW}	Data Hold Time	30		ns
6	t_{CSL}	CE Setup Time	7		ns
7	PW_{EH}	E Pulse Width	120		ns
8	t_{ES}	Enable Setup Time	30		ns
9	t_{RWS}	R/$\overline{W}$ Setup Time	20		ns
10	t_{EH}	E Hold Time	20		ns
11	t_{WC}	Write Cycle Time		5	ms
12	t_{BLC}	Byte Load Time (Page Write)	0.5	100	µs

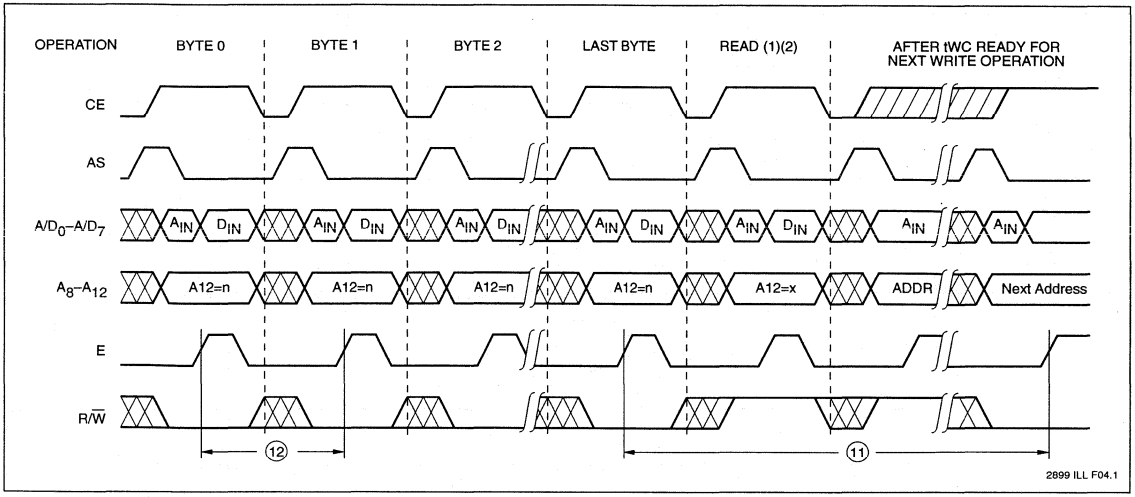
2899 PGM T11

E Controlled Write Cycle



Note: (4) t_{WC} is the minimum cycle time to be allowed from the system perspective unless polling techniques are used. It is the maximum time the device requires to automatically complete the internal write operation.

Page Write Timing Sequence for E Controlled Operation



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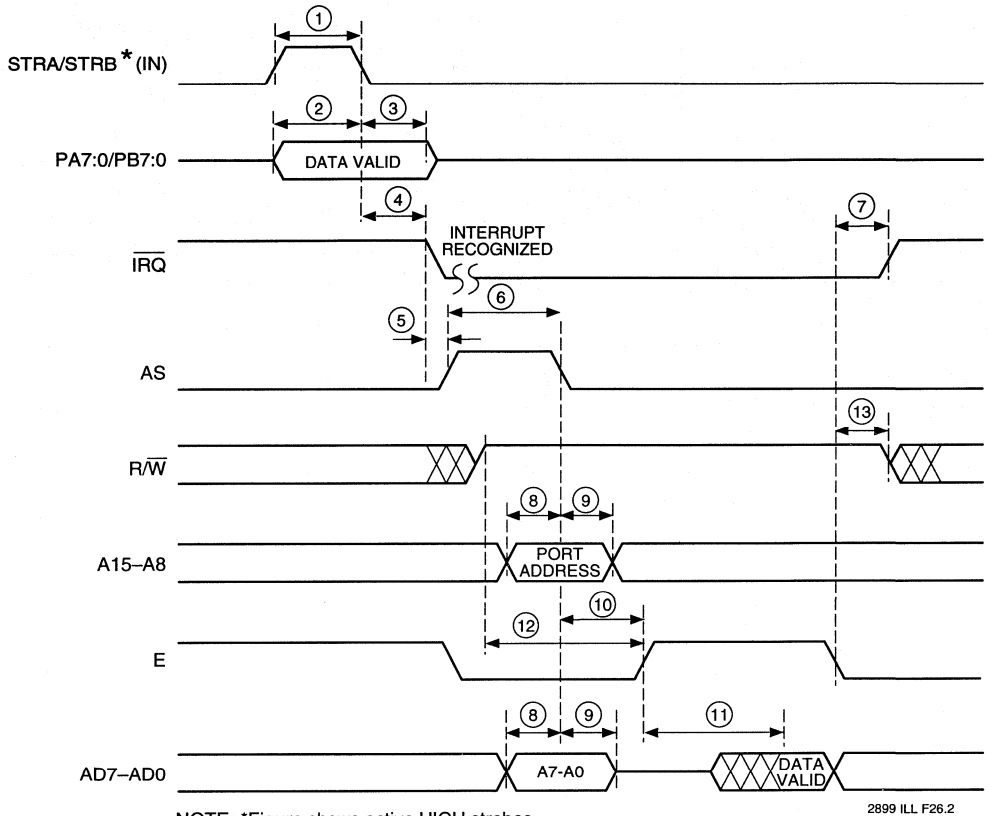
Port Read Diagram



NOTE: *Figure shows active HIGH strobes.

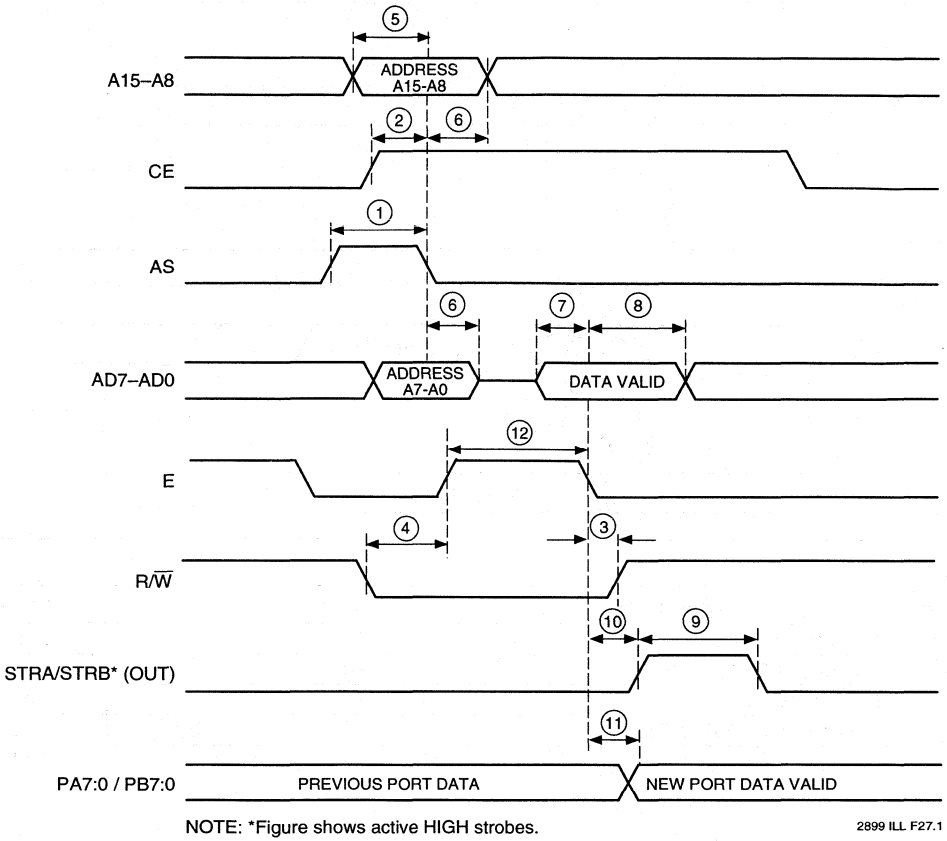
2899 ILL F26.2

PORT READ TIMING

No.	Symbol	Parameter	Min.	Max.	Units
1	t_{SVSX}	Strobe Pulse Width	80		ns
2	t_{IS}	Data Port Setup	20		ns
3	t_{IH}	Data Port Hold Time	30		ns
4	t_{SVIV}	Interrupt Request to Strobe		50	ns
5	t_{IAD}	$\overline{IRQ}$ to AS	0		ns
6	PW_{ASH}	AS Pulse Width	80		ns
7	t_{RXIX}	E to $\overline{IRQ}$ High	30		ns
8	t_{ASL}	Address setup time	20		ns
9	t_{AHL}	Address hold time	30		ns
10	t_{ASE}	AS to E High	30		ns
11	t_{ACCE}	E Access Time		120	ns
12	t_{RWS}	R/$\overline{W}$ Setup Time	30		ns
13	t_{RWH}	R/$\overline{W}$ Hold time	10		ns

2899 PGM T12.1

Port Write Diagram



NOTE: *Figure shows active HIGH strobes.

2899 ILL F27.1

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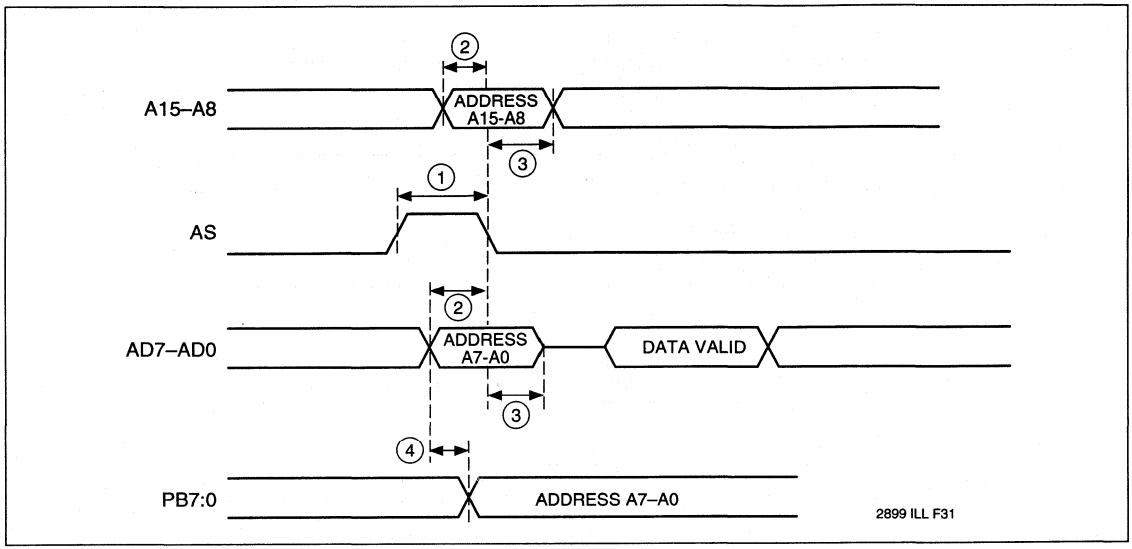
PORT WRITE TIMING

No.	Symbol	Parameter	Min.	Max.	Units
1	PW_{ASH}	AS Pulse Width	80		ns
2	t_{WCS}	Write Chip Select Setup Time	20		ns
3	t_{WH}	Write Pulse Hold Time	10		ns
4	t_{WV}	Write Pulse Valid to E Rise	30		ns
5	t_{AVLL}	Address Setup Time	20		ns
6	t_{LLAX}	Write Address Hold Time	30		ns
7	t_{DVWH}	Data Setup Time	50		ns
8	t_{WHDX}	Data Hold Time	10		ns
9	t_{SVSX}	Strobe Pulse Width	120		ns
10	t_{QVSV}	Strobe Access Time		40	ns
11	t_{POS}	Port Output Setup Time		40	ns
12	P_{WEH}	E Clock Pulse Width	150		ns

2899 PGM T13.1

LAM (Latch Address Mode) Diagram

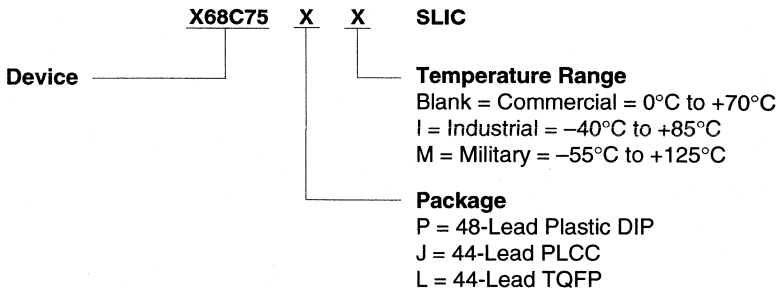


LAM TIMING

No.	Symbol	Parameter	Min.	Max.	Units
1	t_{LHLL}	AS Pulse Width	80		ns
2	t_{AVLL}	Address Setup Time	20		ns
3	t_{LLAX}	Address Hold Time	30		ns
4	t_{POS}	Port Output Setup Time		20	ns

2899 PGM T14.1

ORDERING INFORMATION



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NOTES

256K X68257 32,768 x 8 Bit

E^2 Micro-Peripheral

FEATURES

- **Multiplexed Address/Data Bus**
  - **—Direct Interface to Popular 68HC11 Family**
- **High Performance CMOS**
  - **—Fast Access Time, 120ns**
  - **—Low Power**
    - **—60mA Active Maximum**
    - **—500μA Standby Maximum**
- **Software Data Protection**
- **Toggle Bit Polling**
  - **—Early End of Write Detection**
- **Page Mode Write**
  - **—Allows up to 128 Bytes to be Written in One Write Cycle**
- **High Reliability**
  - **—Endurance: 10,000 Write Cycle**
  - **—Data Retention: 100 Years**

DESCRIPTION

The X68257 is an 32K x 8 E²PROM fabricated with advanced CMOS Textured Poly Floating Gate Technology. The X68257 features a multiplexed address and data bus allowing direct interface to a variety of popular single-chip microcontrollers operating in expanded multiplexed mode without the need for additional interface circuitry.

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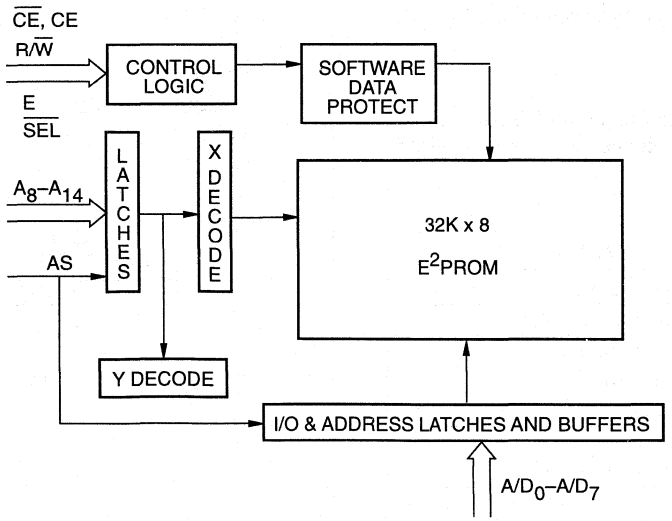
FUNCTIONAL DIAGRAM



6539 ILL F02.2

PIN DESCRIPTIONS

Address/Data (A/D_0–A/D_7)

Multiplexed low-order addresses and data. The addresses flow into the device while AS is HIGH. After AS transitions from a HIGH to LOW the addresses are latched. Once the addresses are latched these pins input data or output data depending on R/$\overline{W}$, $\overline{SEL}$, and CE.

Addresses (A_8–A_{14})

High order addresses flow into the device when AS = V_{IH} and are latched when AS goes LOW.

Chip Enable ($\overline{CE}$)

The Chip Enable input must be LOW to enable all read/write operations. When $\overline{CE}$ is HIGH, AS is LOW, and CE is LOW, the X68257 is placed in the low power standby mode.

Chip Enable (CE)

Chip Enable is active HIGH. When CE is used to select the device, the CE must be tied HIGH.

Program Store Enable ($\overline{SEL}$)

When the X68257 is to be used in a 68XX-based system, $\overline{SEL}$ is tied to V_{SS}.

Read/Write (R/$\overline{W}$)

When the X68257 is to be used in a 68XX-based system, R/$\overline{W}$ is tied directly to the microcontroller's R/$\overline{W}$ output.

Address Strobe (AS)

Addresses flow through the latches to address decoders when AS is HIGH and are latched when AS transitions from a HIGH to LOW.

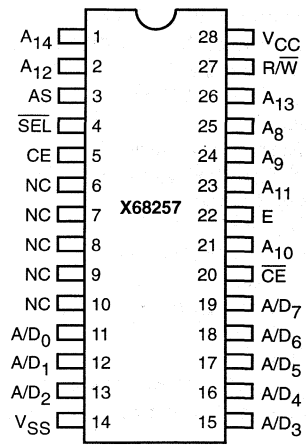
PIN NAMES

Symbol	Description
AS	Address Strobe
A/D_0–A/D_7	Address Inputs/Data I/O
A_8–A_{12}	Address Inputs
E	Enable Input
R/$\overline{W}$	Read/Write Input
CE, $\overline{CE}$	Chip Enable
$\overline{WC}$	Write Control
$\overline{SEL}$	Device Select—Connect to V_{SS}
V_{SS}	Ground
V_{CC}	Supply Voltage

6539 PGM T01.1

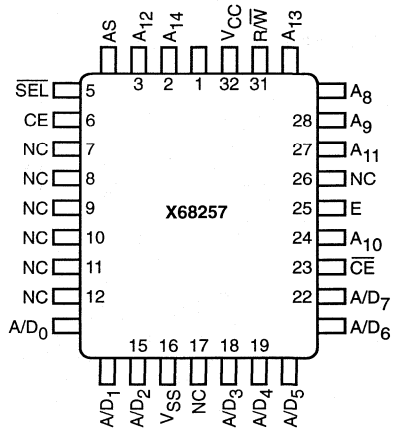
PIN CONFIGURATION

PDIP
CERDIP
SOIC



6539 FHD F01.2

LCC
PLCC



6539 FHD F01A.3

PRINCIPLES OF OPERATION

The X68257 is a highly integrated peripheral device for a wide variety of single-chip microcontrollers. The X68257 provides 32K-bytes of 5V E²PROM which can be used either for program storage, data storage, or a combination of both, in systems based upon Von Neumann (68XX) architectures. The X68257 incorporates the interface circuitry normally needed to decode the control signals and demultiplex the address/data bus to provide a "seamless" interface.

The interface inputs on the X68257 are configured such that it is possible to directly connect them to the proper interface signals of the appropriate single-chip microcontroller.

The X68257 features the industry standard 5V E²PROM characteristics such as byte or page mode write and Toggle Bit Polling.

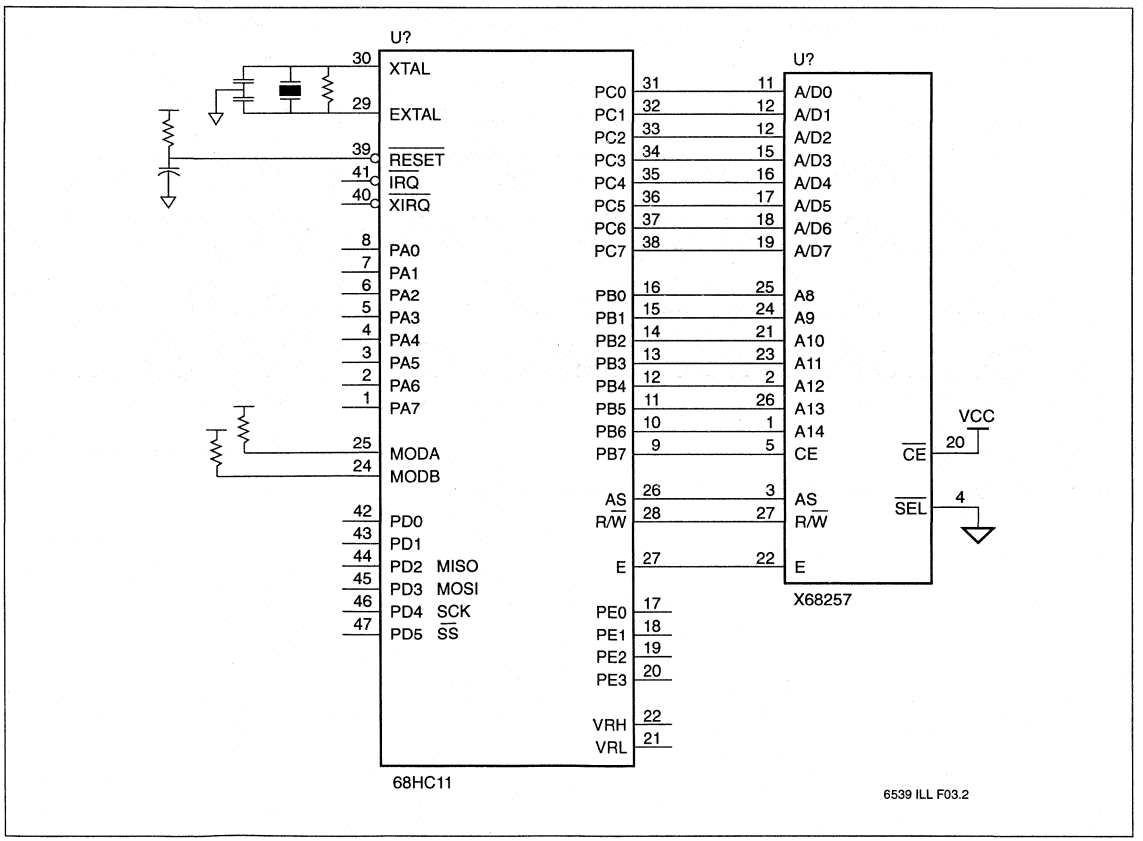
DEVICE OPERATION

Motorola 68XX operation requires the microcontroller AS, E, and R/$\overline{W}$ outputs to be tied to the X68257 AS, E, and R/$\overline{W}$ inputs respectively.

The falling edge of AS will latch the addresses for both a read and write operation. The state of the R/$\overline{W}$ output determines the operation to be performed, with the E signal acting as a data strobe.

If R/$\overline{W}$ is HIGH and CE is HIGH (read operation) data will be output on A/D_0–A/D_7 after E transitions HIGH. If R/$\overline{W}$ is LOW and CE is HIGH (write operation) data present at A/D_0–A/D_7 will be strobed into the X68257 on the HIGH to LOW transition of E.

Typical Application



MODE SELECTION

CE	E	R/$\overline{W}$	Mode	I/O	Power
V_{SS}	X	X	Standby	High Z	Standby (CMOS)
LOW	X	X	Standby	High Z	Standby (TTL)
HIGH	HIGH	HIGH	Read	D_{OUT}	Active
HIGH	↘	LOW	Write	D_{IN}	Active

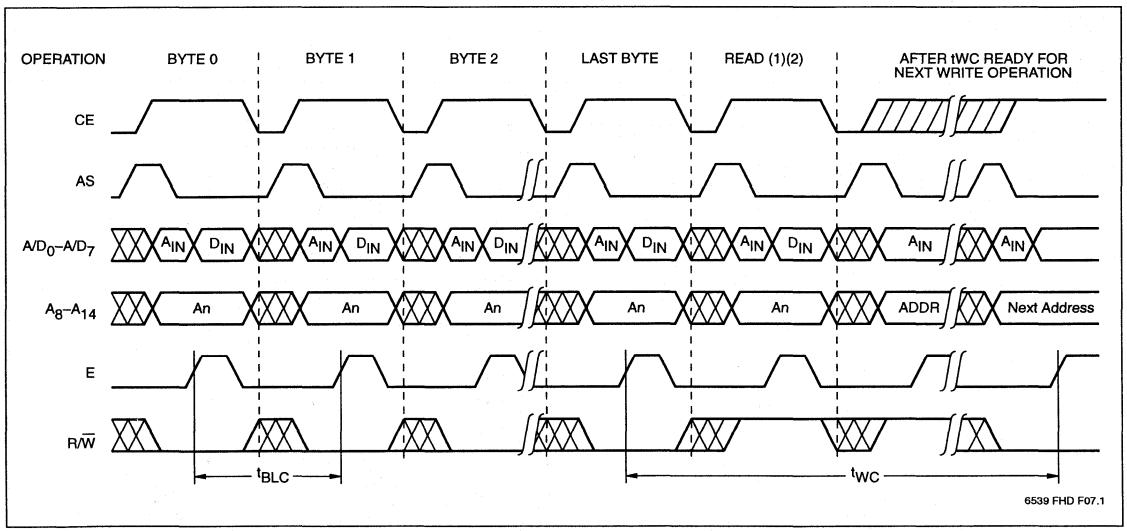
6539 PGM T02.2

PAGE WRITE OPERATION

Regardless of the microcontroller employed, the X68257 supports page mode write operations. This allows the microcontroller to write from 1 to 128 bytes of data to the X68257. Each individual write within a page write operation must conform to the byte write timing requirements.

The rising edge of E starts a timer delaying the internal programming cycle 100µs. Therefore, each successive write operation must begin within 100µs of the last byte written. The following waveforms illustrate the sequence and timing requirements.

Page Write Timing Sequence for E Controlled Operation

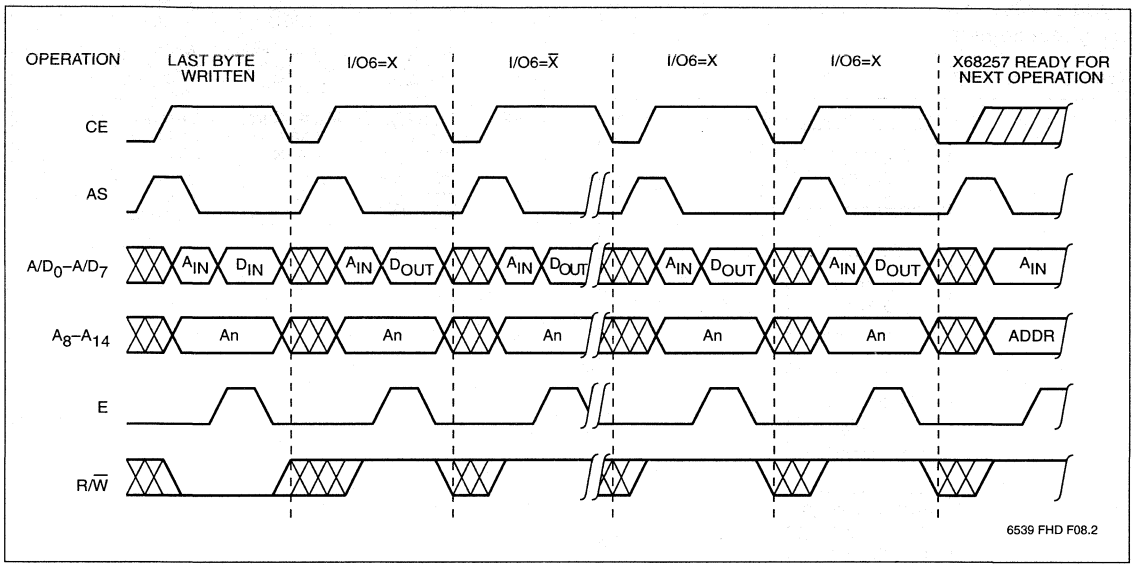


Note: (1) For each successive write within a page write cycle A_7–A_{14} must be the same.

Toggle Bit Polling

Because the typical write timing is less than the specified 5ms, Toggle Bit Polling has been provided to determine the early end of write. During the internal programming cycle I/O_6 will toggle from "1" to "0" and "0" to "1" on subsequent attempts to read the device. When the internal cycle is complete, the toggling will cease and the device will be accessible for additional read or write operations.

Toggle Bit Polling E Control



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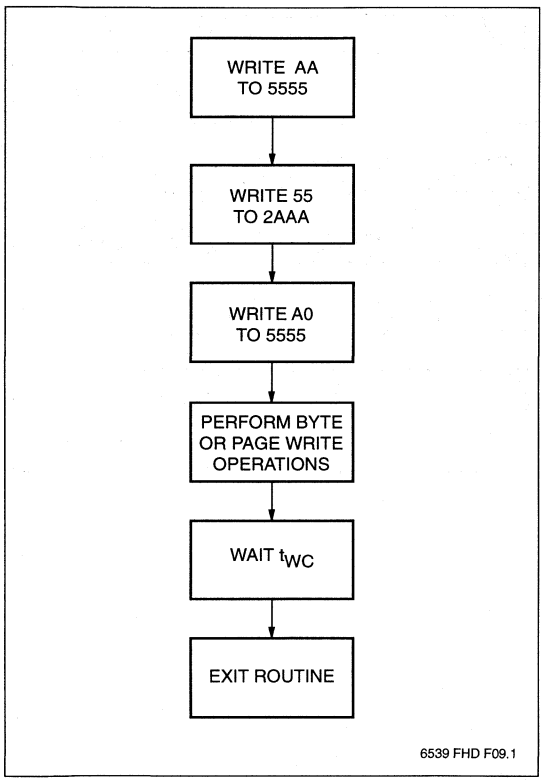
Software Data Protection

Software Data Protection (SDP) is employed to protect the entire array against inadvertent writes. To write to the X68257, a three-byte command sequence must precede the byte(s) being written.

All write operations, both the command sequence and any data write operations must conform to the page write timing requirements.

Writing with SDP



SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
———	Must be steady	Will be steady
———		
///	May change from LOW to HIGH	Will change from LOW to HIGH
\\\	May change from HIGH to LOW	Will change from HIGH to LOW
XXX	Don't Care: Changes Allowed	Changing: State Not Known
>>>	N/A	Center Line is High Impedance

ABSOLUTE MAXIMUM RATINGS*

Temperature under Bias ..... –65°C to +135°C
Storage Temperature ..... –65°C to +150°C
Voltage on any Pin with
Respect to V_{SS} ..... –1V to +7V
D.C. Output Current 5mA
Lead Temperature
(Soldering, 10 seconds) ..... 300°C

***COMMENT**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	+70°C
Industrial	–40°C	+85°C
Military	–55°C	+125°C

6539 PGM T03.1

Supply Voltage	Limits
X68257	5V ±10%

6539 PGM T04.1

D.C. OPERATING CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
I_{CC}	V_{CC} Current (Active)		60	mA	CE = V_{IL}, All I/O's = Open, Other Inputs = V_{CC}, AS = V_{IH}
$I_{SB1(CMOS)}$	V_{CC} Current (Standby)		500	µA	CE = V_{SS}, All I/O's = Open,Other Inputs = V_{CC} – 0.3V, AS = V_{SS}
$I_{SB2(TTL)}$	V_{CC} Current (Standby)		6	mA	CE = V_{IH}, All I/O's = Open, Other Inputs = V_{IH}, AS = V_{IL}
I_{LI}	Input Leakage Current		10	µA	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output Leakage Current		10	µA	V_{OUT} = V_{SS} to V_{CC}, E = V_{IL}
V_{IL}(1)	Input LOW Voltage	–1	0.8	V	
V_{IH}(1)	Input HIGH Voltage	2	V_{CC} + 0.5	V	
V_{OL}	Output LOW Voltage		0.4	V	I_{OL} = 2.1mA
V_{OH}	Output HIGH Voltage	2.4		V	I_{OH} = –400µA

6539 PGM T05.1

CAPACITANCE T_A = +25°C, f = 1MHz, V_{CC} = 5V

Symbol	Test	Max.	Units	Conditions
$C_{I/O}$(2)	Input/Output Capacitance	10	pF	$V_{I/O}$ = 0V
C_{IN}(2)	Input Capacitance	6	pF	V_{IN} = 0V

6539 PGM T06

POWER-UP TIMING

Symbol	Parameter	Max.	Units
t_{PUR}(2)	Power-Up to Read	1	ms
t_{PUW}(2)	Power-Up to Write	5	ms

6539 PGM T07

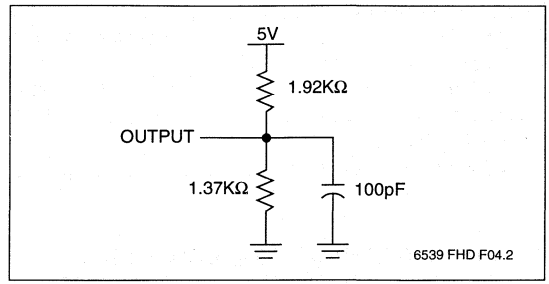
Notes: (1) V_{IL} min. and V_{IH} max. are for reference only and are not tested.
(2) This parameter is periodically sampled and not 100% tested.

A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3V
Input Rise and Fall Times	10ns
Input and Output Timing Levels	1.5V

6539 PGM T08.1

TEST CIRCUIT



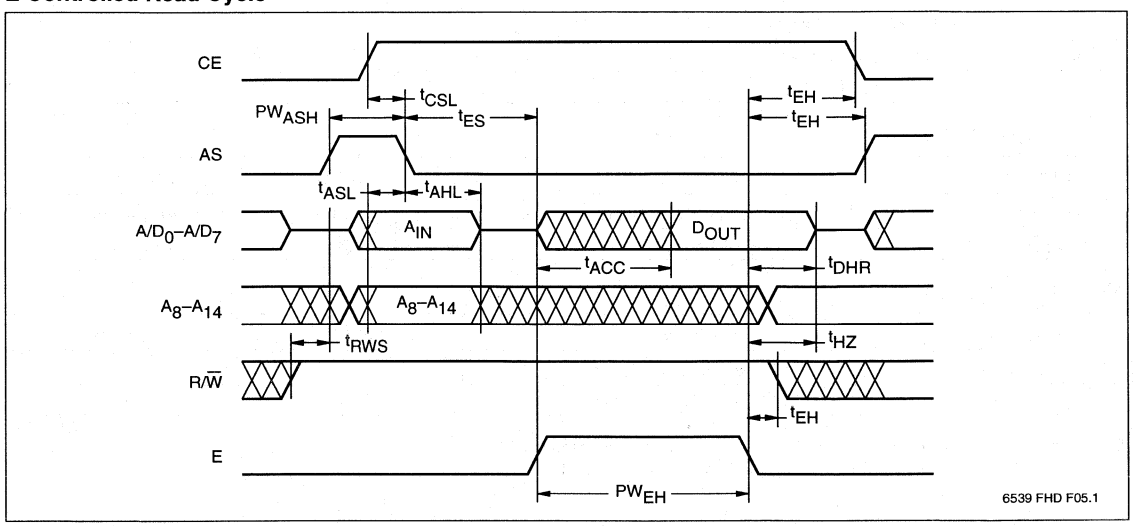
A.C. CHARACTERISTICS (Over the recommended operating conditions unless otherwise specified.)

E Controlled Read Cycle

Symbol	Parameter	Min.	Max.	Units
PW_{ASH}	Address Strobe Pulse Width	80		ns
t_{ASL}	Address Setup Time	20		ns
t_{AHL}	Address Hold Time	30		ns
t_{ACC}	Data Access Time		120	ns
t_{DHR}	Data Hold Time	0		ns
t_{CSL}	CE Setup Time	7		ns
PW_{EH}	E Pulse Width	150		ns
t_{ES}	Enable Setup Time	30		ns
t_{EH}	E Hold Time	20		ns
t_{RWS}	R/$\overline{W}$ Setup Time	20		ns
t_{HZ}(3)	E LOW to High Z Output		50	ns
t_{LZ}(3)	E HIGH to Low Z Output	0		ns

6539 PGM T09.1

E Controlled Read Cycle



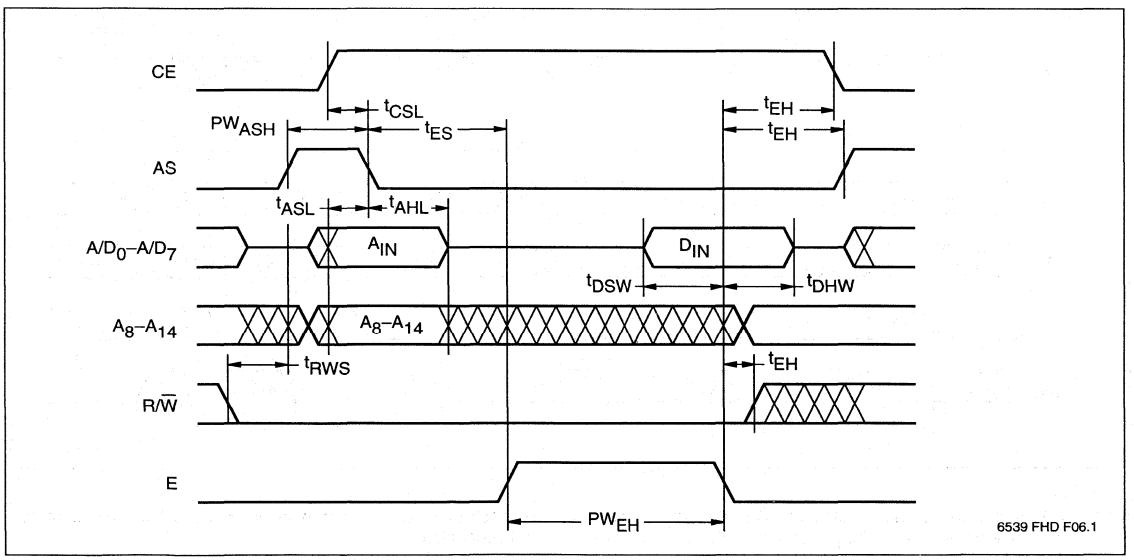
Note: (3) This parameter is periodically sampled and not 100% tested.

E Controlled Write Cycle

Symbol	Parameter	Min.	Max.	Units
PW_{ASH}	Address Strobe Pulse Width	80		ns
t_{ASL}	Address Setup Time	20		ns
t_{AHL}	Address Hold Time	30		ns
t_{DSW}	Data Setup Time	50		ns
t_{DHW}	Data Hold Time	30		ns
t_{CSL}	CE Setup Time	7		ns
PW_{EH}	E Pulse Width	120		ns
t_{WC}	Write Cycle Time		5	ms
t_{ES}	Enable Setup Time	30		ns
t_{RWS}	R/$\overline{W}$ Setup Time	20		ns
t_{EH}	E Hold Time	20		ns
t_{BLC}	Byte Load Time (Page Write)	0.5	100	µs

6539 PGM T10

E Controlled Write Cycle



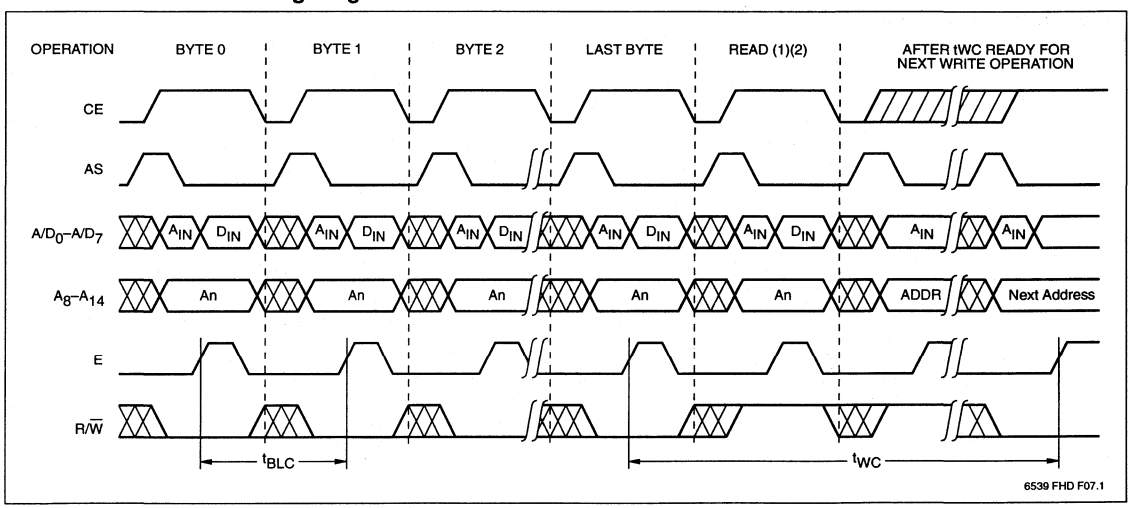
Note: (4) t_{WC} is the minimum cycle time to be allowed from the system perspective unless polling techniques are used. It is the maximum time the device requires to automatically complete the internal write operation.

$\overline{WR}$ Controlled Write Cycle

Symbol	Parameter	Min.	Max.	Units
t_{LHLL}	ALE Pulse Width	80		ns
t_{AVLL}	Address Setup Time	20		ns
t_{LLAX}	Address Hold Time	30		ns
t_{DVWH}	Data Setup Time	50		ns
t_{WHDX}	Data Hold Time	30		ns
t_{ELLL}	Chip Enable Setup Time	7		ns
t_{WLWH}	$\overline{WR}$ Pulse Width	120		ns
t_{WRS}	$\overline{WR}$ Setup Time	30		ns
t_{WRH}	$\overline{WR}$ Hold Time	20		ns
t_{BLC}	Byte Load Time (Page Write)	0.5	100	µs
t_{WC} (7)	Write Cycle Time		5	ms

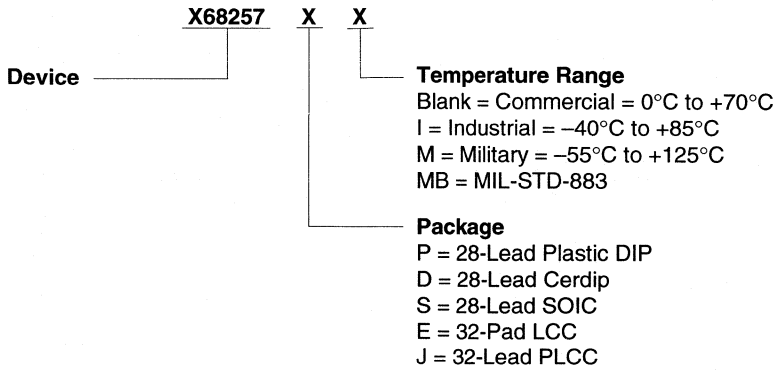
6539 PGM T11

$\overline{WR}$ Controlled Write Timing Diagram



Note: (7) t_{WC} is the minimum cycle time to be allowed from the system perspective unless polling techniques are used. It is the maximum time the device requires to automatically complete the internal write operation.

ORDERING INFORMATION



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NOTES

8051 Microcontroller Family Compatible

64K X88C64 8192 x 8 Bit

E² Micro-Peripheral

FEATURES

- CONCURRENT READ WRITE™
  - —Dual Plane Architecture
    - —Isolates Read/Write Functions Between Planes
    - —Allows Continuous Execution of Code From One Plane While Writing in the Other Plane
- Multiplexed Address/Data Bus
  - —Direct Interface to Popular 8051 Family
- High Performance CMOS
  - —Fast Access Time, 120ns
  - —Low Power
    - —60mA Active Maximum
    - —500µA Standby Maximum
- Software Data Protection
- Block Protect Register
  - —Individually Set Write Lock Out in 1K Blocks
- Toggle Bit Polling
  - —Early End of Write Detection
- Page Mode Write
  - —Allows up to 32 Bytes to be Written in One Write Cycle
- High Reliability
  - —Endurance: 100,000 Write Cycle
  - —Data Retention: 100 Years

DESCRIPTION

The X88C64 is an 8K x 8 E²PROM fabricated with advanced CMOS Textured Poly Floating Gate Technology. The X88C64 features a Multiplexed Address and Data bus allowing a direct interface to a variety of popular single-chip microcontrollers operating in expanded multiplexed mode without the need for additional interface circuitry.

The X88C64 is internally configured as two independent 4K x 8 memory arrays. This feature provides the ability to perform nonvolatile memory updates in one array and continue operation out of code stored in the other array; effectively eliminating the need for an auxiliary memory device for code storage.

To write to the X88C64, a three-byte command sequence must precede the byte(s) being written. The X88C64 also provides a second generation software data protection scheme called Block Protect. Block Protect can provide write lockout of the entire device or selected 1K blocks. There are eight 1K x 8 blocks that can be write protected individually in any combination required by the user. Block Protect, in addition to Write Control input, allows the different segments of the memory to have varying degrees of alterability in normal system operation.

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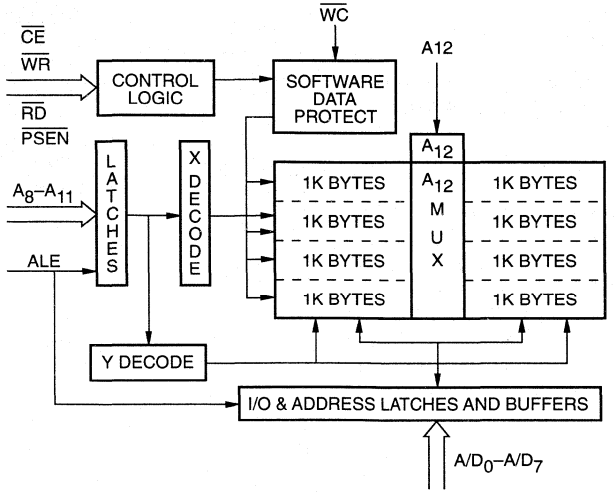
FUNCTIONAL DIAGRAM



3867 FHD F02

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PIN DESCRIPTIONS

Address/Data (A/D_0–A/D_7)

Multiplexed low-order addresses and data. The Addresses flow into the device while ALE is HIGH. After ALE transitions from a HIGH to LOW the addresses are latched. Once the addresses are latched these pins input data or output data depending on $\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, and $\overline{CE}$.

Addresses (A_8–A_{12})

High order addresses flow into the device when ALE is HIGH and are latched when ALE goes LOW.

Chip Enable ($\overline{CE}$)

The Chip Enable input must be LOW to enable all read/write operations. When $\overline{CE}$ is HIGH and ALE is LOW, the X88C64 is placed in the low power standby mode.

Program Store Enable ($\overline{PSEN}$)

When the X88C64 is to be used in a 8051 based system, $\overline{PSEN}$ is tied directly to the microcontroller's $\overline{PSEN}$ output.

Read ($\overline{RD}$)

When the X88C64 is to be used in a 8051 based system, $\overline{RD}$ is tied directly to the microcontroller's $\overline{RD}$ output.

Write ($\overline{WR}$)

When the X88C64 is to be used in a 8051 based system, $\overline{WR}$ is tied directly to the microcontroller's $\overline{WR}$ output.

Address Latch Enable (ALE)

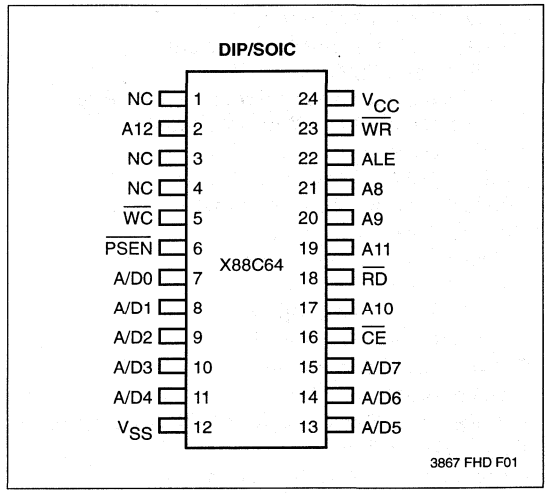
Addresses flow through the latches to address decoders when ALE is HIGH and are latched when ALE transitions from a HIGH to LOW.

Write Control ($\overline{WC}$)

The Write Control allows external circuitry to abort a page load cycle once it has been initiated. This input is useful in applications in which a power failure or processor RESET could interrupt a page load cycle. In this case, the microcontroller might drive all signals HIGH, causing bad data to be latched into the E^2PROM. If the Write Control input is driven HIGH (before t_{BLC} Max) after Write ($\overline{WR}$) goes HIGH, the write cycle will be aborted.

When $\overline{WC}$ is LOW (tied to V_{SS}) the X88C64 will be enabled to perform write operations. When $\overline{WC}$ is HIGH normal read operations may be performed, but all attempts to write to the device will be disabled.

PIN CONFIGURATION



PIN NAMES

Symbol	Description
ALE	Address Latch Enable
A/D_0–A/D_7	Address Inputs/Data I/O
A_8–A_{12}	Address Inputs
$\overline{RD}$	Read Input
$\overline{WR}$	Write Input
$\overline{PSEN}$	Program Store Enable Input
$\overline{CE}$	Chip Enable
$\overline{WC}$	Write Control
V_{SS}	Ground
V_{CC}	Supply Voltage
NC	No Connect

3867 PGM T01.1

PRINCIPLES OF OPERATION

The X88C64 is a highly integrated peripheral device for a wide variety of single-chip microcontrollers. The X88C64 provides 8K bytes of E²PROM which can be used either for Program Storage, Data Storage, or a combination of both in systems based upon Harvard (80XX) architectures. The X88C64 incorporates the interface circuitry normally needed to decode the control signals and demultiplex the Address/Data bus to provide a "Seamless" interface.

The interface inputs on the X88C64 are configured such that it is possible to directly connect them to the proper interface signals of the appropriate single-chip microcontroller. In the Harvard type system, the reading of data from the chip is controlled either by the $\overline{PSEN}$ or the $\overline{RD}$ signal, which essentially maps the X88C64 into both the Program and the Data Memory address map.

The X88C64 is internally organized as two independent planes of 4K bytes of memory with the A_{12} input selecting which of the two planes of memory are to be accessed. While the processor is executing code out of one plane, write operations can take place in the other plane, allowing the processor to continue execution of code out of the X88C64 during a byte or page write to the device.

The X88C64 also features an advanced implementation of the Software Data Protection scheme, called Block Protect, which allows the device to be broken into 8 independent sections of 1K bytes. Each of these sections can be independently enabled for write operations; thereby allowing certain sections of the device to be secured so that updates can only occur in a controlled environment (e.g. in an automotive application, only at an authorized service center). The desired set-up configuration is stored in a nonvolatile register, ensuring the configuration data will be maintained after the device is powered down.

The X88C64 also features a Write Control input ($\overline{WC}$), which serves as an external control over the completion of a previously initiated page load cycle.

The X88C64 also features the industry standard E²PROM characteristics such as byte or page mode write and Toggle Bit Polling.

DEVICE OPERATION

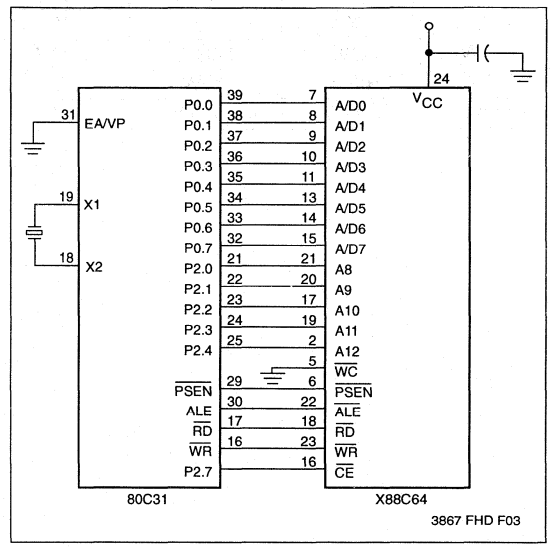
MODES

Mixed Program/Data Memory

By properly assigning the address spaces, a single X88C64 can be used as both the Program and Data Memory. This would be accomplished by connecting all of the 8051 control outputs to the corresponding inputs of the X88C64.

In this configuration, one plane of memory could be dedicated to Program Storage and the other plane dedicated to Data Storage. The Data Storage can be fully protected by enabling block protect write lockout.

TYPICAL APPLICATION



Program Memory Mode

This mode of operation is read-only. The $\overline{PSEN}$ and $\overline{ALE}$ inputs of the X88C64 are tied directly to the $\overline{PSEN}$ and ALE outputs of the microcontroller. The $\overline{RD}$ and $\overline{WR}$ inputs are tied HIGH.

When ALE is HIGH, the A/D_0–A/D_7 and A_8–A_{12} addresses flow into the device. The addresses, both low and high order, are latched when ALE transitions LOW (V_{IL}). $\overline{PSEN}$ will then go LOW and after t_{PLDV}, valid data is presented on the A/D_0–A/D_7 pins. $\overline{CE}$ must be LOW during the entire operation.

Data Memory Mode

This mode of operation allows both read and write functions. The $\overline{PSEN}$ input is tied to V_{IH} or to V_{CC} through a pull-up resistor. The ALE, $\overline{RD}$, and $\overline{WR}$ inputs are tied directly to the microcontroller's ALE, $\overline{RD}$, and $\overline{WR}$ outputs.

Read

This operation is quite similar to the Program Memory read. A HIGH to LOW transition on ALE latches the addresses and the data will be output on the AD pins after $\overline{RD}$ goes LOW (t_{RLDV}).

Write

A write is performed by latching the addresses on the falling edge of ALE. Then $\overline{WR}$ is strobed LOW followed by valid data being presented at the A/D_0–A/D_7 pins. The data will be latched into the X88C64 on the rising edge of $\overline{WR}$. To write to the X88C64, a three-byte command sequence must precede the byte(s) being written. (See Software Data Protection.)

MODE SELECTION

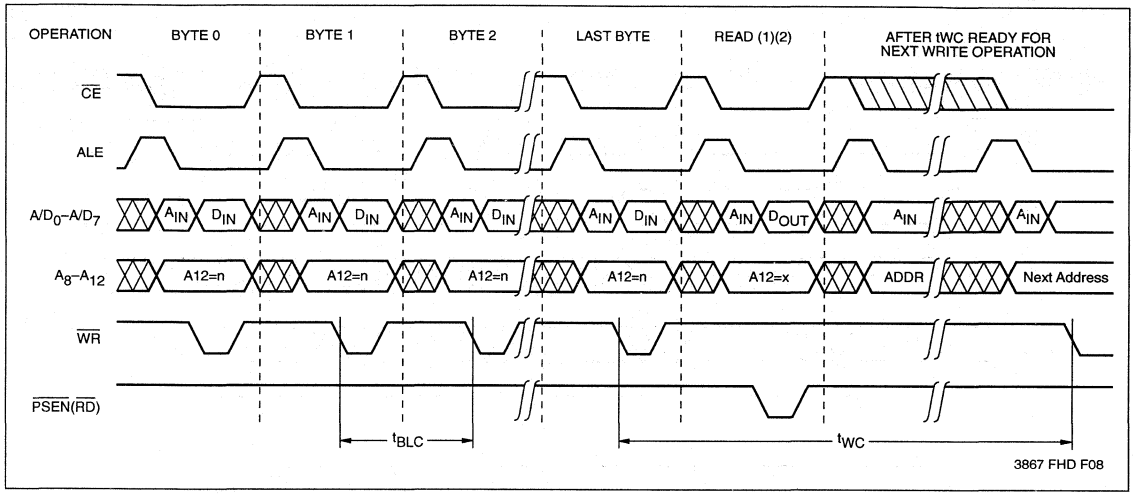
$\overline{CE}$	$\overline{PSEN}$	$\overline{RD}$	$\overline{WR}$	Mode	I/O	Power
V_{CC}	X	X	X	Standby	High Z	Standby (CMOS)
HIGH	X	X	X	Standby	High Z	Standby (TTL)
LOW	LOW	HIGH	HIGH	Program Fetch	D_{OUT}	Active
LOW	HIGH	LOW	HIGH	Data Read	D_{OUT}	Active
LOW	HIGH	HIGH	⌐	Write	D_{IN}	Active

3867 PGM T02.2

PAGE WRITE OPERATION

Regardless of the microcontroller employed, the X88C64 supports page mode write operations. This allows the microcontroller to write from one to thirty-two bytes of data to the X88C64. Each individual write within a page write operation must conform to the byte write timing requirements. The falling edge of $\overline{WR}$ starts a timer delaying the internal programming cycle 100µs. Therefore, each successive write operation must begin within 100µs of the last byte written. The following waveforms illustrate the sequence and timing requirements.

Page Write Timing Sequence for $\overline{WR}$ Controlled Operation



Notes: (1) For each successive write within a page write cycle A_5–A_{12} must be the same.

(2) Although it is not illustrated, the microcontroller may interleave read operations between the individual byte writes within the page write operation. Two responses are possible:

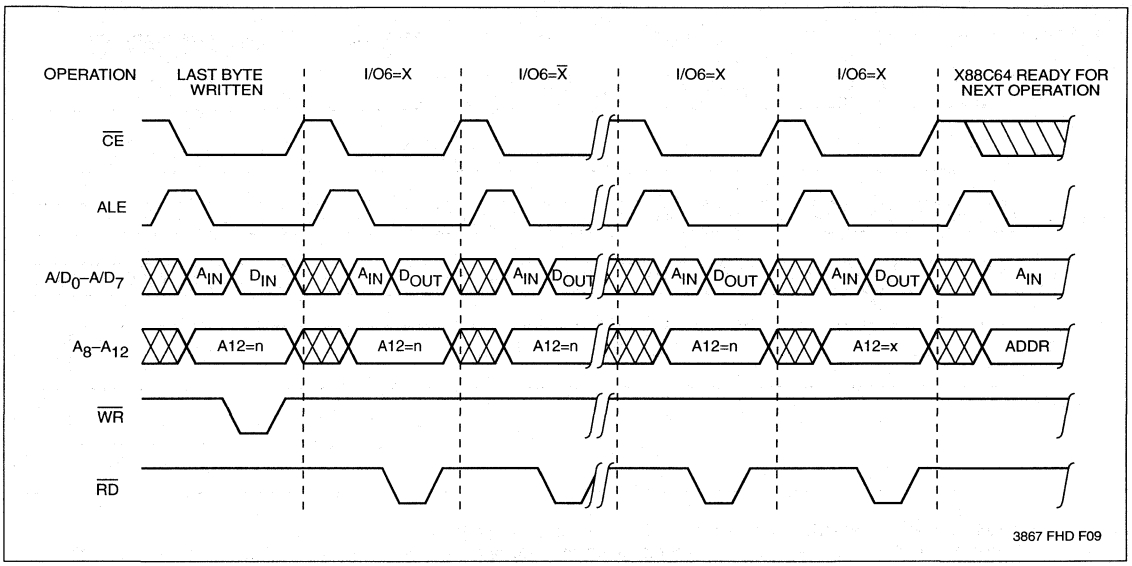
a. Reading from the same plane being written (A_{12} of Read = A_{12} of Write) is effectively a Toggle Bit Polling operation.

b. Reading from the opposite plane being written (A_{12} of Read ≠ A_{12} of Write) true data will be returned, facilitating the use of a single memory component as both program and data storage.

TOGGLE BIT POLLING

Because the X88C64 typical nonvolatile write cycle time is less than the specified 5ms, Toggle Bit Polling has been provided to determine the early completion of write. During the internal programming cycle I/O_6 will toggle from HIGH to LOW and LOW to HIGH on subsequent attempts to read the device. When the internal cycle is complete, the toggling will cease and the device will be accessible for additional read or write operations. Due to the dual plane architecture, reads for polling must occur in the plane that was written; that is, the state of A_{12} during a write must match the state of A_{12} during Toggle Bit Polling.

Toggle Bit Polling $\overline{RD}/\overline{WR}$ Control



SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

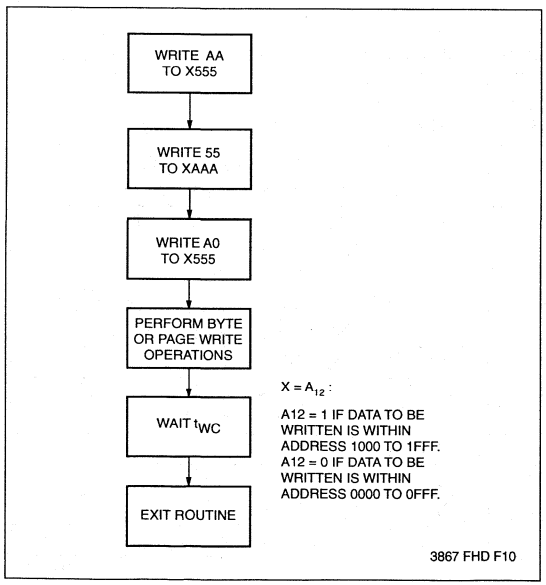
DATA PROTECTION

The X88C64 provides two levels of data protection through software control. There is a global software data protection feature similar to the industry standard for E²PROMs and a new Block Protect write lockout protection providing a secondary level of data security.

SOFTWARE DATA PROTECTION

Software Data Protection (SDP) is employed to protect the entire array against inadvertent writes. To write to the X88C64, a three-byte command sequence must precede the byte(s) being written. All write operations, both the command sequence and any data write operations, must conform to the page write timing requirements.

Writing with SDP

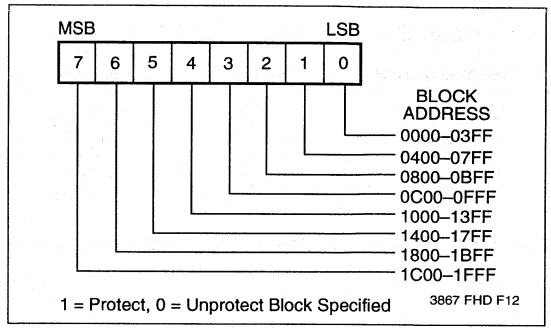


Block Protect Write Lockout

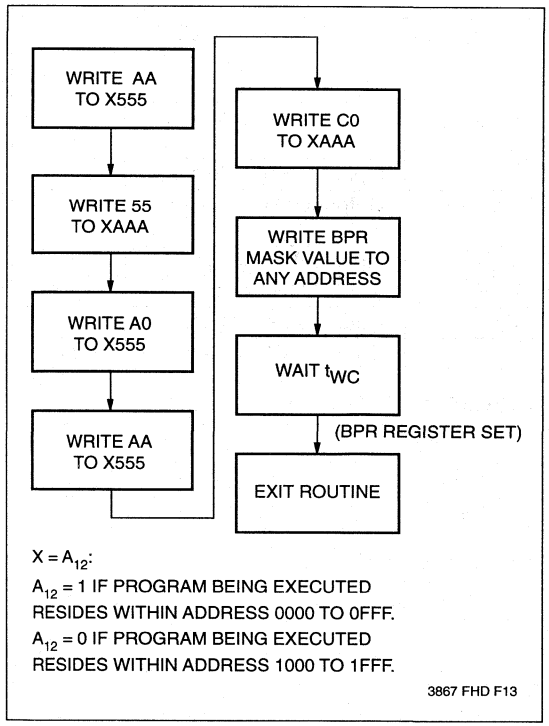
The X88C64 provides a secondary level of data security referred to as Block Protect write lockout. This is accessed through an extension of the SDP command sequence. Block Protect allows the user to lockout writes to any 1K x 8 blocks of memory. Unlike SDP which prevents inadvertent writes, but still allows easy system access to writing the memory, Block Protect will lockout all attempts unless it is specifically disabled by the host. This could be used to set a higher level of protection in a system where a portion of the memory is used for Program Storage and another portion is used as Data Storage.

Setting write lockout is accomplished by writing a five-byte command sequence, opening access to the Block Protect Register (BPR). After the fifth byte is written, the user writes to the BPR, selecting which blocks to protect or unprotect. All write operations, both the command sequence and writing the data to the BPR, must conform to the page write timing requirements.

Block Protect Register Format



Setting BPR Sequence



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ABSOLUTE MAXIMUM RATINGS*

Temperature under Bias ..... –65°C to +135°C
Storage Temperature ..... –65°C to +150°C
Voltage on any Pin with
Respect to V_{SS} ..... –1V to +7V
D.C. Output Current ..... 5 mA
Lead Temperature
(Soldering, 10 seconds) ..... 300°C

***COMMENT**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	+70°C
Industrial	–40°C	+85°C
Military	–55°C	+125°C

3867 PGM T03.1

Supply Voltage	Limits
X88C64	5V ±10%

3867 PGM T04.1

D.C. OPERATING CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
I_{CC}	V_{CC} Current (Active)		60	mA	$\overline{CE}$ = $\overline{RD}$ = V_{IL}, All I/O's = Open,Other Inputs = V_{CC}
$I_{SB1(CMOS)}$	V_{CC} Current (Standby)		500	µA	$\overline{CE}$ = V_{CC} – 0.3V, All I/O's = Open,Other Inputs = V_{CC} – 0.3V, ALE = V_{IL}
$I_{SB2(TTL)}$	V_{CC} Current (Standby)		6	mA	$\overline{CE}$ = V_{IH}, All I/O's = Open, Other Inputs = V_{IH}, ALE = V_{IL}
I_{LI}	Input Leakage Current		10	µA	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output Leakage Current		10	µA	V_{OUT} = V_{SS} to V_{CC}, $\overline{RD}$ = V_{IH} = $\overline{PSEN}$
V_{IL}(3)	Input LOW Voltage	–1	0.8	V	
V_{IH}(3)	Input HIGH Voltage	2	V_{CC} + 0.5	V	
V_{OL}	Output LOW Voltage		0.4	V	I_{OL} = 2.1 mA
V_{OH}	Output HIGH Voltage	2.4		V	I_{OH} = –400 µA

3867 PGM T05.2

CAPACITANCE T_A = +25°C, f = 1MHz, V_{CC} = 5V

Symbol	Test	Max.	Units	Conditions
$C_{I/O}$(4)	Input/Output Capacitance	10	pF	$V_{I/O}$ = 0V
C_{IN}(4)	Input Capacitance	6	pF	V_{IN} = 0V

3867 PGM T06

POWER-UP TIMING

Symbol	Parameter	Max.	Units
t_{PUR}(4)	Power-Up to Read	1	ms
t_{PUW}(4)	Power-Up to Write	5	ms

3867 PGM T07

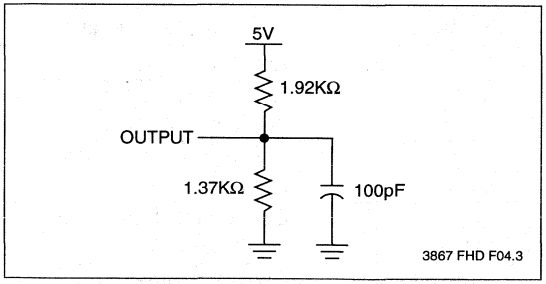
Notes: (3) V_{IL} min. and V_{IH} max. are for reference only and are not tested.
(4) This parameter is periodically sampled and not 100% tested.

A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3V
Input Rise and Fall Times	10ns
Input and Output Timing Levels	1.5V

3867 PGM T08.1

EQUIVALENT A.C. TEST CIRCUIT



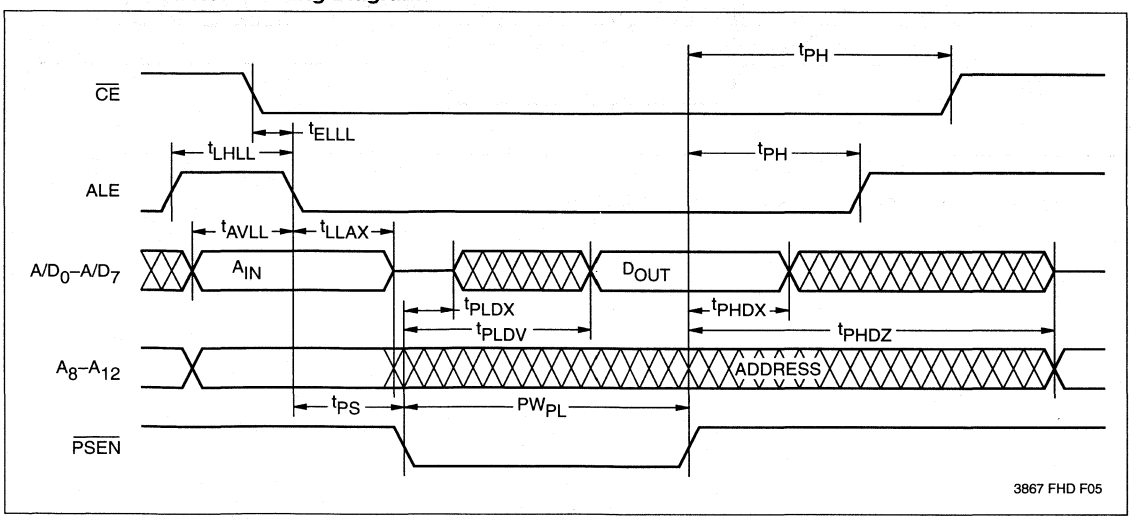
A.C. CHARACTERISTICS (Over the recommended operating conditions unless otherwise specified.)

$\overline{PSEN}$ Controlled Read Cycle

Symbol	Parameter	Min.	Max.	Units
t_{LHLL}	ALE Pulse Width	80		ns
t_{AVLL}	Address Setup Time	20		ns
t_{LLAX}	Address Hold Time	30		ns
t_{PLDV}	$\overline{PSEN}$ Read Access Time		120	ns
t_{PHDX}	Data Hold Time	0		ns
t_{ELLL}	Chip Enable Setup Time	7		ns
PW_{PL}	$\overline{PSEN}$ Pulse Width	150		ns
t_{PS}	$\overline{PSEN}$ Setup Time	30		ns
t_{PH}	$\overline{PSEN}$ Hold Time	20		ns
t_{PHDZ} (5)	$\overline{PSEN}$ Disable to Output in High Z		50	ns
t_{PLDX} (5)	$\overline{PSEN}$ to Output in Low Z	10		ns

3867 PGM T09

$\overline{PSEN}$ Controlled Read Timing Diagram



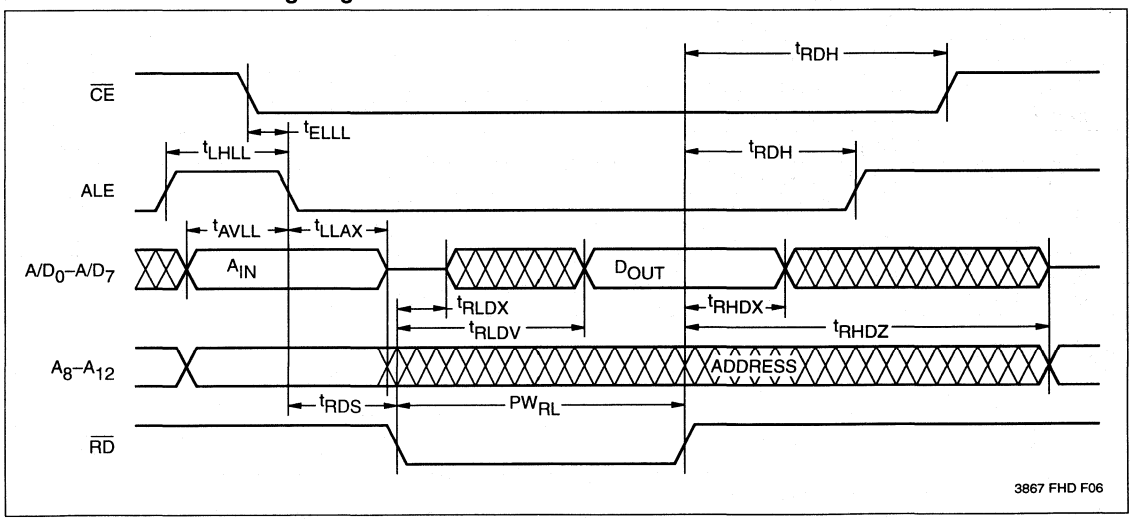
Note: (5) This parameter is periodically sampled and not 100% tested.

$\overline{RD}$ Controlled Read Cycle

Symbol	Parameter	Min.	Max.	Units
t_{LHLL}	ALE Pulse Width	80		ns
t_{AVLL}	Address Setup Time	20		ns
t_{LLAX}	Address Hold Time	30		ns
t_{RLDV}	$\overline{RD}$ Read Access Time		120	ns
t_{RHDX}	Data Hold Time	0		ns
t_{ELLL}	Chip Enable Setup Time	7		ns
PW_{RL}	$\overline{RD}$ Pulse Width	150		ns
t_{RDS}	$\overline{RD}$ Setup Time	30		ns
t_{RDH}	$\overline{RD}$ Hold Time	20		ns
t_{RHDZ} (6)	$\overline{RD}$ Disable to Output in High Z		50	ns
t_{RLDX} (6)	$\overline{RD}$ to Output in Low Z	0		ns

3867 PGM T10

$\overline{RD}$ Controlled Read Timing Diagram



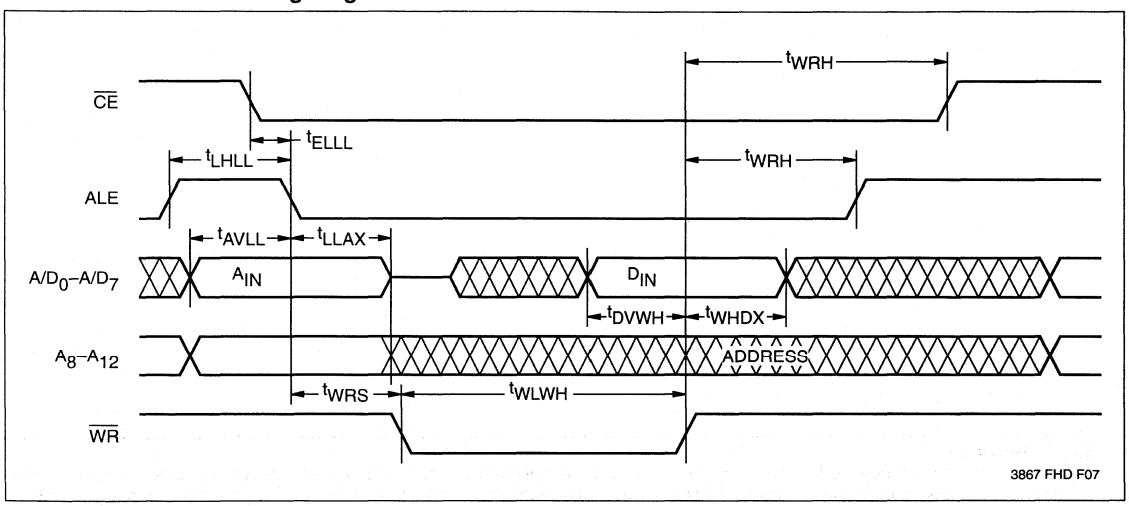
Note: (6) This parameter is periodically sampled and not 100% tested.

$\overline{WR}$ Controlled Write Cycle

Symbol	Parameter	Min.	Max.	Units
t_{LHLL}	ALE Pulse Width	80		ns
t_{AVLL}	Address Setup Time	20		ns
t_{LLAX}	Address Hold Time	30		ns
t_{DVWH}	Data Setup Time	50		ns
t_{WHDX}	Data Hold Time	30		ns
t_{ELLL}	Chip Enable Setup Time	7		ns
t_{WLWH}	$\overline{WR}$ Pulse Width	120		ns
t_{WRS}	$\overline{WR}$ Setup Time	30		ns
t_{WRH}	$\overline{WR}$ Hold Time	20		ns
t_{BLC}	Byte Load Time (Page Write)	0.5	100	µs
t_{WC} (7)	Write Cycle Time		5	ms

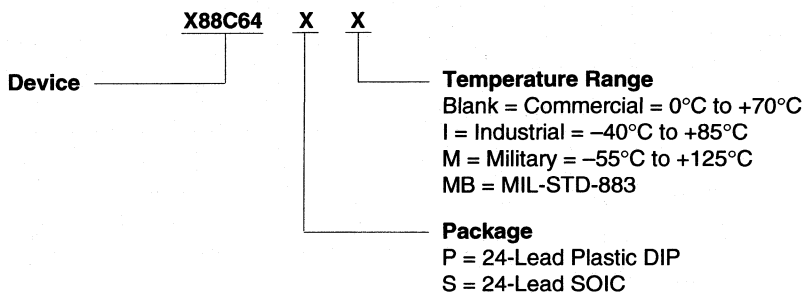
3867 PGM T11

$\overline{WR}$ Controlled Write Timing Diagram



Note: (7) t_{WC} is the minimum cycle time to be allowed from the system perspective unless polling techniques are used. It is the maximum time the device requires to automatically complete the internal write operation.

ORDERING INFORMATION



NOTES

Xicor®

#4

Design Engineering Bulletin

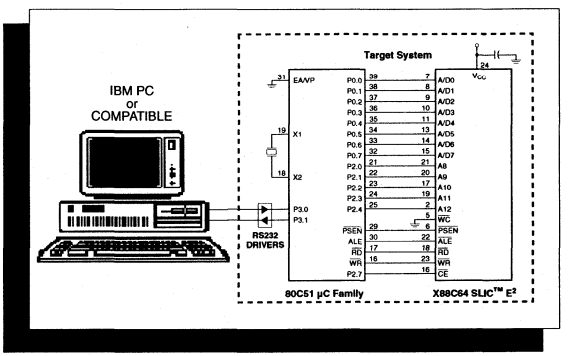
New Product and Applications Information for Design Engineers

SLIC® E²PROM Simplifies Embedded Systems Firmware / Software Programming and Updating

The new SLIC E²PROM devices provide embedded systems with a convenient method to program/update firmware and parametric data while reducing chip count and offering substantial cost savings. The SLIC E²PROM devices, without a need for an external latch, are addaptable to multiplexed address/data buses of the most popular microcontrollers. The SLIC E²PROMs are 5V in circuit re-programmable, thus eliminating off board programming and storage costs. The application firmware is transferred to the SLIC E² over the communication link established between the target system board and a host computer. This may be done many times during life of the end product, either at different stages of the manufacturing process, or after the system is installed in the field.

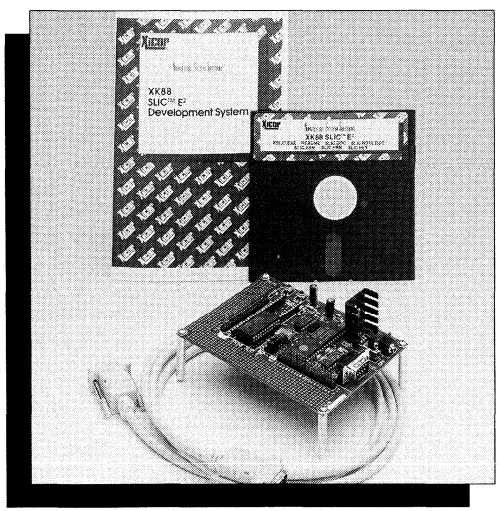
The 88C64/8051 and 68C64/68HC11 SLIC E²PROMs have 8Kx8 of program/data storage, approximately 500 bytes of that are taken up by the SLIC E² code. Other advanced features of the SLIC E²PROM family are: the concurrent read/write capability, software data protection (SDP), block protection (BPR), and byte/page alterablity.

The SLIC E²PROM devices contain controller specific routines written in assembly language to handle the following tasks: Boot firmware, Receive/ Transmit buffer management, command parser, system reset, device programming/verifying, and other device dependent operations. Using subroutine calls, the system application programs may interface the SLIC E²PROM BIOS code for I/O operations.



System example using an 80C31 and an X88C64 SLIC.

XK88 / 80C31 SLIC® E² Development System



XK88 SLIC Development System provides a complete design environment for 80C31 based systems.

The XK88 Development System is ideal for 80C51 based embedded system applications. It is useful for program debugging and/or 88C64 SLIC E² evaluation. The supplied emulation cable allows this system to replace a microcontroller in an existing design, and by transferring system firmware to the on-board SLIC E², execute and modify that code.

A prototype area is provided to design in additional functions. The diskette contains all the program files, device driver, and schematics drawing of the board along with the ORCAD's library files.

The XK88 is available from Xicor or Xicor's distributors. To order a XK88 SLIC E² Development System directly from Xicor.

APPLICATION NOTES AND DEVELOPMENT SYSTEM
AVAILABLE
AN62–64 • AN66 • AN68 • XK88

80C51 Microcontroller Family Compatible

64K X88C64 SLIC® E² 8192 x 8 Bit

E² Micro-Peripheral

FEATURES

SLIC (SELF LOADING INTEGRATED CODE) FIRMWARE

- **Automatically Downloads User's Software into 8051 Based Systems**
- **Features Load, Verify, and Block Protection Capabilities**
- **Transfers Baud Rate 9600 at 11MHz**
- **CONCURRENT READ WRITE™**
  - **—Dual Plane Architecture**
    - **—Isolates Read/Write Functions Between Planes**
    - **—Allows Continuous Execution of Code From One Plane While Writing in the Other Plane**
- **Multiplexed Address/Data Bus**
  - **—Direct Interface to Popular 8051 Family**
- **Block Protect Register**
  - **—Individually Set Write Lock Out in 1K Blocks**
- **Toggle Bit Polling**
  - **—Early End of Write Detection**
- **Page Mode Write**
  - **—Allows up to 32 Bytes to be Written in One Write Cycle**

DESCRIPTION

The X88C64 SLIC E² is a highly integrated E² Microcontroller peripheral which combines the functionality of the X88C64 component with pre-loaded software routines allowing any embedded system using it to upgrade and download software via the serial port. This self-loading integrated code eliminates the need to initially program the firmware into a memory device at the time of initial manufacture. The SLIC routines also greatly facilitate the loading of subsequent versions of the firmware into the system.

The SLIC routines consist of approximately 500 bytes of instructions for the 8051 which will initialize the microcontroller and its on-board UART and download the user's software through the UART. The baud rate for the transfer is 9600 based on a crystal frequency of 11MHz. Data transfer is accomplished using a proprietary format called XCOM. Xicor also has developed a program for IBM PCs and compatibles called XSLIC, which will translate an Intel HEX format file into XCOM format and upload the program to an X88C64 SLIC E².

The X88C64 device itself is an 8K x 8 E²PROM fabricated with advanced CMOS Textured Poly Float-

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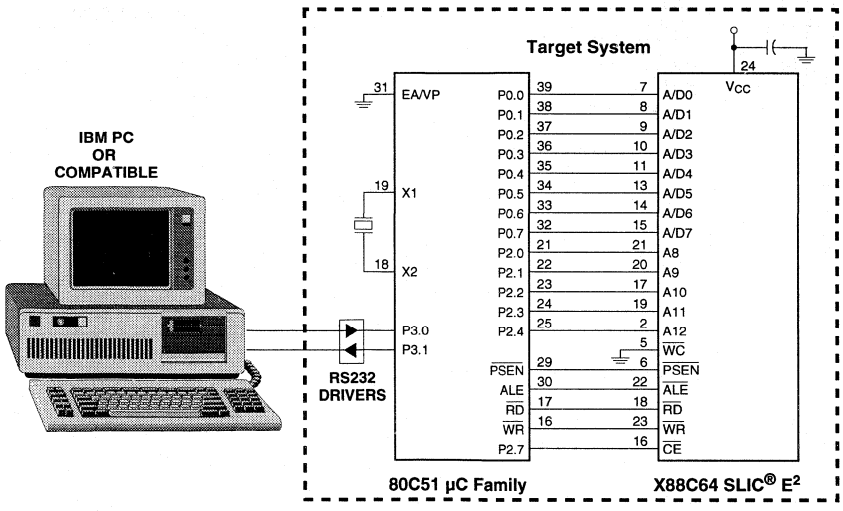
TYPICAL APPLICATION



6540 ILL F01.1

SLIC® E² and CONCURRENT READ WRITE™ are trademarks of Xicor, Inc.

ing Gate Technology. The X88C64 features a Multiplexed Address and Data bus allowing direct interface to a variety of popular single-chip microcontrollers operating in expanded multiplexed mode without the need for additional interface circuitry.

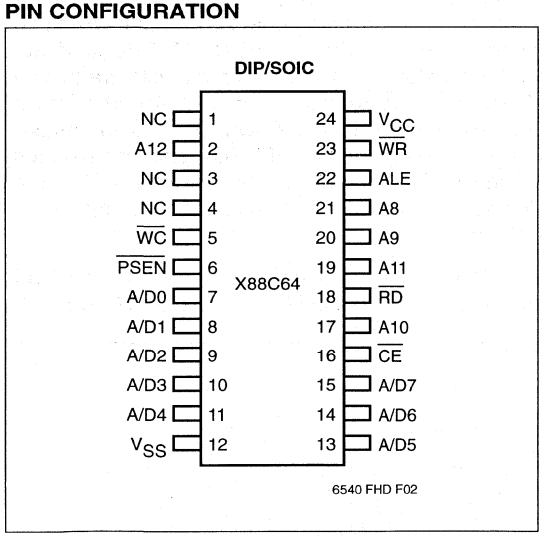
The X88C64 is internally configured as two independent 4K x 8 memory arrays. This feature provides the ability to perform nonvolatile memory updates in one array and continue operation out of code stored in the other array; effectively eliminating the need for an auxiliary memory device for code storage.

To write to the X88C64 SLIC E², a three-byte command sequence must precede the byte(s) being written. This sequence called Software Data Protection prevents the loss of data or program information due to inadvertant write cycles during power-up or power-down. The X88C64 SLIC E² also provides a second generation software data protection scheme called Block Protect.

Block Protect can provide write lockout of the entire device or selected 1K blocks. There are eight 1K x 8 blocks that can be write protected individually in any combination required by the user. Block Protect, in additional to Write Control input, allows the different segments of the memory to have varying degrees of alterability in normal system operation.

For further information on the X88C64 hardware interface, consult the X88C64 Data Sheet.

PIN CONFIGURATION

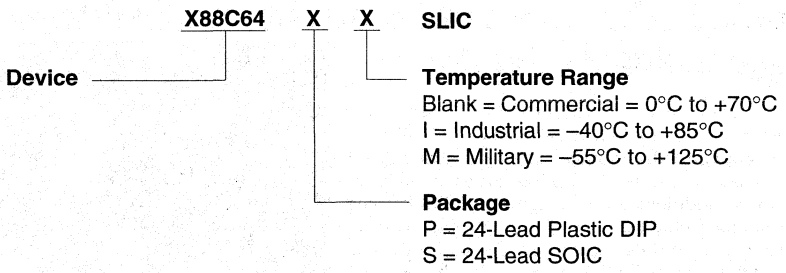


PIN NAMES

Symbol	Description
ALE	Address Latch Enable
A/D_0–A/D_7	Address Inputs/Data I/O
A_8–A_{12}	Address Inputs
$\overline{RD}$	Read Input
$\overline{WR}$	Write Input
$\overline{PSEN}$	Program Store Enable Input
$\overline{CE}$	Chip Enable
$\overline{WC}$	Write Control
V_{SS}	Ground
V_{CC}	Supply Voltage

6540 PGM T01

ORDERING INFORMATION



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Xicor®

#6

Design Engineering Bulletin

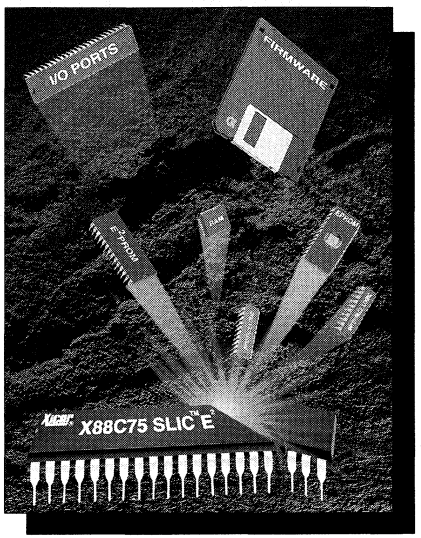
New Product and Applications Information for Design Engineers

X88C75 SLIC® E² Microcontroller Peripheral adds I/O ports, E²PROM, Static RAM, Interrupt controller and Address Decoding Logic to 80C31 Family

The X88C75 SLIC Microcontroller Peripheral is the ideal enhancement to 80C31 type systems. The device features 8K Bytes of E²PROM which may be used for either program or data storage and 16 bytes of static RAM for data parameter storage. The sophisticated 16 I/O lines are configurable as either Inputs or Outputs with two additional strobing signals for either latching data into the ports or for strobing data out. The Programmable Interrupt controller can be configured to generate interrupts from either data input into the ports or the completion of the internal E²PROM write cycle. The E²PROM features concurrent read during write operation which allows the controller to continue program execution from the E²PROM during a write cycle to the same device.

All internal resources are memory mapped and their location is programmable through the internal nonvolatile programmable decoder. This allows multiple X88C75 SLIC devices to be used to provide up to 64K bytes of E²PROM, 128 Bytes of RAM and 128 I/O lines without any additional logic. The X88C75 SLIC device also features an optional LAM (Latched Address Mode) mode of operation where the 8- I/O lines of port B are used to output the demultiplexed low order address byte of the 80C31 bus. This simplifies the inclusion of standard byte-wide memory devices such as SRAM, NOVRAM or EPROM into the system applications.

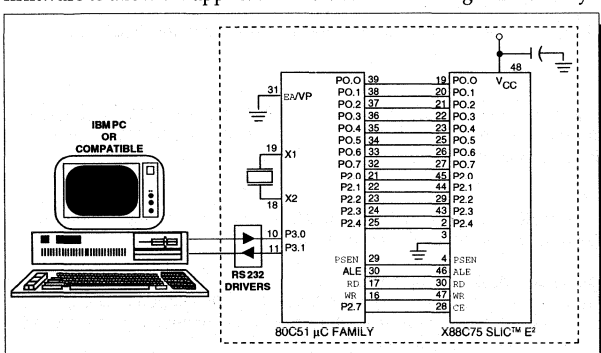
Data Sheet Enclosed



X88C75 Combines E²PROM, RAM, I/O Ports and Interface logic into an integrated, cost effective E² Micropheripheral.

X88C75 SLIC Provides Complete Solution to Firmware in Embedded Systems

The need for software upgradability is becoming increasingly important in embedded systems. The X88C75 SLIC device provides a complete hardware and software solution to this need. The device is delivered with a small library of routines loaded into the device. Upon initial power-up, the 80C31 will be initialized, and the SLIC firmware will download the applications software through the UART on the 80C31. Subsequent downloads can be performed by re-invoking the SLIC firmware to allow the applications software to be changed once the system is in the field. The software update can be performed over an RS232 interface, a network connection, a local serial bus, RF link or a fiber optics cable. The updates may be performed in a random fashion allowing a single byte, numerous bytes or the entire applications program to be updated.



Upon initial power-up, the 80C31 will be initialized, and the SLIC firmware will download the applications software through the UART on the 80C31.

Designing systems based on the X88C75 SLIC E² is simplified by making the SLIC firmware routines readily available to the application software. A PC based program called XSLIC was developed to handle the X88C75 SLIC to host system interface. The XSLIC facilitates reconfiguration of the communication link parameters and downloading application programs to the target system. Provisions have also been made to relocate the SLIC firmware in case of address conflicts with on chip resources of the 80C51 derivative employed by the system.

Data Sheet Enclosed

X88C75 SLIC® E² Microperipheral

Port Expander and E² Memory

FEATURES

- Highly Integrated Microcontroller Peripheral
  - —8K x 8 E² Memory
  - —2 x 8 General Purpose Bidirectional I/O Ports
  - —16 x 8 General Purpose Registers
  - —Integerated Interrupt Controller Module
  - —Internal Programmable Address Decoding
- Self Loading Integrated Code (SLIC)
  - —On-Chip BIOS and Boot Loader
  - —IBM/PC Based Interface Software(XSLIC)
- Concurrent Read During Write
  - —Dual Plane Architecture
- Isolates Read/Write Functions Between Planes
- Allows Continuous Execution Of Code From One Plane While Writing In The Other Plane
- Multiplexed Address/Data Bus
  - —Direct Interface to Popular 80C51 Family of Microcontrollers
- Software Data Protection
  - —Protect Entire Array During Power-up/-down
- Block Lock™ Data Protection
  - —Set Write Lockout in 1K Blocks
- Toggle Bit Polling
- High Performance CMOS
  - —Fast Access Time, 120ns
  - —Low Power
    - 60mA Active
    - 100µA Standby
- PDIP, PLCC, and TQFP Packaging Available

DESCRIPTION

The X88C75 SLIC is a highly integrated peripheral for the 80C51 family of microcontrollers. The device integrates 8K-bytes of 5V byte-alterable nonvolatile memory, two bidirectional 8-bit ports, 16 general purpose registers, programmable internal address decoding and a multiplexed address and data bus.

The 5V byte-alterable nonvolatile memory can be used as program storage, data storage, or a combination of both. The memory array is separated into two 4K-bytes sections which allows read accesses to one section while a write operation is taking place in the other section. The nonvolatile memory also features Software Data Protection to protect the contents during power transitions, and an advanced Block Protect register

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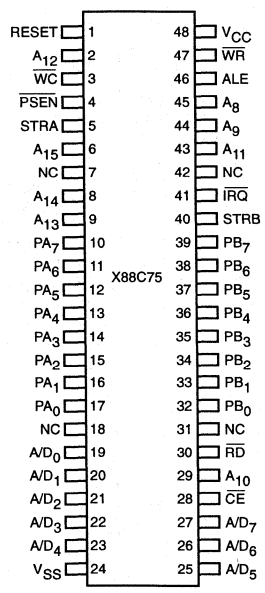
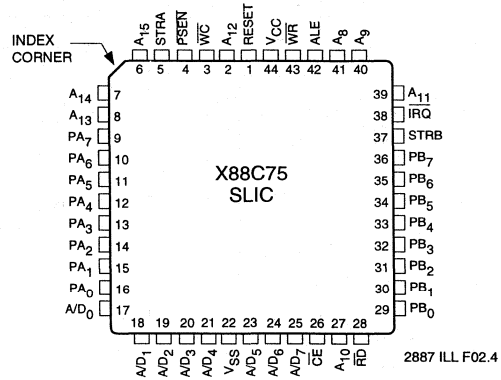
PIN CONFIGURATIONS

DIP



2887 ILL F01

PLCC
TQFP



2887 ILL F02.4

Concurrent Read During Write, Block Lock, and SLIC® E² are registered trademarks of Xicor, Inc.

which allows Individual blocks of the memory to be configured as read-only or read/write.

Each bidirectional port consists of 8 general purpose I/O lines and 1 data strobe line. The ports also feature a configurable interrupt request output.

Access to the X88C75 is accomplished through the multiplexed address/data bus of the 80C51 type controllers. An internal programmable address decoder maps the internal memory and register locations into the desired address space.

ARCHITECTURAL OVERVIEW

The X88C75 incorporates the interface circuitry normally needed to decode the control signals and demultiplex the address/data bus to provide a "seamless" interface.

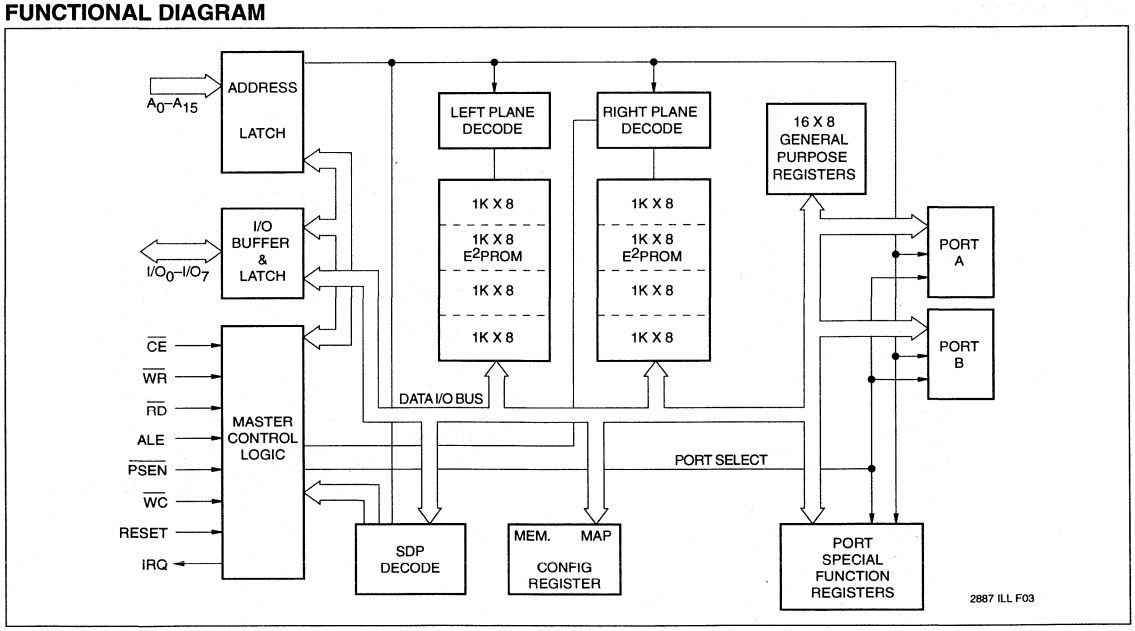
The control inputs on the X88C75 are configured such that it is possible to directly connect them to the proper interface signals of the 80C51 microcontroller. The reading of data from the chip is controlled either by the $\overline{PSEN}$ or the $\overline{RD}$ signal, which essentially maps the X88C75 into both the Program and the Data Memory address map.

Reading and writing of the nonvolatile memory array is analogous to RAM operation. During a write operation to either the nonvolatile memory or the control registers, ALE latches the address to be written into the X88C75. The rising edge of $\overline{WR}$ latches the data to be written.

The nonvolatile memory of the X88C75 is internally organized as two independent arrays of 4K-bytes with the A12 input selecting which of the two planes of memory is to be accessed. While the processor is executing code out of one plane, write operations can take place in the other plane; allowing the processor to continue execution of code out of the X88C75 during a byte or page write to the device. This feature is called Concurrent Read During Write.

The X88C75 also features an advanced implementation of the Software Data Protection scheme, called Block Lock Protect, which allows the nonvolatile memory array to be treated as 8 independent sections of 1K-bytes. Each of these sections can be independently enabled for write operations. This allows segmentation of the memory contents into writable and non-writable sections, thereby, allowing certain sections of the device to be secured so that updates can only occur in a controlled environment. (e.g. in an automotive application, only at

FUNCTIONAL DIAGRAM



an authorized service center). The Block Protect configuration is stored in a nonvolatile register, ensuring that the configuration data will be maintained after the device is powered-down.

The X88C75 write control input, serves as an external control over the completion of a previously initiated page load cycle.

The X88C75 also features the industry standard 5V E² memory characteristics such as byte or page mode write and Toggle Bit Polling.

Read

A HIGH to LOW transition on ALE latches the address; the data will be output on the AD pins after either $\overline{RD}$ or $\overline{PSEN}$ goes LOW (t_{RDLV}).

Write

A write is performed by latching the addresses on the falling edge of ALE. The $\overline{WR}$ is strobed LOW followed by valid data being presented on the AD_0–AD_7 pins. The data will be latched into the X88C75 on the rising edge of $\overline{WR}$.

Page Write Operation

The X88C75 supports page mode write operations. This allows the microcontroller to write from one to thirty-two bytes of data to the X88C75. Each individual write within a page write operation must conform to the byte write timing requirements. The falling edge of $\overline{WR}$ starts a timer delaying the internal programming cycle 100µs: therefore, each successive write operation must begin within 100µs of the last byte written. The waveform on page 4 illustrates the sequence and timing requirements.

PIN DESCRIPTIONS

PIN NAME	I/O	DESCRIPTION
RESET	I	RESET is used to initialize the internal static registers and has no effect on the E² memory operations. The default active level is HIGH, but it can be reconfigured in EEM register.
$\overline{PSEN}$	I	Content of E² memory can be read by lowering the $\overline{PSEN}$ and holding both $\overline{RD}$ and $\overline{WR}$ HIGH. The device then places on the data bus (AD_7–AD_0) the contents of E² memory at the latched address.
STRA, STRB	I/O	The STRA controls port A and STRB controls port B. When ports are configured as inputs, a valid transition on their strobe pins will latch into their port data register the data present at the port input pins. Writing to an output port data register generates a pulse of fixed duration on its corresponding strobe pin. The output data presented at the output pins stay valid until the next data is written to the output port data register.
PA_7–PA_0	I/O	The I/O lines of port A. The output driver can be configured as either CMOS or open-drain using the AWO bit in CR. The I/O direction bit (DIRA) in CR is used to select port A I/O mode.
PB_7–PB_0	I/O	The I/O lines of port B. The output driver can be configured as either CMOS or open-drain using the BWO bit in CR. The I/O direction bit (DIRB) in CR is used to select port B I/O mode.
A_{15}–A_8	I	Non-multiplexed high-order Address Bus inputs for the upper byte of the address.
AD_7–AD_0	I/O	Multiplexed low-order Address and Data Bus. The addresses are latched when ALE makes a HIGH to LOW transition.
$\overline{WR}$	I	During a byte/page write cycle $\overline{WR}$ is brought LOW while $\overline{RD}$ is held HIGH and the data is placed on the Data Bus. The rising edge of $\overline{WR}$ will latch the data into the device.
$\overline{RD}$	I	The $\overline{RD}$ input is active LOW and is used to read content of either the E² memory or the SFR at the latched address. Both $\overline{PSEN}$ and $\overline{WR}$ signals must be held HIGH during $\overline{RD}$ controlled read operation.
$\overline{IRQ}$	O	The $\overline{IRQ}$ is an open-drain output. It can be configured to signal latching of new data into any of the ports, and/or completion of the E² memory internal write cycle.
$\overline{WC}$	I	WC input has to be held LOW during a write cycle. It can be permanently tied HIGH in order to disable write to the E² memory. Taking $\overline{WC}$ HIGH prior to t_{BLC} (100µs, the time delay from the last write cycle to the start of internal programming cycle) will inhibit the write operation.
$\overline{CE}$	I	The device select ($\overline{CE}$) is an active LOW input. This signal has to be asserted prior to ALE HIGH to LOW transition in order to generate a valid internal device select signal. Holding this pin HIGH and ALE LOW will place the device in standby mode. The ports stay active at all times.
ALE	I	Address Latch Enable input is used to latch the addresses present on the address lines A_{15}–A_8 and AD_7–AD_0 into the device. The addresses are latched when ALE transitions from HIGH to LOW.

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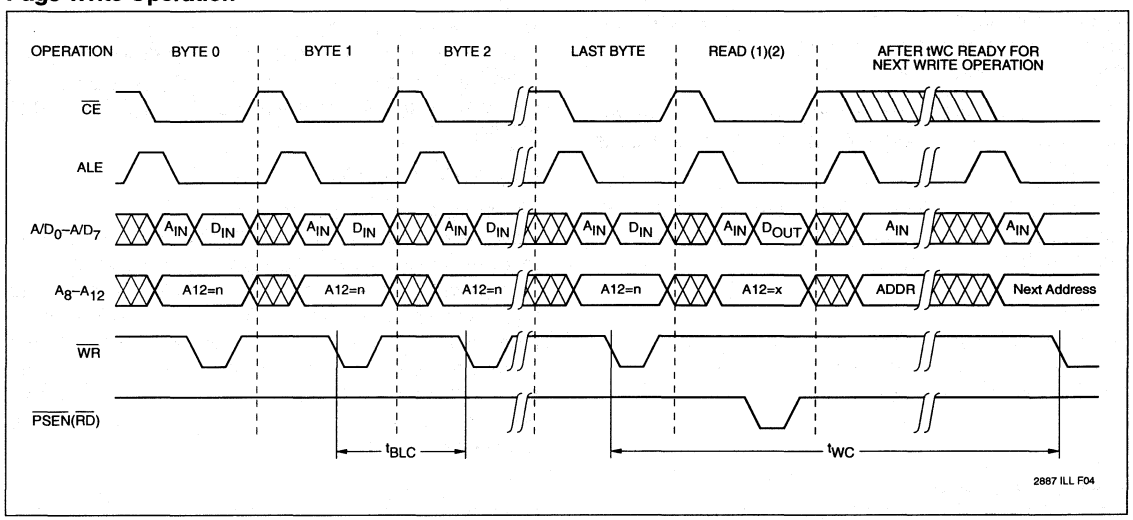
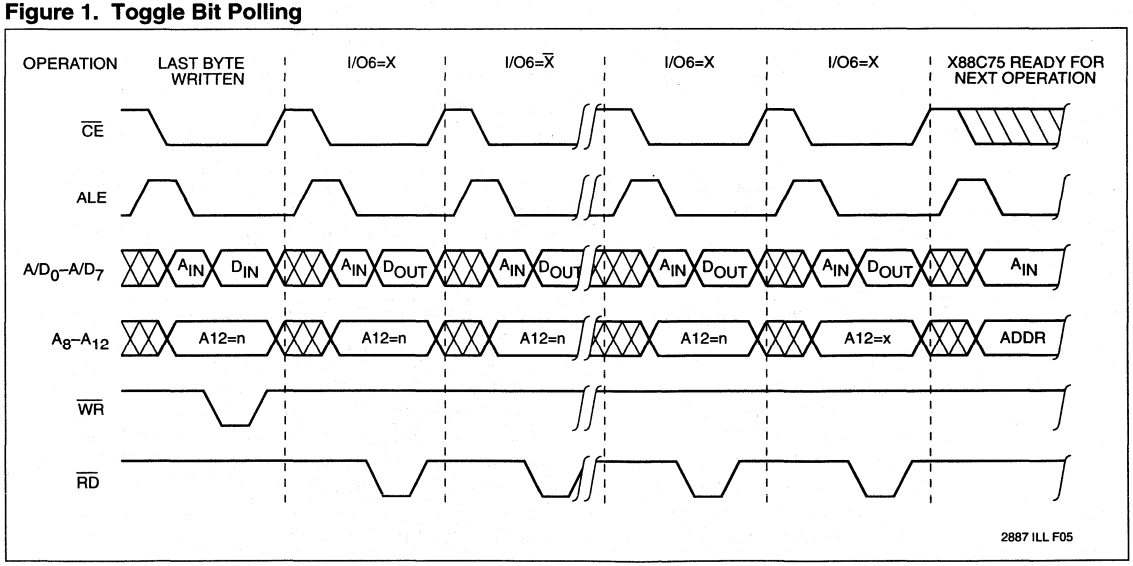
Page Write Operation



Toggle Bit Polling

Because the X88C75 typical write timing is less than the specified 5ms, Toggle Bit Polling has been provided to determine the early completion of a write cycle. During the internal programming cycle, I/O_6 will toggle from "1" to "0" and "0" to "1" on subsequent attempts to read from the memory plane that is being updated. When the internal cycle is complete, the toggling will cease and the device will be accessible for additional read or write operations. Due to the dual plane architecture, reads for polling must occur from the plane that was written; that is, the state of A_{12} during a write must match the state of A_{12} during polling.

Figure 1. Toggle Bit Polling



DATA PROTECTION

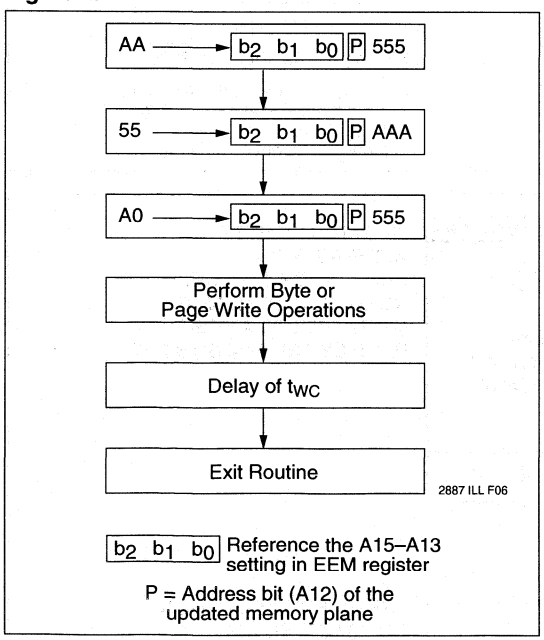
The X88C75 provides two levels of data protection through software control. There is a global software data protection feature similar to the industry standard for E²PROMs and a new Block Lock Protect write lockout protection providing a secondary level data security option.

Software Data Protection

Software Data Protection (SDP) can be employed to protect the entire array against inadvertent writes during power-up/power-down operations. The X88C75 is shipped from the factory with SDP enabled. With SDP enabled, inadvertent attempts to write to the X88C75 will be blocked.

The system can still write data, but only when the write operation (page or byte) is preceded by the three-byte command sequence. All write operations, both the command sequence and any data write operations must conform to the page write timing requirements.

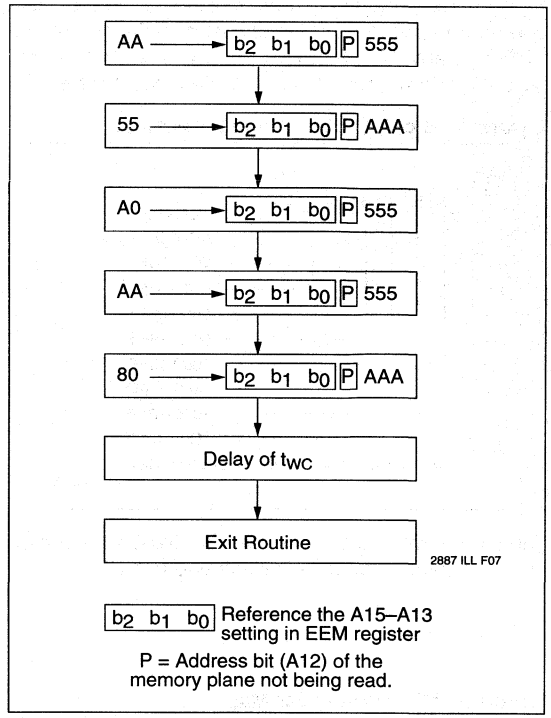
Figure 2.



Writing With SDP Enabled

The SDP mode is also enabled anytime one of the nonvolatile configuration registers are modified. These include writing to EE map, SFR map, and BPR.

Figure 3. Sequence to Deactivate Software Data Protection



Block Lock Protect Write Lockout

The X88C75 provides a second level of data security referred to as Block Lock Protect write lockout (or Block Protect). This is accessed through an extension of the SDP command sequence. Block Protect allows the user to lockout writes to 1K x 8 blocks of memory. Unlike SDP which prevents inadvertent writes, but still allows easy system access to writing the memory, Block Protect will lockout all attempts unless it is specifically disabled by issuing the deactivation sequence. This feature can be used to set a higher level of protection in a system where a portion of the memory is used to store the system kernel and protect it from the application programs residing in the other blocks.

Setting write lockout is accomplished by writing a five-byte command sequence opening access to the Block Protect Register (BPR). After the fifth byte is written, the user writes to the BPR, selecting which blocks to protect or unprotect. All write operations, both the command sequence and writing the data to the BPR, must conform to the page write timing requirements. It should be noted

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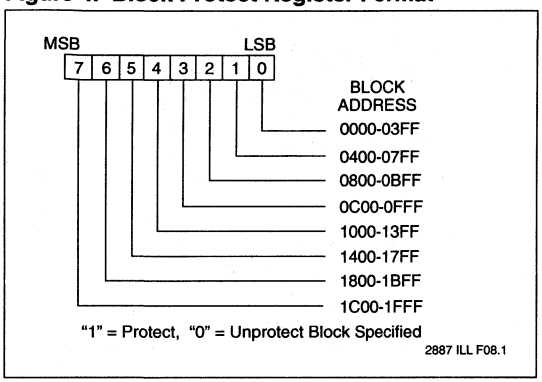
that accessing the BPR automatically sets the upper level SDP. If for some reason the user does not want SDP enabled, they may reset it using the normal reset command sequence. This will not affect the state of the BPR and any 1K x 8 blocks that were set to the write lockout state will remain in the write lockout state.

Figure 4. Block Protect Register Format



The BPR format and block map are illustrated above. The command sequence is illustrated to the right.

Figure 5. Setting BPR Command Sequence

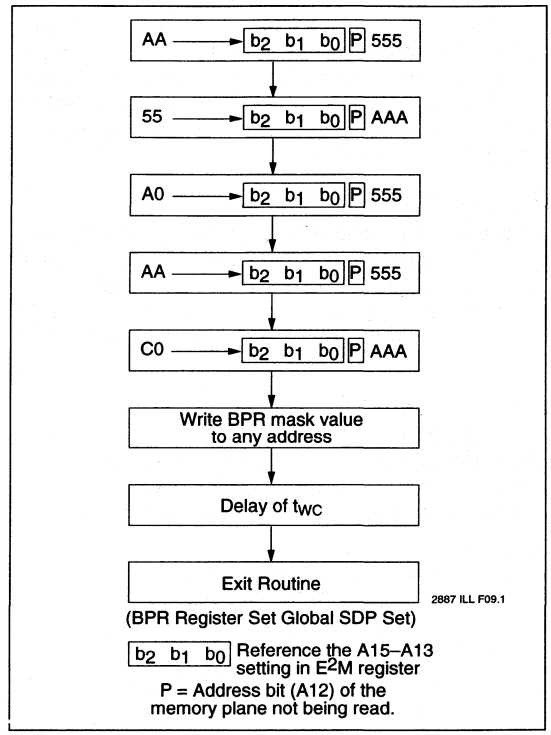


Figure 6. Microcontroller Map

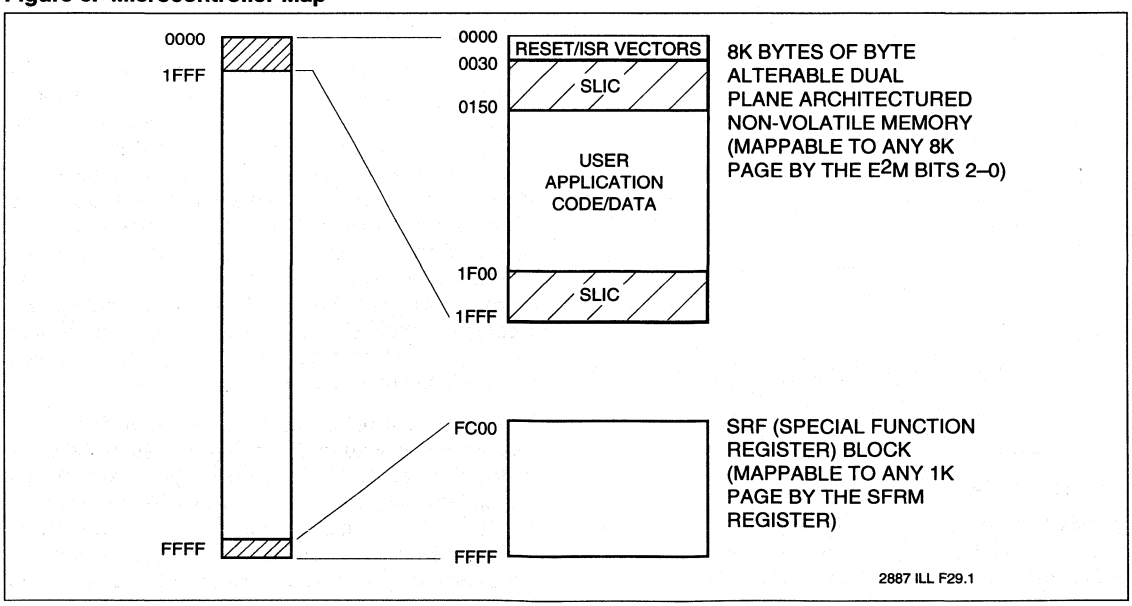
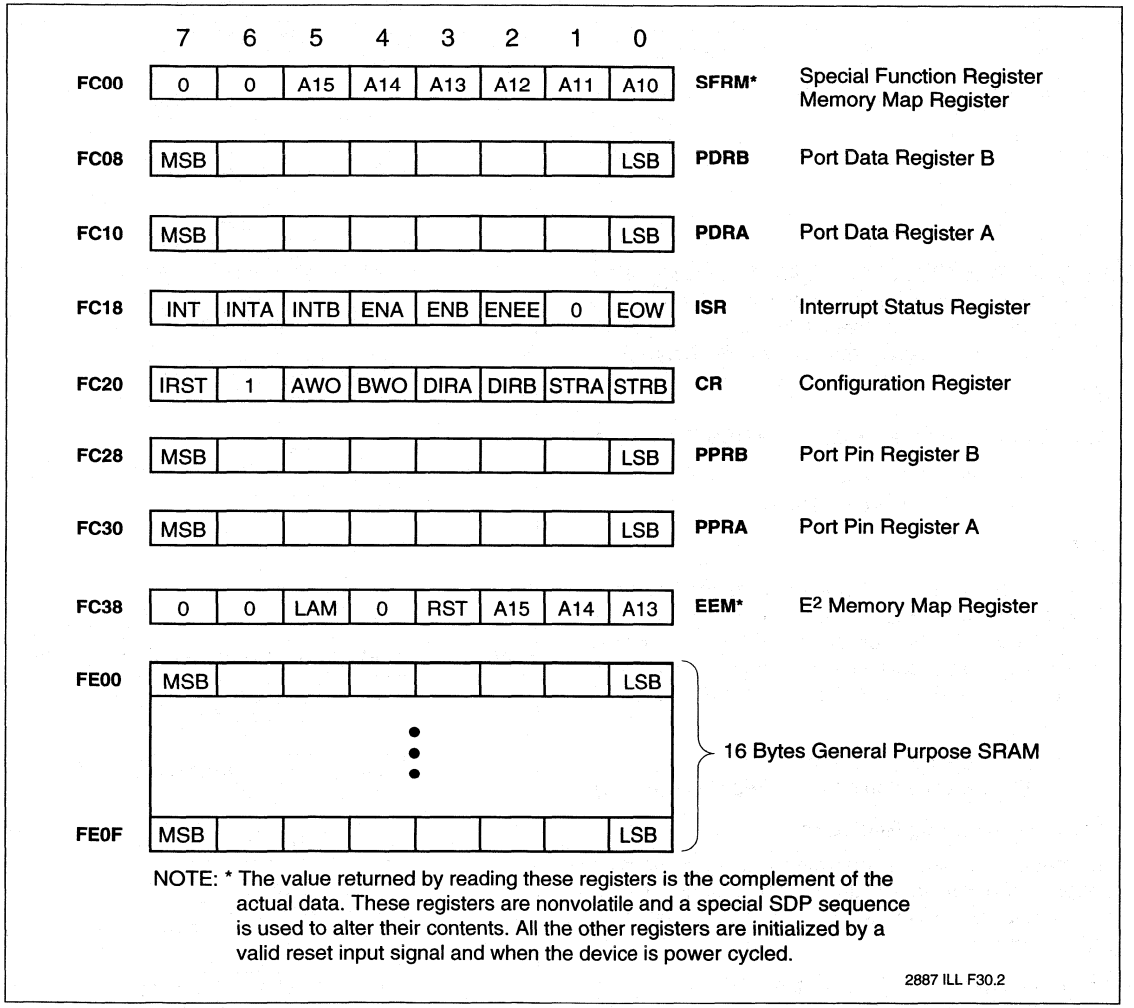


Figure 7. On-Chip Registers



NOTE: * The value returned by reading these registers is the complement of the actual data. These registers are nonvolatile and a special SDP sequence is used to alter their contents. All the other registers are initialized by a valid reset input signal and when the device is power cycled.

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Programmable Address Decoding

The X88C75 features an internal programmable address decoder which allows the nonvolatile memory array and the internal registers to be mapped in various locations of the 64K-byte memory map. The register set is mappable into a 1K-byte block, while the nonvolatile memory array is mappable into an 8K-byte block. The mapping is controlled by two nonvolatile configuration registers, the SFR Map Register and the E² Memory Map Register. Their bits are mapped as follows:

SFR Map Register (SFRM) **Default = 3F**

7	6	5	4	3	2	1	0
0	0	A15	A14	A13	A12	A11	A10

2887 ILL F10

A15-A10

The A15-A10 are upper address bits for the 1K-byte page where the SFR memory is mapped.

BITS 7:6

Setting these two bits to any combination other than "00" or "11" will interfere with device proper operation.

E² Memory Map Register (EEM) **Default = 08**

7	6	5	4	3	2	1	0
0	0	LAM	0	RST	A15	A14	A13

2887 ILL F11

A15-A13

Modifying these three bits changes the location of the program memory within the address map.The A15-A13 correspond to the upper three address bits of the 8K-byte page where program memory will be mapped.

RST

The RST bit controls the polarity of the RESET input pin.

"0" = RESET is Active LOW
"1" = RESET is Active HIGH

LAM

Port B can be configured as either a general purpose I/O port (normal I/O mode), or latched address mode (LAM). The LAM option programs port B to output the demultiplexed low order byte of the address latched into the X88C75 by ALE. The LAM bit selects between these two modes.

"0" = PORT B is I/O Port
"1" = Port B outputs low address byte (A7-A0)

Setting the Mapping Registers

The mapping registers are written using a modified version of the Software Data Protection sequence. All timings must adhere to the normal Software Data Protection sequence.

The complemented contents of the SFR map register and the E² memory map register can be read by the microcontroller at their corresponding SFR addresses. The physical memory location of these registers can be derived by adding the following offset to the SFR base address:

SFR Map Register	00H
E² Memory Map Register	38H

If the regions specified in the map registers overlap, only the SFR will be accessible.

Figure 8. Setting the SFR Map Register

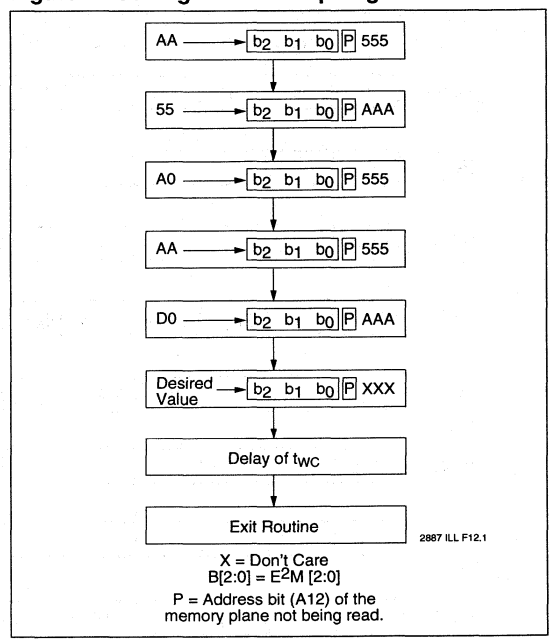
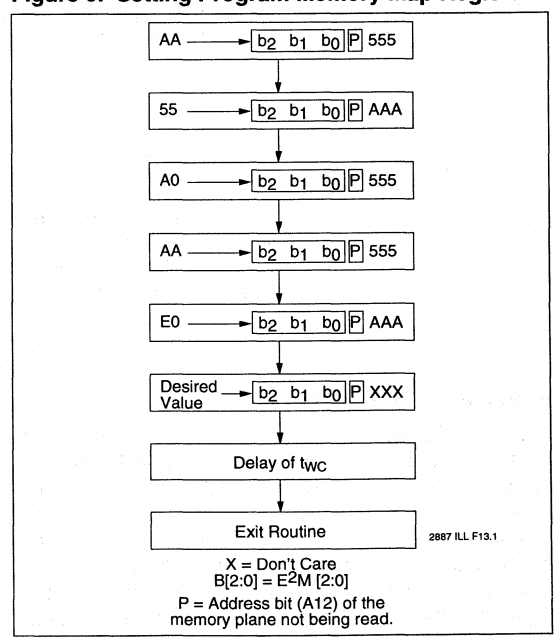


Figure 9. Setting Program Memory Map Register



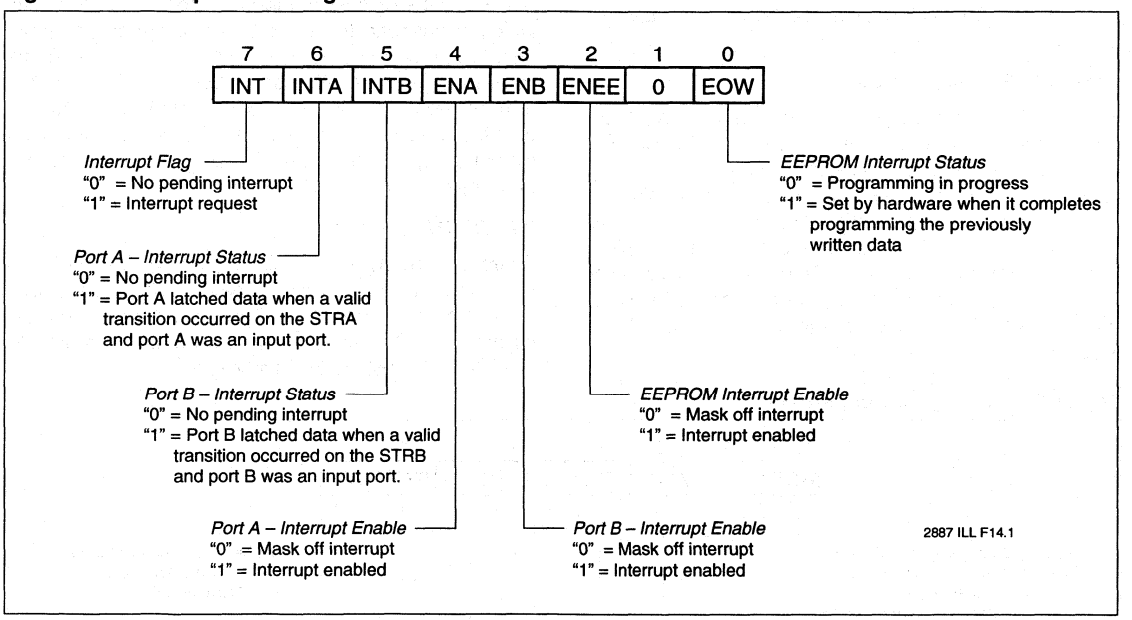
Interrupt Status Register (ISR)

The Interrupt Status Register is a volatile register used to configure the interrupt condition for the I/O ports as well as to determine the interrupt status of the ports. The X88C75 ports can generate an interrupt to the microcontroller upon the proper transition (as specified in the configuration register) on either STRA or STRB pins when the corresponding I/O port is configured as an input.

The INT flag is set when any of the input strobes are toggled provided that their corresponding interrupt enable bits (ENA, ENB) are set. The INT flag is cleared when latched data is read (PDR) or pending interrupt status flag (INTA, INTB) in ISR is forced to "0" by the interrupt service routine. Interrupt service routine should examine the interrupt status flags (INTA, INTB) and identify the source of pending interrupt.

The E^2 memory interrupt status flag (EOW) is another means to detect the early completion of a write cycle. When ENEE is enabled, the hardware will set the EOW flag, and interrupt the microcontroller at the end of an internal programming cycle. Toggle Bit Polling can be replaced by this hardware interrupt, which reduces the software overhead. The EOW flag should be cleared by software. The interrupt status register bits are mapped as follows.

Figure 10. Interrupt Status Register



Configuration Register (CR)

The Configuration Register is a volatile register used to configure the operation of the I/O ports. The configuration register allows the microcontroller to designate whether each of the two ports is an input or output, what type of output drive is to be used, and what is the polarity of the two strobe lines, STRA and STRB. The bit map of configuration register is shown below.

The IRST bit in the configuration register controls the method used to clear the port interrupt request flags(INTA, INTB). The interrupts are reset by either reading the interrupt source or writing to the Interrupt Status Register. The interrupt must be disabled prior to changing strobe polarity bits(STPA, SPTB), or port direction bits (DIRA, DIRB) in CR. Otherwise, any attempt to modify status of these bits may cause an interrupt to occur.

Port Data Registers (PDR)

The PDRA/PDRB are byte-wide latches which hold port data. When a port is configured as output, the outputs of its PDR latch are connected to the port pins. Writing to PDR generates a pulse on the port strobe pin and latches the data. If a port is configured as an input, the inputs of its PDR latch are connected to the port pins. External data is latched into PDR on the positive edge of its clock. The port strobe input and strobe polarity bit (STPA, STPB) are XORed to generate the PDR input clock.

Port Pin Registers (PPR)

The read-only Port Pin Registers are used for reading the current status of the external I/O port pins. Accessing the PPR causes the values on the port pins to be placed on the data bus.

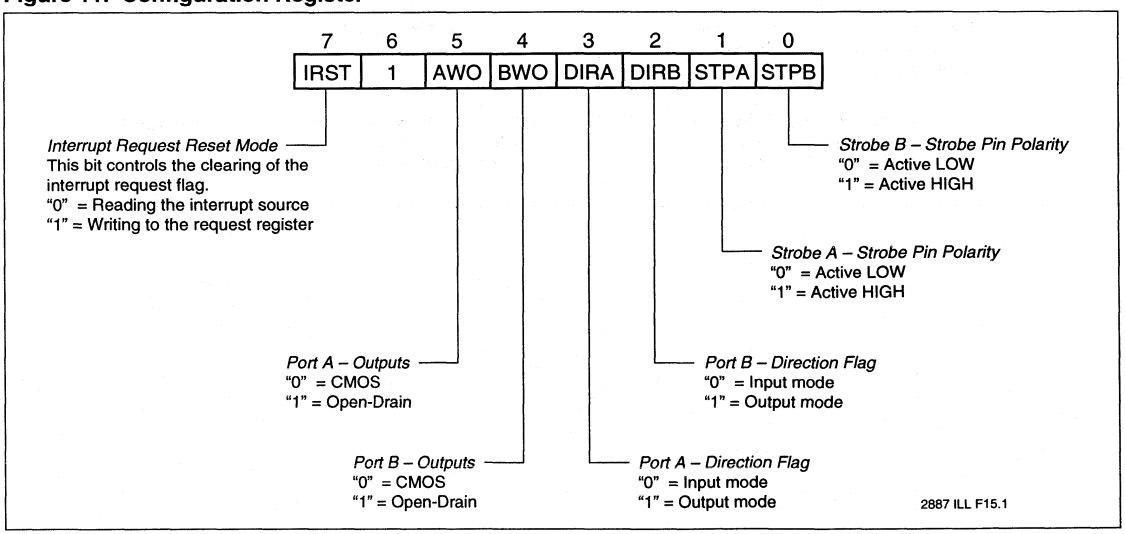
The port direction control bits in configuration register set the direction for the entire port and no control mechanism is provided to program the direction of individual pins. However, the ports have a flexible architecture which allows operating the I/O ports in bidirectional mode using the PPR read feature.

A port can be operated in input/output mode by configuring it as an open-drain output port. The port wire-OR bit (AWO, or BWO in CR) and its port data direction bit (DIRA, or DIRB in CR) should be set to "1". The PDR bits which correspond to the port pins assigned as inputs should be programmed to "1". For monitoring the status of the input pins, the PPR can be read. In this application the port strobe pin and the PDR latch are in output mode. In open-drain mode, there are weak internal pull-ups on the port pins, however external pull-ups must be used for proper switching of the I/O lines.

STATIC RAM BLOCK

There are 16 bytes of volatile static RAM registers mapped to the SFR region. They reside in the 200H-20FH area offset from the SFR base address. Accessing these registers has to be done through external RAM operations for both writes and reads.

Figure 11. Configuration Register



PRINCIPLES OF OPERATION

I/O Port Operation

The expansion ports are accessible to the software using their assigned memory mapped addresses. Each port occupies two addresses in the SFR plane, the Port Data Register and Port Pin Register. These registers and their location in the 1K-byte register memory space is shown on page 7.

The ports can be configured as either inputs or outputs, the DIRA and DIRB bits in the configuration register are used to select between the modes. The input signal on the strobe pin, when the corresponding port is configured as an input, is fed to the clock input of the port latch. These are transparent latches and the trailing edge of the strobe pulse is used to latch the data present on the input pins. The strobe signal polarity is configurable using the STPA and STPB bits in the configuration register.

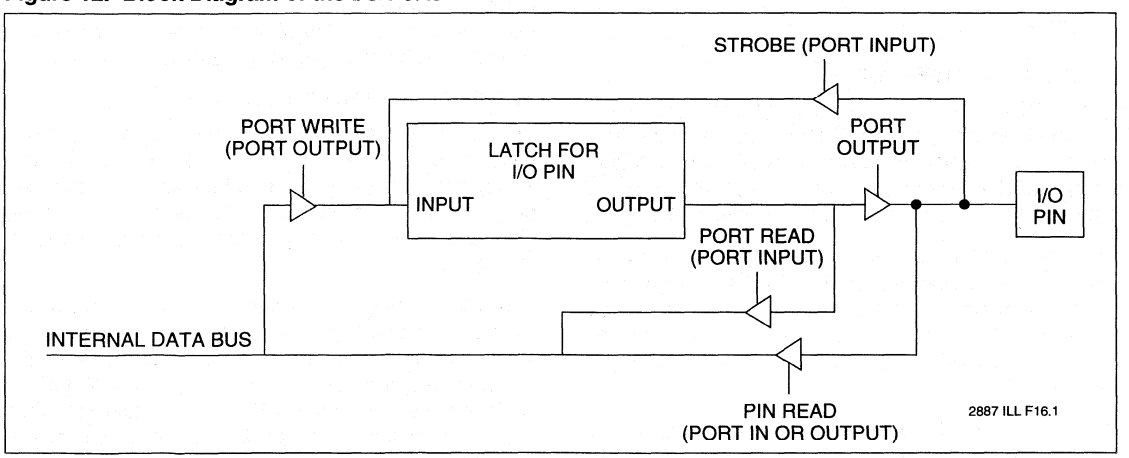
Writing to the port data register of an output port will generate a pulse of fixed duration on its strobe pin. The data also simultaneously arrives at the port output pins. The latched data stays there until new data is written to the port data register. The strobe pulse shape is controlled by the state of the STPA and STPB bits in the configuration register. A "1" forces the valid transition on the corresponding strobe pin as active HIGH ( ), and a "0" sets it to active LOW ( ).

When an external strobe signal is applied to an input port, the latching of input data is followed by the setting of the interrupt flags. The INTA and INTB interrupt flags are used by ports A and B respectively, and are set along with the INT interrupt flag at the end of strobe pulse input. External interrupt ($\overline{IRQ}$) is generated if the interrupt enable flags (ENA and ENB) are set by the software. The former enables the port A interrupt and the latter enables the port B interrupt.

The port output drivers can be either CMOS or open-drain. The wire-OR bits (AWO, BWO) in the configuration register are used to make the selection. When the bits are "0" the CMOS drivers are enabled. Setting these bits will enable the open-drain output drivers. Small pull-up resistors should be used on the pins of open-drain ports.

5

Figure 12. Block Diagram of the I/O Ports



IRQ

The $\overline{IRQ}$ pin is an active LOW open-drain output. In embedded systems applications, this signal is connected to the microcontroller interrupt input pin through either a direct connection or via an interrupt controller.

Table 1 depicts the three sources of interrupts and their associated flags. Under normal conditions, the INT and port interrupt flags are set, if the port which is configured as an input has its strobe line toggled. If the port interrupt enable flag is set, or gets set while the INT flag is set, then the $\overline{IRQ}$ signal is asserted. The $\overline{IRQ}$ stays valid as long as the interrupt flags are not cleared by the software or the hardware.

Another interrupt source is the End Of Write flag (EOW) which is set by the hardware at the end of every internal programming cycle. The interrupt from this source is controlled by the ENEE bit in ISR. If ENEE is enabled, then EOW can generate an external interrupt. The interrupt is cleared by setting EOW to "0".

Table 1. X88C75 Interrupt Sources

Interrupt Source	Interrupt Enable	Status Flag	INT Flag
PORT A	ENA	INTA	"1"
PORT B	ENB	INTB	"1"
EOW	ENEE	EOW	—

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PORTS A & B INTERRUPTS

The X88C75 features two 8-bit I/O ports which are equipped with a configurable interrupt module. The interrupts are used to signal the reception of new data at an input port data latch. When a port is configured as an output, it can no longer generate any interrupts.

The input port interrupt mechanism is controlled by the external strobe pins (STRA, STRB). Detecting a valid transition on the pin will set the interrupt flags and latch in the input data. The external interrupts from the ports can be masked off using the interrupt enable bits (ENA, ENB) in ISR.

Once an external interrupt is asserted, clearing the interrupt flags will cause the $\overline{IRQ}$ signal to return to its idle state. There are two ways of resetting the interrupt flags. The selection is made using the IRST bit in the configuration register. If IRST is set, then the interrupt flags are cleared by writing "0" to the bit positions corresponding to the interrupt flags (INTA, INTB) in ISR. When the IRST is cleared, reading the PDR automatically clears the interrupt flags.

SOFTWARE CONTROLLED PORT OPERATIONS

The individual clock signals, that control the PDR input latches and load the external data present on the port pins, are generated by XORing the strobe polarity bit and the strobe input of the port. The strobe polarity bits (STPA, STPB) in CR can be used to program the active edge of the strobe inputs. However, if the external strobe input is permanently tied to V_{SS} or V_{CC}, then the strobe polarity bit controls the PDR input latch clock signal.

When a port strobe and its polarity bit have identical logic levels, the corresponding PDR latch is active and any change in the port inputs will show up at the PDR latch outputs. Holding the strobe input at current levels and changing the strobe polarity bit value will generate a positive transition on the PDR clock signal, causing the latch outputs to reflect the previous logic state of the port pins. The clock transition sets the interrupt flags, and if the interrupts have been enabled, then an external interrupt signal will be asserted.

This feature allows the port input operation by permanently tying the STRx inputs to V_{CC} or V_{SS}, and using the STPx bits in CR to control PDR latches. Another advantage of this feature are software generated interrupts. Since the clocking of the PDR latch causes the corresponding port INTx flags to be set, by enabling the interrupts the microcontroller is forced to execute the ISR responsible to service the newly latched data.

END OF WRITE (EOW) INTERRUPT

The internal programming cycle requires several milliseconds for either a single byte write or a page write. The updated memory plane is inaccessible while the programming is in progress. However, the opposite plane is still available for program fetch and data read operations.

The X88C75 has two means of signaling end of an internal programming cycle. In the Toggle Bit Polling technique, the last written byte is successively read. Bit 6 of read data toggles while the programming cycle is still in progress. The software has to continually monitor device responses and determine if it can again access the plane.

In the other method, at the end of an internal programming cycle, the hardware sets the EOW flag. The software can either poll this flag or enable the interrupts by setting the ENEE bit in ISR. Effective use of EOW is made by clearing it prior to initiating a write operation. If

the interrupt is enabled, an external interrupt will be asserted at the completion of the internal write cycle. The interrupt is cleared by setting EOW to "0".

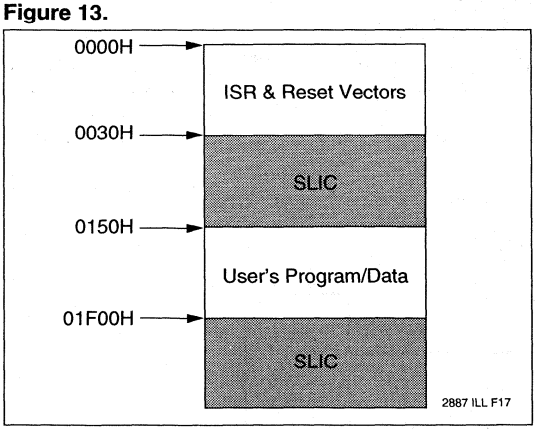
USING A PORT IN BIDIRECTIONAL MODE

In order to use a port in bidirectional mode, it has to be configured as an open drain output port. Small pull-up resistors are required on all port output pins. Bit positions in the Port Data Register corresponding to port inputs should contain "1". The inputs are then read by accessing PPR. Data is not latched into the device, so the inputs must stay valid throughout the read cycle. The port strobe pin is configured as an output and cannot be used as port latch clock input.

SLIC FUNCTIONS (80C51 Specific SLIC)

The resident SLIC E² has designated memory spaces allocated for its use. The user's application code should avoid using these areas as part of its code segment, otherwise it will overwrite the SLIC E². Version 3.0 of the X88C75 SLIC E² occupies 256 bytes in the upper memory bank, starting at address 1F00H, and 288 bytes in the lower bank's address range 30H-14FH. Prior to downloading code, assemble and link the source files using the above address information. Use memory space taken up by the SLIC E² as a run-time data storage, if there is no further need to modify the X88C75 SLIC E² content.

Figure 13.



The current version of the SLIC E² configures the 80C51 serial port to the variable baud rate mode. It sets a timer 1 reload value for a system clock rate of 11.059MHz. For other clock rates end user must recalculate timer 1 reload value for 9600 baud rate and write it into the X88C75 location 00E8H. The XSLIC software, a PC based communication driver, automates changing of the default parameters when using its SETUP option menu. The boot-firmware (SLIC) residing on the X88C75 contains a lookup table which can be accessed from the subroutine (EXEC_SUB), located at location 0126H. Two bytes are used per table entry. The EXEC_SUB input requirements are as follows:

R0 = Contains a Function Number from the following Function Table.

The table entry at location (014E-014FH) is reserved for user's application code. This function will be executed on power-up if the SLIC receives any characters other than those for the RESET (ASCII 'R'), or ID (ASCII 'X') commands. The table entry can be changed to point to other code responsible for power-up initialization. This is preferred method than changing the reset vector, since the SLIC code can still be invoked upon power-up.

Other functions available through the EXEC_SUB calls is as follows:

FUNCTION NO.	DESCRIPTION
0 - PROC_PROG	Download and program a page
1 - PROC_BPR	Program BPR
2 - RESET	Start execution from location 0000H
3 - PROC_VER	Download and verify a page
4 - DUMMY	Command not recognized
5 - INIT_UART	Initialize UART parameters to default
6 - PROG_PG	Program a page
7 - SEND_CHAR	Send a character to the UART
8 - GET_CHAR	Read a character from the RAM receive buffer (40H-5FH)
9 - SDP_HI_PLANE	Generate SDP off sequence for upper plane
10- SDP_LO_PLANE	Generate SDP off sequence for lower plane
11- USER_CODE	Execute user's code

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For detailed information about the listed functions, including their input requirements, refer to the SLIC software specification document.

APPLICATION EXAMPLES

This section gives examples of most widely used embedded systems architectures using the X88C75 and 80C51 microcontroller. However, keep in mind that other microcontrollers are also supported by the X88C75 and/or other SLIC devices that Xicor manufactures.

Example 1

In this system, the X88C75 is the only parallel device residing on the multiplexed address and data bus. There may be other peripherals on the system board which are controlled by the ports on the X88C75. This configuration maps the EEM to a program/data memory address in the range of 0000-1FFFH. The SFRM can be mapped to any of the 64 x 1K pages within the data memory space.

Example 2

Applications requiring more than 8K bytes of program memory space can be implemented using the basic system architecture depicted in example 1 along with an additional memory device such as the X28C256. Since this device requires non-multiplexed address/data buses, the X88C75 LAM feature is used to output the low order address byte. The SFRM can be mapped to any 64x1K page, but the X28C256 should be mapped to the upper program memory address space and out of the E²M address range (0000-1FFFH.) This technique may also be used for other external byte wide memories such as SRAMs or EPROMs.

Figure 14. Example 1

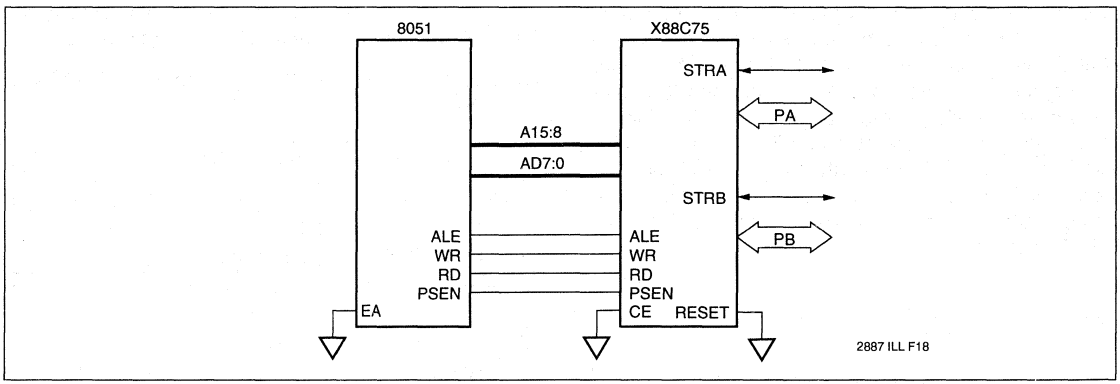
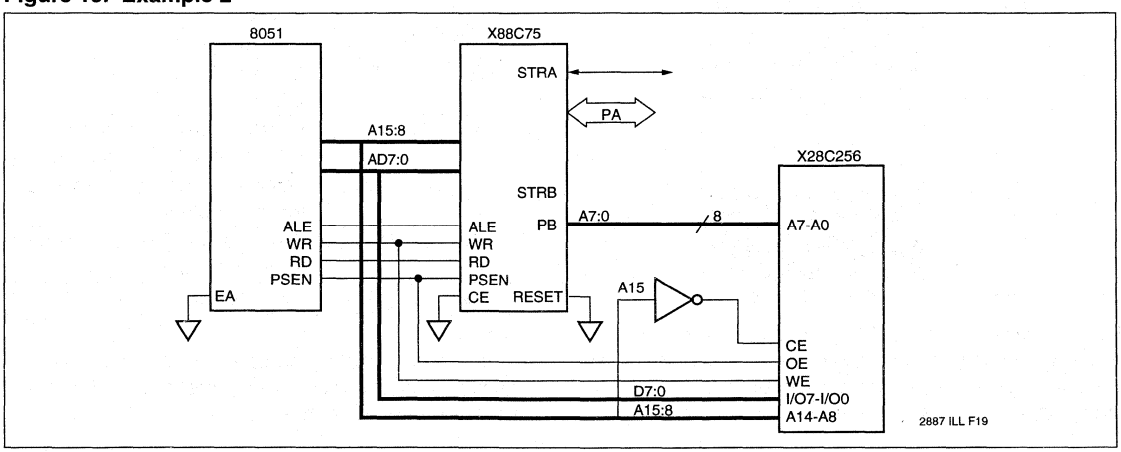


Figure 15. Example 2



Example 3

If an application requires larger program memory storage and both extra ports, then example 2 does not meet this requirement. Since the LAM feature uses port B to output the non-multiplexed address, then port B cannot be also used as general purpose I/O. The solution to this problem is to use X68C64, which interfaces to a multiplexed bus and takes an active HIGH CE input. Example 3 maps the X68C64 to the top 8K program memory space in the range of 8000-FFFFH. This approach provides a total of 16K-bytes of program memory. Using the same approach, two additional X68C64 device can be added and A13-A14 can be used as their CE inputs, for the total of 32K-bytes of program memory. Ports A and B are still available to handle any general purpose I/O functions.

Example 4

For those applications using extensive I/O, up to 128 I/O pins are obtained by placing 8 of the X88C75 devices on the same bus. This approach gives a total of 64K-bytes of program memory space, and 128 I/O pins. Note that the SFRM can overlap the E²M address space, however, only the SFR resources are accessible and the associated E² memory location are not available.

Figure 16. Example 3

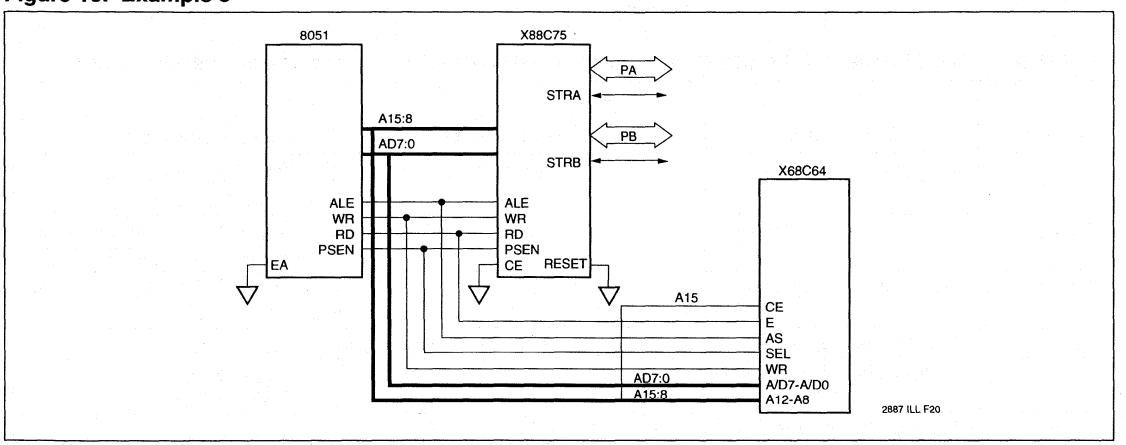
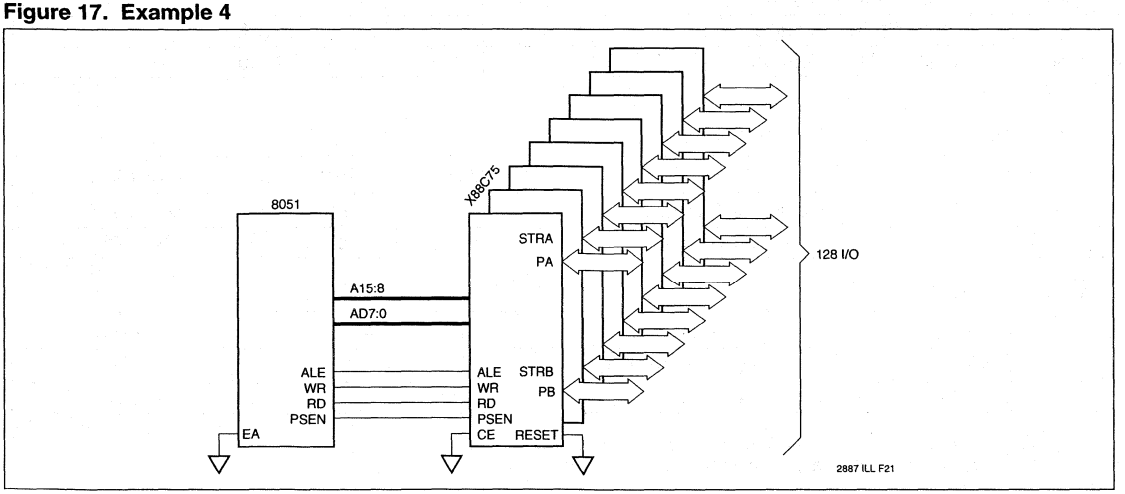


Figure 17. Example 4



ABSOLUTE MAXIMUM RATINGS*

Temperature under Bias ..... −65°C to +135°C
Storage Temperature ..... −65°C to +150°C
Voltage on any Pin with
Respect to V_{SS} ..... −1V to +7V
D.C. Output Current ..... 5 mA
Lead Temperature
(Soldering, 10 seconds) ..... 300°C

***COMMENT**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	+70°C
Industrial	−40°C	+85°C
Military	−55°C	+125°C

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Supply Voltage	Limits
X88C75	5V ±10%

2887 PGM T05.1

D.C. OPERATING CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
I_{CC}	V_{CC} Current (Active)		60	mA	$\overline{CE}$ = $\overline{RD}$ = V_{IL}, All I/O's = Open,Other Inputs = V_{CC}
$I_{SB1(CMOS)}$	V_{CC} Current (Standby)		100	µA	$\overline{CE}$ = V_{IH}, All I/O's = Open, Other Inputs = V_{CC} − 0.3V, ALE = V_{IL}
$I_{SB2(TTL)}$	V_{CC} Current (Standby)		2	mA	$\overline{CE}$ = V_{IH}, All I/O's = Open, Other Inputs = V_{IH}, ALE = V_{IL}
I_{LI}	Input Leakage Current		10	µA	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output Leakage Current		10	µA	V_{OUT} = V_{SS} to V_{CC}, $\overline{RD}$ = $\overline{PSEN}$ = V_{IH}
V_{IL}(3)	Input LOW Voltage	−1	0.8	V	
V_{IH}(3)	Input HIGH Voltage	2	V_{CC} + 0.5	V	
V_{OL}	Output LOW Voltage		0.4	V	I_{OL} = 2.1mA
V_{OH}	Output HIGH Voltage	2.4		V	I_{OH} = −400µA

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CAPACITANCE T_A = +25°C, f = 1MHz, V_{CC} = 5V

Symbol	Test	Max.	Units	Conditions
$C_{I/O}$(4)	Input/Output Capacitance	10	pF	$V_{I/O}$ = 0V
C_{IN}(4)	Input Capacitance	6	pF	V_{IN} = 0V

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POWER-UP TIMING

Symbol	Parameter	Max.	Units
t_{PUR}(4)	Power-Up to Read	1	ms
t_{PUW}(4)	Power-Up to Write	5	ms

2887 PGM T08

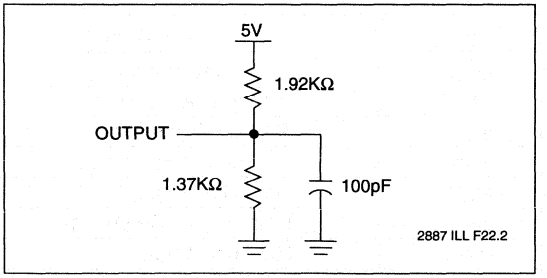
Notes: (3) V_{IL} min. and V_{IH} max. are for reference only and are not tested.
(4) This parameter is periodically sampled and not 100% tested.

A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3V
Input Rise and Fall Times	10ns
Input and Output Timing Levels	1.5V

2887 PGM T09.1

EQUIVALENT A.C. TEST CIRCUIT



A.C. CHARACTERISTICS (Over the recommended operating conditions unless otherwise specified.)

$\overline{PSEN}$ Controlled Read Cycle

Symbol	Parameter	Min.	Max.	Units
t_{LHLL}	ALE Pulse Width	80		ns
t_{AVLL}	Address Setup Time	20		ns
t_{LLAX}	Address Hold Time	30		ns
t_{PLDV}	$\overline{PSEN}$ Read Access Time		120	ns
t_{PHDX}	Data Hold Time	0		ns
t_{ELLL}	Chip Enable Setup Time	7		ns
PW_{PL}	$\overline{PSEN}$ Pulse Width	150		ns
t_{PS}	$\overline{PSEN}$ Setup Time	30		ns
t_{PH}	$\overline{PSEN}$ Hold Time	20		ns
t_{PHDZ} (5)	$\overline{PSEN}$ Disable to Output in High Z		50	ns
t_{PLDX} (5)	$\overline{PSEN}$ to Output in Low Z	10		ns

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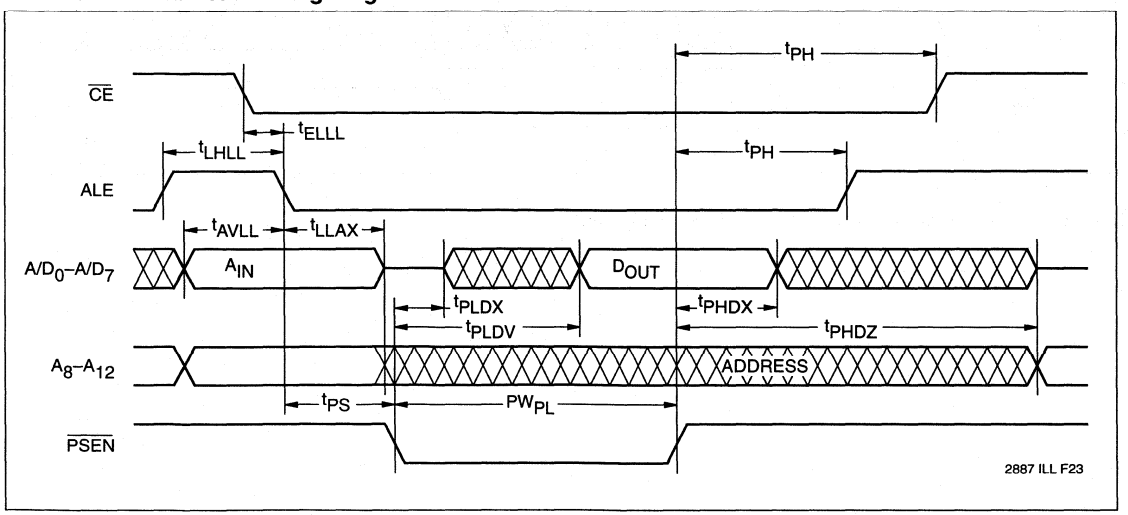
$\overline{PSEN}$ Controlled Read Timing Diagram



Note: (5) This parameter is periodically sampled and not 100% tested.

$\overline{RD}$ Controlled Read Cycle

Symbol	Parameter	Min.	Max.	Units
t_{LHLL}	ALE Pulse Width	80		ns
t_{AVLL}	Address Setup Time	20		ns
t_{LLAX}	Address Hold Time	30		ns
t_{RLDV}	$\overline{RD}$ Read Access Time		120	ns
t_{RHDX}	Data Hold Time	0		ns
t_{ELLL}	Chip Enable Setup Time	7		ns
PW_{RL}	$\overline{RD}$ Pulse Width	150		ns
t_{RDS}	$\overline{RD}$ Setup Time	30		ns
t_{RDH}	$\overline{RD}$ Hold Time	20		ns
t_{RHDZ} (6)	$\overline{RD}$ Disable to Output in High Z		50	ns
t_{RLDX} (6)	$\overline{RD}$ to Output in Low Z	0		ns

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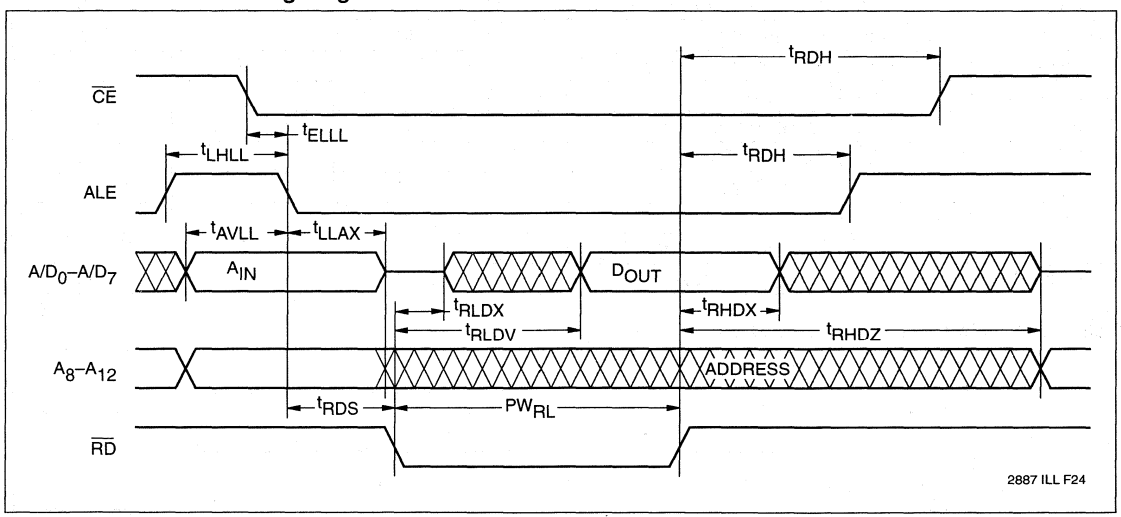
$\overline{RD}$ Controlled Read Timing Diagram



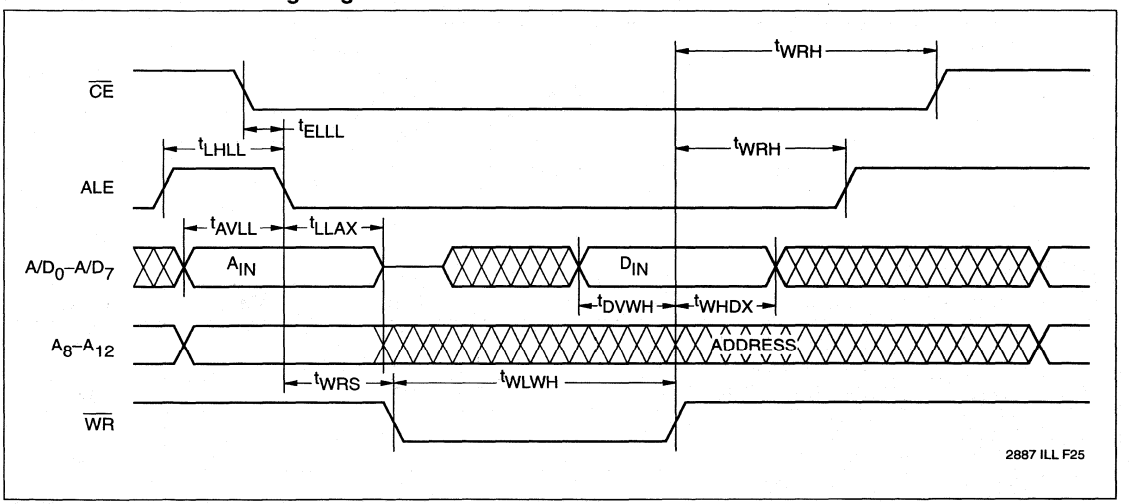
Note: (6) This parameter is periodically sampled and not 100% tested.

$\overline{WR}$ Controlled Write Cycle

Symbol	Parameter	Min.	Max.	Units
t_{LHLL}	ALE Pulse Width	80		ns
t_{AVLL}	Address Setup Time	20		ns
t_{LLAX}	Address Hold Time	30		ns
t_{DVWH}	Data Setup Time	50		ns
t_{WHDX}	Data Hold Time	30		ns
t_{ELLL}	Chip Enable Setup Time	7		ns
t_{WLWH}	$\overline{WR}$ Pulse Width	120		ns
t_{WRS}	$\overline{WR}$ Setup Time	30		ns
t_{WRH}	$\overline{WR}$ Hold Time	20		ns
t_{BLC}	Byte Load Time (Page Write)	0.5	100	µs
t_{WC} (7)	Write Cycle Time		5	ms

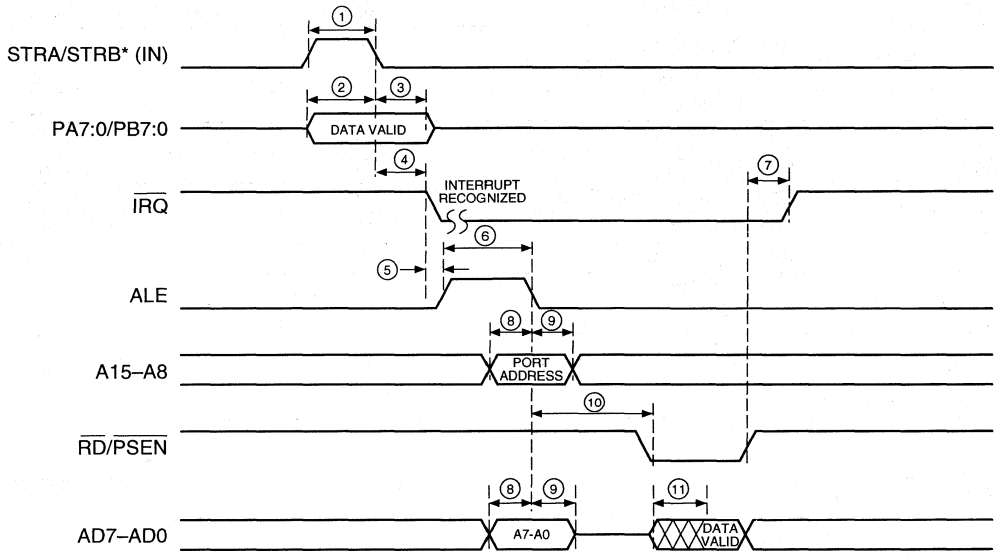
2887 PGM T12

$\overline{WR}$ Controlled Write Timing Diagram



Note: (7) t_{WC} is the minimum cycle time to be allowed from the system perspective unless polling techniques are used. It is the maximum time the device requires to automatically complete the internal write operation.

Port Read Diagram



NOTE: *Figure shows active HIGH strobes.

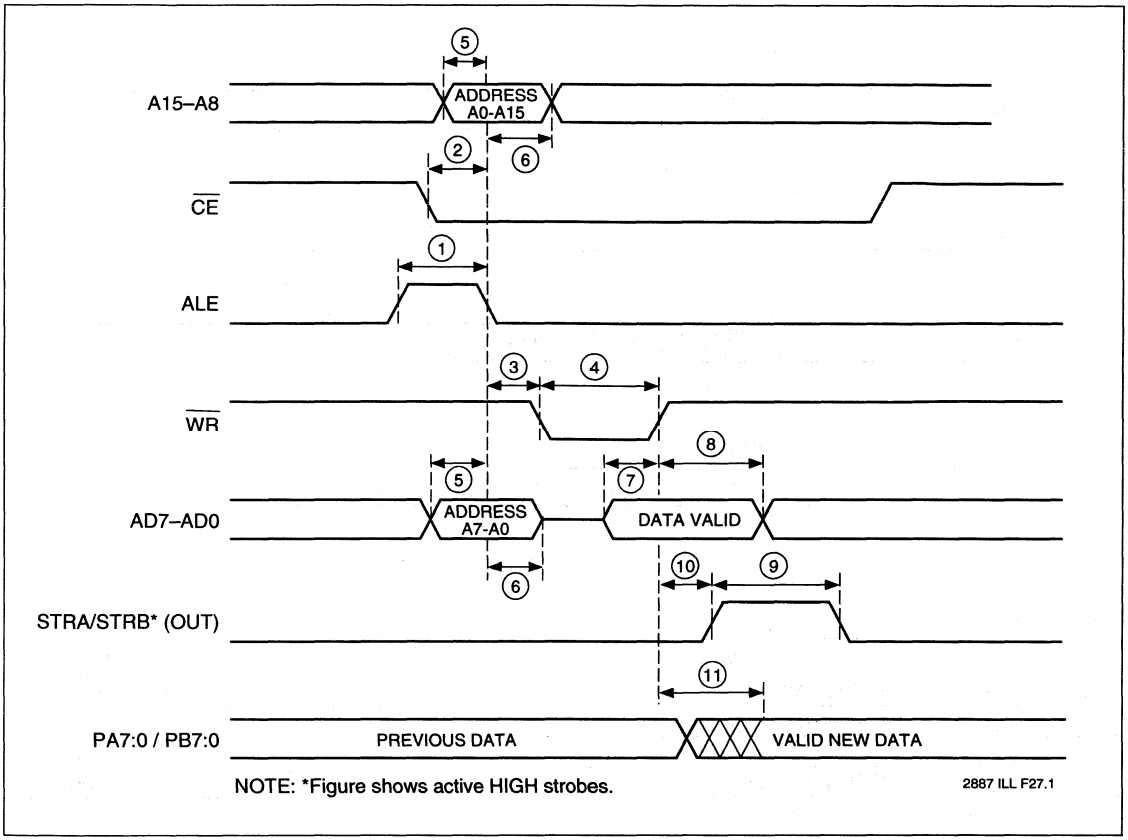
2887 ILL F26.1

PORT READ TIMING

No.	Symbol	Parameter	Min.	Max.	Units
1	t_{SVSX}	Strobe Pulse Width	80		ns
2	t_{DVSV}	Data Port Setup	20		ns
3	t_{SVDX}	Data Port Hold Time	30		ns
4	t_{SVIV}	Interrupt Request to Strobe		50	ns
5	t_{IAD}	$\overline{IRQ}$ to ALE	0		ns
6	t_{LHLL}	ALE Pulse Width	80		ns
7	t_{RXIX}	$\overline{RD}$ to $\overline{IRQ}$	30		ns
8	t_{AVLL}	Address setup time	20		ns
9	t_{LLAX}	Address hold time	30		ns
10	t_{LLWL}	ALE to $\overline{RD}$ LOW	30		ns
11	t_{RLDV}	$\overline{RD}$ Access Time		120	ns

2887 PGM T13.2

Port Write Diagram



NOTE: *Figure shows active HIGH strobes.

2887 ILL F27.1

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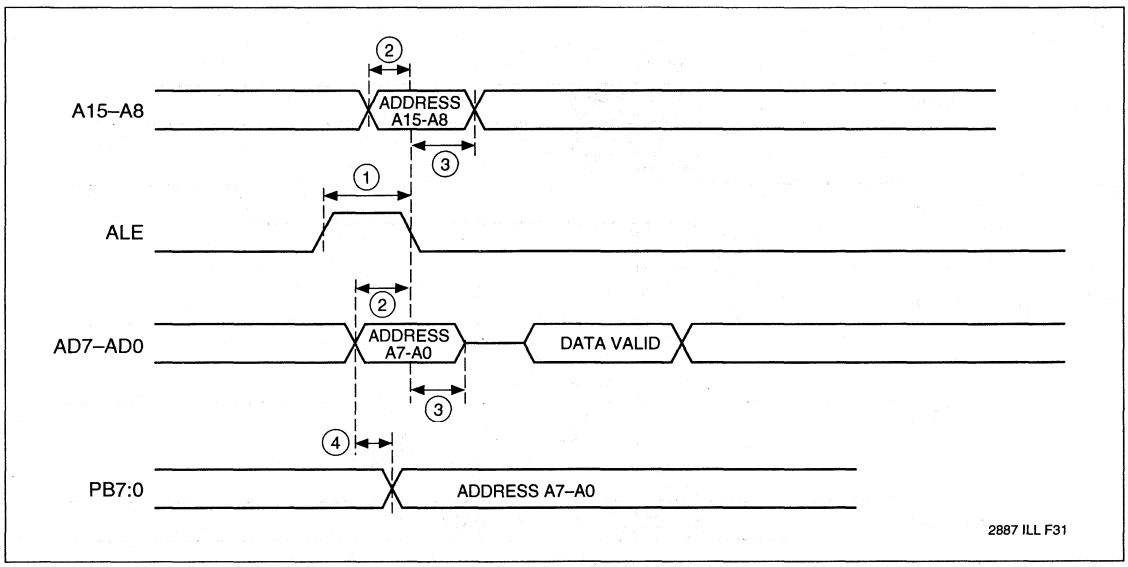
PORT WRITE TIMING

No.	Symbol	Parameter	Min.	Max.	Units
1	t_{LHLL}	ALE Pulse Width	80		ns
2	t_{WCS}	Write Chip Select Setup Time	20		ns
3	t_{LLWL}	ALE to $\overline{WR}$	10		ns
4	t_{WLWH}	$\overline{WR}$ Pulse Width	120		ns
5	t_{AVLL}	Write Address Setup Time	20		ns
6	t_{LLAX}	Write Address Hold Time	30		ns
7	t_{DVWH}	Data Setup Time	50		ns
8	t_{WHDX}	Data Hold Time	10		ns
9	t_{SVSX}	Strobe Pulse Width	120		ns
10	t_{QVSV}	Strobe Access Time		40	ns
11	t_{POS}	Port Output Setup Time		40	ns

2887 PGM T14.1

LAM (Latch Address Mode) Diagram



LAM TIMING

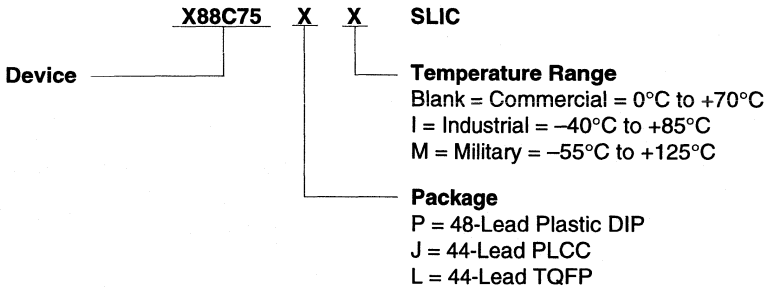
No.	Symbol	Parameter	Min.	Max.	Units
1	t_{LHLL}	ALE Pulse Width	80		ns
2	t_{AVLL}	Address Setup Time	20		ns
3	t_{LLAX}	Address Hold Time	30		ns
4	t_{POS}	Port Output Setup Time		20	ns

2887 PGM T15

SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

ORDERING INFORMATION



5

NOTES

APPLICATION NOTE AND DEVELOPMENT SYSTEM
A V A I L A B L E
AN65 • LAPKIT DEMO

LapKit™ X88C75 SLIC® E² Microperipheral

Port Expander and E² Memory

FEATURES

- **Highly Integrated Microcontroller Peripheral**
  - **—8K x 8 E² Memory**
  - **—2 x 8 General Purpose Bidirectional I/O Ports**
  - **—16 x 8 General Purpose Registers**
  - **—Integerated Interrupt Controller Module**
  - **—Internal Programmable Address Decoding**
- **Concurrent Read During Write**
  - **—Dual Plane Architecture**
- **Isolates Read/Write Functions Between Planes**
- **Allows Continuous Execution Of Code From One Plane While Writing In The Other Plane**
- **Multiplexed Address/Data Bus**
  - **—Direct Interface to Popular 80C51 Family of Microcontrollers**
- **Software Data Protection**
  - **—Protect Entire Array During Power-up/-down**
- **Block Lock™ Data Protection**
  - **—Set Write Lockout in 1K Blocks**
- **Toggle Bit Polling**
- **High Performance CMOS**
  - **—Fast Access Time, 120 ns**
  - **—Low Power**
    - **60mA Active**
    - **100µA Standby**
- **PDIP, PLCC, and TQFP Packaging Available**

DESCRIPTION

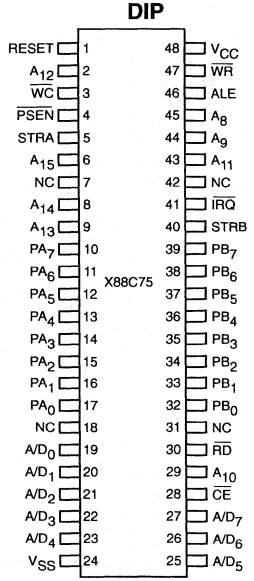
The X88C75 SLIC is a highly integrated peripheral for the 80C51 family of microcontrollers. The device integrates 8K-bytes of 5V byte-alterable nonvolatile memory, two bidirectional 8-bit ports, 16 general purpose registers, programmable internal address decoding and a multiplexed address and data bus.

The 5V byte-alterable nonvolatile memory can be used as program storage, data storage, or a combination of both. The memory array is separated into two 4K-bytes sections which allows read accesses to one section while a write operation is taking place in the other section. The nonvolatile memory also features Software Data Protection to protect the contents during power transitions, and an advanced Block Protect register which allows Individual blocks of the memory to be configured as read-only or read/write.

5

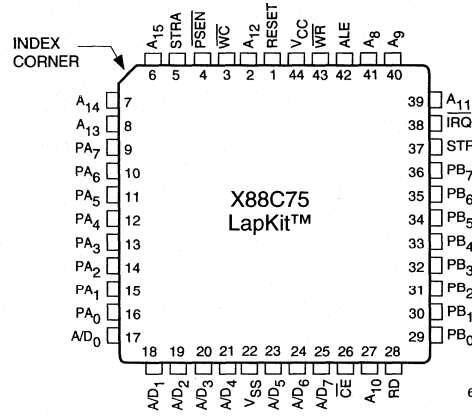
PIN CONFIGURATIONS

DIP



6340 ILL F01.0

PLCC
TQFP



6340 ILL F02.2

SLIC® E², Concurrent Read During Write, Block Lock, and Lapkit are registered trademarks of Xicor, Inc.

Each bidirectional port consists of 8 general purpose I/O lines and 1 data strobe line. The ports also feature a configurable interrupt request output.

Access to the X88C75 is accomplished through the multiplexed address/data bus of the 80C51 type controllers. An internal programmable address decoder maps the internal memory and register locations into the desired address space.

ARCHITECTURAL OVERVIEW

The X88C75 incorporates the interface circuitry normally needed to decode the control signals and demultiplex the address/data bus to provide a "seamless" interface.

The control inputs on the X88C75 are configured such that it is possible to directly connect them to the proper interface signals of the 80C51 microcontroller. The reading of data from the chip is controlled either by the $\overline{PSEN}$ or the $\overline{RD}$ signal, which essentially maps the X88C75 into both the Program and the Data Memory address map.

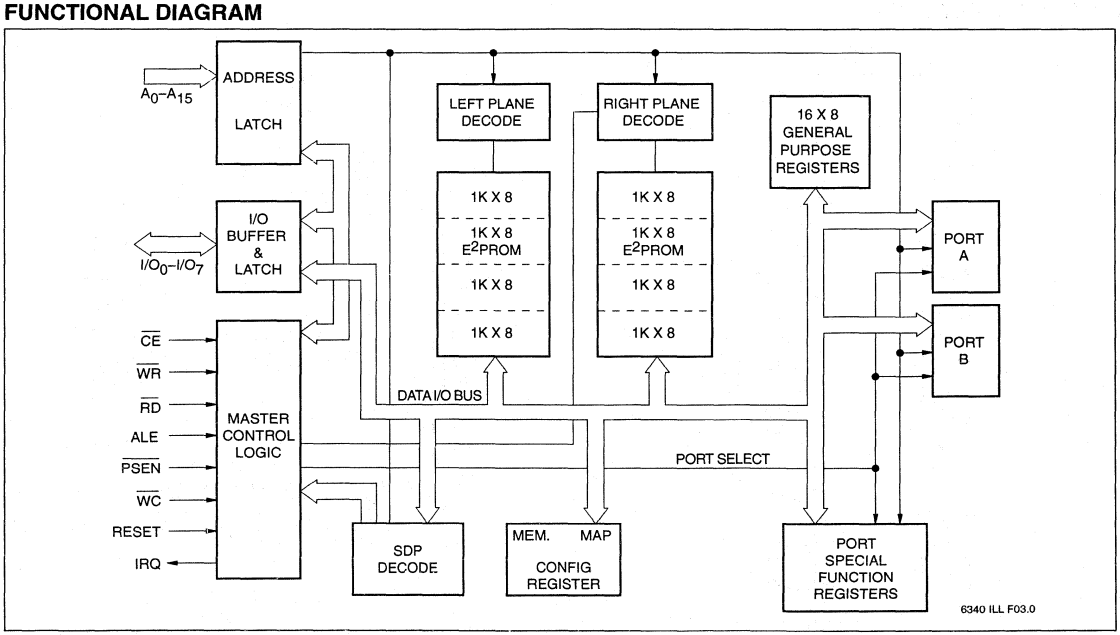
Reading and writing of the nonvolatile memory array is analogous to RAM operation. During a write operation to either the nonvolatile memory or the control registers, ALE latches the address to be written into the X88C75.

The rising edge of $\overline{WR}$ latches the data to be written.

The nonvolatile memory of the X88C75 is internally organized as two independent arrays of 4K-bytes with the A12 input selecting which of the two planes of memory is to be accessed. While the processor is executing code out of one plane, write operations can take place in the other plane; allowing the processor to continue execution of code out of the X88C75 during a byte or page write to the device. This feature is called Concurrent Read During Write.

The X88C75 also features an advanced implementation of the Software Data Protection scheme, called Block Lock Protect, which allows the nonvolatile memory array to be treated as 8 independent sections of 1K-bytes. Each of these sections can be independently enabled for write operations. This allows segmentation of the memory contents into writable and non-writable sections, thereby, allowing certain sections of the device to be secured so that updates can only occur in a controlled environment. (e.g. in an automotive application, only at an authorized service center). The Block Protect configuration is stored in a nonvolatile register, ensuring that the configuration data will be maintained after the device is powered-down.

FUNCTIONAL DIAGRAM



The X88C75 write control input, serves as an external control over the completion of a previously initiated page load cycle.

The X88C75 also features the industry standard 5V E² memory characteristics such as byte or page mode write and Toggle Bit Polling.

Read

A HIGH to LOW transition on ALE latches the address; the data will be output on the AD pins after either $\overline{RD}$ or $\overline{PSEN}$ goes LOW (t_{RDLV}).

Write

A write is performed by latching the addresses on the falling edge of ALE. The $\overline{WR}$ is strobed LOW followed by valid data being presented on the AD_0–AD_7 pins. The data will be latched into the X88C75 on the rising edge of $\overline{WR}$.

Page Write Operation

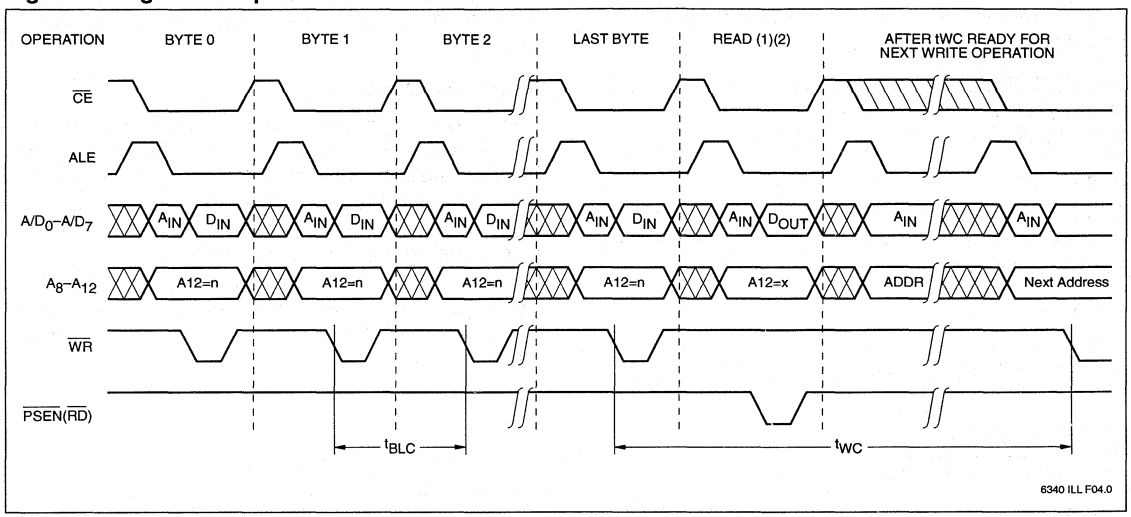
The X88C75 supports page mode write operations. This allows the microcontroller to write from one to thirty-two bytes of data to the X88C75. Each individual write within a page write operation must conform to the byte write timing requirements. The falling edge of $\overline{WR}$ starts a timer delaying the internal programming cycle 100µs: therefore, each successive write operation must begin within 100µs of the last byte written. The waveform on page 4 illustrates the sequence and timing requirements.

PIN DESCRIPTIONS

PIN NAME	I/O	DESCRIPTION
RESET	I	RESET is used to initialize the internal static registers and has no effect on the E² memory operations. The default active level is HIGH, but it can be reconfigured in EEM register.
$\overline{PSEN}$	I	Content of E² memory can be read by lowering the $\overline{PSEN}$ and holding both $\overline{RD}$ and $\overline{WR}$ HIGH. The device then places on the data bus (AD_7–AD_0) the contents of E² memory at the latched address.
STRA, STRB	I/O	The STRA controls port A and STRB controls port B. When ports are configured as inputs, a valid transition on their strobe pins will latch into their port data register the data present at the port input pins. Writing to an output port data register generates a pulse of fixed duration on its corresponding strobe pin. The output data presented at the output pins stay valid until the next data is written to the output port data register.
PA_7–PA_0	I/O	The I/O lines of port A. The output driver can be configured as either CMOS or open-drain using the AWO bit in CR. The I/O direction bit (DIRA) in CR is used to select port A I/O mode.
PB_7–PB_0	I/O	The I/O lines of port B. The output driver can be configured as either CMOS or open-drain using the BWO bit in CR. The I/O direction bit (DIRB) in CR is used to select port B I/O mode.
A_{15}–A_8	I	Non-multiplexed high-order Address Bus inputs for the upper byte of the address.
AD_7–AD_0	I/O	Multiplexed low-order Address and Data Bus. The addresses are latched when ALE makes a HIGH to LOW transition.
$\overline{WR}$	I	During a byte/page write cycle $\overline{WR}$ is brought LOW while $\overline{RD}$ is held HIGH and the data is placed on the Data Bus. The rising edge of $\overline{WR}$ will latch the data into the device.
$\overline{RD}$	I	The $\overline{RD}$ input is active LOW and is used to read content of either the E² memory or the SFR at the latched address. Both $\overline{PSEN}$ and $\overline{WR}$ signals must be held HIGH during $\overline{RD}$ controlled read operation.
$\overline{IRQ}$	O	The $\overline{IRQ}$ is an open-drain output. It can be configured to signal latching of new data into any of the ports, and/or completion of the E² memory internal write cycle.
$\overline{WC}$	I	$\overline{WC}$ input has to be held LOW during a write cycle. It can be permanently tied HIGH in order to disable write to the E² memory. Taking the $\overline{WC}$ HIGH prior to t_{BIC} (100µs; the time delay from the last write cycle to the start of internal programming cycle) will inhibit the write operation.
$\overline{CE}$	I	The device select ($\overline{CE}$) is an active LOW input. This signal has to be asserted prior to ALE HIGH to LOW transition in order to generate a valid internal device select signal. Holding this pin HIGH and ALE LOW will place the device in standby mode. The ports stay active at all times.
ALE	I	Address Latch Enable input is used to latch the addresses present on the address lines A_{15}–A_8 and AD_7–AD_0 into the device. The addresses are latched when ALE transitions from HIGH to LOW.

6340 PGM T01.1

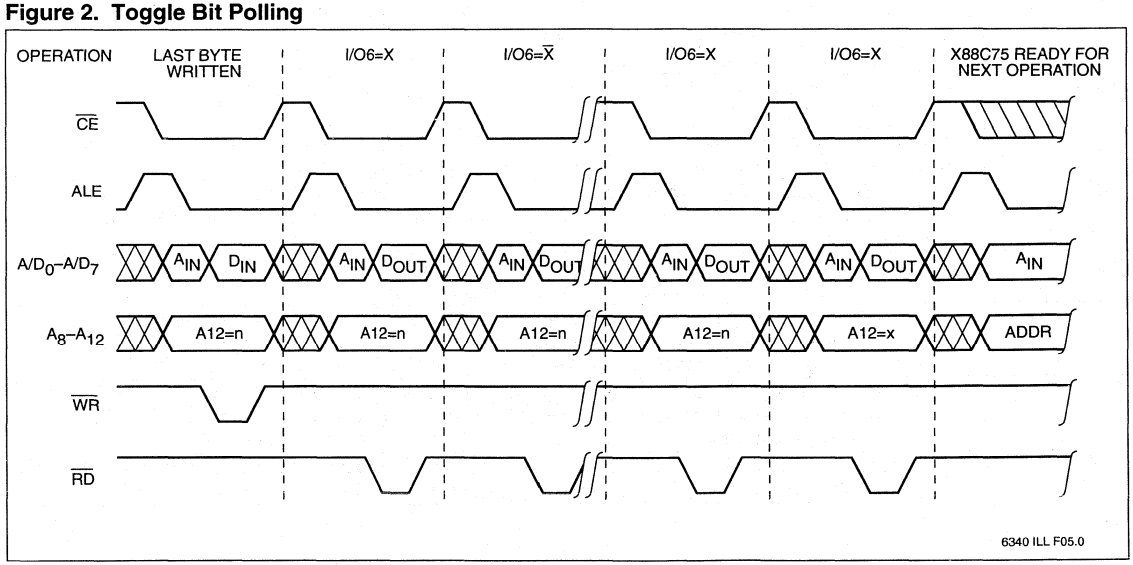
Figure 1. Page Write Operation



Toggle Bit Polling

Because the X88C75 typical write timing is less than the specified 5ms, Toggle Bit Polling has been provided to determine the early completion of a write cycle. During the internal programming cycle, I/O_6 will toggle from "1" to "0" and "0" to "1" on subsequent attempts to read from the memory plane that is being updated. When the internal cycle is complete, the toggling will cease and the device will be accessible for additional read or write operations. Due to the dual plane architecture, reads for polling must occur from the plane that was written; that is, the state of A_{12} during a write must match the state of A_{12} during polling.

Figure 2. Toggle Bit Polling



DATA PROTECTION

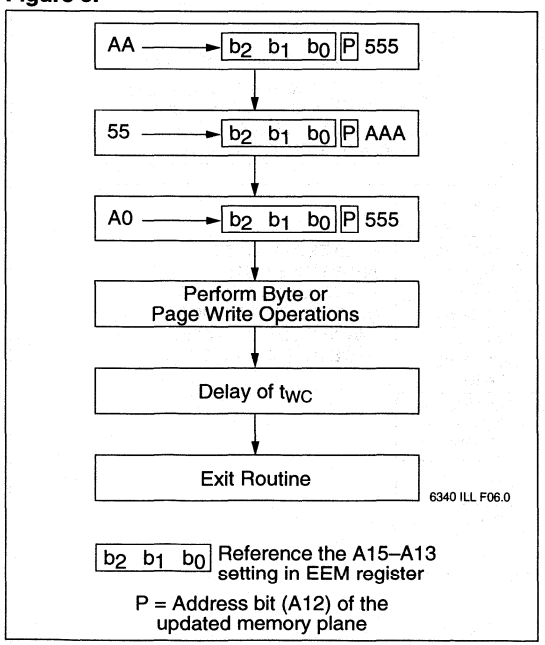
The X88C75 provides two levels of data protection through software control. There is a global software data protection feature similar to the industry standard for E²PROMs and a new Block Lock Protect write lockout protection providing a secondary level data security option.

Software Data Protection

Software Data Protection (SDP) can be employed to protect the entire array against inadvertent writes during power-up/power-down operations. The X88C75 is shipped from the factory with SDP enabled. With SDP enabled, inadvertent attempts to write to the X88C75 will be blocked.

The system can still write data, but only when the write operation (page or byte) is preceded by the three-byte command sequence. All write operations, both the command sequence and any data write operations must conform to the page write timing requirements.

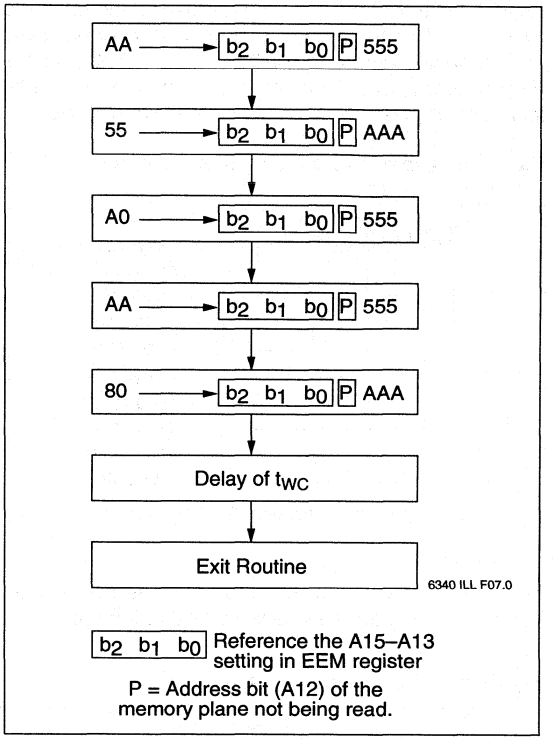
Figure 3.



Writing With SDP Enabled

The SDP mode is also enabled anytime one of the nonvolatile configuration registers are modified. These include writing to EE map, SFR map, and BPR.

Figure 4. Sequence to Deactivate Software Data Protection



Block Lock Protect Write Lockout

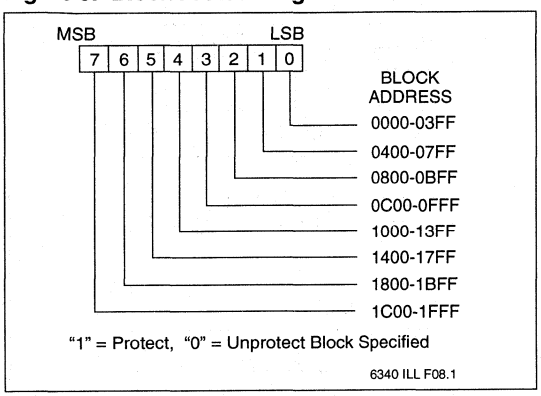
The X88C75 provides a second level of data security referred to as Block Lock Protect write lockout (or Block Protect). This is accessed through an extension of the SDP command sequence. Block Protect allows the user to lockout writes to 1K x 8 blocks of memory. Unlike SDP which prevents inadvertent writes, but still allows easy system access to writing the memory, Block Protect will lockout all attempts unless it is specifically disabled by issuing the deactivation sequence. This feature can be used to set a higher level of protection in a system where a portion of the memory is used to store the system kernel and protect it from the application programs residing in the other blocks.

Setting write lockout is accomplished by writing a five-byte command sequence opening access to the Block Protect Register (BPR). After the fifth byte is written, the user writes to the BPR, selecting which blocks to protect or unprotect. All write operations, both the command sequence and writing the data to the BPR, must conform

5

to the page write timing requirements. It should be noted that accessing the BPR automatically sets the upper level SDP. If for some reason the user does not want SDP enabled, they may reset it using the normal reset command sequence. This will not affect the state of the BPR and any 1K x 8 blocks that were set to the write lockout state will remain in the write lockout state.

Figure 5. Block Protect Register Format



The BPR format and block map are illustrated above. The command sequence is illustrated to the right.

Figure 6. Setting BPR Command Sequence

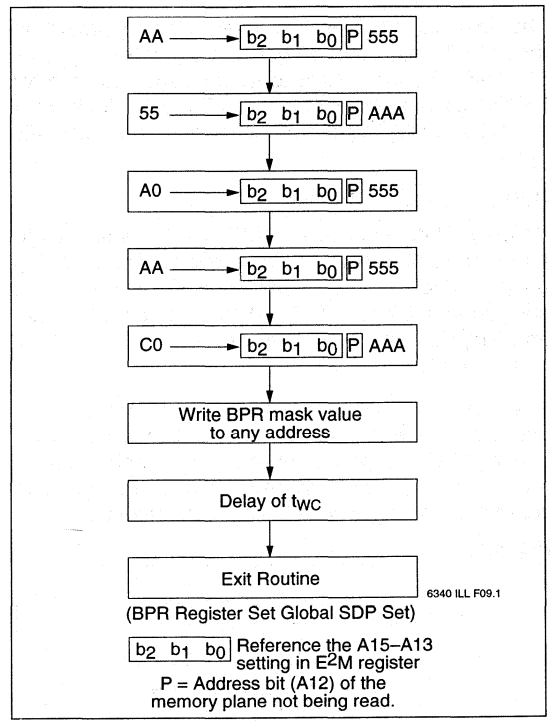


Figure 7. Microcontroller Map

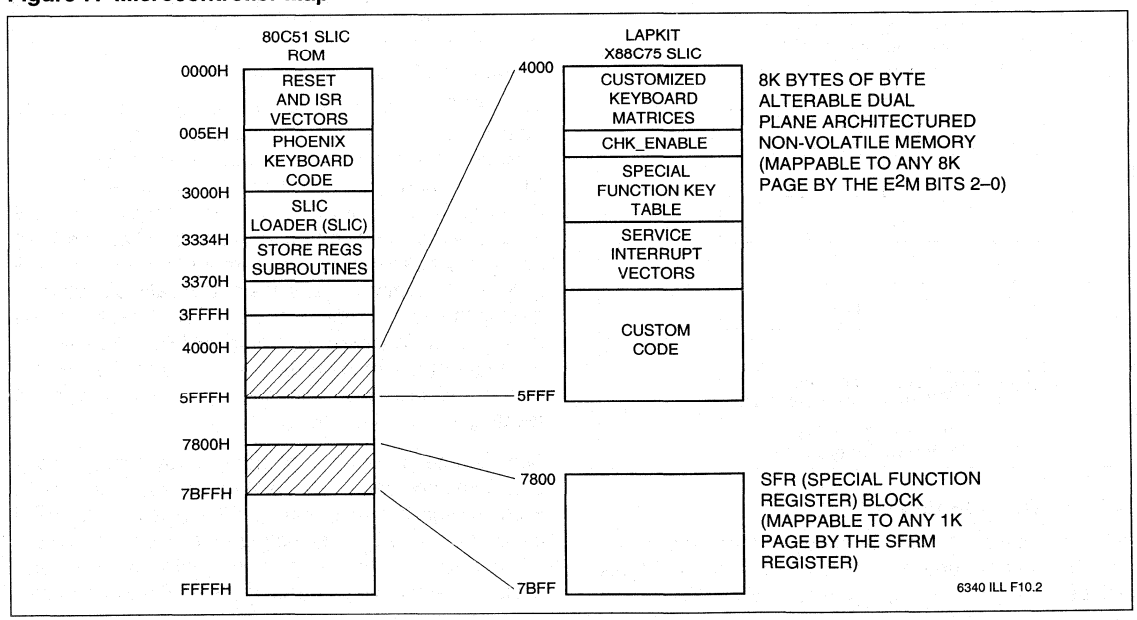
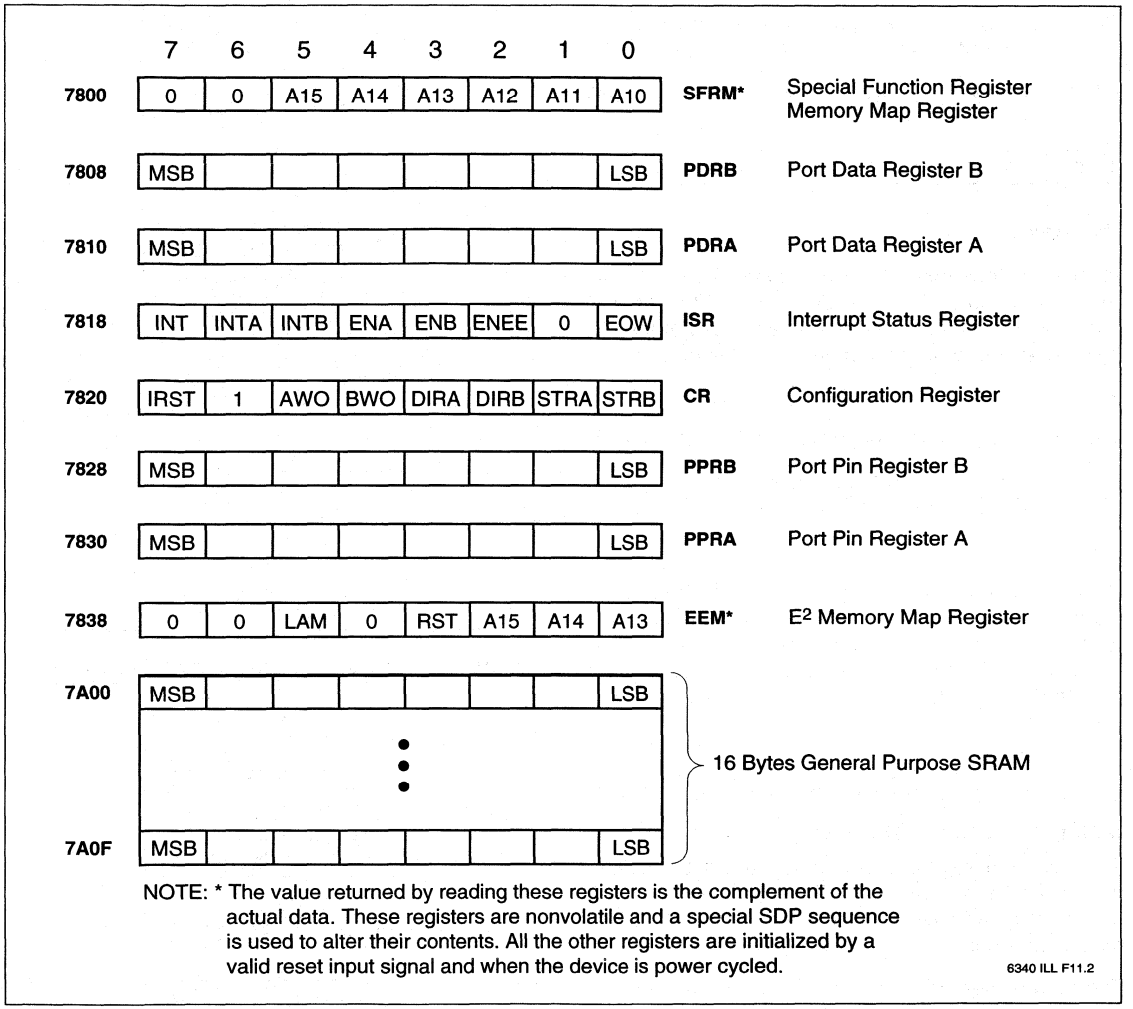


Figure 8. On Chip Registers



NOTE: * The value returned by reading these registers is the complement of the actual data. These registers are nonvolatile and a special SDP sequence is used to alter their contents. All the other registers are initialized by a valid reset input signal and when the device is power cycled.

6340 ILL F11.2

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Programmable Address Decoding

The X88C75 features an internal programmable address decoder which allows the nonvolatile memory array and the internal registers to be mapped in various locations of the 64K-byte memory map. The register set is mappable into a 1K-byte block, while the nonvolatile memory array is mappable into an 8K-byte block. The mapping is controlled by two nonvolatile configuration registers, the SFR Map Register and the E² Memory Map Register. Their bits are mapped as follows:

SFR Map Register (SFRM) **Default = 1E**

7	6	5	4	3	2	1	0
0	0	A15	A14	A13	A12	A11	A10

6340 ILL F12.0

A15-A10

The A15-A10 are upper address bits for the 1K-byte page where the SFR memory is mapped.

BITS 7:6

Setting these two bits to any combination other than "00" or "11" will interfere with device proper operation.

E² Memory Map Register (EEM) **Default = 0A**

7	6	5	4	3	2	1	0
0	0	LAM	0	RST	A15	A14	A13

6340 ILL F13.0

A15-A13

Modifying these three bits changes the location of the program memory within the address map.The A15-A13 correspond to the upper three address bits of the 8K-byte page where program memory will be mapped.

RST

The RST bit controls the polarity of the RESET input pin.

"0" = RESET is Active LOW
"1" = RESET is Active HIGH

LAM

Port B can be configured as either a general purpose I/O port (normal I/O mode), or latched address mode (LAM). The LAM option programs port B to output the demultiplexed low order byte of the address latched into the X88C75 by ALE. The LAM bit selects between these two modes.

"0" = PORT B is I/O Port
"1" = Port B outputs low address byte (A7-A0)

Setting the Mapping Registers

The mapping registers are written using a modified version of the Software Data Protection sequence. All timings must adhere to the normal Software Data Protection sequence.

The complemented contents of the SFR map register and the E² memory map register can be read by the microcontroller at their corresponding SFR addresses. The physical memory location of these registers can be derived by adding the following offset to the SFR base address:

SFR Map Register	00H
E² Memory Map Register	38H

If the regions specified in the map registers overlap, only the SFR will be accessible.

Figure 9. Setting the SFR Map Register

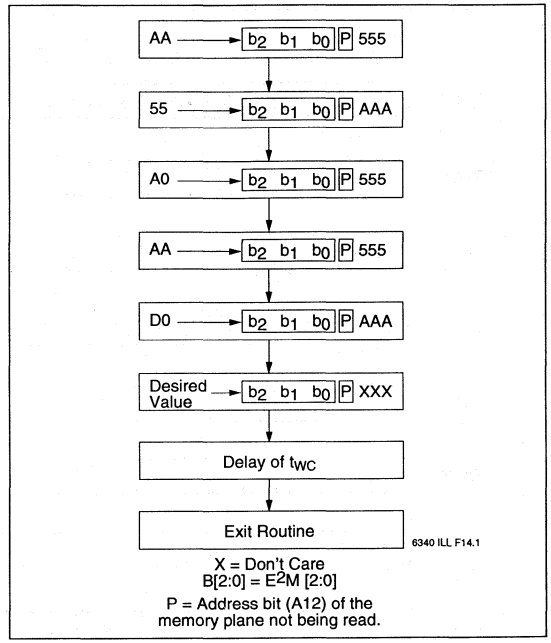
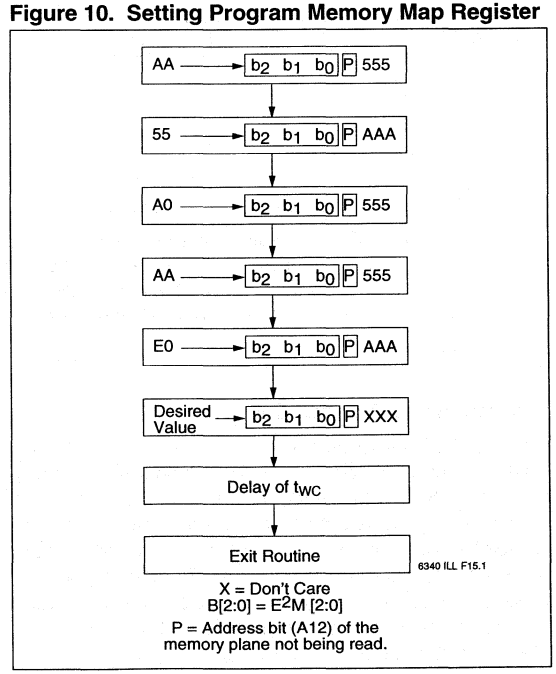


Figure 10. Setting Program Memory Map Register



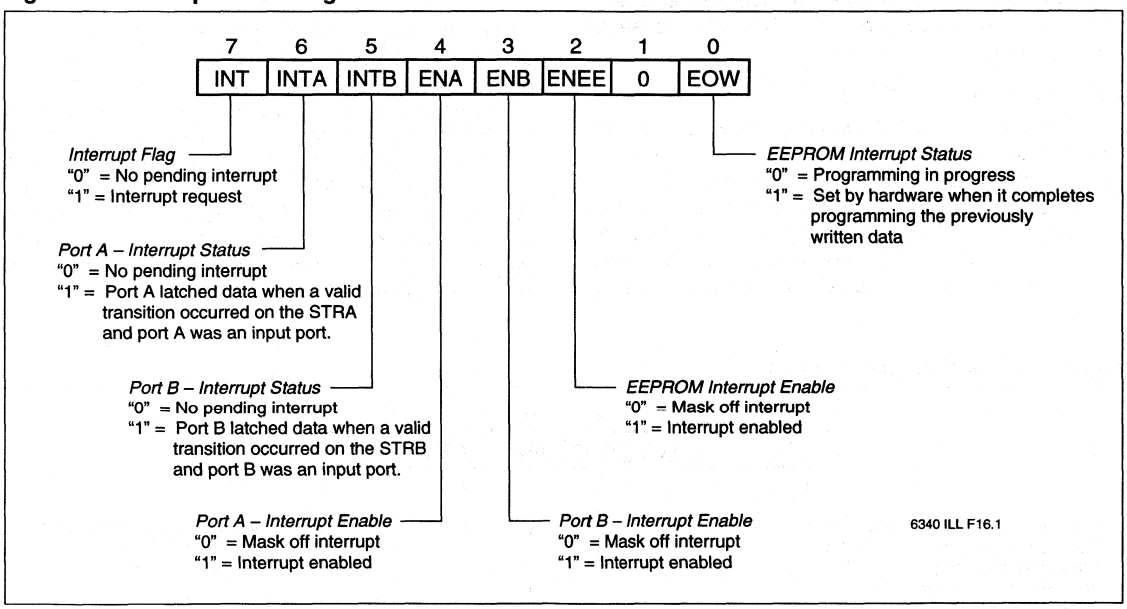
Interrupt Status Register (ISR)

The Interrupt Status Register is a volatile register used to configure the interrupt condition for the I/O ports as well as to determine the interrupt status of the ports. The X88C75 ports can generate an interrupt to the microcontroller upon the proper transition (as specified in the configuration register) on either STRA or STRB pins when the corresponding I/O port is configured as an input.

The INT flag is set when any of the input strobes are toggled provided that their corresponding interrupt enable bits (ENA, ENB) are set. The INT flag is cleared when latched data is read (PDR) or pending interrupt status flag (INTA, INTB) in ISR is forced to "0" by the interrupt service routine. Interrupt service routine should examine the interrupt status flags (INTA, INTB) and identify the source of pending interrupt.

The E² memory interrupt status flag (EOW) is another means to detect the early completion of a write cycle. When ENEE is enabled, the hardware will set the EOW flag, and interrupt the microcontroller at the end of an internal programming cycle. Toggle Bit Polling can be replaced by this hardware interrupt, which reduces the software overhead. The EOW flag should be cleared by software. The interrupt status register bits are mapped as follows.

Figure 11. Interrupt Status Register



Configuration Register (CR)

The Configuration Register is a volatile register used to configure the operation of the I/O ports. The configuration register allows the microcontroller to designate whether each of the two ports is an input or output, what type of output drive is to be used, and what is the polarity of the two strobe lines, STRA and STRB. The bit map of configuration register is shown below.

The IRST bit in the configuration register controls the method used to clear the port interrupt request flags(INTA, INTB). The interrupts are reset by either reading the interrupt source or writing to the Interrupt Status Register. The interrupt must be disabled prior to changing strobe polarity bits(STPA, SPTB), or port direction bits (DIRA, DIRB) in CR. Otherwise, any attempt to modify status of these bits may cause an interrupt to occur.

Port Data Registers (PDR)

The PDRA/PDRB are byte-wide latches which hold port data. When a port is configured as output, the outputs of its PDR latch are connected to the port pins. Writing to PDR generates a pulse on the port strobe pin and latches the data. If a port is configured as an input, the inputs of its PDR latch are connected to the port pins. External data is latched into PDR on the positive edge of its clock. The port strobe input and strobe polarity bit(STPA, STPB) are XORed to generate the PDR input clock.

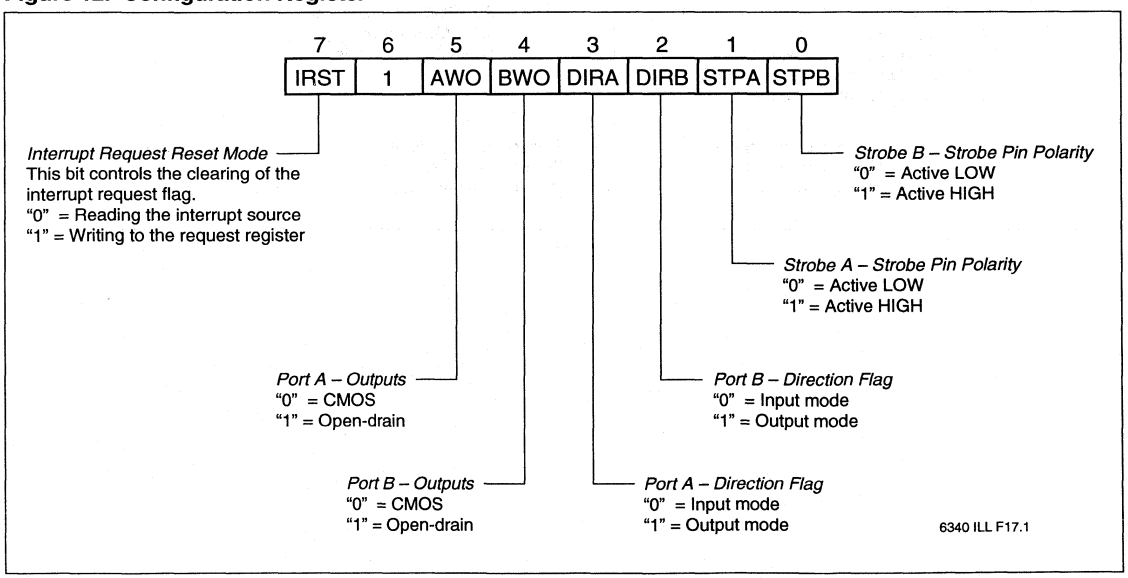
Port Pin Registers (PPR)

The read-only Port Pin Registers are used for reading the current status of the external I/O port pins. Accessing the PPR causes the values on the port pins to be placed on the data bus.

The port direction control bits in configuration register set the direction for the entire port and no control mechanism is provided to program the direction of individual pins. However, the ports have a flexible architecture which allows operating the I/O ports in bidirectional mode using the PPR read feature.

A port can be operated in input/output mode by configuring it as an open-drain output port. The port wire-OR bit (AWO, or BWO in CR) and its port data direction bit (DIRA, or DIRB in CR) should be set to "1". The PDR bits which correspond to the port pins assigned as inputs should be programmed to "1". For monitoring the status of the input pins, the PPR can be read. In this application the port strobe pin and the PDR latch are in output mode. In open-drain mode, there are weak internal pull-ups on the port pins, however external pull-ups must be used for proper switching of the I/O lines.

Figure 12. Configuration Register



STATIC RAM BLOCK

There are 16 bytes of volatile static RAM registers mapped to the SFR region. They reside in the 200H-20FH area offset from the SFR base address. Accessing these registers has to be done through external RAM operations for both writes and reads.

PRINCIPLES OF OPERATION

I/O Port Operation

The expansion ports are accessible to the software using their assigned memory mapped addresses. Each port occupies two addresses in the SFR plane, the Port Data Register and Port Pin Register. These registers and their location in the 1K-byte register memory space is shown on page 7.

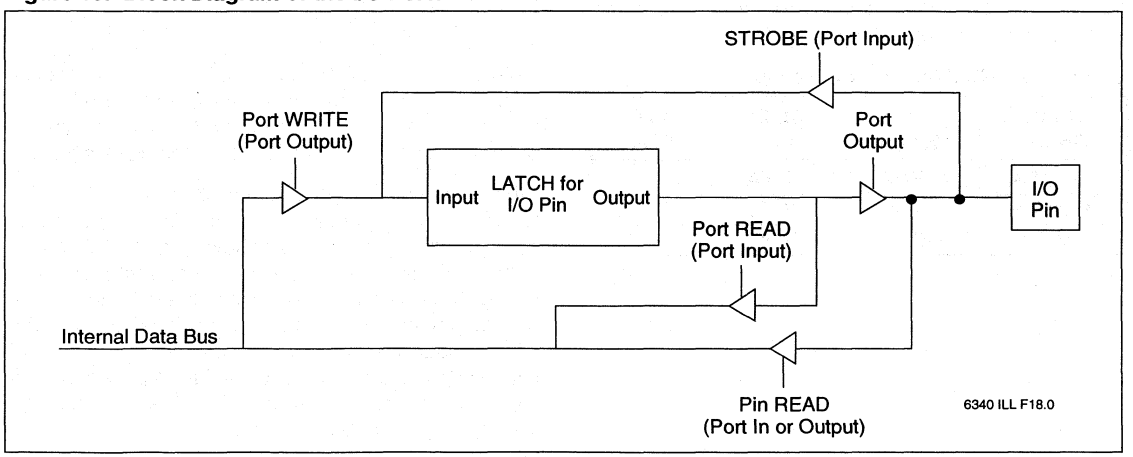
The ports can be configured as either inputs or outputs, the DIRA and DIRB bits in the configuration register are used to select between the modes. The input signal on the strobe pin, when the corresponding port is configured as an input, is fed to the clock input of the port latch. These are transparent latches and the trailing edge of the strobe pulse is used to latch the data present on the input pins. The strobe signal polarity is configurable using the STPA and STPB bits in the configuration register.

Writing to the port data register of an output port will generate a pulse of fixed duration on its strobe pin. The data also simultaneously arrives at the port output pins. The latched data stays there until new data is written to the port data register. The strobe pulse shape is controlled by the state of the STPA and STPB bits in the configuration register. A "1" forces the valid transition on the corresponding strobe pin as active HIGH (_┌┐_), and a "0" sets it to active LOW (‾└┘‾).

When an external strobe signal is applied to an input port, the latching of input data is followed by the setting of the interrupt flags. The INTA and INTB interrupt flags are used by ports A and B respectively, and are set along with the INT interrupt flag at the end of strobe pulse input. External interrupt ($\overline{IRQ}$) is generated if the interrupt enable flags (ENA and ENB) are set by the software. The former enables the port A interrupt and the latter enables the port B interrupt.

5

Figure 13. Block Diagram of the I/O Ports



The port output drivers can be either CMOS or open-drain. The wire-OR bits (AWO, BWO) in the configuration register are used to make the selection. When the bits are "0" the CMOS drivers are enabled. Setting these bits will enable the open-drain output drivers. Small pull-up resistors should be used on the pins of open-drain ports.

IRQ

The $\overline{IRQ}$ pin is an active LOW open-drain output. In embedded systems applications, this signal is connected to the microcontroller interrupt input pin through either a direct connection or via an interrupt controller.

Table 1 depicts the three sources of interrupts and their associated flags. Under normal conditions, the INT and port interrupt flags are set, if the port which is configured as an input has its strobe line toggled. If the port interrupt enable flag is set, or gets set while the INT flag is set, then the $\overline{IRQ}$ signal is asserted. The $\overline{IRQ}$ stays valid as long as the interrupt flags are not cleared by the software or the hardware.

Another interrupt source is the End Of Write flag (EOW) which is set by the hardware at the end of every internal programming cycle. The interrupt from this source is controlled by the ENEE bit in ISR. If ENEE is enabled, then EOW can generate an external interrupt. The interrupt is cleared by setting EOW to "0".

Table 1. X88C75 Interrupt Sources

Interrupt Source	Interrupt Enable	Status Flag	INT Flag
PORT A	ENA	INTA	"1"
PORT B	ENB	INTB	"1"
EOW	ENEE	EOW	—

6340 PGM T02.1

PORTS A & B INTERRUPTS

The X88C75 features two 8-bit I/O ports which are equipped with a configurable interrupt module. The interrupts are used to signal the reception of new data at an input port data latch. When a port is configured as an output, it can no longer generate any interrupts.

The input port interrupt mechanism is controlled by the external strobe pins (STRA, STRB). Detecting a valid transition on the pin will set the interrupt flags and latch in the input data. The external interrupts from the ports can be masked off using the interrupt enable bits (ENA, ENB) in ISR.

Once an external interrupt is asserted, clearing the interrupt flags will cause the $\overline{IRQ}$ signal to return to its idle state. There are two ways of resetting the interrupt flags. The selection is made using the IRST bit in the configuration register. If IRST is set, then the interrupt flags are cleared by writing "0" to the bit positions corresponding to the interrupt flags (INTA, INTB) in ISR. When the IRST is cleared, reading the PDR automatically clears the interrupt flags.

SOFTWARE CONTROLLED PORT OPERATIONS

The individual clock signals, that control the PDR input latches and load the external data present on the port pins, are generated by XORing the strobe polarity bit and the strobe input of the port. The strobe polarity bits (STPA, STPB) in CR can be used to program the active edge of the strobe inputs. However, if the external strobe input is permanently tied to V_{SS} or V_{CC}, then the strobe polarity bit controls the PDR input latch clock signal.

When a port strobe and its polarity bit have identical logic levels, the corresponding PDR latch is active and any change in the port inputs will show up at the PDR latch outputs. Holding the strobe input at current levels and changing the strobe polarity bit value will generate a positive transition on the PDR clock signal, causing the latch outputs to reflect the previous logic state of the port pins. The clock transition sets the interrupt flags, and if the interrupts have been enabled, then an external interrupt signal will be asserted.

This feature allows the port input operation by permanently tying the STRx inputs to V_{CC} or V_{SS}, and using the STPx bits in CR to control PDR latches. Another advantage of this feature are software generated interrupts. Since the clocking of the PDR latch causes the corresponding port INTx flags to be set, by enabling the interrupts the microcontroller is forced to execute the ISR responsible to service the newly latched data.

END OF WRITE (EOW) INTERRUPT

The internal programming cycle requires several milliseconds for either a single byte write or a page write. The updated memory plane is inaccessible while the programming is in progress. However, the opposite plane is still available for program fetch and data read operations.

The X88C75 has two means of signaling end of an internal programming cycle. In the Toggle Bit Polling technique, the last written byte is successively read. Bit 6 of read data toggles while the programming cycle is still in progress. The software has to continually monitor device responses and determine if it can again access the plane.

In the other method, at the end of an internal programming cycle, the hardware sets the EOW flag. The software can either poll this flag or enable the interrupts by setting the ENEE bit in ISR. Effective use of EOW is made by clearing it prior to initiating a write operation. If the interrupt is enabled, an external interrupt will be asserted at the completion of the internal write cycle. The interrupt is cleared by setting EOW to "0".

USING A PORT IN BIDIRECTIONAL MODE

In order to use a port in bidirectional mode, it has to be configured as an open drain output port. Small pull-up resistors are required on all port output pins. Bit positions in the Port Data Register corresponding to port inputs should contain "1". The inputs are then read by accessing PPR. Data is not latched into the device, so the inputs must stay valid throughout the read cycle. The port strobe pin is configured as an output and cannot be used as port latch clock input.

ABSOLUTE MAXIMUM RATINGS*

Temperature under Bias
- X88C75 ..... −10°C to +85°C
- X88C75I ..... −65°C to +135°C

Storage Temperature ..... −65°C to +150°C
Voltage on any Pin with
- Respect to V_{SS} ..... −1V to +7V

D.C. Output Current 5mA
Lead Temperature
- (Soldering, 10 seconds) ..... 300°C

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	+70°C
Industrial	−40°C	+85°C
Military	−55°C	+125°C

6340 PGM T03.1

Supply Voltage	Limits
X88C75	5V ±10%

6340 PGM T04.1

D.C. OPERATING CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
I_{CC}	V_{CC} Current (Active)		60	mA	$\overline{CE}$ = $\overline{RD}$ = V_{IL}, All I/O's = Open,Other Inputs = V_{CC}
$I_{SB1(CMOS)}$	V_{CC} Current (Standby)		100	µA	$\overline{CE}$ = V_{IH}, All I/O's = Open, Other Inputs = V_{IH}, ALE = V_{IL}
$I_{SB2(TTL)}$	V_{CC} Current (Standby)		2	mA	$\overline{CE}$ = V_{IH}, All I/O's = Open, Other Inputs = V_{IH}, ALE = V_{IL}
I_{LI}	Input Leakage Current		10	µA	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output Leakage Current		10	µA	V_{OUT} = V_{SS} to V_{CC}, $\overline{RD}$ = $\overline{PSEN}$ = V_{IH}
V_{IL}(3)	Input LOW Voltage	−1	0.8	V	
V_{IH}(3)	Input HIGH Voltage	2	V_{CC} + 0.5	V	
V_{OL}	Output LOW Voltage		0.4	V	I_{OL} = 2.1mA
V_{OH}	Output HIGH Voltage	2.4		V	I_{OH} = −400µA

6340 PGM T05.2

CAPACITANCE T_A = +25°C, f = 1MHz, V_{CC} = 5V

Symbol	Test	Max.	Units	Conditions
$C_{I/O}$(4)	Input/Output Capacitance	10	pF	$V_{I/O}$ = 0V
C_{IN}(4)	Input Capacitance	6	pF	V_{IN} = 0V

6340 PGM T06.0

POWER-UP TIMING

Symbol	Parameter	Max.	Units
t_{PUR}(4)	Power-Up to Read	1	ms
t_{PUW}(4)	Power-Up to Write	5	ms

6340 PGM T07.0

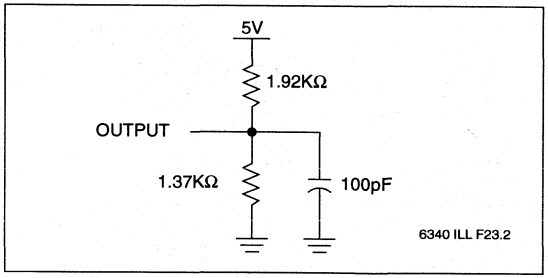
Notes: (3) V_{IL} min. and V_{IH} max. are for reference only and are not tested.
(4) This parameter is periodically sampled and not 100% tested.

A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3V
Input Rise and Fall Times	10ns
Input and Output Timing Levels	1.5V

6340 PGM T08.1

EQUIVALENT A.C. TEST CIRCUIT



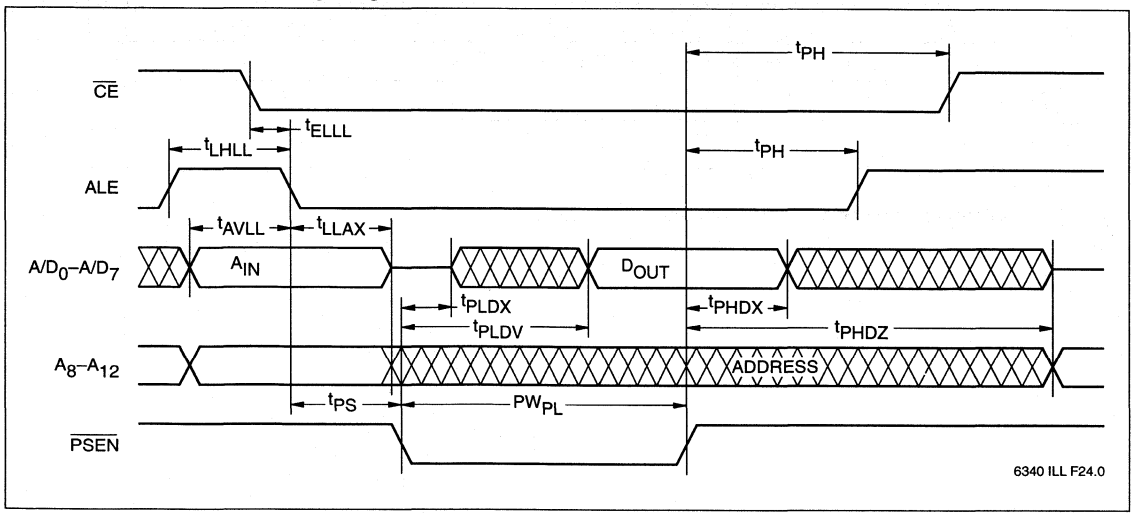
A.C. CHARACTERISTICS (Over the recommended operating conditions unless otherwise specified.)

$\overline{PSEN}$ Controlled Read Cycle

Symbol	Parameter	Min.	Max.	Units
t_{LHLL}	ALE Pulse Width	80		ns
t_{AVLL}	Address Setup Time	20		ns
t_{LLAX}	Address Hold Time	30		ns
t_{PLDV}	$\overline{PSEN}$ Read Access Time		120	ns
t_{PHDX}	Data Hold Time	0		ns
t_{ELLL}	Chip Enable Setup Time	7		ns
PW_{PL}	$\overline{PSEN}$ Pulse Width	150		ns
t_{PS}	$\overline{PSEN}$ Setup Time	30		ns
t_{PH}	$\overline{PSEN}$ Hold Time	20		ns
t_{PHDZ} (5)	$\overline{PSEN}$ Disable to Output in High Z		50	ns
t_{PLDX} (5)	$\overline{PSEN}$ to Output in Low Z	10		ns

6340 PGM T09.0

$\overline{PSEN}$ Controlled Read Timing Diagram



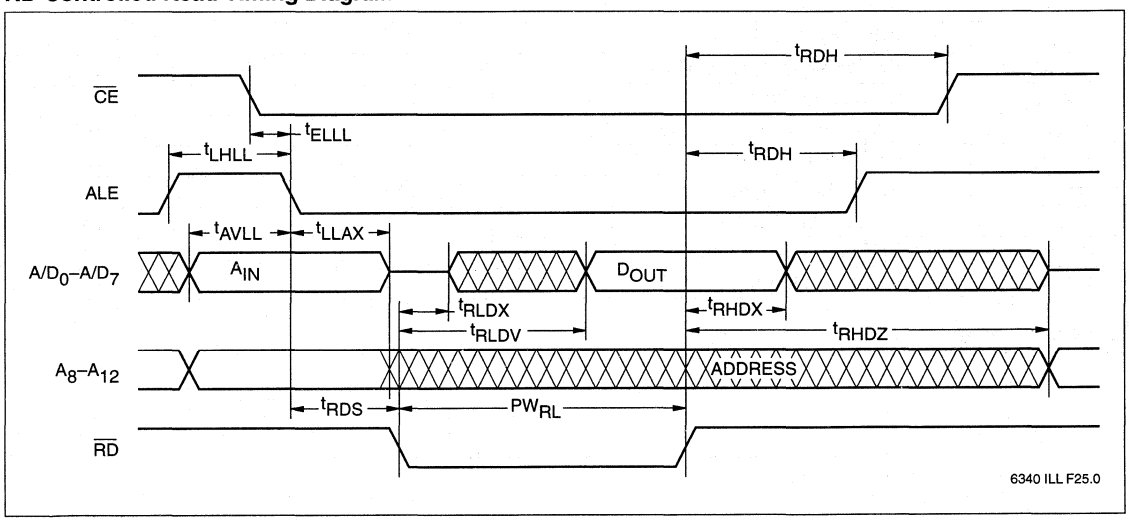
Note: (5) This parameter is periodically sampled and not 100% tested.

$\overline{RD}$ Controlled Read Cycle

Symbol	Parameter	Min.	Max.	Units
t_{LHLL}	ALE Pulse Width	80		ns
t_{AVLL}	Address Setup Time	20		ns
t_{LLAX}	Address Hold Time	30		ns
t_{RLDV}	$\overline{RD}$ Read Access Time		120	ns
t_{RHDX}	Data Hold Time	0		ns
t_{ELLL}	Chip Enable Setup Time	7		ns
PW_{RL}	$\overline{RD}$ Pulse Width	150		ns
t_{RDS}	$\overline{RD}$ Setup Time	30		ns
t_{RDH}	$\overline{RD}$ Hold Time	20		ns
t_{RHDZ} (6)	$\overline{RD}$ Disable to Output in High Z		50	ns
t_{RLDX} (6)	$\overline{RD}$ to Output in Low Z	0		ns

6340 PGM T10.0

$\overline{RD}$ Controlled Read Timing Diagram



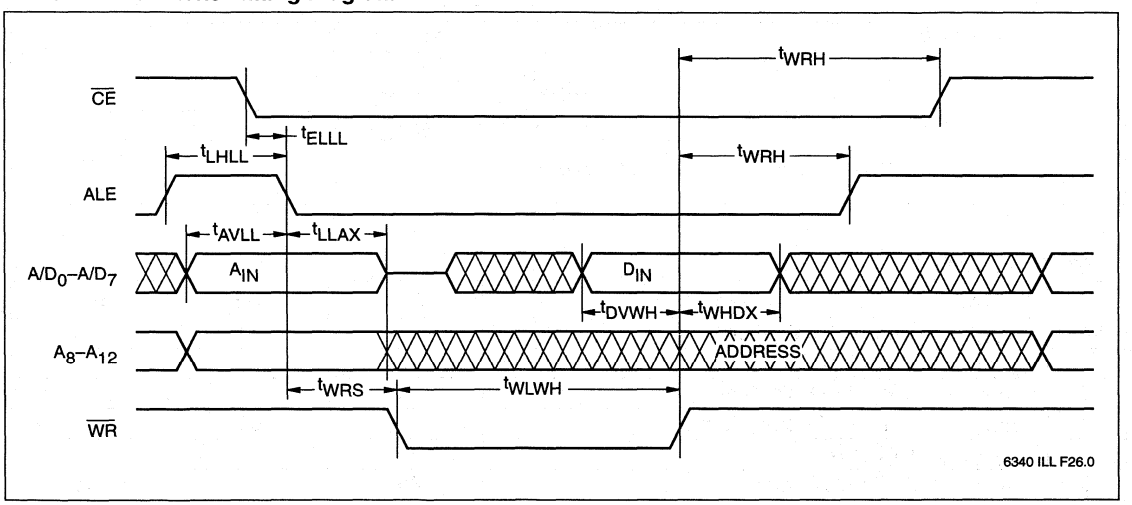
Note: (6) This parameter is periodically sampled and not 100% tested.

$\overline{WR}$ Controlled Write Cycle

Symbol	Parameter	Min.	Max.	Units
t_{LHLL}	ALE Pulse Width	80		ns
t_{AVLL}	Address Setup Time	20		ns
t_{LLAX}	Address Hold Time	30		ns
t_{DVWH}	Data Setup Time	50		ns
t_{WHDX}	Data Hold Time	30		ns
t_{ELLL}	Chip Enable Setup Time	7		ns
t_{WLWH}	$\overline{WR}$ Pulse Width	120		ns
t_{WRS}	$\overline{WR}$ Setup Time	30		ns
t_{WRH}	$\overline{WR}$ Hold Time	20		ns
t_{BLC}	Byte Load Time (Page Write)	0.5	100	µs
t_{WC} (7)	Write Cycle Time		5	ms

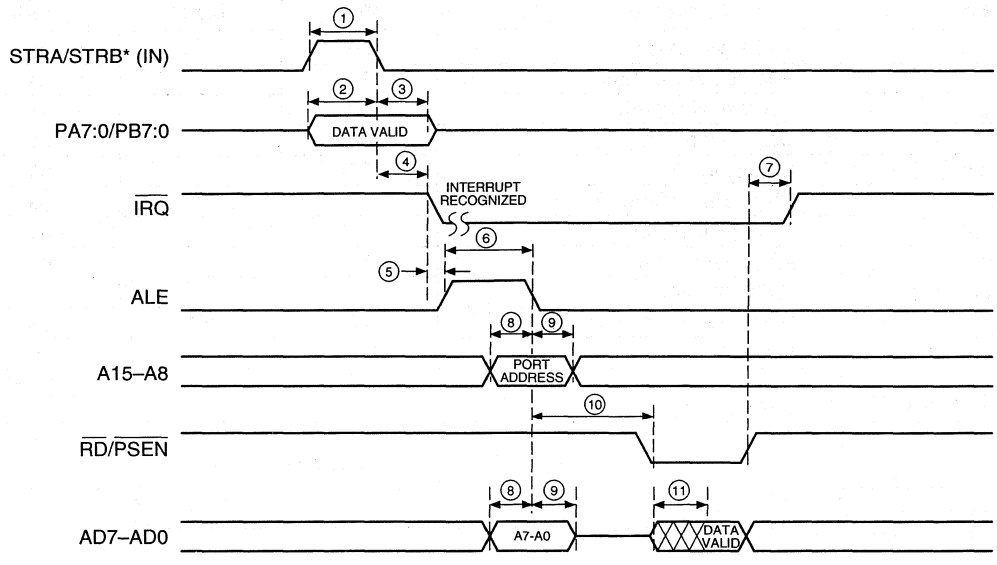
6340 PGM T11.0

$\overline{WR}$ Controlled Write Timing Diagram



Note: (7) t_{WC} is the minimum cycle time to be allowed from the system perspective unless polling techniques are used. It is the maximum time the device requires to automatically complete the internal write operation.

Port Read Diagram



NOTE: *Figure shows active HIGH strobes.

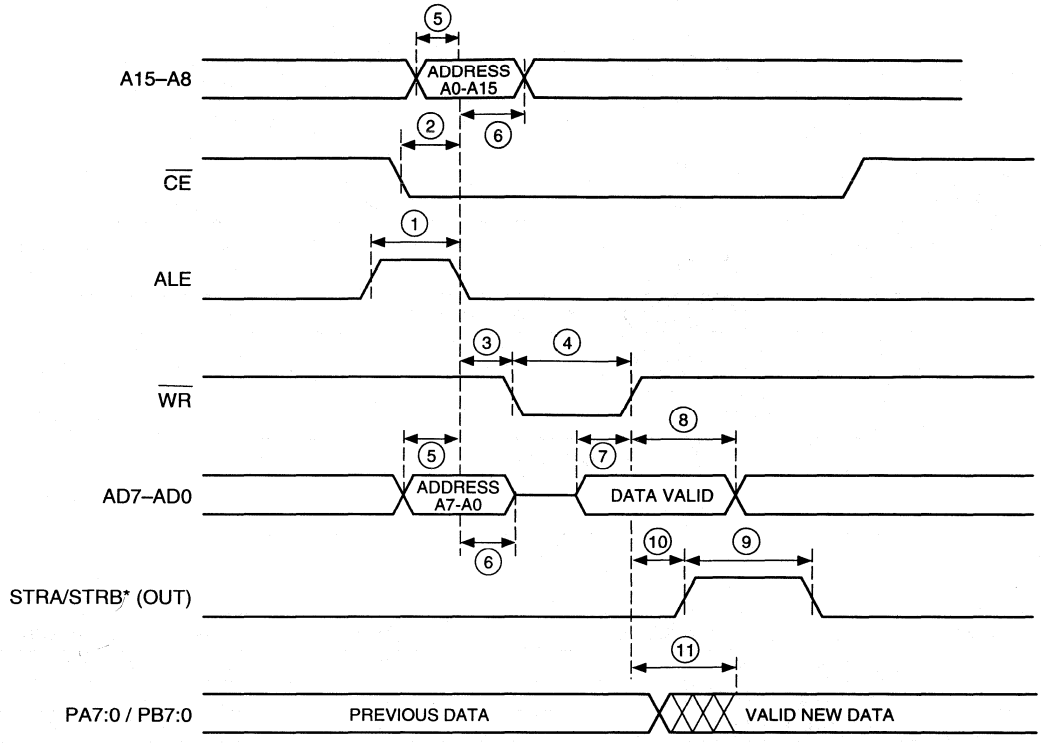
6340 ILL F27.1

PORT READ TIMING

No.	Symbol	Parameter	Min.	Max.	Units
1	t_{SVSX}	Strobe Pulse Width	80		ns
2	t_{DVSV}	Data Port Setup	20		ns
3	t_{SVDX}	Data Port Hold Time	30		ns
4	t_{SVIV}	Interrupt Request to Strobe		50	ns
5	t_{IAD}	$\overline{IRQ}$ to ALE	0		ns
6	t_{LHLL}	ALE Pulse Width	80		ns
7	t_{RXIX}	$\overline{RD}$ to $\overline{IRQ}$	30		ns
8	t_{AVLL}	Address setup time	20		ns
9	t_{LLAX}	Address hold time	30		ns
10	t_{LLWL}	ALE to $\overline{RD}$ LOW	30		ns
11	t_{RLDV}	$\overline{RD}$ Access Time		120	ns

6340 PGM T12.2

Port Write Diagram



NOTE: *Figure shows active HIGH strobes.

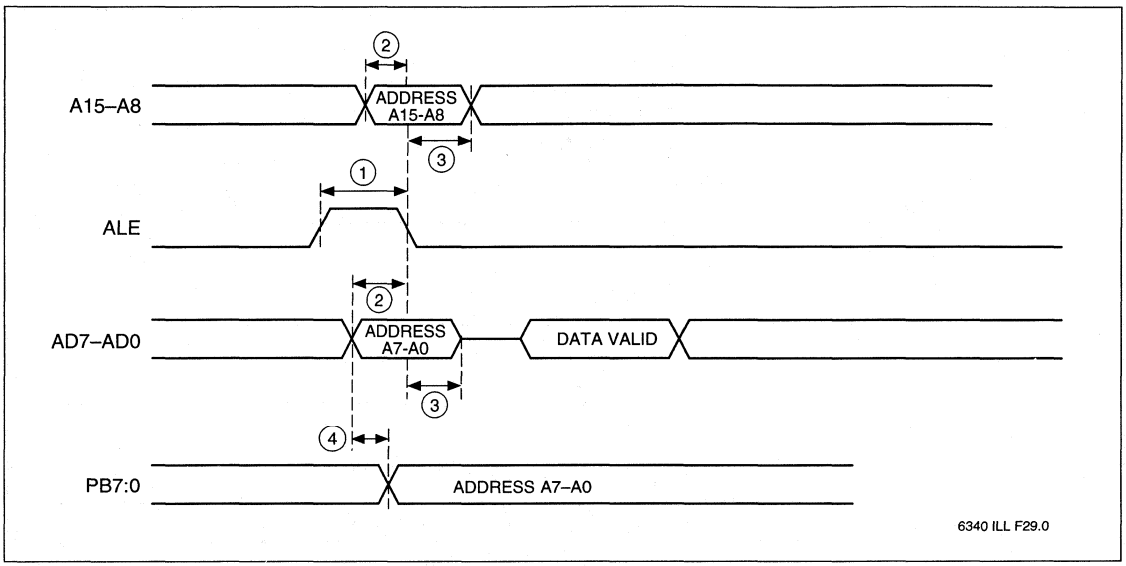
6340 ILL F28.1

PORT WRITE TIMING

No.	Symbol	Parameter	Min.	Max.	Units
1	t_{LHLL}	ALE Pulse Width	80		ns
2	t_{WCS}	Write Chip Select Setup Time	20		ns
3	t_{LLWL}	ALE to $\overline{WR}$	10		ns
4	t_{WLWH}	$\overline{WR}$ Pulse Width	120		ns
5	t_{AVLL}	Write Address Setup Time	20		ns
6	t_{LLAX}	Write Address Hold Time	30		ns
7	t_{DVWH}	Data Setup Time	50		ns
8	t_{WHDX}	Data Hold Time	10		ns
9	t_{SVSX}	Strobe Pulse Width	120		ns
10	t_{QVSV}	Strobe Access Time		40	ns
11	t_{POS}	Port Output Setup Time		40	ns

6340 PGM T13.1

LAM (Latch Address Mode) Diagram



LAM TIMING

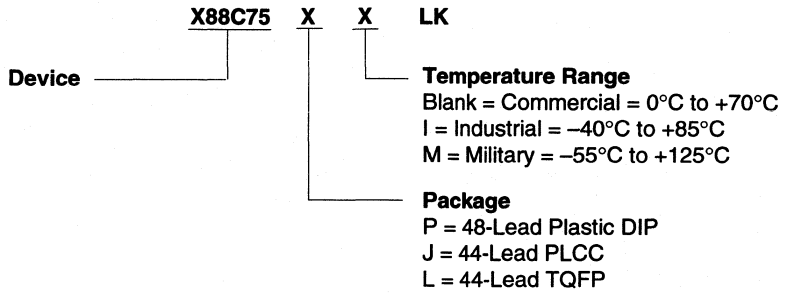
No.	Symbol	Parameter	Min.	Max.	Units
1	t_{LHLL}	ALE Pulse Width	80		ns
2	t_{AVLL}	Address Setup Time	20		ns
3	t_{LLAX}	Address Hold Time	30		ns
4	t_{POS}	Port Output Setup Time		20	ns

6340 PGM T14.1

SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

ORDERING INFORMATION



5

NOTES

256K X88257 32,768 x 8 Bit

E^2 Micro-Peripheral

FEATURES

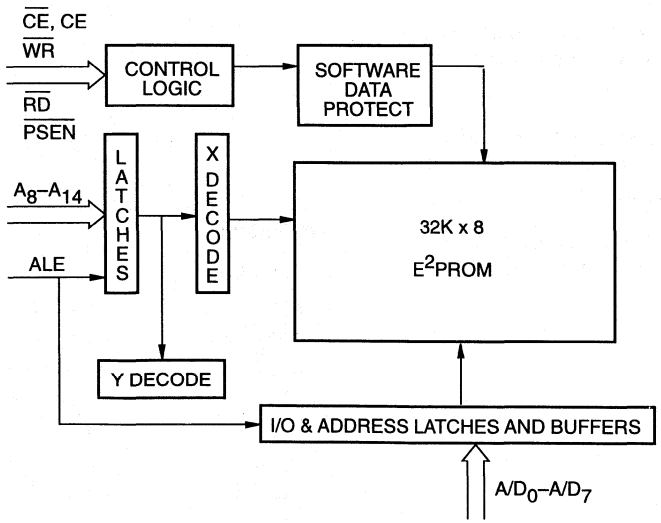
- **Multiplexed Address/Data Bus**
  - **—Direct Interface to Popular 8051 Family**
- **High Performance CMOS**
  - **—Fast Access Time, 120ns**
  - **—Low Power**
    - **—60mA Active Maximum**
    - **—500µA Standby Maximum**
- **Software Data Protection**
- **Toggle Bit Polling**
  - **—Early End of Write Detection**
- **Page Mode Write**
  - **—Allows up to 128 Bytes to be Written in One Write Cycle**
- **High Reliability**
  - **—Endurance: 10,000 Write Cycle**
  - **—Data Retention: 100 Years**

DESCRIPTION

The X88257 is an 32K x 8 E^2PROM fabricated with advanced CMOS Textured Poly Floating Gate Technology. The X88257 features a multiplexed address and data bus allowing direct interface to a variety of popular single-chip microcontrollers operating in expanded multiplexed mode without the need for additional interface circuitry.

5

FUNCTIONAL DIAGRAM



6509 ILL F02.1

PIN DESCRIPTIONS

Address/Data (A/D_0–A/D_7)

Multiplexed low-order addresses and data. The addresses flow into the device while ALE is HIGH. After ALE transitions from a HIGH to LOW the addresses are latched. Once the addresses are latched these pins input data or output data depending on $\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, and $\overline{CE}$.

Addresses (A_8–A_{14})

High order addresses flow into the device when ALE = V_{IH} and are latched when ALE goes LOW.

Chip Enable ($\overline{CE}$)

The Chip Enable input must be LOW to enable all read/write operations. When $\overline{CE}$ is HIGH, ALE is LOW, and CE is LOW, the X88257 is placed in the low power standby mode. If $\overline{CE}$ is used to select the device, the CE must be tied LOW.

Chip Enable (CE)

Chip enable is active HIGH. When CE is used to select the device, the $\overline{CE}$ must be tied HIGH.

Program Store Enable ($\overline{PSEN}$)

When the X88257 is to be used in a 8051-based system, $\overline{PSEN}$ is tied directly to the microcontroller's $\overline{PSEN}$ output.

Read ($\overline{RD}$)

When the X88257 is to be used in a 8051-based system, $\overline{RD}$ is tied directly to the microcontroller's $\overline{RD}$ output.

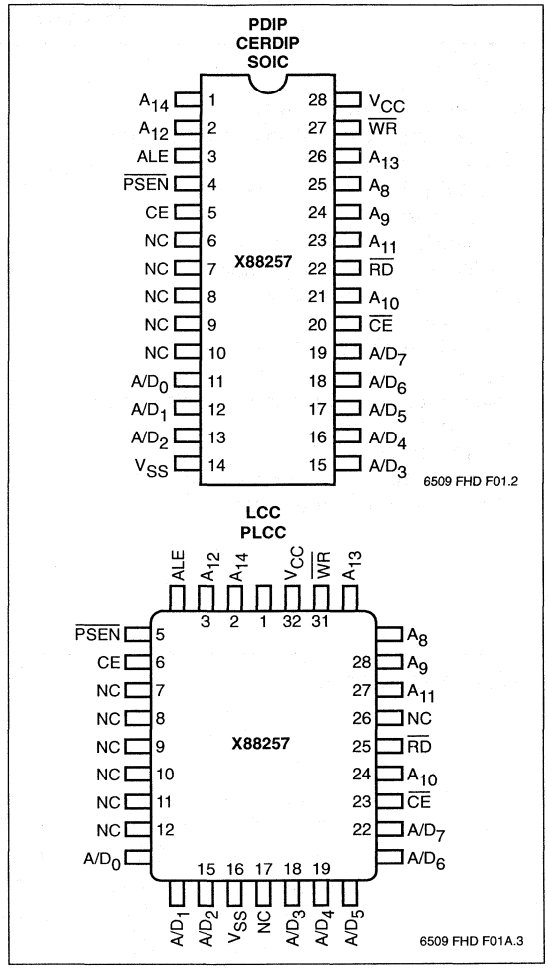
Write ($\overline{WR}$)

When the X88257 is to be used in a 8051-based system, $\overline{WR}$ is tied directly to the microcontroller's $\overline{WR}$ output.

Address Latch Enable (ALE)

Addresses flow through the latches to address decoders when ALE is HIGH and are latched when ALE transitions from a HIGH to LOW.

PIN CONFIGURATION

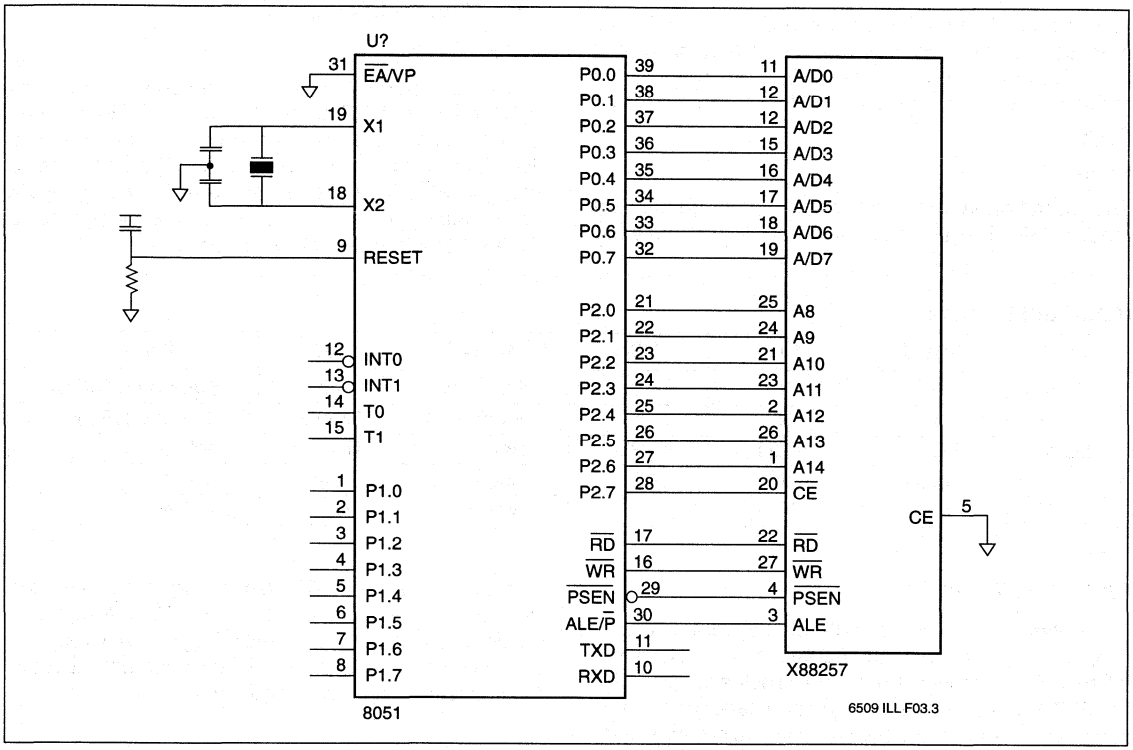


PIN NAMES

Symbol	Description
ALE	Address Latch Enable
A/D_0–A/D_7	Address Inputs/Data I/O
A_8–A_{14}	Address Inputs
$\overline{RD}$	Read Input
$\overline{WR}$	Write Input
$\overline{PSEN}$	Program Store Enable Input
$\overline{CE}$, CE	Chip Enable
V_{SS}	Ground
V_{CC}	Supply Voltage

6509 PGM T01

TYPICAL APPLICATION



PRINCIPLES OF OPERATION

The X88257 is a highly integrated peripheral device for a wide variety of single-chip microcontrollers. The X88257 provides 32K-bytes of 5V E²PROM which can be used either for program storage, data storage or a combination of both, in systems based upon Harvard (80XX) architectures. The X88257 incorporates the interface circuitry normally needed to decode the control signals and demultiplex the address/data bus to provide a "seamless" interface.

The interface inputs on the X88257 are configured such that it is possible to directly connect them to the proper interface signals of the appropriate single-chip microcontroller. In the Harvard type system, the reading of data from the chip is controlled either by the $\overline{PSEN}$ or the $\overline{RD}$ signal, which essentially maps the X88257 into both the Program and the Data Memory address map.

The X88257 also features the industry standard 5V E²PROM characteristics such as byte or page mode write and Toggle Bit Polling.

DEVICE OPERATION

Modes—Mixed Program/Data Memory

By properly assigning the address spaces, a single X88257 can be used as both the program and data memory. This would be accomplished by connecting all the 8051 control outputs to the corresponding inputs of the X88257.

Program Memory Mode

This mode of operation is read-only. The $\overline{PSEN}$ and $\overline{ALE}$ inputs of the X88257 are tied directly to the $\overline{PSEN}$ and ALE outputs of the microcontroller. The $\overline{RD}$ and $\overline{WR}$ inputs are tied HIGH.

When ALE is HIGH, the A/D_0–A/D_7 and A_8–A_{14} addresses flow into the device. The addresses, both low- and high-order, are latched when ALE transitions LOW (V_{IL}). $\overline{PSEN}$ will then go LOW and after t_{PLDV}; Valid data is presented on the A/D_0–A/D_7 pins. $\overline{CE}$ must be LOW during the entire operation.

DATA MEMORY MODE

This mode of operation allows both read and write functions. The $\overline{PSEN}$ input is tied to V_{IH} or to V_{CC} through a pull-up resistor. The ALE, $\overline{RD}$, and $\overline{WR}$ inputs are tied directly to the microcontroller ALE, $\overline{RD}$, and $\overline{WR}$ outputs.

Read

This operation is quite similar to the program memory read. A HIGH to LOW transition on ALE latches the addresses and the data will be output on the AD pins after $\overline{RD}$ goes LOW (t_{RLDV}).

Write

A write is performed by latching the addresses on the falling edge of ALE. Then $\overline{WR}$ is strobed LOW followed by valid data being presented at the A/D_0–A/D_7 pins. The data will be latched into the X88257 on the rising edge of $\overline{WR}$. To write to the X88257, a three-byte command sequence must precede the byte(s) being written. (See Software Data Protection.)

MODE SELECTION

$\overline{CE}$	$\overline{PSEN}$	$\overline{RD}$	$\overline{WR}$	Mode	I/O	Power
V_{CC}	X	X	X	Standby	High Z	Standby (CMOS)
HIGH	X	X	X	Standby	High Z	Standby (TTL)
LOW	LOW	HIGH	HIGH	Read	D_{OUT}	Active
LOW	HIGH	LOW	HIGH	Read	D_{OUT}	Active
LOW	HIGH	HIGH	⌐	Write	D_{IN}	Active

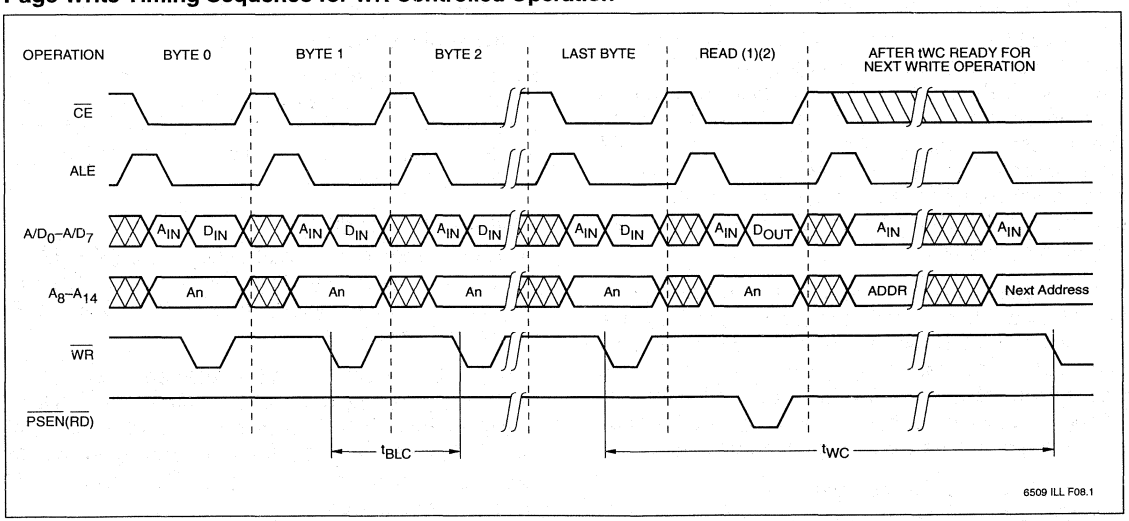
6509 PGM T02

PAGE WRITE OPERATION

Regardless of the microcontroller employed, the X88257 supports page mode write operations. This allows the microcontroller to write from 1 to 128 bytes of data to the X88257. Each individual write within a page write operation must conform to the byte write timing requirements.

The falling edge of $\overline{WR}$ starts a timer delaying the internal programming cycle 100µs. Therefore, each successive write operation must begin within 100µs of the last byte written. The following waveforms illustrate the sequence and timing requirements.

Page Write Timing Sequence for $\overline{WR}$ Controlled Operation

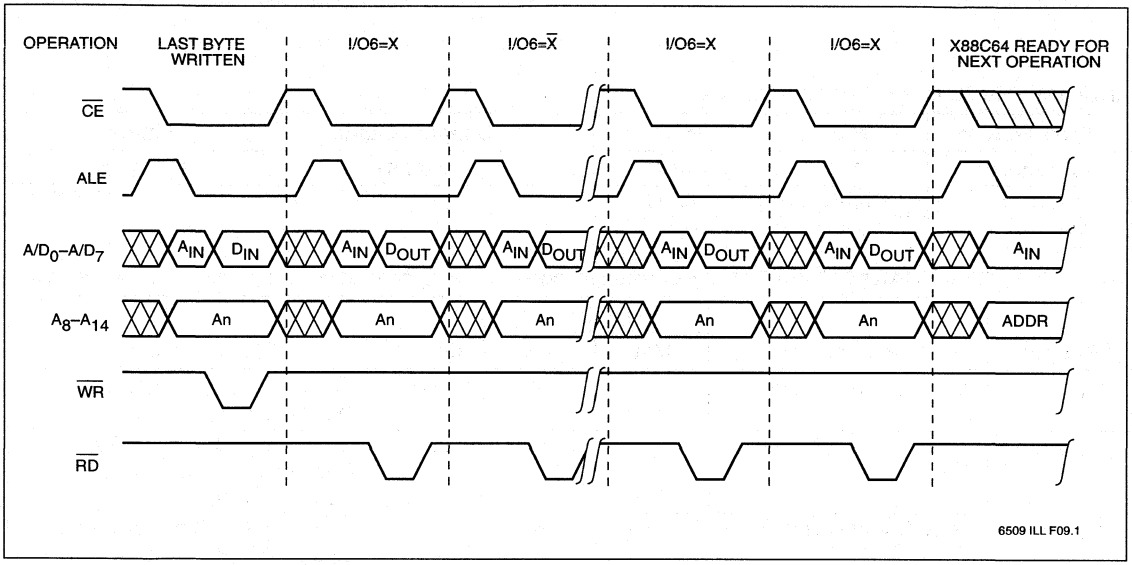


Notes: (1) For each successive write within a page write cycle A_7–A_{14} must be the same.

TOGGLE BIT POLLING

Because the typical write timing is less than the specified 5ms, Toggle Bit Polling has been provided to determine the early end of write. During the internal programming cycle I/O_6 will toggle from "1" to "0" and "0" to "1" on subsequent attempts to read the device. When the internal cycle is complete the toggling will cease and the device will be accessible for additional read or write operations.

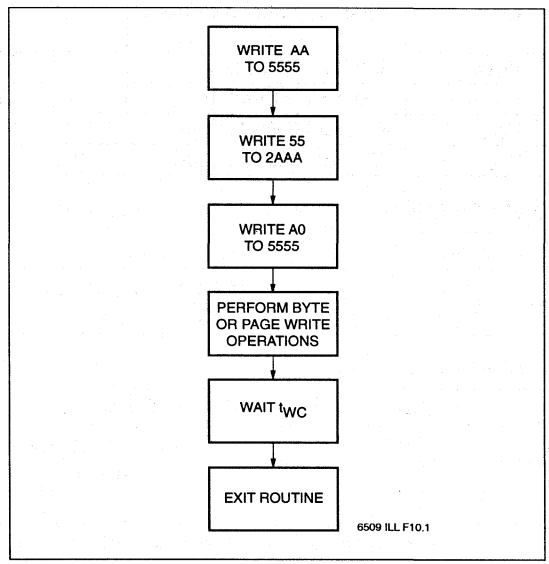
Toggle Bit Polling $\overline{RD}/\overline{WR}$ Control



SOFTWARE DATA PROTECTION

Software Data Protection (SDP) is employed to protect the entire array against inadvertent writes. To write to the X88257, a three-byte command sequence must precede the byte(s) being written. All write operations, both the command sequence and any data write operations must conform to the page write timing requirements.

Writing with SDP



ABSOLUTE MAXIMUM RATINGS*

Temperature under Bias ..... –65°C to +135°C
Storage Temperature ..... –65°C to +150°C
Voltage on any Pin with
Respect to V_{SS} ..... –1V to +7V
D.C. Output Current 5mA
Lead Temperature
(Soldering, 10 seconds) ..... 300°C

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	+70°C
Industrial	–40°C	+85°C
Military	–55°C	+125°C

6509 PGM T03.1

Supply Voltage	Limits
X88257	5V ±10%

6509 PGM T04.1

D.C. OPERATING CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
I_{CC}	V_{CC} Current (Active)		60	mA	$\overline{CE}$ = $\overline{RD}$ = V_{IL}, All I/O's = Open,Other Inputs = V_{CC}
$I_{SB1(CMOS)}$	V_{CC} Current (Standby)		500	µA	$\overline{CE}$ = V_{CC} – 0.3V, All I/O's = Open,Other Inputs = V_{CC} – 0.3V, ALE = V_{IL}
$I_{SB2(TTL)}$	V_{CC} Current (Standby)		6	mA	$\overline{CE}$ = V_{IH}, All I/O's = Open, Other Inputs = V_{IH}, ALE = V_{IL}
I_{LI}	Input Leakage Current		10	µA	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output Leakage Current		10	µA	V_{OUT} = V_{SS} to V_{CC}, $\overline{RD}$ = V_{IH} = $\overline{PSEN}$
V_{IL}(3)	Input LOW Voltage	–1	0.8	V	
V_{IH}(3)	Input HIGH Voltage	2	V_{CC} + 0.5	V	
V_{OL}	Output LOW Voltage		0.4	V	I_{OL} = 2.1mA
V_{OH}	Output HIGH Voltage	2.4		V	I_{OH} = –400µA

6509 PGM T05.1

CAPACITANCE T_A = +25°C, f = 1MHz, V_{CC} = 5V

Symbol	Test	Max.	Units	Conditions
$C_{I/O}$(4)	Input/Output Capacitance	10	pF	$V_{I/O}$ = 0V
C_{IN}(4)	Input Capacitance	6	pF	V_{IN} = 0V

6509 PGM T06

POWER-UP TIMING

Symbol	Parameter	Max.	Units
t_{PUR}(4)	Power-Up to Read	1	ms
t_{PUW}(4)	Power-Up to Write	5	ms

6509 PGM T07

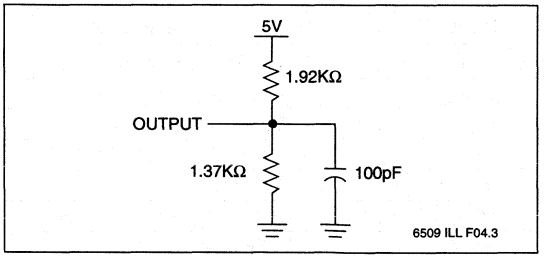
Notes: (3) V_{IL} min. and V_{IH} max. are for reference only and are not tested.
(4) This parameter is periodically sampled and not 100% tested.

A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3V
Input Rise and Fall Times	10ns
Input and Output Timing Levels	1.5V

6509 PGM T08.1

EQUIVALENT A.C. TEST CIRCUIT



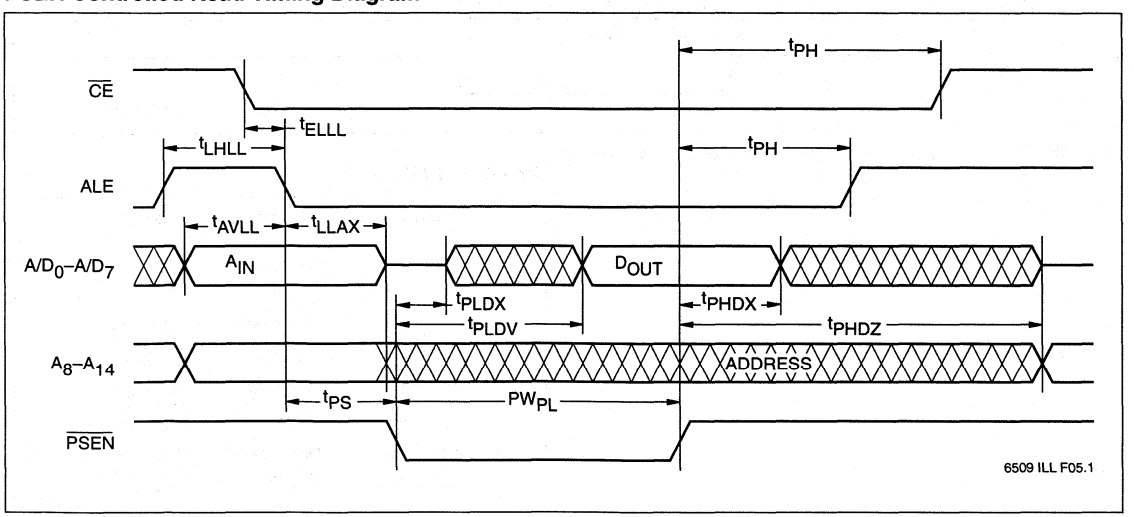
A.C. CHARACTERISTICS (Over the recommended operating conditions unless otherwise specified.)

$\overline{PSEN}$ Controlled Read Cycle

Symbol	Parameter	Min.	Max.	Units
t_{LHLL}	ALE Pulse Width	80		ns
t_{AVLL}	Address Setup Time	20		ns
t_{LLAX}	Address Hold Time	30		ns
t_{PLDV}	$\overline{PSEN}$ Read Access Time		120	ns
t_{PHDX}	Data Hold Time	0		ns
t_{ELLL}	Chip Enable Setup Time	7		ns
PW_{PL}	$\overline{PSEN}$ Pulse Width	150		ns
t_{PS}	$\overline{PSEN}$ Setup Time	30		ns
t_{PH}	$\overline{PSEN}$ Hold Time	20		ns
t_{PHDZ} (5)	$\overline{PSEN}$ Disable to Output in High Z		50	ns
t_{PLDX} (5)	$\overline{PSEN}$ to Output in Low Z	10		ns

6509 PGM T09

$\overline{PSEN}$ Controlled Read Timing Diagram



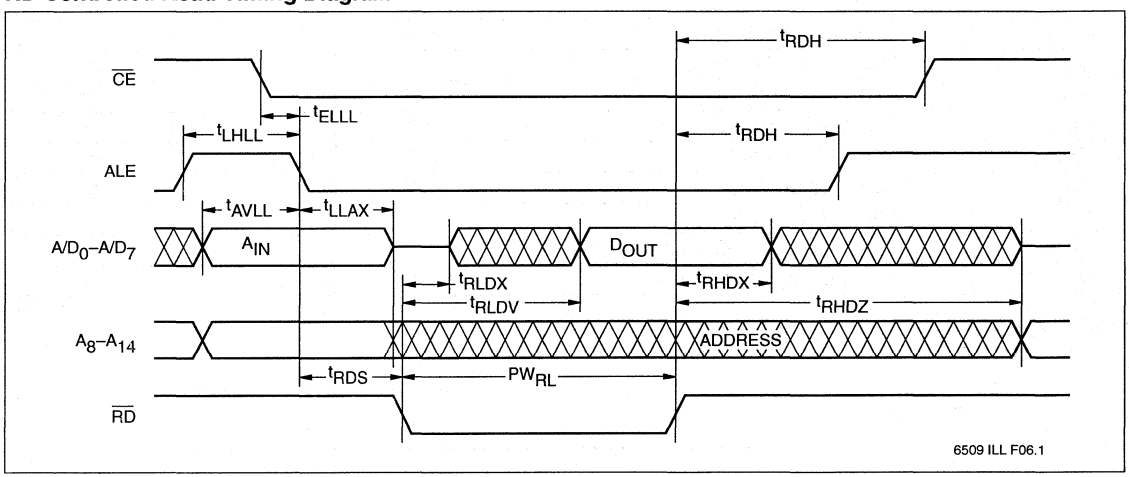
Note: (5) This parameter is periodically sampled and not 100% tested.

$\overline{RD}$ Controlled Read Cycle

Symbol	Parameter	Min.	Max.	Units
t_{LHLL}	ALE Pulse Width	80		ns
t_{AVLL}	Address Setup Time	20		ns
t_{LLAX}	Address Hold Time	30		ns
t_{RLDV}	$\overline{RD}$ Read Access Time		120	ns
t_{RHDX}	Data Hold Time	0		ns
t_{ELLL}	Chip Enable Setup Time	7		ns
PW_{RL}	$\overline{RD}$ Pulse Width	150		ns
t_{RDS}	$\overline{RD}$ Setup Time	30		ns
t_{RDH}	$\overline{RD}$ Hold Time	20		ns
t_{RHDZ} (6)	$\overline{RD}$ Disable to Output in High Z		50	ns
t_{RLDX} (6)	$\overline{RD}$ to Output in Low Z	0		ns

6509 PGM T10

$\overline{RD}$ Controlled Read Timing Diagram



Note: (6) This parameter is periodically sampled and not 100% tested.

SYMBOL TABLE

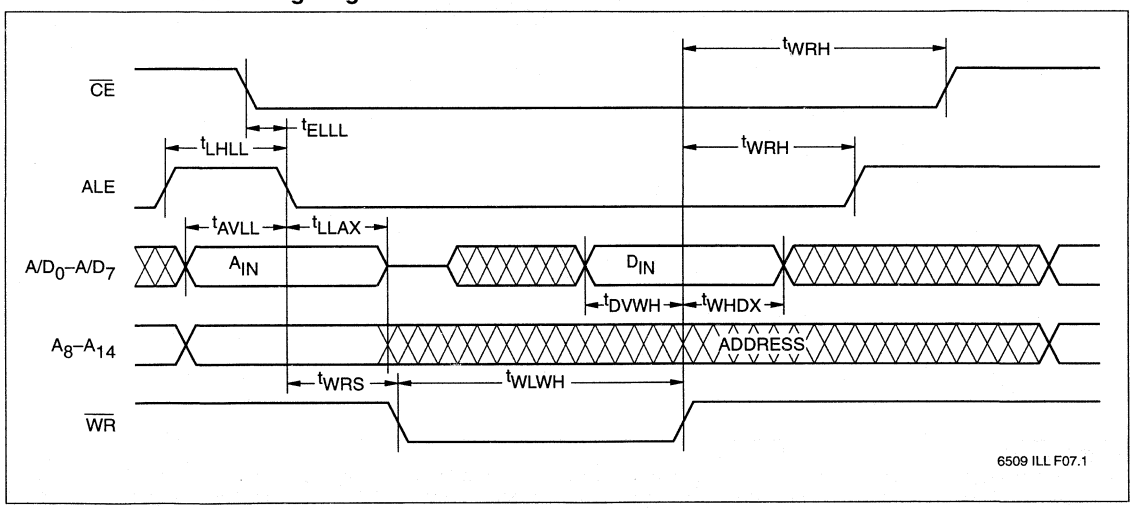
WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

$\overline{WR}$ Controlled Write Cycle

Symbol	Parameter	Min.	Max.	Units
t_{LHLL}	ALE Pulse Width	80		ns
t_{AVLL}	Address Setup Time	20		ns
t_{LLAX}	Address Hold Time	30		ns
t_{DVWH}	Data Setup Time	50		ns
t_{WHDX}	Data Hold Time	30		ns
t_{ELLL}	Chip Enable Setup Time	7		ns
t_{WLWH}	$\overline{WR}$ Pulse Width	120		ns
t_{WRS}	$\overline{WR}$ Setup Time	30		ns
t_{WRH}	$\overline{WR}$ Hold Time	20		ns
t_{BLC}	Byte Load Time (Page Write)	0.5	100	µs
t_{WC} (7)	Write Cycle Time		5	ms

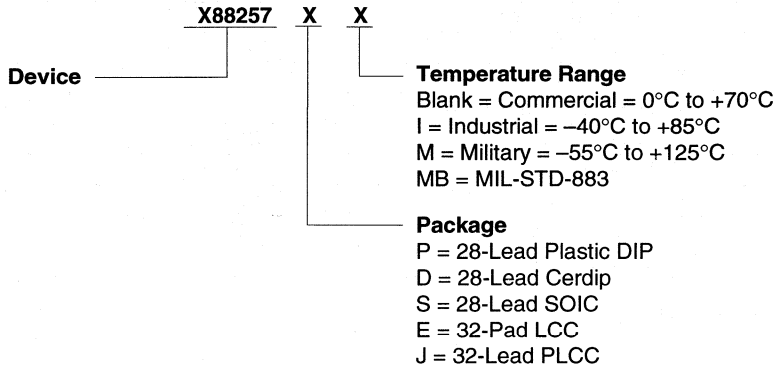
6509 PGM T11

$\overline{WR}$ Controlled Write Timing Diagram



Note: (7) t_{WC} is the minimum cycle time to be allowed from the system perspective unless polling techniques are used. It is the maximum time the device requires to automatically complete the internal write operation.

ORDERING INFORMATION



Xicor®

3807-2.3 12/4/95 T12/C0/D0 NS

High Speed AUTOSTORE™ NOVRAM

FEATURES

- High Speed: t_{AA} = 55ns
- NO Batteries!!
- Low Power CMOS
- AUTOSTORE™ NOVRAM
  - —Automatically Stores RAM data to E²PROM upon Power-fail Detection
- Open Drain AUTOSTORE Output Pin
  - —Provides Interrupt or Status Information
  - —Linkable to System Reset Circuitry
- Auto Recall
  - —Automatically Recalls E²PROM Data During Power-on
- Fully Decoded Module
- Full Military Temperature Range
  - — –55°C to +125°C
- High Reliability
  - —Endurance: 1,000,000 Nonvolatile Store Cycles
  - —Data Retention: 100 Years
- ESD Protection
  - —≥2KV All Pins
- Also Available in 66 Pin PUMA Package

DESCRIPTION

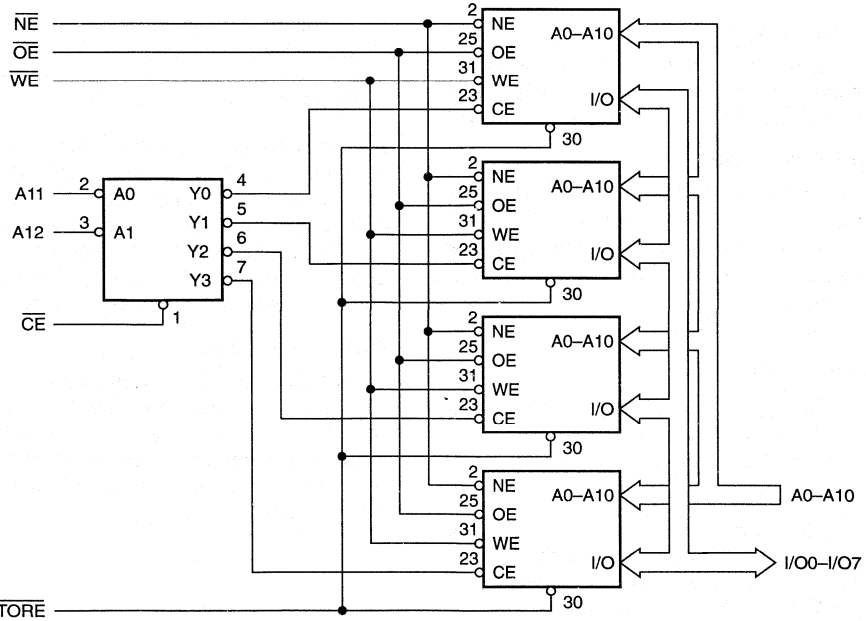
The XM20C64 is a high speed nonvolatile RAM Module. It is comprised of four Xicor X20C16 high speed NOVRAMs, a high speed decoder and decoupling capacitors mounted on a co-fired multilayered Ceramic substrate. The XM20C64 is configured 8K x 8 and is fully decoded. The module is a 28-lead DIP conforming to the industry standard pinout for SRAMs.

The XM20C64 fully supports the AUTOSTORE feature, providing hands-off automatic storing of RAM data into E²PROM when V_{CC} falls below the AUTOSTORE threshold.

The XM20C64 is a highly reliable memory component, supporting unlimited writes to RAM, a minimum 1,000,000 store cycles and a minimum 100 year data retention.

6

FUNCTIONAL DIAGRAM



3874 FHD F01

AUTOSTORE™ NOVRAM is a trademark of Xicor, Inc.

3874-1.3 6/1/95 T4/C2/D16 TD

PIN DESCRIPTIONS

Addresses (A_0-A_{12})

The address inputs select an 8-bit memory location during read and write operations.

Chip Enable ($\overline{CE}$)

The chip enable input must be LOW to enable all read, write and user requested nonvolatile operations.

Output Enable ($\overline{OE}$)

During normal RAM operations $\overline{OE}$ controls the data output buffers. If a hardware nonvolatile operation is selected ($\overline{NE}$ = $\overline{CE}$ = LOW) and $\overline{OE}$ strobes LOW, a recall operation will be initiated.

$\overline{OE}$ LOW will always disable a STORE operation regardless of the state of $\overline{NE}$, $\overline{WE}$, and $\overline{CE}$ so long as the internal transfer has not commenced.

Write Enable ($\overline{WE}$)

During normal RAM operations $\overline{WE}$ = $\overline{CE}$ = LOW will cause data to be written to the RAM address pointed to by the A_0-A_{12} inputs.

Nonvolatile Enable ($\overline{NE}$)

The nonvolatile input controls the transfer of data from the E²PROM array to the RAM array, when strobed LOW in conjunction with $\overline{CE}$ = $\overline{OE}$ = LOW.

Data In/Data Out (I/O_0-I/O_7)

Data is written to or read from the X20C64 through the I/O pins. The I/O pins are placed in the high impedance state when either $\overline{CE}$ or $\overline{OE}$ is HIGH or when $\overline{NE}$ is LOW.

AUTOSTORE Output ($\overline{AS}$)

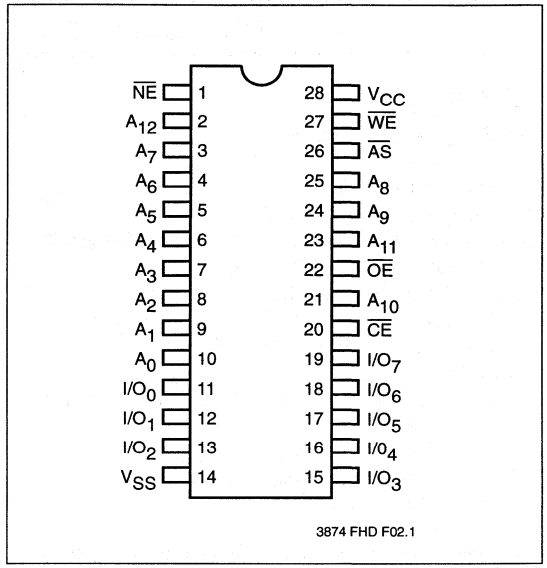
$\overline{AS}$ is an open-drain output. When it is asserted (driving LOW) it indicates V_{CC} has fallen below the AUTOSTORE threshold and an internal store operation has been initiated. Because $\overline{AS}$ is an open drain output it may be wire-ORed with multiple open drain outputs and used as an interrupt input to a microprocessor.

DEVICE OPERATION

NOVRAM operations are identical to those of a standard SRAM. When $\overline{OE}$ and $\overline{CE}$ are asserted data is presented at the I/Os from the address location pointed to by the A_0–A_{12} inputs.

RAM write operations are initiated and the address input is latched by the HIGH to LOW transition of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. Data is latched on the rising edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs first.

PIN CONFIGURATION



An array recall, E²PROM data transferred to RAM, is initiated whenever $\overline{OE}$ = $\overline{NE}$ = $\overline{CE}$ = LOW. A recall is also performed automatically upon power-up.

Command Sequence Operations

The X20C64 employs a version of the industry standard Software Data Protection (SDP). The end user can select various options for transferring data from RAM into the E²PROM array.

All command sequences are comprised of three specific data/address write operations performed with $\overline{NE}$ LOW. A Store operation can be directly selected by issuing a Store command. The user may also enable and disable the AUTOSTORE function through the software data protection sequence. Refer to Table 1 below for a complete description of the command sequence.

Operational Notes

The X20C64 should be viewed as a subsystem when writing software for the various store operations. The module contains four discrete components each needing to be set to the required state individually. The two high order address bits (A_{11} and A_{12}) select only one of the four components.

TABLE 1

Step	Operation	A_0–A_{10}*	Data Pattern
1	Write	555	AA
2	Write	2AA	55
3	Write	555	Command

3874 PGM T11

* It should be noted, the high order addresses should remain stable during the operations. It should also be noted that these commands are not global, that is only one device on the module will be affected by each command operation.

TABLE 2

Command	Function
CC[H]	Enable Autostore
CD[H]	Disable Autostore
33[H]	Store Operation

3874 PGM T12.2

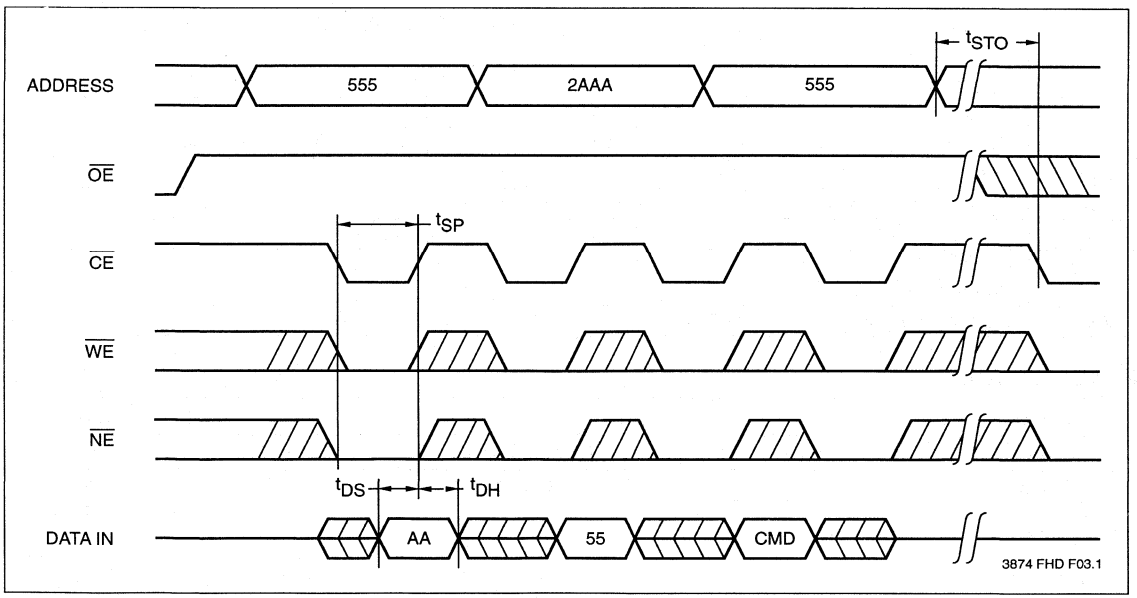
Command Sequence Timing Limits

Symbol	Parameter	Limits		Units
		Min.	Max.	
t_{STO}	Store Time		5	ms
t_{SP}	Command Write Pulse Width	50		ns
t_{SPH}	Inter Command Delay	55		ns

Note: All Write Command Sequence timings must conform to the standard write timing requirements.

3874 PGM T01.1

Command Sequence



3874 FHD F03.1

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ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... –65°C to +125°C
Storage Temperature ..... –65°C to +125°C
Voltage on any Pin with
Respect to V_{SS} ..... –1V to +7V
Lead Temperature
(Soldering, 10 seconds) ..... 300°C

***COMMENT**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the module. This is a stress rating only and the functional operation of the module at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect module reliability.

RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Military	–55°C	+125°C

3874 PGM T06

Supply Voltage	Limits
XM20C64	5V ±10%

3874 PGM T07

D.C. OPERATING CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits			Test Conditions
		Min.	Max.	Units	
I_{CC1}	V_{CC} Active Current		100	mA	$\overline{NE} = \overline{WE} + V_{IH}$, $\overline{CE} = \overline{OE} = V_{IL}$, Address Inputs = TTL Inputs @ f = 20MHz All I/Os = Open
I_{CC2}	V_{CC} Active Current (AUTOSTORE)		10	mA	All Inputs = V_{IH}, All I/Os = Open
I_{SB}	V_{CC} Standby Current		1.5	mA	All Inputs = V_{CC}–0.3V All I/Os = Open
I_{LI}	Input Leakage Current		10	µA	$V_{IN} = V_{SS}$ to V_{CC}
I_{LO}	Output Leakage Current		10	µA	$V_{IN} = V_{SS}$ to V_{CC}, $\overline{CE} = V_{IH}$
V_{IL}(1)	Input LOW Voltage	–0.5	0.8	V	
V_{IH}(1)	Input HIGH Voltage	2	V_{CC} + 0.5	V	
V_{OL}	Output LOW Voltage		0.4	V	I_{OL} = 5mA
V_{OLAS}	AUTOSTORE Output Voltage		0.4	V	I_{OLAS} = 1mA
V_{OH}	Output HIGH Voltage	2.4		V	I_{OH} = –4mA

3874 PGM T08.2

POWER-UP TIMING

Symbol	Parameter	Max.	Units
t_{PUR}	Power-Up (V_{CC} Min.) to RAM Operation	500	µs
t_{PUST}	Power-Up (V_{CC} Min.) to Store Operation	5	ms

3874 PGM T09

CAPACITANCE T_A = +25°C, f = 1MHz, V_{CC} = 5V.

Symbol	Test	Max.	Units	Conditions
$C_{I/O}$(2)	Input/Output Capacitance	40	pF	$V_{I/O}$ = 0V
C_{IN}(2)	Input Capacitance	24	pF	V_{IN} = 0V

3874 PGM T10.1

Notes: (1) V_{IL} min. and V_{IH} max. are for reference only and are not tested.
(2) This parameter is periodically sampled and not 100% tested.

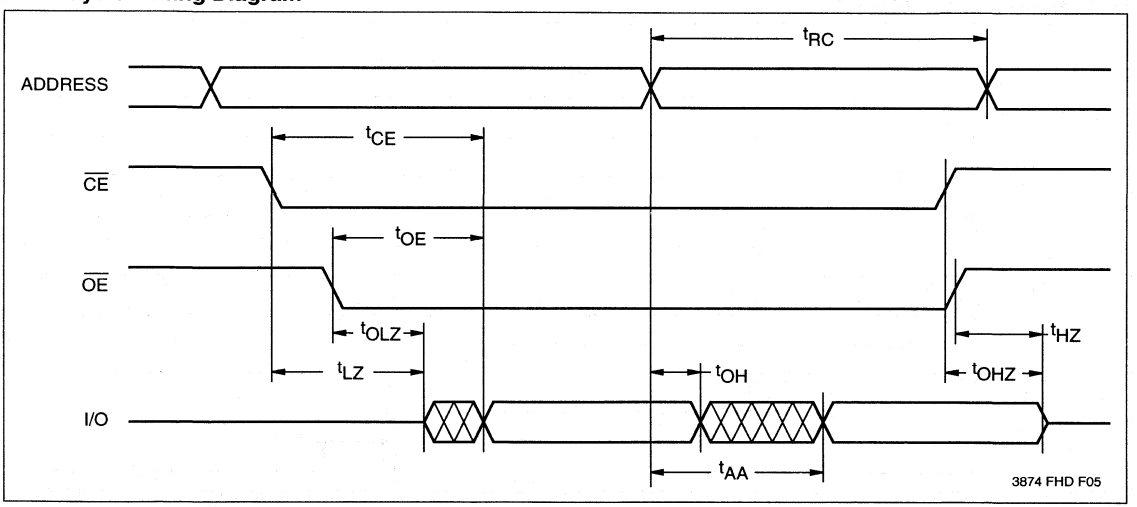
A.C. CHARACTERISTICS (Over the recommended operating conditions unless otherwise specified)

Read Cycle Limits

Symbol	Parameter	Limits		Units
		Min.	Max.	
t_{RC}	Read Cycle Time	55		ns
t_{CE}	Chip Enable Access Time		55	ns
t_{AA}	Address Access Time		55	ns
t_{OE}	Output Enable Access Time		30	ns
t_{LZ}(3)	$\overline{CE}$ Low to Output in Low Z	0		ns
t_{OLZ}(3)	$\overline{OE}$ Low to Output in Low Z	0		ns
t_{HZ}(3)	$\overline{CE}$ High to Output in Low Z	0	25	ns
t_{OHZ}(3)	$\overline{OE}$ High to Output in Low Z	0	25	ns
t_{OH}	Output Hold	0		ns

3874 PGM T03

Read Cycle Timing Diagram



Note: (3) t_{LZ} min., t_{HZ} min., t_{OLZ} min., and t_{OHZ} min. are periodically sampled and not 100% tested. t_{HZ} max. and t_{OHZ} max. are measured from the point when $\overline{CE}$ or $\overline{OE}$ return high (whichever occurs first) to the time when the outputs are no longer driven.

MODE SELECTION

$\overline{CE}$	$\overline{WE}$	$\overline{NE}$	$\overline{OE}$	Mode	I/O State	Power
H	X	X	X	Module Not Selected	High Z	Standby
L	H	H	L	Read RAM Active	Data Output	Active
L	L	H	X	Write RAM	Data Input	Active
L	L	L	H	Issue Software Command	Data Input	Active
L	H	H	H	Output Disabled	High Z	Active
L	H	L	L	Hardware Array Recall	High Z	Active
L	H	L	H	No Operation	High Z	Active
L	L	L	L	Not Allowed	High Z	Active

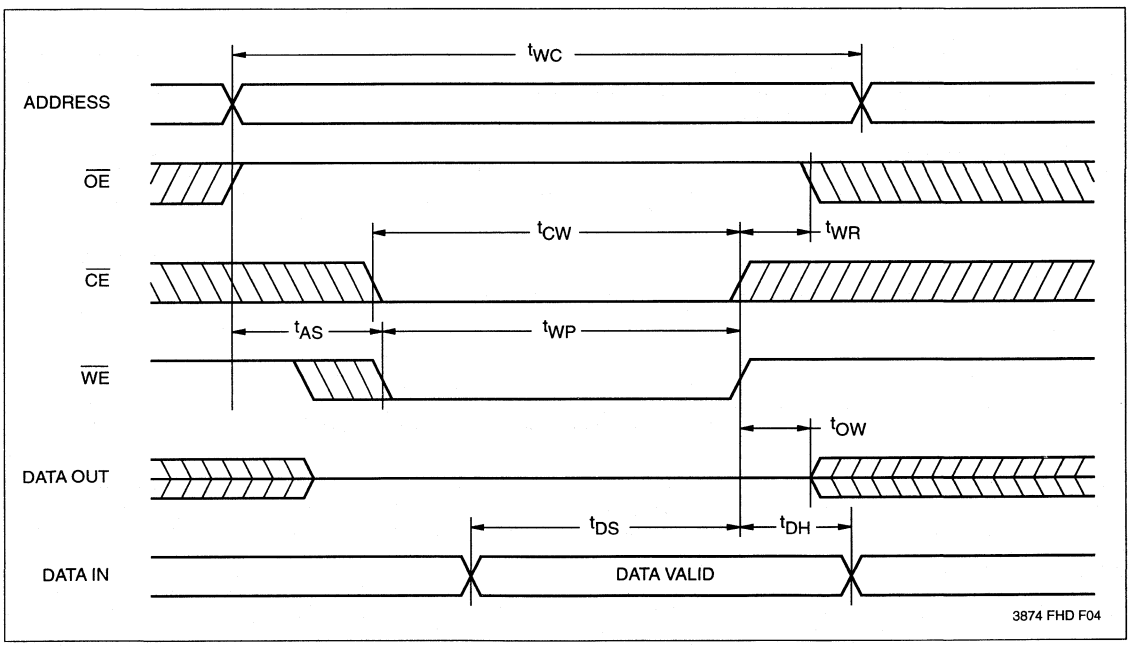
3874 PGM T04.1

Write Cycle Limits

Symbol	Parameter	Limits		Units
		Min.	Max.	
t_{WC}	Write Cycle time	55		ns
t_{WP}	$\overline{WE}$ Pulse Width	40		ns
t_{CW}	$\overline{CE}$ Pulse Width	40		ns
t_{AS}	Address Setup	0		ns
t_{DS}	Data Setup	25		ns
t_{DH}	Data Hold	0		ns
t_{OW}	Output Active from End of Write		5	ns
t_{WR}	End of Write to Read	0		ns

3874 PGM T02

Write Cycle Timing Diagram



3874 FHD F04

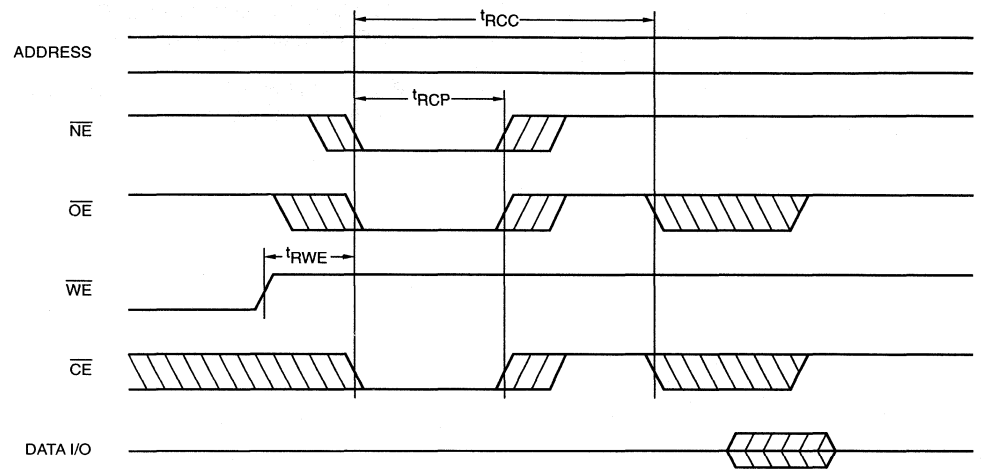
Array Recall Timing

Symbol	Parameter	Limits		Units
		Min.	Max.	
t_{RCC}	Array Recall Time		10	µs
t_{RCP}	Recall Strobe Pulse Width	50		ns
t_{RWE}	Delay From $\overline{WE}$ HIGH to Recall	0		ns

3874 PGM T05.1

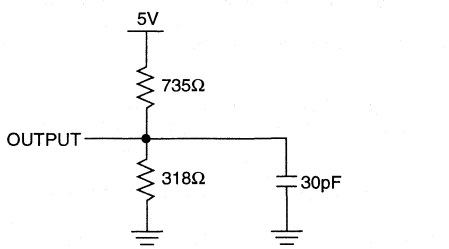
Note: The recall sequence must be repeated for each memory component individually. This is accomplished by sequencing through the Array Recall Cycle with all four combinations of A_{11}, and A_{12}.

Array Recall Cycle



3874 FHD F06.1

EQUIVALENT TEST LOAD CIRCUIT

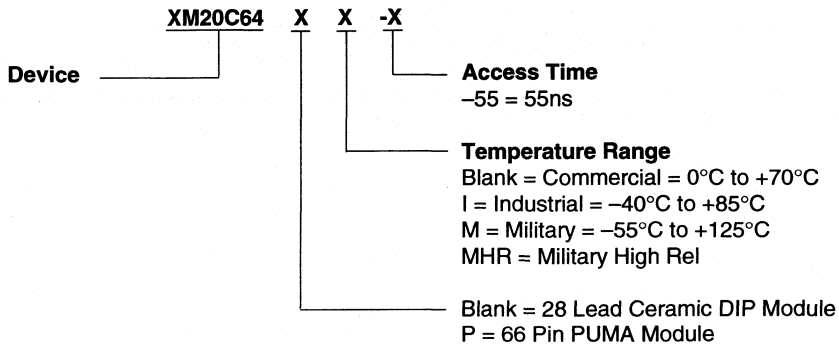


3874 FHD F07.2

SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

ORDERING INFORMATION
XM20C64: 2K X 8 CMOS NOVRAM Memory Module



High Speed 5 Volt Byte Alterable Nonvolatile Memory Array

FEATURES

- **High Speed, High Density Memory Module**
  - **—150ns, 120ns, 90ns and 70ns Access Times Available**
  - **—1 Megabit Memory in 1 square inch.**
- **Flexible Multiplane Architecture**
  - **—Four Separate Chip Selects**
  - **—32 Separate I/Os**
    - **User Configurable I/Os—x8, x16, or x32**
    - **User Configurable Page Size—64 Double-words, 128 Words, or 256 Bytes**
  - **—Concurrent Read/Write Operations**
    - **Able to Continue Reading During a Nonvolatile Write Cycle.**
- **5 Volt Byte or Page Alterable**
  - **—No Erase Before Write**
- **Software Data Protection**
- **Early End of Write Polling**
  - **—$\overline{\text{DATA}}$ Polling**
  - **—Toggle Bit Polling**
- **High Reliability**
  - **—Endurance: 100,000 Cycles**
  - **—Data Retention: 100 Years**

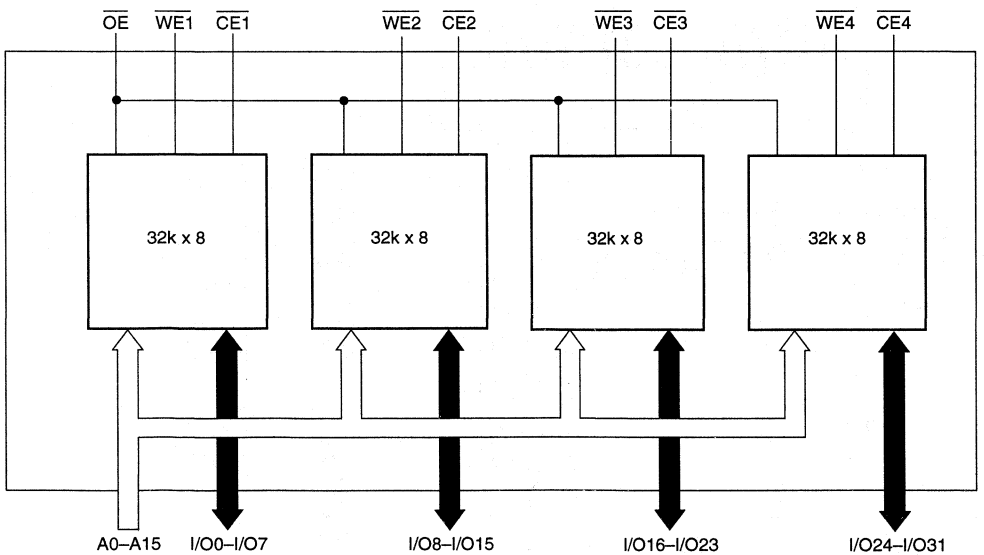
DESCRIPTION

The XM28C010P is a high speed, high density CMOS byte alterable nonvolatile memory array constructed on a co-fired ceramic substrate using Xicor's High Speed 32K x 8 components in 32-pad leadless chip carriers. The Substrate is a 66-pin ceramic pin grid array.

The module is configured with four separate chip enable and write enable inputs and 32 separate I/Os. This, along with the small footprint, provides the end user with a large degree of flexibility in board layout and memory configuration. In addition, with the large number of pins and the growth path being implemented, the module will be able to grow to 16 megabits.

6

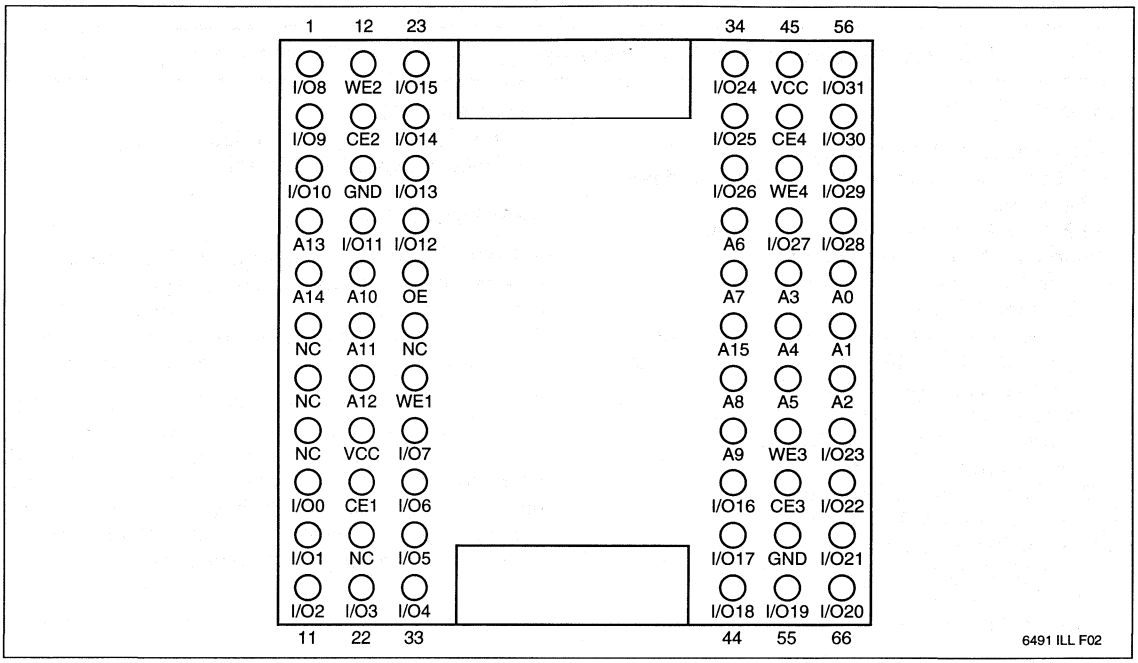
FUNCTIONAL DIAGRAM



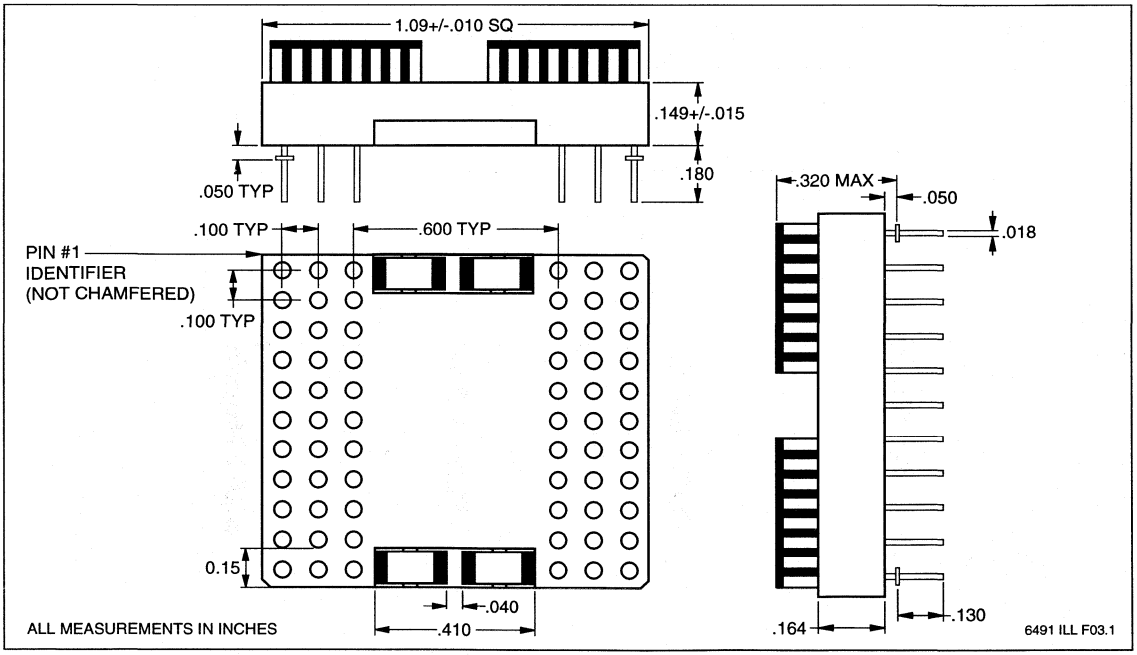
6491 ILL F01

6491-1.2 6/1/95 T5/C1/D0 TD

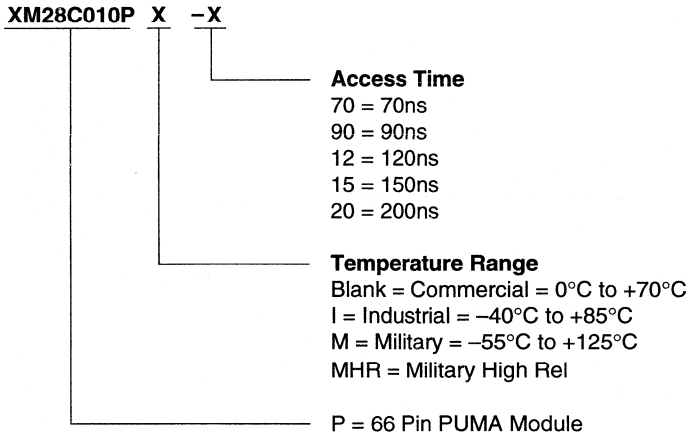
PIN CONFIGURATION



PACKAGE INFORMATION



ORDERING INFORMATION



6

NOTES

5 Volt, Byte Alterable E²PROM

TYPICAL FEATURES

- High Density 2 Megabit (256K x 8) Module
- Access Time of 200ns at –55°C to +125°C
- Base Memory Component: Xicor X28C513
- Pinout conforms to JEDEC Standard for 2 Megabit E²PROM
- Fast Write Cycle Times
  - —128 Byte Page Write
  - —Byte or Page Write Cycle: 5ms Typical
  - —Complete Memory Rewrite: 10 Seconds
- Early End of Write Detection
  - —$\overline{\text{DATA}}$ Polling
  - —Toggle Bit Polling
- Software Data Protection
- Three Temperature Ranges
  - —Commercial: 0°C to +75°C
  - —Industrial: –40° to +85°C
  - —Military: –55° to +125°C
- High Rel Module
  - —100% MIL-STD-883 Compliant Components

DESCRIPTION

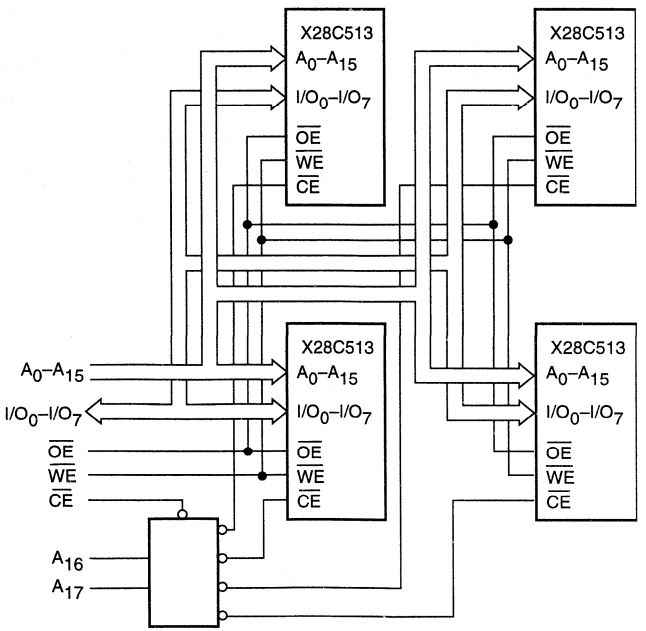
The XM28C020 is a high density 2 Megabit E²PROM comprised of four X28C513 LCCs mounted on a co-fired multilayered ceramic substrate. Individual components are 100% tested prior to assembly in module form and then 100% tested after assembly.

The XM28C020 is configured 256K x 8 bit. The module supports a 128-byte page write operation. This combined with $\overline{\text{DATA}}$ Polling or Toggle Bit Polling, effectively provides a 39µs/byte write cycle, enabling the entire array to be rewritten in 10 seconds.

The XM28C020 provides the same high endurance and data retention as the X28C513.

6

FUNCTIONAL DIAGRAM



3872 FHD F01

PIN DESCRIPTIONS

Addresses (A_0–A_{17})

The Address inputs select an 8-bit memory location during a read or write operation.

Chip Enable ($\overline{CE}$)

The Chip Enable input must be LOW to enable all read/write operations. When $\overline{CE}$ is HIGH, power consumption is reduced (see Note 4).

Output Enable ($\overline{OE}$)

The Output Enable input controls the data output buffers and is used to initiate read operations.

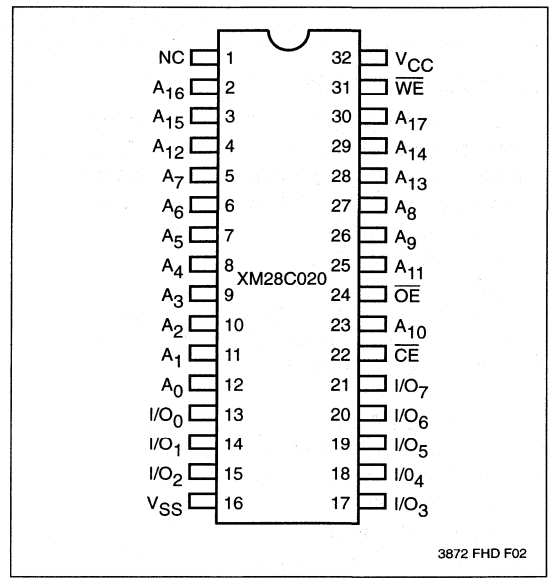
Data In/Data Out (I/O_0–I/O_7)

Data is written to or read from the XM28C020 through the I/O pins.

Write Enable ($\overline{WE}$)

The Write Enable input controls the writing of data to the XM28C020.

PIN CONFIGURATION



PIN NAMES

Symbol	Description
A_0–A_{17}	Address Inputs
I/O_0–I/O_7	Data Input/Output
$\overline{WE}$	Write Enable
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
V_{CC}	+5V
V_{SS}	Ground
NC	No Connect

3872 PGM T01

DEVICE OPERATION

Read

Read operations are initiated by both $\overline{OE}$ and $\overline{CE}$ LOW. The read operation is terminated by either $\overline{CE}$ or $\overline{OE}$ returning HIGH. This 2-line control architecture eliminates bus contention in a system environment. The data bus will be in a high impedance state when either $\overline{OE}$ or $\overline{CE}$ is HIGH.

Write

Write operations are initiated when both $\overline{CE}$ and $\overline{WE}$ are LOW and $\overline{OE}$ is HIGH. The XM28C020 supports both a $\overline{CE}$ and $\overline{WE}$ controlled write cycle. That is, the address is latched by the falling edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs last. Similarly, the data is latched internally by the rising edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs first. A byte write operation, once initiated, will automatically continue to completion, typically within 5ms (see Note 4).

Page Write Operation

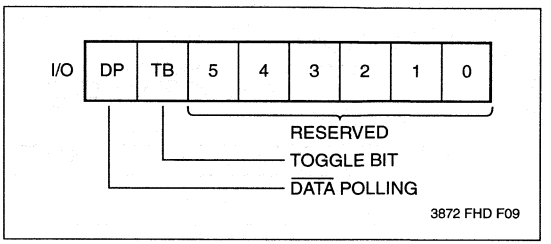
The page write feature of the XM28C020 allows the entire memory to be written in 10 seconds. Page write allows two to 128 bytes of data to be consecutively written to the XM28C020 prior to the commencement of the internal programming cycle. The host can fetch data from another device within the system during a page write operation (change the source address), but the page address (A_7 through A_{17}) for each subsequent valid write cycle to the part during this operation must be the same as the initial page address.

The page write mode can be initiated during any write operation. Following the initial byte write cycle, the host can write an additional one to 127 bytes in the same manner as the first byte was written. Each successive byte load cycle, started by the $\overline{WE}$ HIGH to LOW transition, must begin within 100µs of the falling edge of the preceding $\overline{WE}$. If a subsequent $\overline{WE}$ HIGH to LOW transition is not detected within 100µs, the internal automatic programming cycle will commence. There is no page write window limitation. Effectively the page write window is infinitely wide, so long as the host continues to access the device within the byte load cycle time of 100µs.

Write Operation Status Bits

The XM28C020 provides the user two write operation status bits. These can be used to optimize a system write cycle time. The status bits are mapped onto the I/O bus as shown in Figure 1.

Figure 1. Status Bit Assignment



$\overline{DATA}$ Polling (I/O_7)

The XM28C020 features $\overline{DATA}$ Polling as a method to indicate to the host system that the byte write or page write cycle has completed. $\overline{DATA}$ Polling allows a simple bit test operation to determine the status of the XM28C020, eliminating additional interrupt inputs or external hardware. During the internal programming cycle, any attempt to read the last byte written will produce the complement of that data on I/O_7 (i.e., write data = 0xxx xxxx, read data = 1xxx xxxx). Once the programming cycle is complete, I/O_7 will reflect true data. Note: If the XM28C020 is in the protected state and an illegal write operation is attempted, $\overline{DATA}$ Polling will not operate.

Toggle Bit (I/O_6)

The XM28C020 also provides another method for determining when the internal write cycle is complete. During the internal programming cycle I/O_6 will toggle from "1" to "0" and "0" to "1" on subsequent attempts to read the last byte written. When the internal cycle is complete the toggling will cease and the device will be accessible for additional read or write operations.

$\overline{\text{DATA}}$ POLLING I/O_7

Figure 2. $\overline{\text{DATA}}$ Polling Bus Sequence

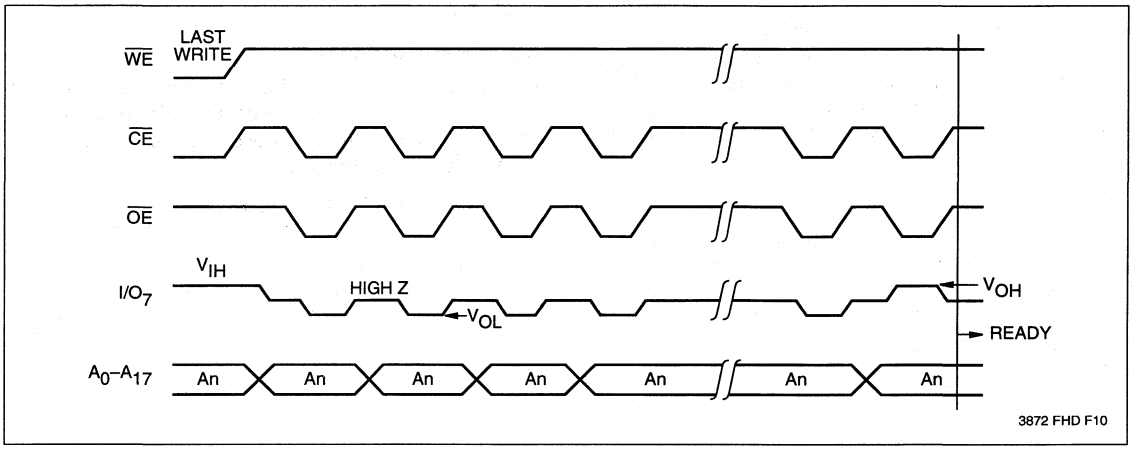
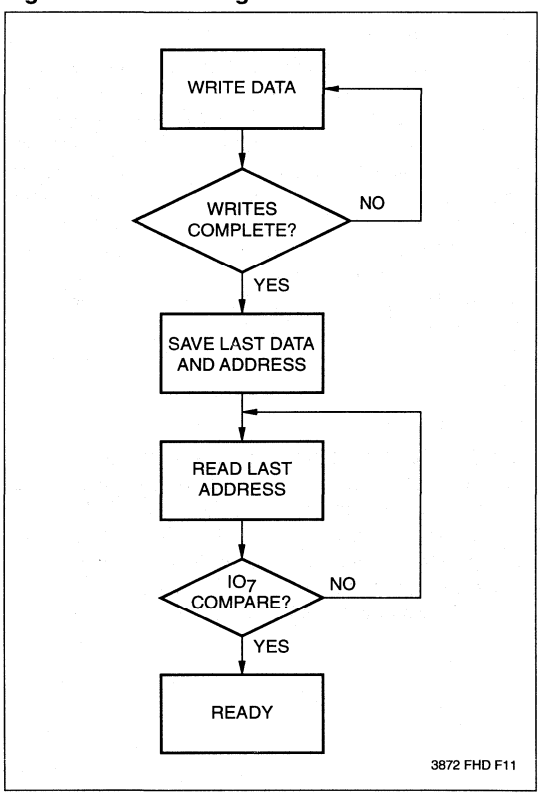


Figure 3. $\overline{\text{DATA}}$ Polling Software Flow



$\overline{\text{DATA}}$ Polling can effectively halve the time for writing to the XM28C020. The timing diagram in Figure 2 illustrates the sequence of events on the bus. The software flow diagram in Figure 3 illustrates one method of implementing the routine.

THE TOGGLE BIT I/O_6

Figure 4. Toggle Bit Bus Sequence

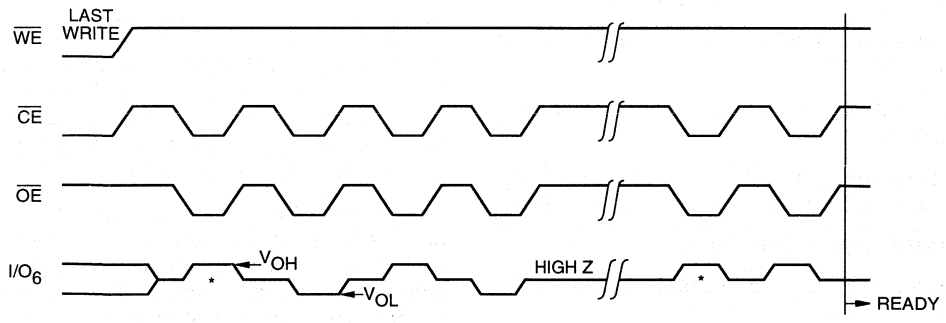
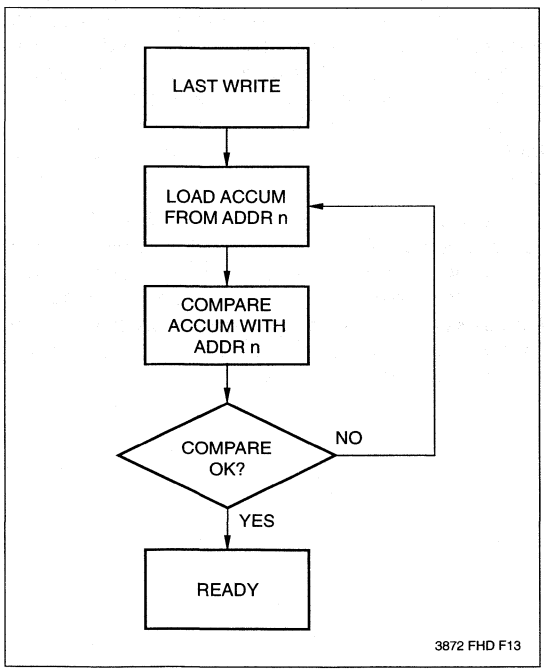


Figure 5. Toggle Bit Software Flow



The Toggle Bit can eliminate the software housekeeping chore of saving and fetching the last address and data written to a device in order to implement $\overline{DATA}$ Polling. This can be especially helpful in an array comprised of multiple XM28C020 memories that is frequently updated. The timing diagram in Figure 4 illustrates the sequence of events on the bus. The software flow diagram in Figure 5 illustrates a method for testing the Toggle Bit.

6

HARDWARE DATA PROTECTION

The XM28C020 provides three hardware features that protect nonvolatile data from inadvertent writes.

- Noise Protection—A $\overline{WE}$ pulse less than 10ns will not initiate a write cycle.
- Default V_{CC} Sense—All functions are inhibited when V_{CC} is ≤ 3V.
- Write Inhibit—Holding $\overline{OE}$ LOW will prevent an inadvertent write cycle during power-up and power-down.

SOFTWARE DATA PROTECTION

The XM28C020 does provide the Software Data Protection (SDP) feature.

The module is shipped from Xicor with the Software Data Protection NOT ENABLED; that is, the module will be in the standard operating mode. In this mode, data should be protected during power-up/-down operations through the use of external circuits. The host system will then have open read and write access of the module once V_{CC} is stable.

The module can be automatically protected during power-up/-down without the need for external circuits by employing the SDP feature. The internal SDP circuit is enabled after the first write operation utilizing the SDP command sequence.

When this feature is employed, it will be easiest to incorporate in the system software if the module is viewed as a subsystem composed of four discrete memory devices with an address decoder (see Functional Diagram). In this manner, system memory mapping will extend onto the module. That is, the discrete memory ICs and decoder should be considered memory board components and SDP can be implemented at the component level as described in the next section.

SOFTWARE COMMAND SEQUENCE

A_{16} and A_{17} are used by the decoder to select one of the four LCCs. Therefore, only one of the four memory devices can be accessed at one time. In order to protect the entire module, the command sequence must be issued separately to each device.

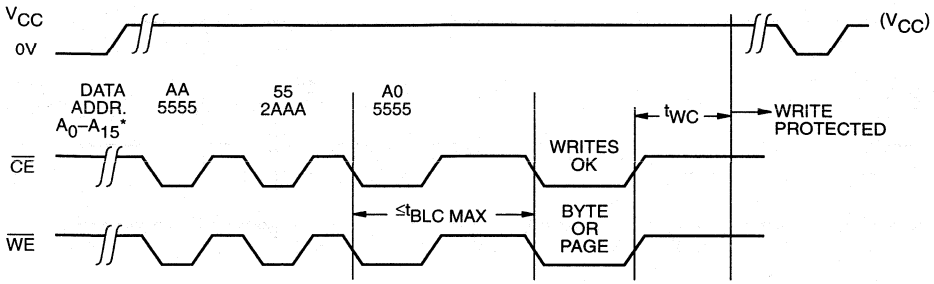
Enabling the software data protection mode requires the host system to issue a series of three write operations: each write operation must conform to the data and address sequence illustrated in Figures 6 and 7. Because this involves writing to a nonvolatile bit, the device will become protected after t_{WC} has elapsed. After this point in time devices will inhibit inadvertent write operations.

Once in the protected mode, authorized writes may be performed by issuing the same command sequence that enables SDP, immediately followed by the address/data combination desired. The command sequence opens the page write window enabling the host to write from one to 128 bytes of data. Once the data has been written, the device will automatically be returned to the protected state.

In order to facilitate testing of the devices the SDP mode can be deactivated. This is accomplished by issuing a series of six write operations: each write operation must conform to the data and address sequence illustrated in Figures 8 and 9. This is a nonvolatile operation, and the host will have to wait a minimum t_{WC} before attempting to write new data.

SOFTWARE DATA PROTECTION

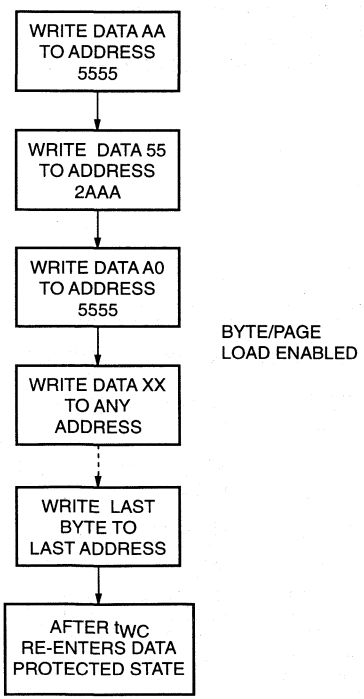
Figure 6. Timing Sequence—Byte or Page Write



*A_{16} & A_{17} select one of four devices on the module.

3872 FHD F14

Figure 7. Write Sequence for Software Data Protection



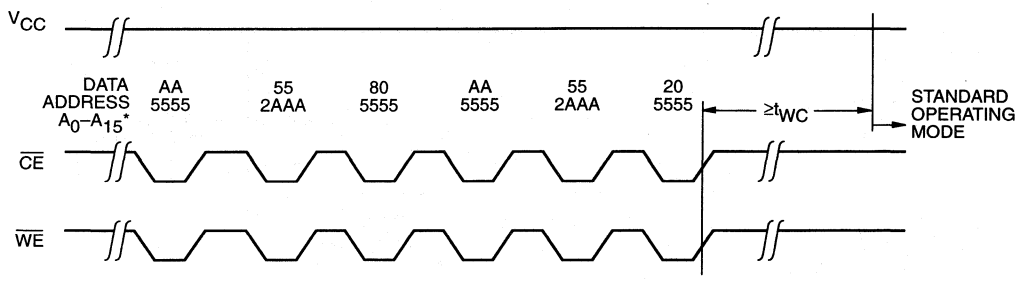
3872 FHD F15

Regardless of whether the device has previously been protected or not, once the software data protected algorithm is used and data has been written, the device will automatically disable further writes unless another command is issued to cancel it. If no further commands are issued the device will be write protected during power-down and after any subsequent power-up.

6

RESETTING SOFTWARE DATA PROTECTION

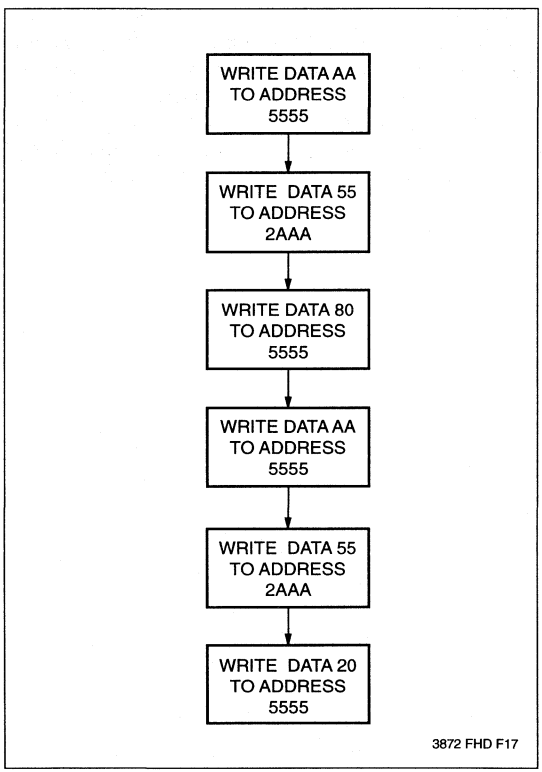
Figure 8. Reset Software Data Protection Timing Sequence



*A_{16} & A_{17} select one of four devices on the module.

3872 FHD F16

Figure 9. Software Sequence to Deactivate Software Data Protection



3872 FHD F17

In the event the user wants to deactivate the software data protection feature for testing or reprogramming in an E^2PROM programmer, the following six step algorithm will reset the internal protection circuit. After t_{WC}, the device will be in standard operating mode.

SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

SYSTEM CONSIDERATIONS

Because the XM28C020 is frequently used in large memory arrays it is provided with a two line control architecture for both read and write operations. Proper usage can provide the lowest possible power dissipation and eliminate the possibility of contention where multiple I/O pins share the same bus.

To gain the most benefit it is recommended that $\overline{CE}$ be decoded from the address bus and be used as the primary device selection input. Both $\overline{OE}$ and $\overline{WE}$ would then be common among all devices in the array. For a read operation this assures that all deselected devices are in their standby mode and that only the selected device(s) is outputting data on the bus.

Because the XM28C020 has two power modes, standby and active, proper decoupling of the memory array is of prime concern. Enabling $\overline{CE}$ will cause transient current spikes. The magnitude of these spikes is dependent on the output capacitive loading of the I/Os. Therefore, the larger the array sharing a common bus, the larger the transient spikes. The voltage peaks associated with the current transients can be suppressed by the proper selection and placement of decoupling capacitors. As a minimum, it is recommended that a 0.1μF high frequency ceramic capacitor be used between V_{CC} and V_{SS} at each device. Depending on the size of the array, the value of the capacitor may have to be larger.

In addition, it is recommended that a 4.7μF electrolytic bulk capacitor be place between V_{CC} and V_{SS} for every two modules employed in the array. This bulk capacitor is employed to overcome the voltage droop caused by the inductive effects of the PC board traces.

ABSOLUTE MAXIMUM RATINGS*

Temperature under Bias ..... –65°C to +135°C
Storage Temperature ..... –65°C to +150°C
Voltage on any Pin with
Respect to V_{SS} ..... –1V to +7V
D.C. Output Current 5mA
Lead Temperature
(Soldering, 10 seconds) ..... 300°C

***COMMENT**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. OPERATING CHARACTERISTICS

XM28C020 T_A = 0°C to +70°C, V_{CC} = +5V ±10%, unless otherwise specified.
XM28C020I T_A = –40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.
XM28C020M T_A = –55°C to +125°C, V_{CC} = +5V ±10%, unless otherwise specified.

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
I_{CC}	V_{CC} Current (Active) (TTL Inputs)		100	mA	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}, All I/O's = Open, 1 Device Active Address Inputs = TTL Levels @ f = 5MHz
I_{SB1}	V_{CC} Current (Standby) (TTL Inputs)		25	mA	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IL} All I/O's = Open, Other Inputs = V_{IH}
I_{SB2}	V_{CC} Current (Standby) (CMOS Inputs)		5	mA	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IL} All I/O's = Open, Other Inputs = V_{CC}
I_{LI}	Input Leakage Current		20	µA	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output Leakage Current		20	µA	V_{OUT} = V_{SS} to V_{CC}, $\overline{CE}$ = V_{IH}
V_{IL}	Input LOW Voltage	–1	0.8	V	
V_{IH}	Input HIGH Voltage	2	V_{CC} + 1	V	
V_{OL}	Output LOW Voltage		0.4	V	I_{OL} = 2.1mA
V_{OH}	Output HIGH Voltage	2.4		V	I_{OH} = –400µA

3856 PGM T02.2

POWER-UP TIMING

Symbol	Parameter	Typ.(1)	Units
t_{PUR}(2)	Power-up to Initiation of Read Operation	100	µs
t_{PUW}(2)	Power-up to Initiation of Write Operation	5	ms

3872 PGM T03

CAPACITANCE T_A = +25°C, f = 1MHz, V_{CC} = 5V

Symbol	Parameter	Max.	Units	Test Conditions
$C_{I/O}$(2)	Input/Output Capacitance	50	pF	$V_{I/O}$ = 0V
C_{IN}(2)	Input Capacitance	50	pF	V_{IN} = 0V

3872 PGM T04.1

Notes: (1) Typical values are for T_A = 25°C and nominal supply voltage.
(2) This parameter is periodically sampled and not 100% tested.

A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3V
Input Rise and Fall Times	10ns
Input and Output Timing Levels	1.5V
Output Load	1 TTL Gate and C_L = 100pF

3872 PGM T05.1

MODE SELECTION

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O	Power
L	L	H	Read	D_{OUT}	Active
L	H	L	Write	D_{IN}	Active
H	X	X	Standby and Write Inhibit	High Z	Standby
X	L	X	Write Inhibit	—	—
X	X	H	Write Inhibit	—	—

3872 PGM T06

A.C. CHARACTERISTICS

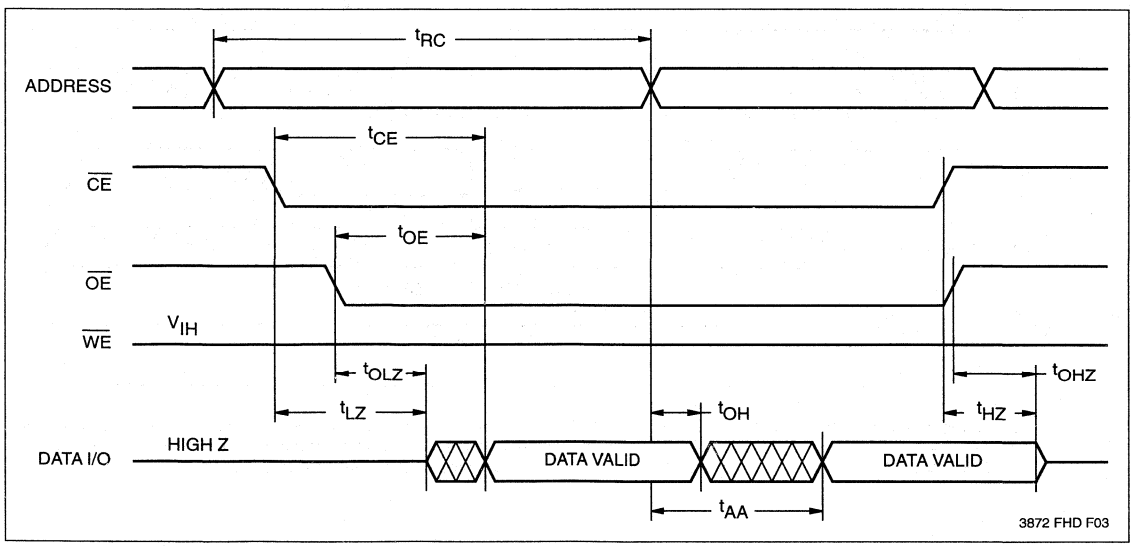
XM28C020 T_A = 0°C to +75°C, V_{CC} = +5V ±10%, unless otherwise specified.
XM28C020I T_A = –40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.
XM28C020M T_A = –55°C to +125°C, V_{CC} = +5V ±10%, unless otherwise specified.

Read Cycle Limits

Symbol	Parameter	XM28C020-20		XM28C020-25		XM28C020		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	200		250		300		ns
t_{CE}	Chip Enable Access Time		200		250		300	ns
t_{AA}	Address Access Time		200		250		300	ns
t_{OE}	Output Enable Access Time		80		100		100	ns
t_{LZ}(3)	$\overline{CE}$ Low to Active Output	0		0		0		ns
t_{OLZ}(3)	$\overline{OE}$ Low to Active Output	0		0		0		ns
t_{HZ}(4)	$\overline{CE}$ High to High Z Output		100		100		100	ns
t_{OHZ}(4)	$\overline{OE}$ High to High Z Output		100		100		100	ns
t_{OH}	Output Hold From Address Change	0		0		0		ns

3872 PGM T07

Read Cycle



Note: (3) t_{LZ} and t_{OLZ} are shown for reference only, they are periodically characterized and are not 100% tested.
(4) t_{HZ} and t_{OHZ} are measured from the point when $\overline{CE}$ or $\overline{OE}$ return high (whichever occurs first) to the time when the outputs are no longer driven.

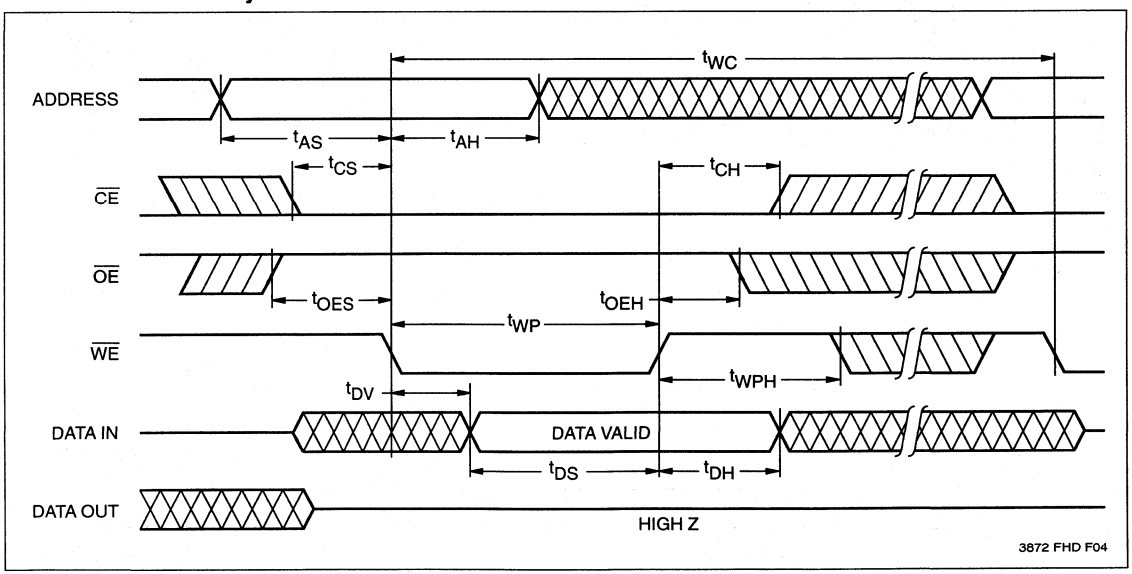
6

Write Cycle Limits

Symbol	Parameter	$\overline{WE}$ Controlled Write		$\overline{CE}$ Controlled Write (4)		Units
		Min.	Max.	Min.	Max.	
t_{WC}	Write Cycle Time		10		10	ms
t_{AS}	Address Setup Time	0		0		ns
t_{AH}	Address Hold Time	125		125		ns
t_{CS}	Write Setup Time	25		0		ns
t_{CH}	Write Hold Time	0		25		ns
t_{CW}	$\overline{CE}$ Pulse Width	125		100		ns
t_{OES}	$\overline{OE}$ High Setup Time	10		10		ns
t_{OEH}	$\overline{OE}$ High Hold Time	10		35		ns
t_{WP}	$\overline{WE}$ Pulse Width	100		125		ns
t_{WPH}	$\overline{WE}$ High Recovery	100		100		ns
t_{DV}	Data Valid		1		1	µs
t_{DS}	Data Setup	50		50		ns
t_{DH}	Data Hold	10		35		ns
t_{DW}	Delay to Next Write	10		10		µs
t_{BLC}	Byte Load Cycle	0.3	100	0.3	100	µs

3872 PGM T08.1

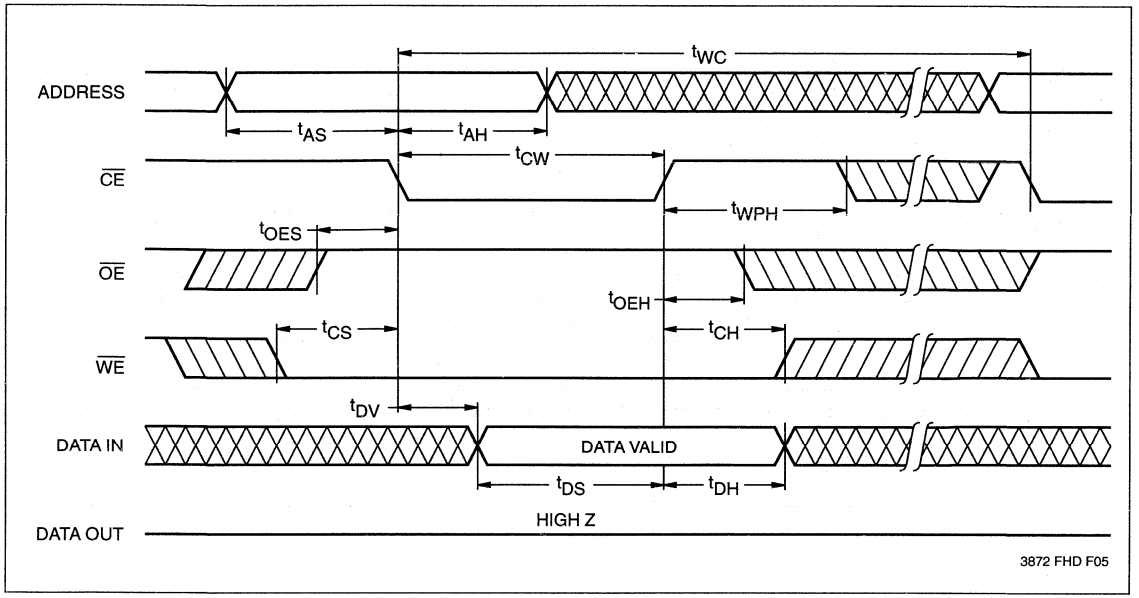
$\overline{WE}$ Controlled Write Cycle



3872 FHD F04

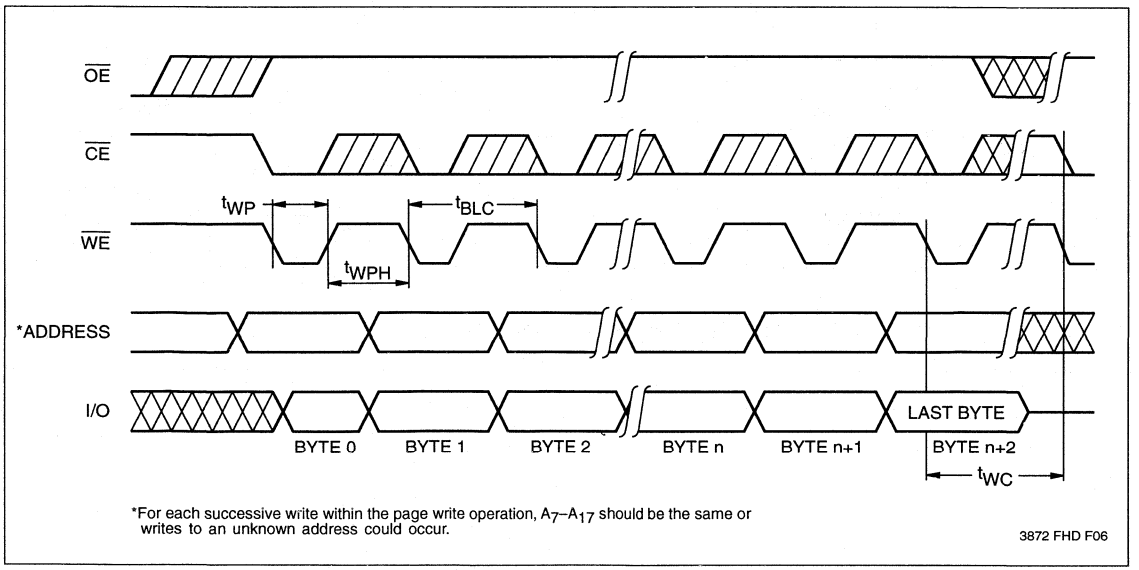
Note: (4) Due to the inclusion of the decoder IC on board the module the $\overline{WE}$ and $\overline{CE}$ write controlled timings will vary. When utilizing the $\overline{CE}$ controlled write operation all the hold timings must be extended by the worst case propagation delay of the decoder. For a $\overline{WE}$ controlled write operation $\overline{CE}$ must be a minimum 125ns to accommodate the additional setup time required.

$\overline{CE}$ Controlled Write Cycle

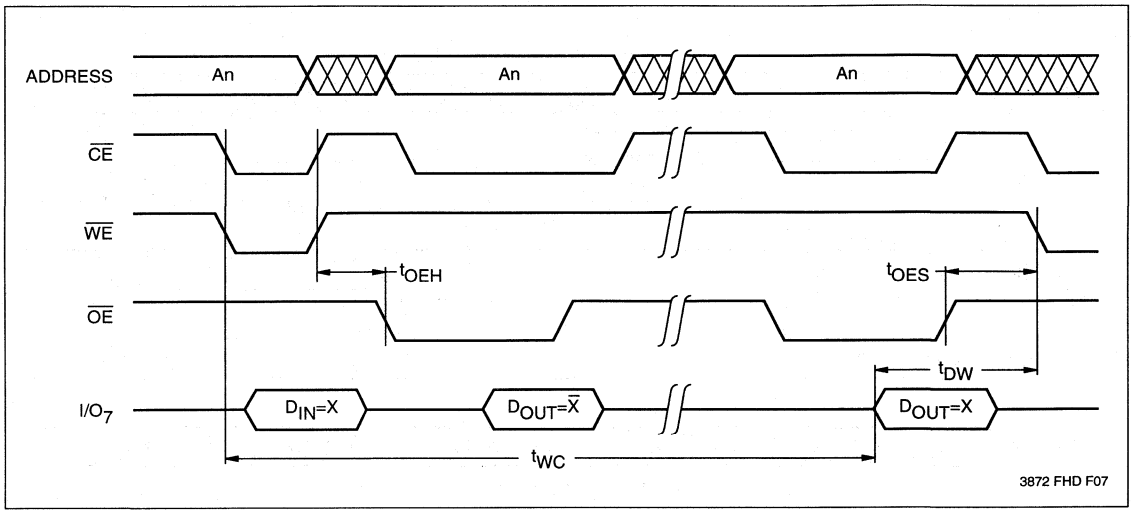


6

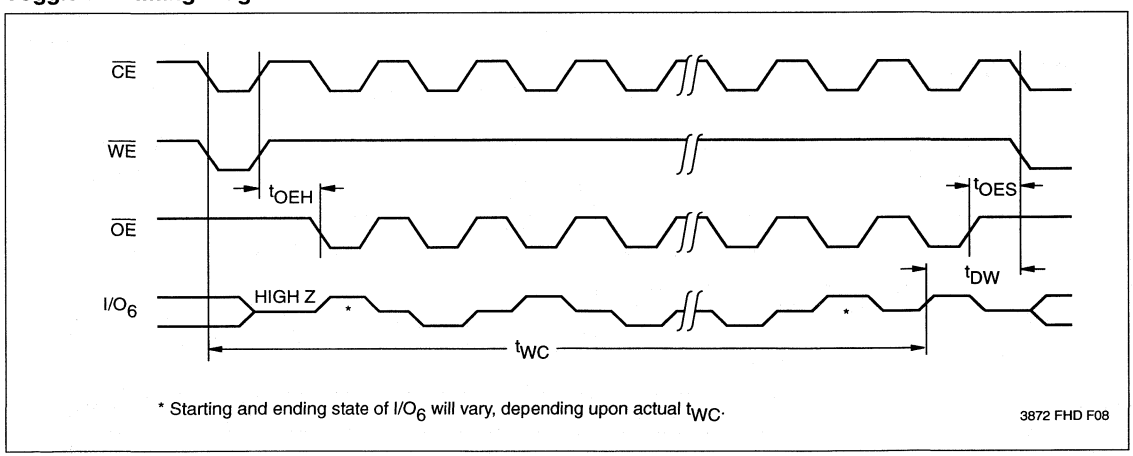
Page Write Cycle



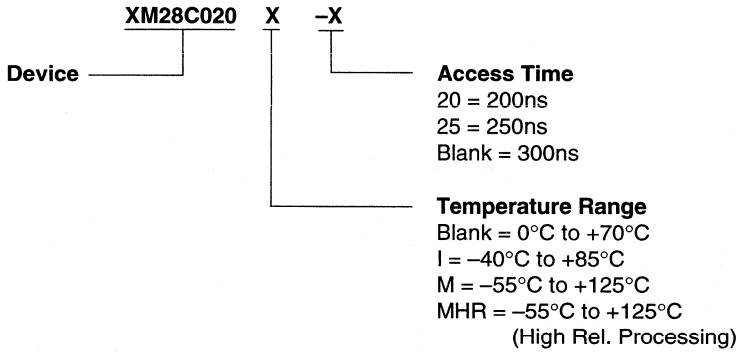
$\overline{\text{DATA}}$ Polling Timing Diagram



Toggle Bit Timing Diagram



ORDERING INFORMATION
2 MEGABIT E^2 MODULES



6

NOTES

High Speed 5 Volt Byte Alterable Nonvolatile Memory Array

FEATURES

- High Speed, High Density Memory Module
  - —200ns, 150ns, 120ns Access Times Available
  - —2 Megabit Memory in 1 square inch.
- Flexible Multiplane Architecture
  - —Four Separate Chip Selects
  - —32 Separate I/Os
    - User Configurable I/Os—x8, x16, or x32
    - User Configurable Page Size—64 Double-words, 128 Words, or 256 Bytes
  - —Concurrent Read/Write Operations
    - Able to Continue Reading During a Nonvolatile Write Cycle.
  - —5 Volt Byte or Page Alterable
    - No Erase Before Write
- Software Data Protection
- Early End of Write Polling
  - —$\overline{\text{DATA}}$ Polling
  - —Toggle Bit Polling
- High Reliability
  - —Endurance: 100,000 Cycles
  - —Data Retention: 100 Years

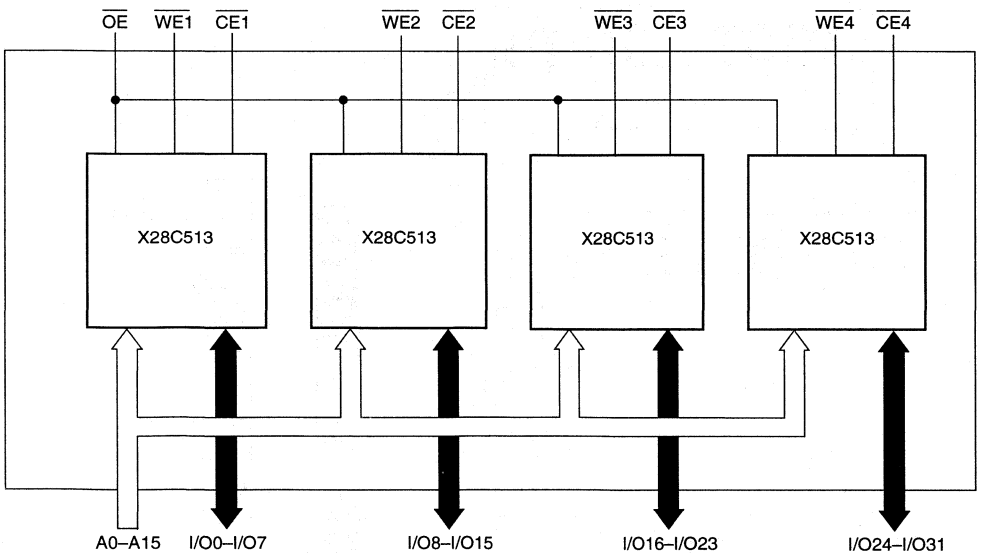
DESCRIPTION

The XM28C020P is a high speed, high density CMOS byte alterable nonvolatile memory array constructed on a co-fired ceramic substrate using Xicor's high speed X28C513 components in 32-pad leadless chip carriers. The substrate is a 66-pin ceramic pin grid array.

The module is configured with four separate chip enable and write enable inputs and 32 separate I/Os. This, along with the small footprint, provides the end user with a large degree of flexibility in board layout and memory configuration. In addition, with the large number of pins and the growth path being implemented, the module will be able to grow to 16 megabits.

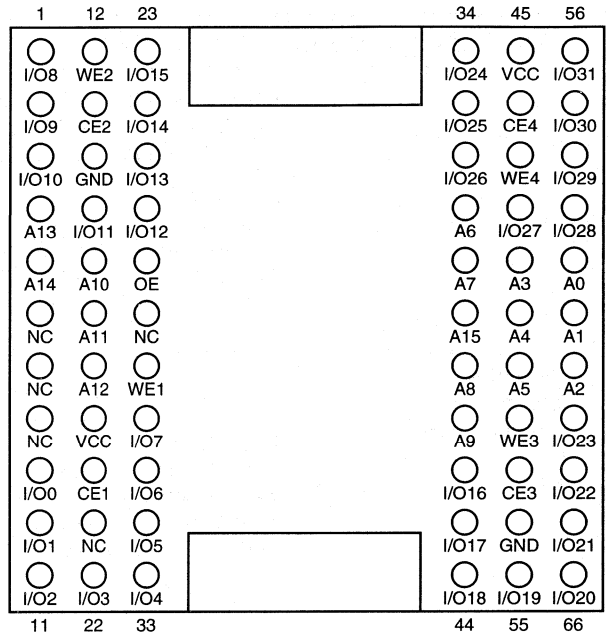
6

FUNCTIONAL DIAGRAM



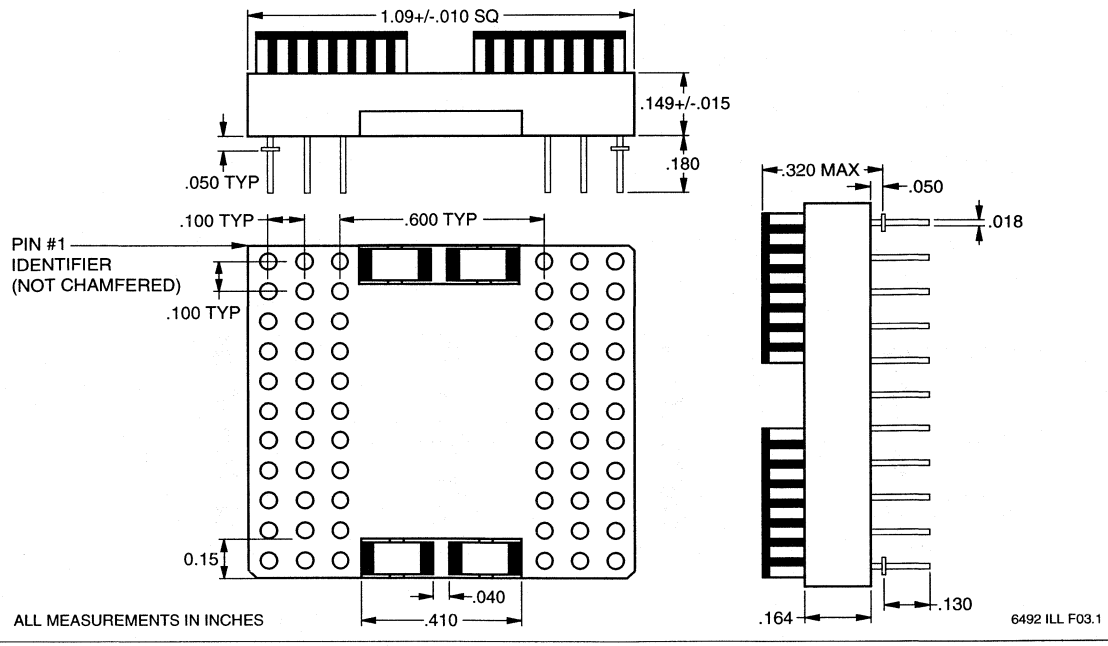
6492 ILL F01

PIN CONFIGURATION



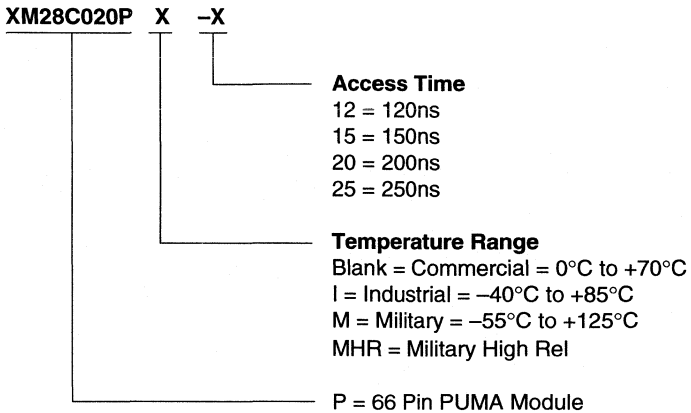
6492 ILL F02

PACKAGE INFORMATION



6492 ILL F03.1

ORDERING INFORMATION



6

NOTES

5 Volt, Byte Alterable E²PROM

TYPICAL FEATURES

- High Density 4 Megabit (512K x 8) Module
- Access Time of 200ns at –55°C to +125°C
- Base Memory Component: Xicor X28C010
- Pinout Conforms to JEDEC Standard for 4 Megabit E²PROM
- Fast Write Cycle Times
  - —256 Byte Page Write
- Early End of Write Detection
  - —DATA Polling
  - —Toggle Bit Polling
- Software Data Protection
- Three Temperature Ranges
  - —Commercial: 0°C to +75°C
  - —Industrial: –40° to +85°C
  - —Military: –55° to +125°C
- High Rel Modules all Components are MIL-STD-883 Compliant

DESCRIPTION

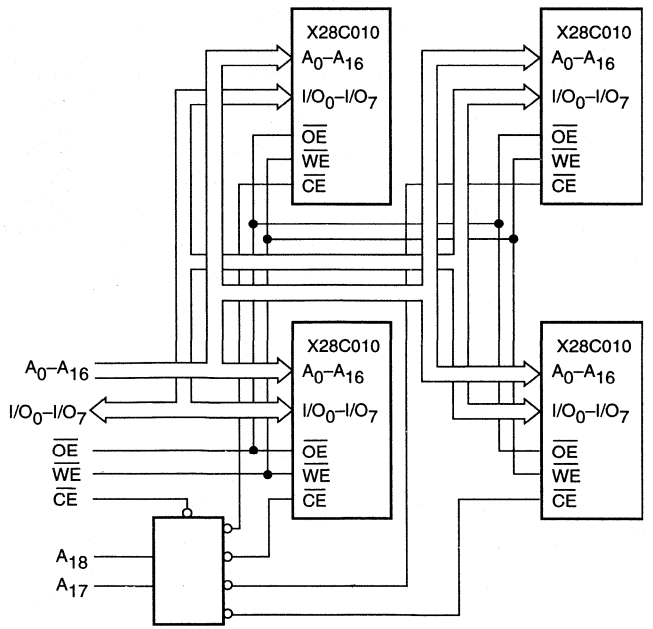
The XM28C040 is a high density 4 Megabit E²PROM comprised of four X28C010's mounted on a co-fired multilayered ceramic substrate. Individual components are 100% tested prior to assembly in module form and then 100% tested after assembly.

The XM28C040 is configured 512K x 8 bit. The module supports a 256-byte page write operation. This combined with DATA Polling or Toggle Bit Polling, effectively provides a 39µs/byte write cycle, enabling the entire array to be rewritten in 10 seconds.

The XM28C040 provides the same high endurance and data retention as the X28C010.

6

FUNCTIONAL DIAGRAM



3873 FHD F01

PIN DESCRIPTIONS

Addresses (A_0–A_{18})

The Address inputs select an 8-bit memory location during a read or write operation.

Chip Enable ($\overline{CE}$)

The Chip Enable input must be LOW to enable all read/write operations. When $\overline{CE}$ is HIGH, power consumption is reduced (see Note 4).

Output Enable ($\overline{OE}$)

The Output Enable input controls the data output buffers and is used to initiate read operations.

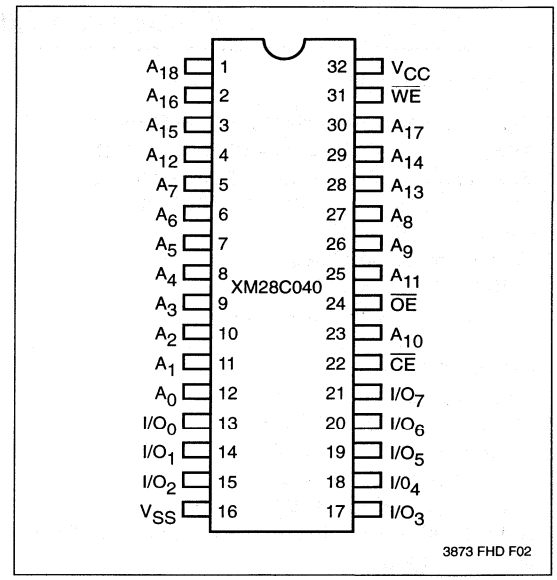
Data In/Data Out (I/O_0–I/O_7)

Data is written to or read from the XM28C040 through the I/O pins.

Write Enable ($\overline{WE}$)

The Write Enable input controls the writing of data to the XM28C040.

PIN CONFIGURATION



3873 FHD F02

PIN NAMES

Symbol	Description
A_0–A_{18}	Address Inputs
I/O_0–I/O_8	Data Input/Output
$\overline{WE}$	Write Enable
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
V_{CC}	+5V
V_{SS}	Ground
NC	No Connect

3873 PGM T01

DEVICE OPERATION

Read

Read operations are initiated by both $\overline{OE}$ and $\overline{CE}$ LOW. The read operation is terminated by either $\overline{CE}$ or $\overline{OE}$ returning HIGH. This 2-line control architecture eliminates bus contention in a system environment. The data bus will be in a high impedance state when either $\overline{OE}$ or $\overline{CE}$ is HIGH.

Write

Write operations are initiated when both $\overline{CE}$ and $\overline{WE}$ are LOW and $\overline{OE}$ is HIGH. The XM28C040 supports both a $\overline{CE}$ and $\overline{WE}$ controlled write cycle. That is, the address is latched by the falling edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs last. Similarly, the data is latched internally by the rising edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs first. A byte write operation, once initiated, will automatically continue to completion, typically within 5ms (see Note 4).

Page Write Operation

The page write feature of the XM28C040 allows the entire memory to be written in 10 seconds. Page write allows two to 256 bytes of data to be consecutively written to the XM28C040 prior to the commencement of the internal programming cycle. The host can fetch data from another device within the system during a page write operation (change the source address), but the page address (A_8 through A_{18}) for each subsequent valid write cycle to the part during this operation must be the same as the initial page address.

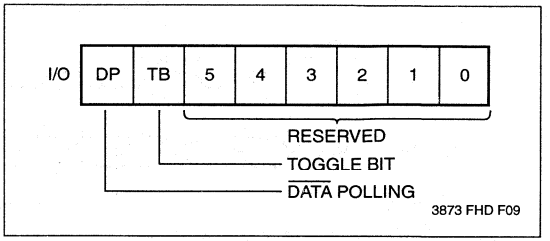
The page write mode can be initiated during any write operation. Following the initial byte write cycle, the host can write an additional one to 255 bytes in the same manner as the first byte was written. Each successive byte load cycle, started by the $\overline{WE}$ HIGH to LOW transition, must begin within 100µs of the falling edge of the preceding $\overline{WE}$. If a subsequent $\overline{WE}$ HIGH to LOW transition is not detected within 100µs, the internal automatic programming cycle will commence. There is no page write window limitation. Effectively the page write window is infinitely wide, so long as the host continues to access the device within the byte load cycle time of 100µs.

Write Operation Status Bits

The XM28C040 provides the user two write operation status bits. These can be used to optimize a system write cycle time. The status bits are mapped onto the I/O bus as shown in Figure 1.

$\overline{DATA}$ Polling (I/O_7)

Figure 1. Status Bit Assignment



The XM28C040 features $\overline{DATA}$ Polling as a method to indicate to the host system that the byte write or page write cycle has completed. $\overline{DATA}$ Polling allows a simple bit test operation to determine the status of the XM28C040, eliminating additional interrupt inputs or external hardware. During the internal programming cycle, any attempt to read the last byte written will produce the complement of that data on I/O_7 (i.e., write data = 0xxx xxxx, read data = 1xxx xxxx). Once the programming cycle is complete, I/O_7 will reflect true data. Note: If the XM28C040 is in the protected state and an illegal write operation is attempted, $\overline{DATA}$ Polling will not operate.

Toggle Bit (I/O_6)

The XM28C040 also provides another method for determining when the internal write cycle is complete. During the internal programming cycle I/O_6 will toggle from "1" to "0" and "0" to "1" on subsequent attempts to read the last byte written. When the internal cycle is complete the toggling will cease and the device will be accessible for additional read or write operations.

$\overline{\text{DATA}}$ POLLING I/O_7

Figure 2. $\overline{\text{DATA}}$ Polling Bus Sequence

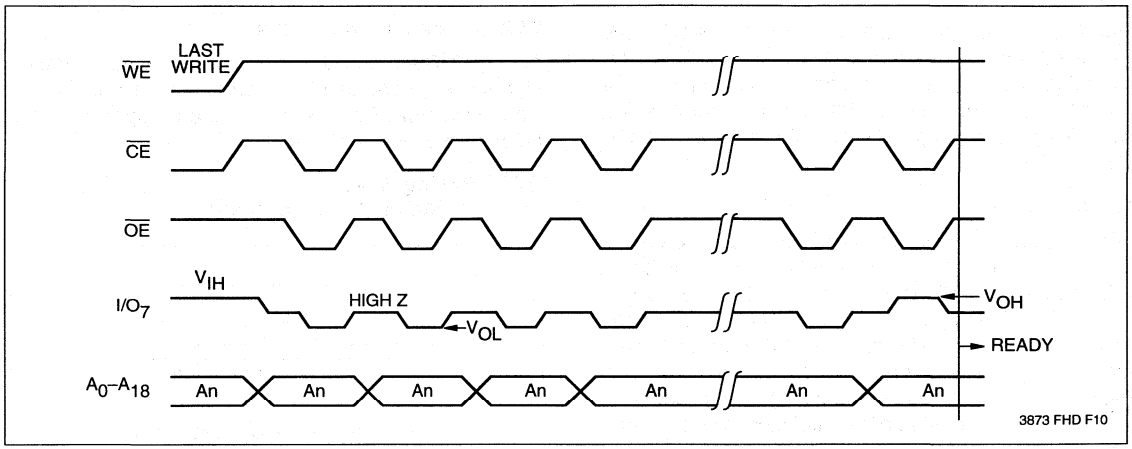
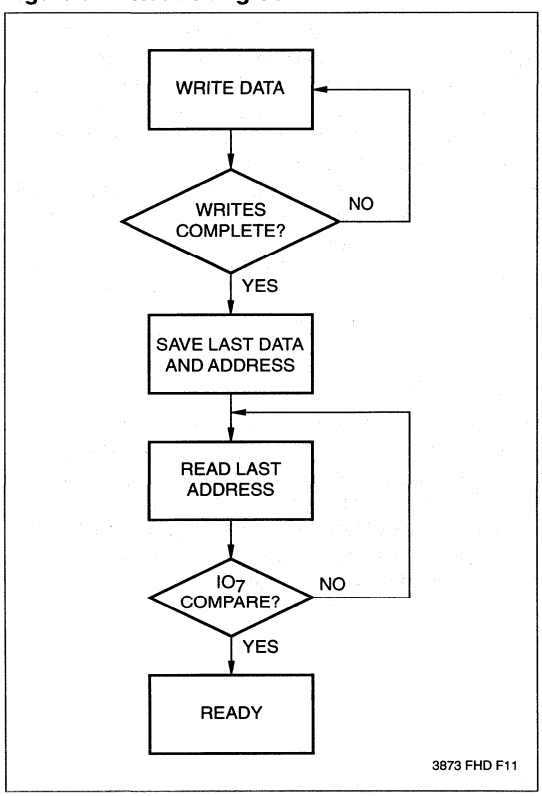


Figure 3. $\overline{\text{DATA}}$ Polling Software Flow



$\overline{\text{DATA}}$ Polling can effectively halve the time for writing to the XM28C040. The timing diagram in Figure 2 illustrates the sequence of events on the bus. The software flow diagram in Figure 3 illustrates one method of implementing the routine.

THE TOGGLE BIT I/O_6

Figure 4. Toggle Bit Bus Sequence

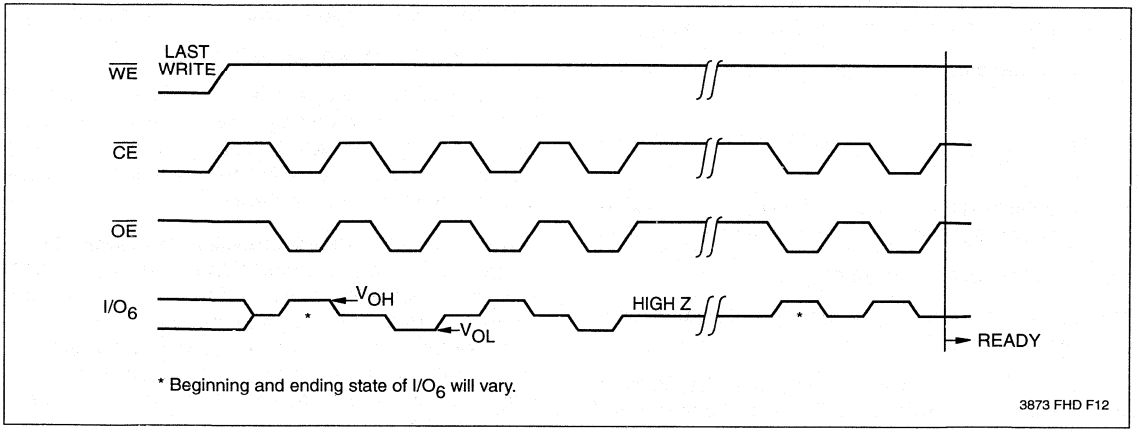
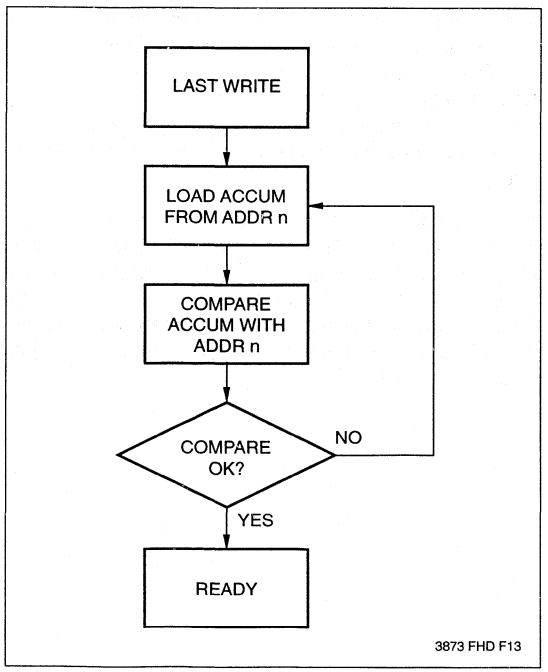


Figure 5. Toggle Bit Software Flow



The Toggle Bit can eliminate the software housekeeping chore of saving and fetching the last address and data written to a device in order to implement $\overline{DATA}$ Polling. This can be especially helpful in an array comprised of multiple XM28C040 memories that is frequently updated. The timing diagram in Figure 4 illustrates the sequence of events on the bus. The software flow diagram in Figure 5 illustrates a method for testing the Toggle Bit.

6

HARDWARE DATA PROTECTION

The XM28C040 provides three hardware features that protect nonvolatile data from inadvertent writes.

- Noise Protection—A $\overline{WE}$ pulse less than 10ns will not initiate a write cycle.
- Default V_{CC} Sense—All functions are inhibited when V_{CC} is ≤ 3V.
- Write Inhibit—Holding $\overline{OE}$ LOW will prevent an inadvertent write cycle during power-up and power-down.

SOFTWARE DATA PROTECTION

The XM28C040 does provide the Software Data Protection (SDP) feature.

The module is shipped from Xicor with the Software Data Protection NOT ENABLED; that is, the module will be in the standard operating mode. In this mode, data should be protected during power-up/-down operations through the use of external circuits. The host system will then have open read and write access of the module once V_{CC} is stable.

The module can be automatically protected during power-up/-down without the need for external circuits by employing the SDP feature. The internal SDP circuit is enabled after the first write operation utilizing the SDP command sequence.

When this feature is employed, it will be easiest to incorporate in the system software if the module is viewed as a subsystem composed of four discrete memory devices with an address decoder (see Functional Diagram). In this manner, system memory mapping will extend onto the module. That is, the discrete memory ICs and decoder should be considered memory board components and SDP can be implemented at the component level as described in the next section.

SOFTWARE COMMAND SEQUENCE

A_{17} and A_{18} are used by the decoder to select one of the four LCCs. Therefore, only one of the four memory devices can be accessed at one time. In order to protect the entire module, the command sequence must be issued separately to each device.

Enabling the software data protection mode requires the host system to issue a series of three write operations: each write operation must conform to the data and address sequence illustrated in Figures 6 and 7. Because this involves writing to a nonvolatile bit, the device will become protected after t_{WC} has elapsed. After this point in time devices will inhibit inadvertent write operations.

Once in the protected mode, authorized writes may be performed by issuing the same command sequence that enables SDP, immediately followed by the address/data combination desired. The command sequence opens the page write window enabling the host to write from one to 256 bytes of data. Once the data has been written, the device will automatically be returned to the protected state.

In order to facilitate testing of the devices the SDP mode can be deactivated. This is accomplished by issuing a series of six write operations: each write operation must conform to the data and address sequence illustrated in Figures 8 and 9. This is a nonvolatile operation, and the host will have to wait a minimum t_{WC} before attempting to write new data.

SOFTWARE DATA PROTECTION

Figure 6. Timing Sequence—Byte or Page Write

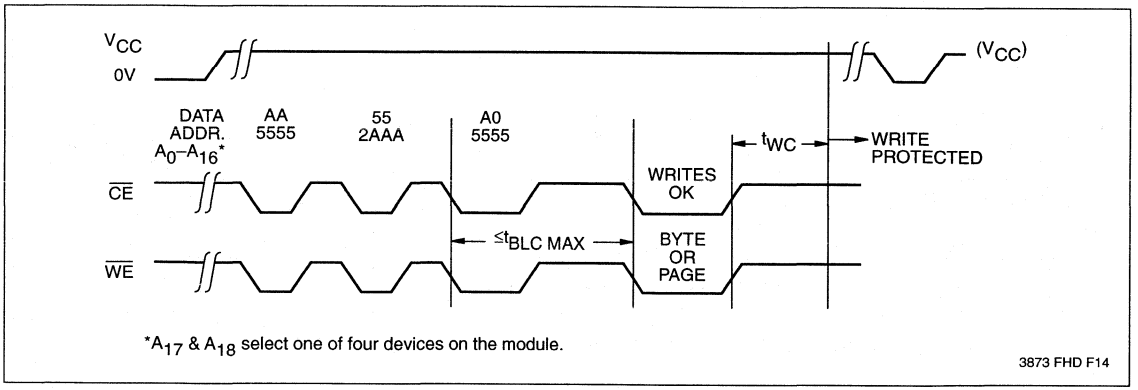
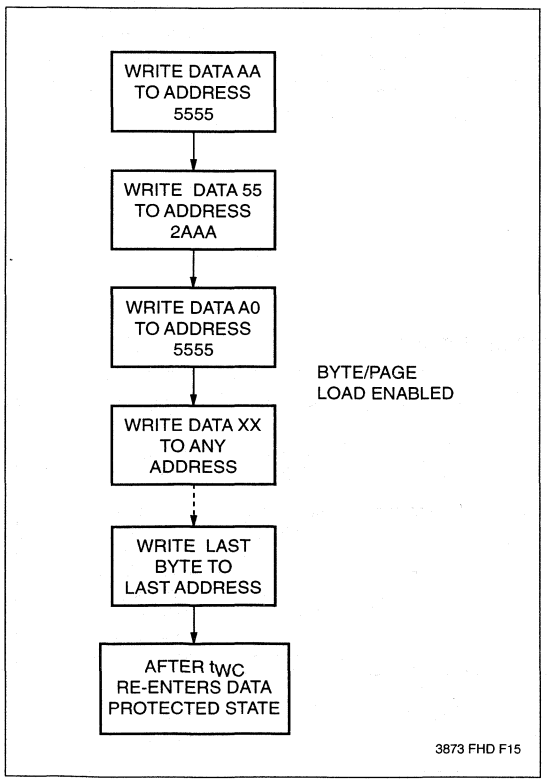


Figure 7. Write Sequence for Software Data Protection



Regardless of whether the device has previously been protected or not, once the software data protected algorithm is used and data has been written, the device will automatically disable further writes unless another command is issued to cancel it. If no further commands are issued the device will be write protected during power-down and after any subsequent power-up.

6

RESETTING SOFTWARE DATA PROTECTION

Figure 8. Reset Software Data Protection Timing Sequence

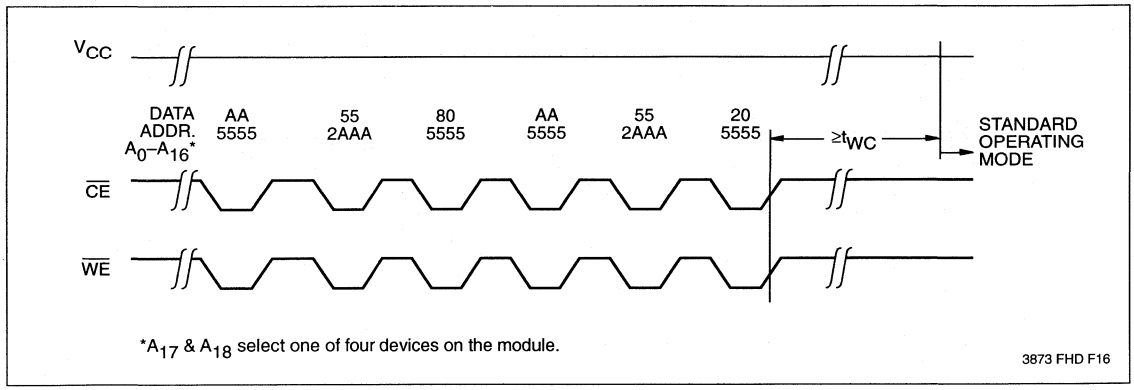
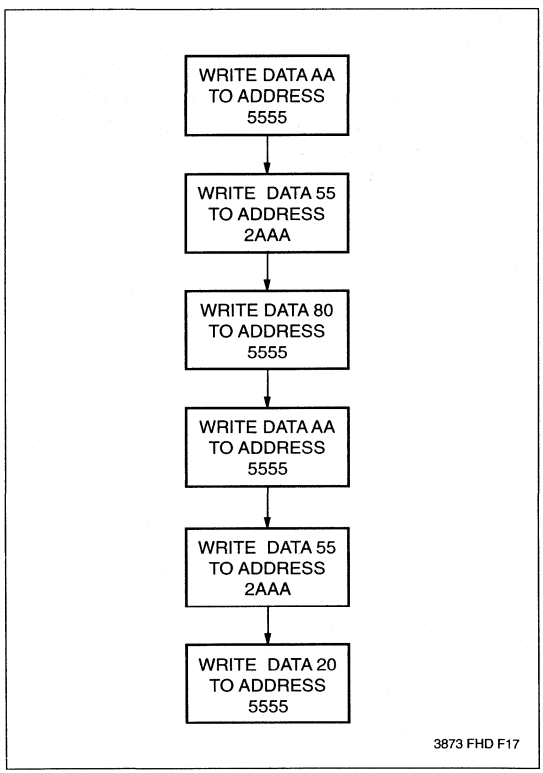


Figure 9. Software Sequence to Deactivate Software Data Protection



In the event the user wants to deactivate the software data protection feature for testing or reprogramming in an E^2PROM programmer, the following six step algorithm will reset the internal protection circuit. After t_{WC}, the device will be in standard operating mode.

SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

SYSTEM CONSIDERATIONS

Because the XM28C040 is frequently used in large memory arrays it is provided with a two line control architecture for both read and write operations. Proper usage can provide the lowest possible power dissipation and eliminate the possibility of contention where multiple I/O pins share the same bus.

To gain the most benefit it is recommended that $\overline{CE}$ be decoded from the address bus and be used as the primary device selection input. Both $\overline{OE}$ and $\overline{WE}$ would then be common among all devices in the array. For a read operation this assures that all deselected devices are in their standby mode and that only the selected device(s) is outputting data on the bus.

Because the XM28C040 has two power modes, standby and active, proper decoupling of the memory array is of prime concern. Enabling $\overline{CE}$ will cause transient current spikes. The magnitude of these spikes is dependent on the output capacitive loading of the I/Os. Therefore, the larger the array sharing a common bus, the larger the transient spikes. The voltage peaks associated with the current transients can be suppressed by the proper selection and placement of decoupling capacitors. As a minimum, it is recommended that a 0.1μF high frequency ceramic capacitor be used between V_{CC} and V_{SS} at each device. Depending on the size of the array, the value of the capacitor may have to be larger.

In addition, it is recommended that a 4.7μF electrolytic bulk capacitor be place between V_{CC} and V_{SS} for every two modules employed in the array. This bulk capacitor is employed to overcome the voltage droop caused by the inductive effects of the PC board traces.

ABSOLUTE MAXIMUM RATINGS*

Temperature under Bias ..... –65°C to +135°C
Storage Temperature ..... –65°C to +150°C
Voltage on any Pin with
Respect to V_{SS} ..... –1V to +7V
D.C. Output Current 5mA
Lead Temperature
(Soldering, 10 seconds) ..... 300°C

***COMMENT**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. OPERATING CHARACTERISTICS

XM28C040 T_A = 0°C to +70°C, V_{CC} = +5V ±10%, unless otherwise specified.
XM28C040I T_A = –40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.
XM28C040M T_A = –55°C to +125°C, V_{CC} = +5V ±10%, unless otherwise specified.

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
I_{CC}	V_{CC} Current (Active) (TTL Inputs)		80	mA	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}, All I/O's = Open, 1 Device Active Address Inputs = TTL Levels @ f = 5MHz
I_{SB}	V_{CC} Current (Standby)		5	mA	$\overline{CE}$, A_{17}, A_{18} = V_{CC} –0.3V All other inputs = V_{IH} All I/Os = OPEN
I_{LI}	Input Leakage Current		10	µA	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output Leakage Current		10	µA	V_{OUT} = V_{SS} to V_{CC}, $\overline{CE}$ = V_{IH}
V_{IL}	Input LOW Voltage	–1	0.8	V	
V_{IH}	Input HIGH Voltage	2	V_{CC} + 1	V	
V_{OL}	Output LOW Voltage		0.4	V	I_{OL} = 2.1mA
V_{OH}	Output HIGH Voltage	2.4		V	I_{OH} = –400µA

3873 PGM T02.2

POWER-UP TIMING

Symbol	Parameter	Typ.(1)	Units
t_{PUR}(2)	Power-up to Initiation of Read Operation	100	ms
t_{PUW}(2)	Power-up to Initiation of Write Operation	5	ms

3873 PGM T03

CAPACITANCE T_A = +25°C, f = 1MHz, V_{CC} = 5V

Symbol	Parameter	Max.	Units	Test Conditions
$C_{I/O}$(2)	Input/Output Capacitance	50	pF	$V_{I/O}$ = 0V
C_{IN}(2)	Input Capacitance	50	pF	V_{IN} = 0V

3873 PGM T04.1

Notes: (1) Typical values are for T_A = 25°C and nominal supply voltage.
(2) This parameter is periodically sampled and not 100% tested.

A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3V
Input Rise and Fall Times	10ns
Input and Output Timing Levels	1.5V
Output Load	1 TTL Gate and C_L = 100pF

3873 PGM T05.1

MODE SELECTION

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O	Power
L	L	H	Read	D_{OUT}	Active
L	H	L	Write	D_{IN}	Active
H	X	X	Standby and Write Inhibit	High Z	Standby
X	L	X	Write Inhibit	—	—
X	X	H	Write Inhibit	—	—

3873 PGM T06

A.C. CHARACTERISTICS

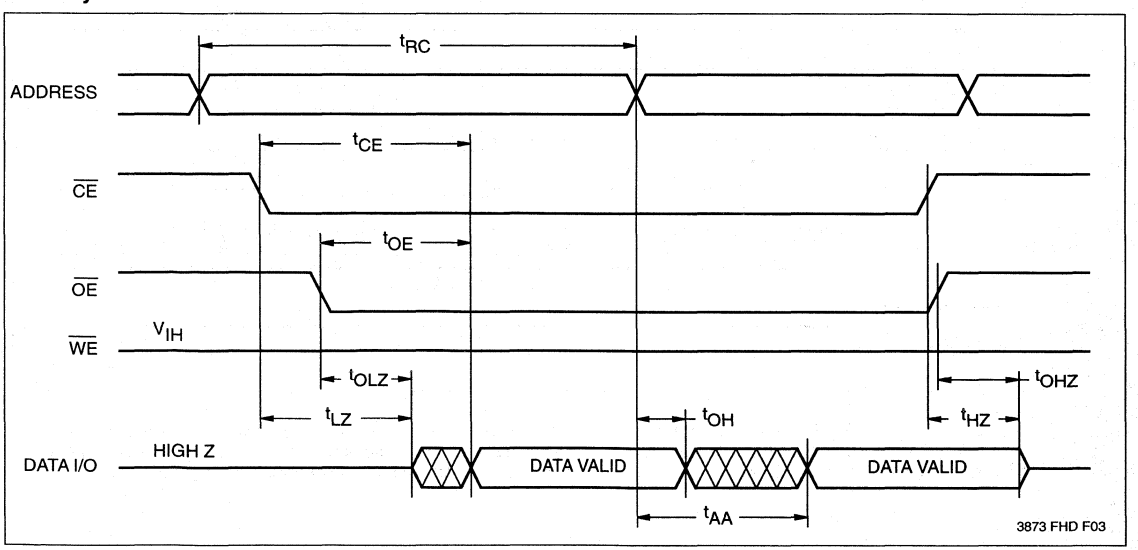
XM28C040 T_A = 0°C to +75°C, V_{CC} = +5V ±10%, unless otherwise specified.
XM28C040I T_A = –40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.
XM28C040M T_A = –55°C to +125°C, V_{CC} = +5V ±10%, unless otherwise specified.

Read Cycle Limits

Symbol	Parameter	XM28C040-20		XM28C040-25		XM28C040		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	200		250		300		ns
t_{CE}	Chip Enable Access Time		200		250		300	ns
t_{AA}	Address Access Time		200		250		300	ns
$t_{\overline{CE}}$	Output Enable Access Time		80		100		100	ns
t_{LZ}[4]	$\overline{CE}$ Low to Active Output	0		0		0		ns
t_{OLZ}[4]	$\overline{OE}$ Low to Active Output	0		0		0		ns
t_{HZ}[4]	$\overline{CE}$ High to High Z Output		100		100		100	ns
t_{OHZ}[4]	$\overline{OE}$ High to High Z Output		100		100		100	ns
t_{OH}	Output Hold From Address Change	0		0		0		ns

3873 PGM T07

Read Cycle



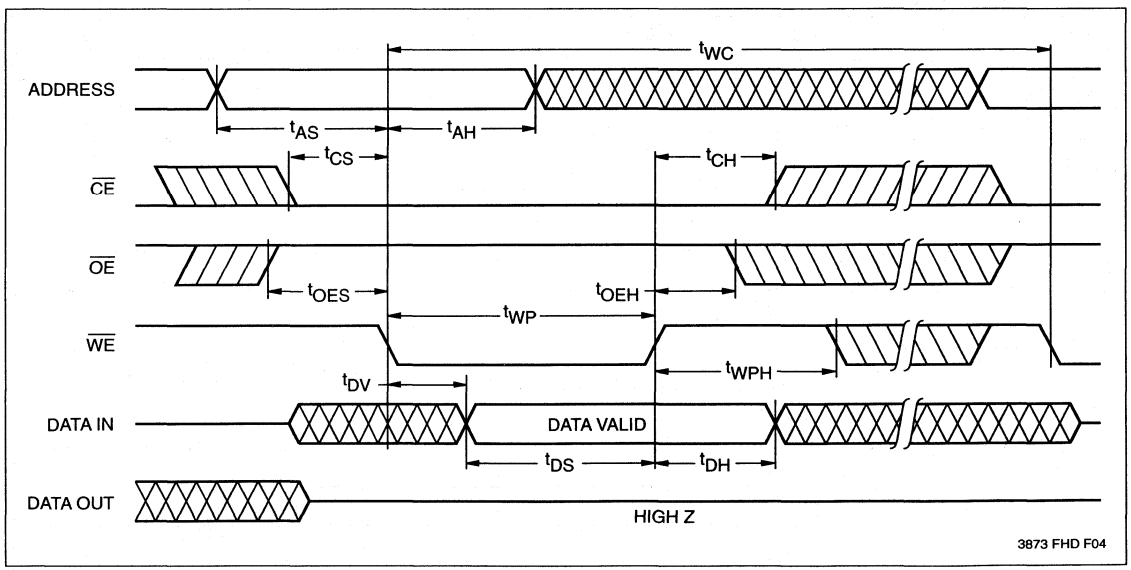
Note: (3) t_{HZ} and t_{OHZ} are measured from the point when $\overline{CE}$ or $\overline{OE}$ return high (whichever occurs first) to the time when the outputs are no longer driven.

Write Cycle Limits

Symbol	Parameter	$\overline{WE}$ Controlled Write		$\overline{CE}$ Controlled Write (4)		Units
		Min.	Max.	Min.	Max.	
t_{WC}	Write Cycle Time		10		10	ms
t_{AS}	Address Setup Time	0		0		ns
t_{AH}	Address Hold Time	125		125		ns
t_{CS}	Write Setup Time	25		0		ns
t_{CH}	Write Hold Time	0		25		ns
t_{CW}	$\overline{CE}$ Pulse Width	125		100		ns
t_{OES}	$\overline{OE}$ High Setup Time	10		10		ns
t_{OEH}	$\overline{OE}$ High Hold Time	10		35		ns
t_{WP}	$\overline{WE}$ Pulse Width	100		125		ns
t_{WPH}	$\overline{WE}$ High Recovery	100		100		ns
t_{DV}	Data Valid		1		1	µs
t_{DS}	Data Setup	50		50		ns
t_{DH}	Data Hold	10		35		ns
t_{DW}	Delay to Next Write	10		10		µs
t_{BLC}	Byte Load Cycle	0.3	100	0.3	100	µs

3873 PGM T08.1

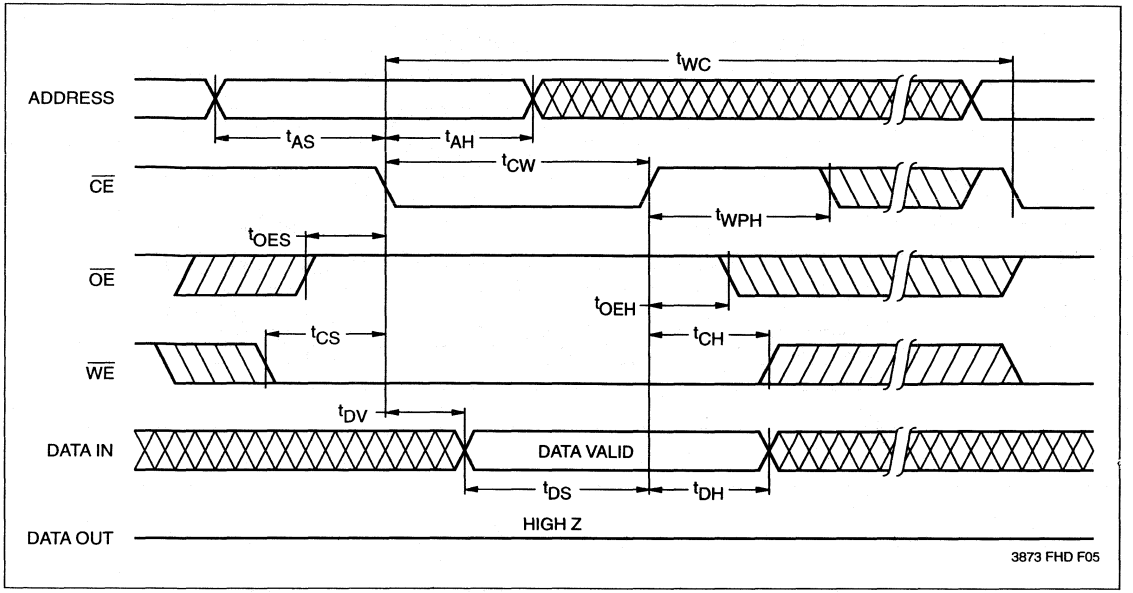
$\overline{WE}$ Controlled Write Cycle



3873 FHD F04

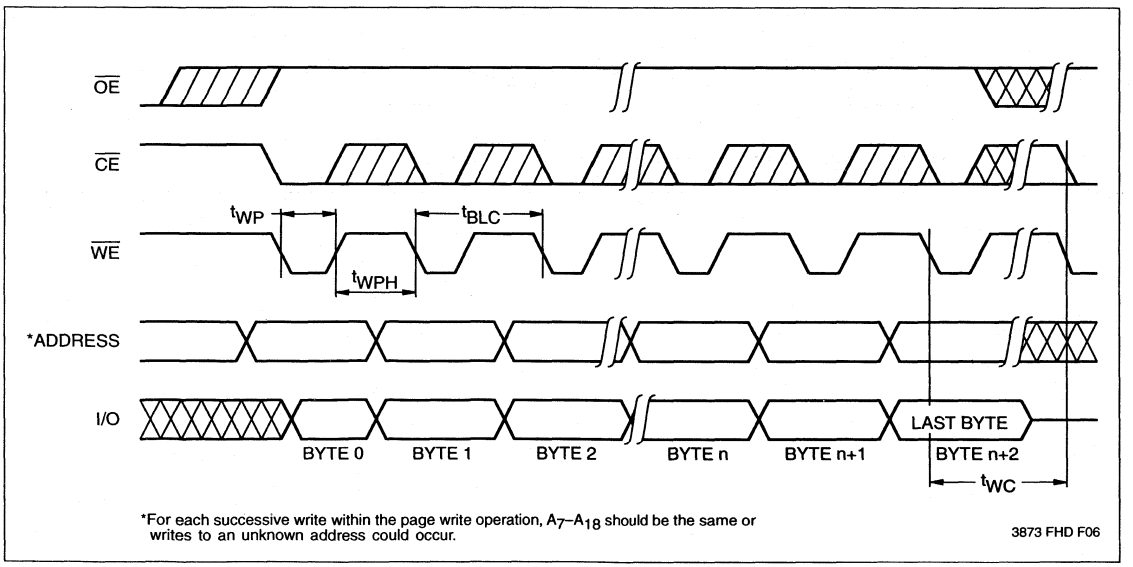
Note: (4) Due to the inclusion of the decoder IC on board the module the $\overline{WE}$ and $\overline{CE}$ write controlled timings will vary. When utilizing the $\overline{CE}$ controlled write operation all the hold timings must be extended by the worst case propagation delay of the decoder. For a $\overline{WE}$ controlled write operation $\overline{CE}$ must be a minimum 125ns to accommodate the additional setup time required.

$\overline{CE}$ Controlled Write Cycle



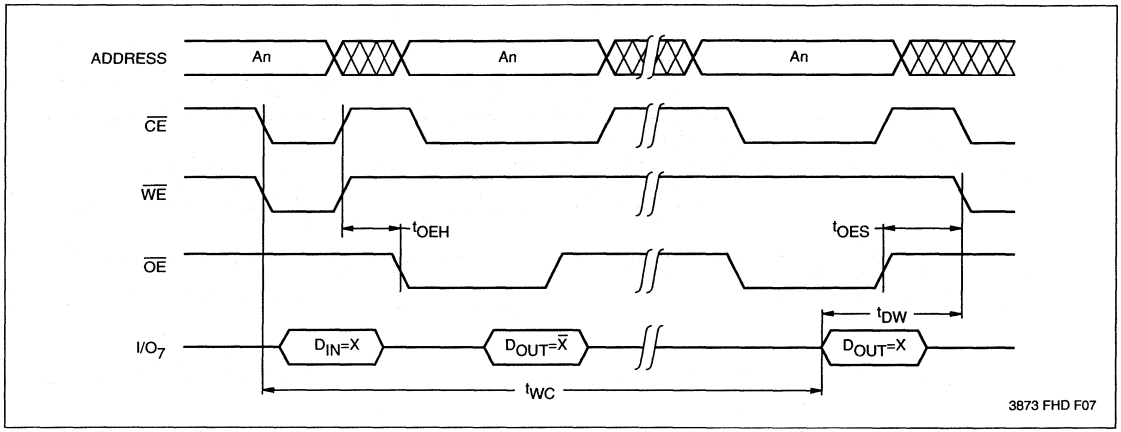
6

Page Write Cycle

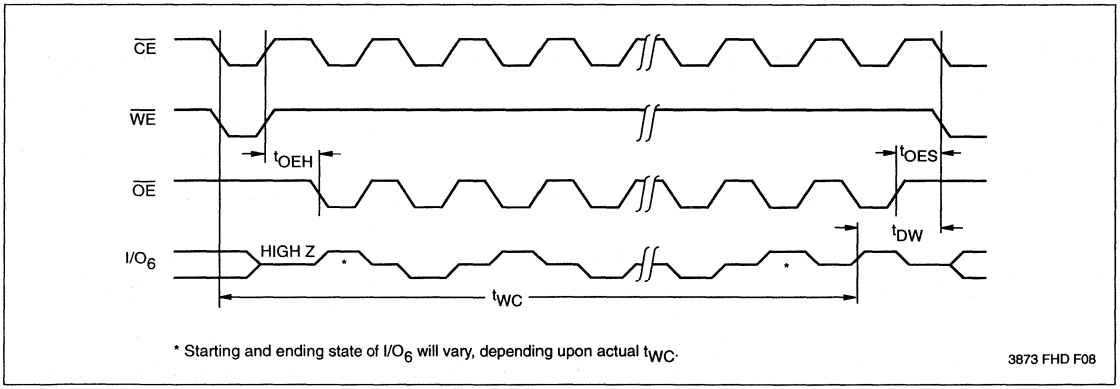


*For each successive write within the page write operation, A_7–A_{18} should be the same or writes to an unknown address could occur.

$\overline{\text{DATA}}$ Polling Timing Diagram



Toggle Bit Timing Diagram



MultiPlane Architecture

The design of the XM28C040 has implemented a multiplane architecture. That is, there are four independent 128K x 8 memory spaces or planes, each selected by its own chip enable input via the on-board decoder chip. This architecture can be utilized in a number of ways.

Separate Data and Program Memory Spaces

The multiplane concept allows the system to write to one plane of the module and still be able to read (continue executing code) from the module, utilizing any plane not performing a write operation.

This concept of separate data and program spaces can be expanded by providing a simple off-module circuit that will disable writes to predetermined portions of memory. A very basic version is shown in the Functional Diagram. Whenever A_{18} is HIGH, the $\overline{WE}$ input is forced HIGH, write protecting one half the module. This half would be reserved for read only program store while the other half would be available for read and write data store.

Expanded Sequential Page Lengths

A standard system implementation would be decoding externally the module's chip enable and then wiring each address of the module to its corresponding address line in the system. This would effectively provide the system a memory organized as four separate memory planes with a sequential page address space of 256 bytes.

In an application such as data logging, the most efficient method of logging the data is in a sequential manner. If the data come in bursts that exceed 256 bytes in length a longer page might be desirable. By swapping address lines externally the effective page length can be expanded to 1024 bytes. Refer to the table below for a matrix illustrating the various page length options.

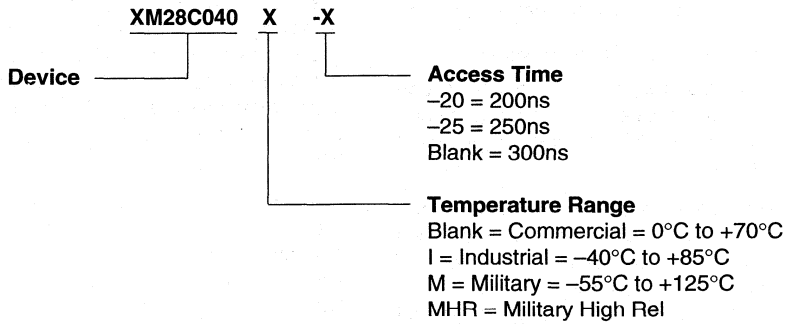
TABLE 1. ADDRESS TRANSLATION MATRIX

	Module Address Inputs				Page Size	Effective No. of Planes
	A_0-A_7	A_8-A_{16}	A17	A_{18}		
System Address Lines	A0-A7	A8-A16	A17	A18	256	4
	A0-A7	A9-A17	A8	A18	512	2
	A0-A7	A10-A18	A8	A9	1024	1

3873 PGM T09

Note: The user should be aware the overall I_{CC} of the module will increase as more individual components on the module are activated.

ORDERING INFORMATION
XM28C040: 512K X 8 CMOS E²PROM Module



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3807-2.3 12/4/95 T12/C0/D0 NS

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#5

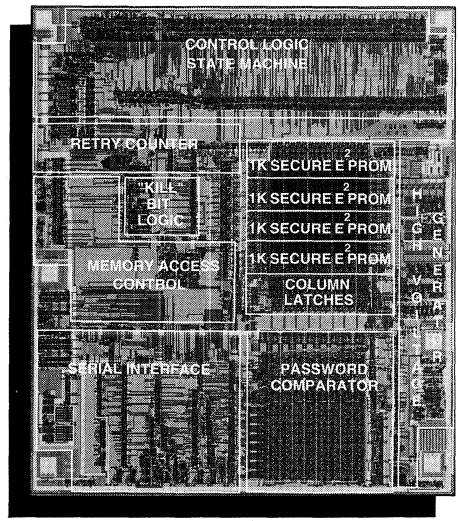
Design Engineering Bulletin

New Product and Applications Information for Design Engineers

PASS™ SecureFlash Protects Access to Embedded Systems Data

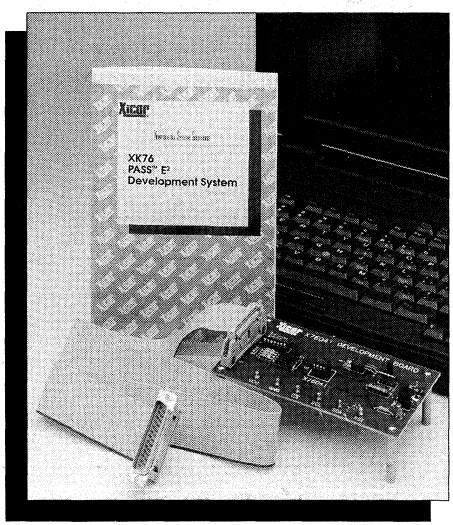
The X76F041 PASS SecureFlash (Password Access Security Supervisor) uses three separate 64 bit passwords to provide ultra high level security to four 1024 bit nonvolatile data arrays. This device can be used to make system data virtually tamper proof without the need for data encryption or decryption. Access to the SecureFlash array is protected by three hierarchical passwords which include a configuration password, a write password and a read password.

The level of data intrusion protection is programmable by the end user, the system manufacturer or a combination of both to provide controlled access to the four independent 1K memory arrays. On chip supervisory circuitry and a programmable retry counter make it ideal for the most sensitive data carrier applications such as cards for banking, telephones, tolls and home security systems. All communications to the device including passwords, instructions and data is via a two wire serial bus. This, coupled with its on chip intelligent supervisory capability provide an ideal single chip solution for cost sensitive data security applications.



The probability of guessing a correct password is one in 18 quintillion (2^{64} = 18,466,744,073,700,000,000.)

The XK76 Development System Provides Total Hardware and Software Development Support for the PASS™ SecureFlash



The XK76 provides a total Development System Solution for PASS SecureFlash Security System Designs.

The XK76 Development System has been designed as a tool that significantly reduces development time of applications using the Xicor X76F041 PASS SecureFlash. It is easy to use and simple to set up, operating with any IBM compatible PC that is equipped with a parallel printer port. The XK76 enables users to quickly examine the capabilities of the X76F041. It provides an ideal platform for evaluating the suitability of the part for a particular application.

The Development System demonstrates the various levels of security available on the X76F041 by enabling the user to configure the part and then attempt to access it using one or none of the passwords, thus simulating system operation without the need for hardware development. The XK76 simplifies debug by controlling an X76F041 residing externally in a Target System (Prototype PC board or Smart Card Reader.) Register and array values can be monitored and preset in-system by connecting an X76F041 in the Target System to the control lines available on the Development Board.

The XK76 also provides the designer with the option of pre-programming parts before use in the Target System. The XK76, PASS SecureFlash Development System saves designers from the laborious task of developing software, hardware and programming support for Security System designs. This results in faster time to market with a higher probability of success.

Password Access Security Supervisor

4K X76F041 4 x 128 x 8 Bit

PASS™ SecureFlash

FEATURES

- **64-Bit Password Security**
- **Three Password Modes**
  - **—Secure Read Access**
  - **—Secure Write Access**
  - **—Secure Configuration Access**
- **Programmable Configuration**
  - **—Read, Write and Configuration Access Passwords**
  - **—Multiple Array Access/Functionality**
  - **—Retry Register/Counter**
- **8 Byte Sector Write**
- **(4) 1K Memory Arrays**
- **ISO Response to Reset**
- **Low Power CMOS**
  - **—50µA Standby Current**
  - **—3mA Active Current**
- **Two Voltage Ranges**
  - **—3V to 3.6V**
  - **—5V ±10%**
- **High Reliability**
  - **—Endurance: 100,000 Cycles**
  - **—Data Retention: 100 Years**
  - **—ESD Protection: 2000V on All Pins**

DESCRIPTION

The X76F041 is a password access security supervisor device, containing four 128 x 8 bit SecureFlash arrays. Access can be controlled by three 64-bit programmable passwords, one for read operations, one for write operations and one for device configuration.

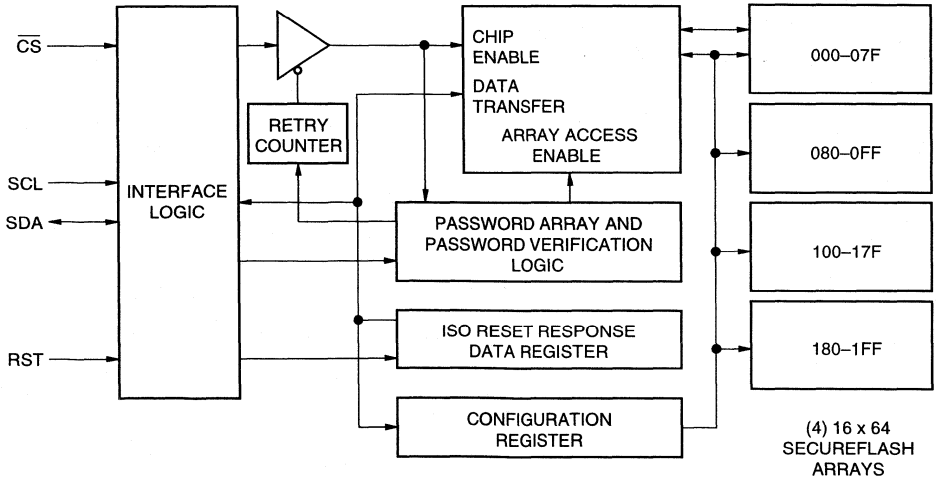
The X76F041 features a serial interface and software protocol allowing operation on a simple two wire bus. The bus signals are a clock input (SCL) and a bidirectional data input and output (SDA). Access to the device is controlled through a chip select input ($\overline{CS}$), allowing any number of devices to share the same bus.

The X76F041 also features a synchronous response to reset; providing an automatic output of a pre-configured 32-bit data stream conforming to the ISO standard for memory cards.

The X76F041 utilizes Xicor's proprietary Direct Write™ cell, providing a minimum endurance of 100,000 cycles per sector and a minimum data retention of 100 years.

7

FUNCTIONAL DIAGRAM



7002 ILL F01

PIN DESCRIPTION

Serial Data Input/Output (SDA)

SDA is a true three state serial data input/output pin. During a read cycle, data is shifted out on this pin. During a write cycle, data is shifted in on this pin. In all other cases this pin is in a high impedance state.

Serial Clock (SCL)

The Serial Clock controls the serial bus timing for data input and output.

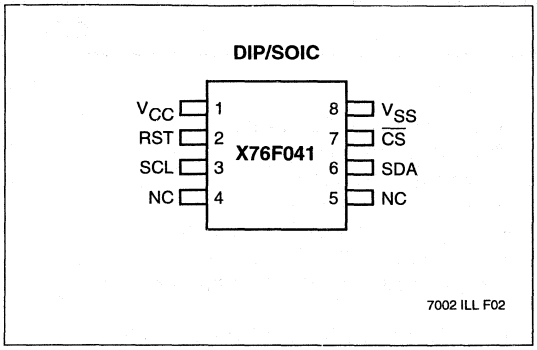
Chip Select ($\overline{CS}$)

When $\overline{CS}$ is HIGH, the X76F041 is deselected and the SDA pin is at high impedance and unless an internal write operation is underway the X76F041 will be in the standby power mode. $\overline{CS}$ LOW enables the X76F041, placing it in the active power mode.

Reset (RST)

RST is a device reset pin. When RST is pulsed HIGH while $\overline{CS}$ is LOW the X76F041 will output 32 bits of fixed data which conforms to the ISO standard for "synchronous response to reset". $\overline{CS}$ must remain LOW and the part must not be in a write cycle for the response to reset to occur. If at any time during the response to reset $\overline{CS}$ goes HIGH, the response to reset will be aborted and the part will return to the standby mode.

PIN CONFIGURATION



Symbol	Description
$\overline{CS}$	Chip Select Input
SDA	Serial Data Input/Output
RST	Reset Input
SCL	Serial Clock Input
V_{SS}	Ground
V_{CC}	Supply Voltage
NC	No Connect

7002 FRM T01

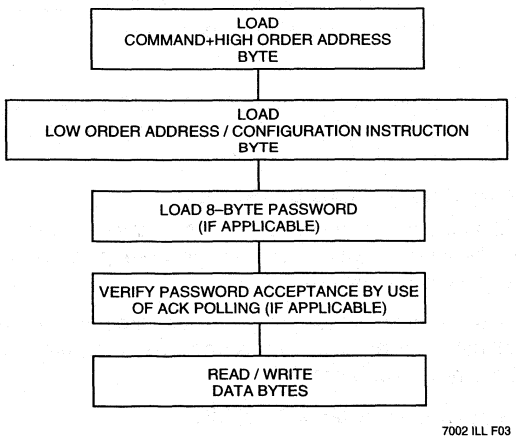
DEVICE OPERATION

There are three primary modes of operation for the X76F041; READ, WRITE and CONFIGURATION. The READ and WRITE modes may be performed with or without an 8-byte password. The CONFIGURATION mode always requires an 8-byte password.

The basic method of communication is established by first enabling the device ($\overline{CS}$ LOW), generating a start condition and then transmitting a command and address field followed by the correct password (if configured to require a password). All parts will be shipped from the factory in the non-password mode. The user must perform an ACK Polling routine to determine the validity of the password and start the data transfer (see Acknowledge Polling). Only after the correct password is accepted and an ACK Polling has been performed can the data transfer occur.

To ensure correct communication, RST must remain LOW under all conditions except when initiating a "Response to Reset sequence".

Figure 1. X76F041 Device Operation



Data is transferred in 8-bit segments, with each transfer being followed by an ACK, generated by the receiving device.

If the X76F041 is in a nonvolatile write cycle a "no ACK" (SDA HIGH) response will be issued in response to loading of the command + high order address byte. If a stop condition is issued prior to the nonvolatile write cycle the write operation will be terminated and the part will reset and enter into a standby mode.

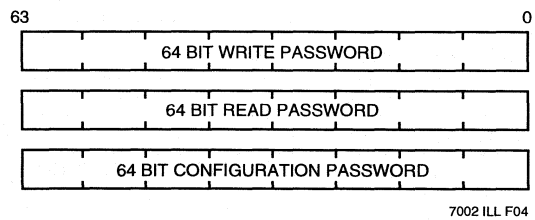
The basic sequence is illustrated in Figure 1.

After each transaction is completed, the X76F041 will reset and enter into a standby mode. This will also be the response if an attempt is made to access any limited array.

Password Registers

The three passwords, Read, Write and Configuration are stored in three 64 bit Write Only registers as illustrated in figure 2.

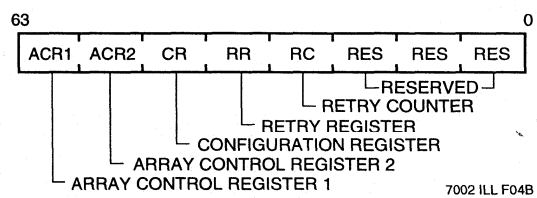
Figure 2. Password Registers



Device Configuration

Five 8-Bit configuration registers are used to configure the X76F041. These are shown in figure 3.

Figure 3. Configuration Registers

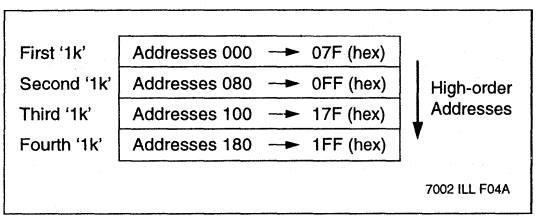


Array Control

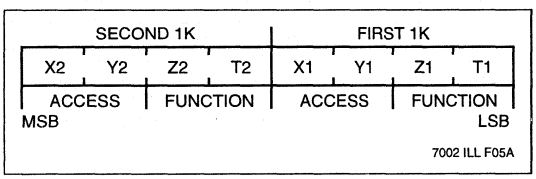
The four 1K arrays, are each programmable to different levels of access and functionality. Each array can be programmed to require or not require the read/write passwords. The functional options are:

- Read and Write Access.
- Read access with all write operations locked out.
- Read access and program only (writing a "1" to a "0"). If an attempt to change a "0" to a "1" occurs the X76F041 will reset, issue a "no ACK" and enter the standby power mode.
- No read or write access to the memory. Access only through use of the configuration password.

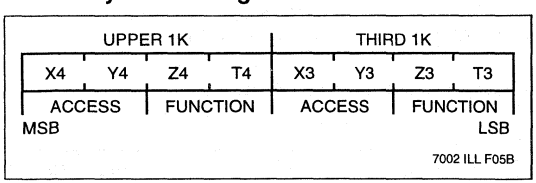
Array Map



8 Bit Array Control Register 1



8 Bit Array Control Register 2



Functional Bits

Z	T	FUNCTIONALITY
0	0	READ AND WRITE UNLIMITED
1	0	READ ONLY, WRITE LIMITED
0	1	PROGRAM & READ ONLY, ERASE LIMITED
1	1	NO READ OR WRITE, FULLY LIMITED

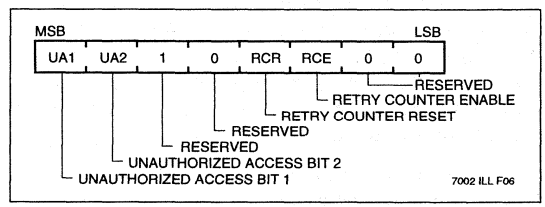
7002 FRM T02

Access Bits

X	Y	READ PASSWORD	WRITE PASSWORD
0	0	NOT REQUIRED	NOT REQUIRED
1	0	NOT REQUIRED	REQUIRED
0	1	REQUIRED	NOT REQUIRED
1	1	REQUIRED	REQUIRED

7002 FRM T03

8-Bit Configuration Register



Unauthorized Access Bits (UA1, UA2):

1 0

Access is forbidden if retry register equals the retry counter (provided that the retry counter is enabled) and no further access of any kind will be allowed.

0 1, 0 0, 1 1

Only configuration operations are allowed if the retry register equals the retry counter (provided that the retry counter is enabled).

Retry Counter Reset Bit (RCR):

If the retry counter reset bit is a "1" then the retry counter will be reset following a correct password, provided the retry counter is enabled.

If the retry counter reset bit is a "0" then the retry counter will not be reset following a correct password, provided the retry counter is enabled.

Retry Counter Enable Bit (RCE):

If the Retry counter enable bit is a "1", then the retry counter is enabled. An initial comparison between the retry register and retry counter determines whether the number of allowed incorrect password attempts has been reached. If not, the protocol continues and in case of a wrong password, the retry counter is incremented by one. If the password is correct then the retry counter will either be reset or unchanged, depending on the reset bit.

The retry register must have a higher value than the retry counter for correct device operation. If the retry counter value is larger than the retry register and the retry counter is enabled, the device will wrap around allowing up to an additional 255 incorrect access attempts.

If the Retry counter enable bit is a "0", then the retry counter is disabled.

Retry Register/Counter

Both the retry register and retry counter are accessible in the configuration mode and may be programmed with a value of 0 to 255.

The difference between the retry register and the retry counter is the number of access attempts allowed, therefore the retry counter must be programmed to a smaller value than the retry register to prevent wrap around.

DEVICE PROTOCOL

The X76F041 supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter, and the receiving device as the receiver. The device controlling the transfer is a master and the device being controlled is the slave. The master will always initiate data transfers, and provide the clock for both transmit and receive operations. Therefore, the X76F041 will be considered a slave in all applications.

Start Condition

All commands except for response to reset are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The X76F041 continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

Figure 4. Data Validity During Write

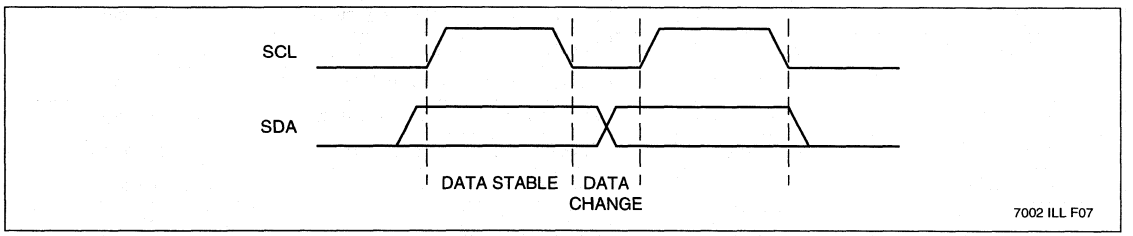
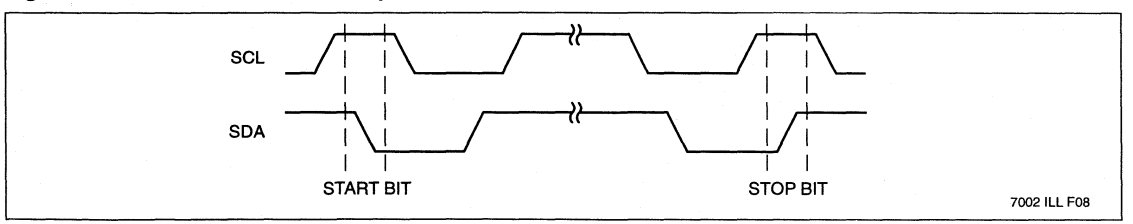


Figure 5. Definition of Start and Stop



NOTE: The part requires the SCL input to be LOW during non-active periods of operation. In other words, the SCL will need to be LOW prior to any START condition and LOW after a STOP condition. This is also reflected in the timing diagram.

Stop Condition

All communications must be terminated by a stop condition, which is a LOW to HIGH transition of SDA when SCL is HIGH. A stop condition can only be issued after the transmitting device has released the bus.

Acknowledge

Acknowledge is a software convention used to indicate successful data transfer. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data.

OPERATIONAL MODES

THE FIRST BYTE IN THE PROTOCOL	THE SECOND BYTE IN THE PROTOCOL	COMMAND DESCRIPTION	PASSWORD USED:
0 0 0XXXXA	Write address	Write (Sector)	Write
0 0 1XXXXA	Read address	Read (Random / Sequential)	Read
0 1 0XXXXA	Write address	Write (Sector)	Configuration
0 1 1XXXXA	Read address	Read (Random / Sequential)	Configuration
1 0 0XXXXX	0 0 0 0 0 0 0 0	Program write-password	Write
1 0 0XXXXX	0 0 0 1 0 0 0 0	Program read-password	Read
1 0 0XXXXX	0 0 1 0 0 0 0 0	Program configuration-password	Configuration
1 0 0XXXXX	0 0 1 1 0 0 0 0	Reset write password (all 0's)	Configuration
1 0 0XXXXX	0 1 0 0 0 0 0 0	Reset read password (all 0's)	Configuration
1 0 0XXXXX	0 1 0 1 0 0 0 0	Program configuration registers	Configuration
1 0 0XXXXX	0 1 1 0 0 0 0 0	Read configuration registers	Configuration
1 0 0XXXXX	0 1 1 1 0 0 0 0	Mass program	Configuration
1 0 0XXXXX	1 0 0 0 0 0 0 0	Mass erase	Configuration
All the rest		Reserved	

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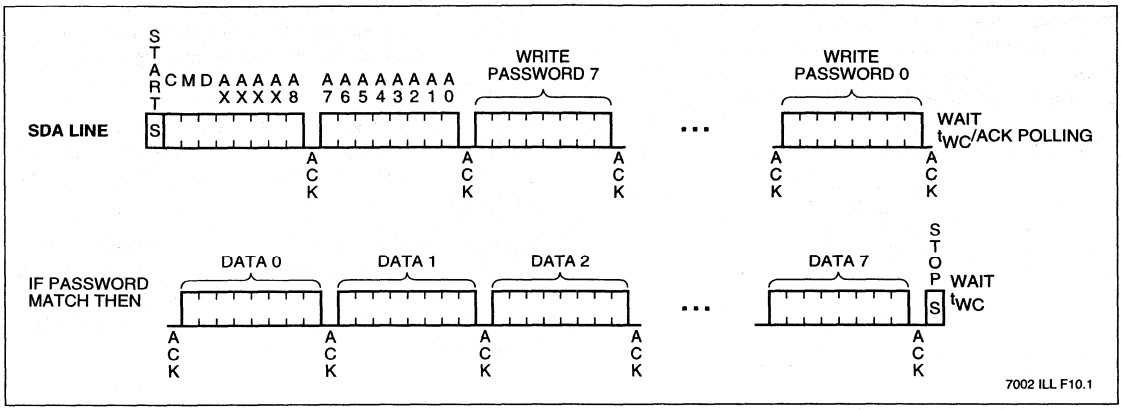
WRITE OPERATION

Sector Write

The Sector Write mode requires issuing the 3-bit write command followed by the address, password if required and then the data bytes transferred as illustrated in Figure 6. Eight bytes must be transferred. After the last byte to be transferred is acknowledged, a stop condition is issued, which starts the nonvolatile write cycle. If more than 8 bytes are transferred the data will wrap around and previous data will be overwritten. All data will be written to the same sector as defined by A_8–A_3.

Figure 6. Sector Write



ACK Polling

Once a stop condition is issued to indicate the end of the host's write sequence, the X76F041 initiates the internal nonvolatile write cycle. In order to take advantage of the typical 5ms write cycle, ACK polling can be initiated immediately. This involves issuing the Start condition followed by the new command code of eight bits (1st byte of the protocol). If the X76F041 is still busy with the nonvolatile write operation, it will issue a "no ACK" in response. If the nonvolatile write operation has completed, an "ACK" will be returned and the host can then proceed with the rest of the protocol. Refer to the following flow:

ACK Polling Sequence

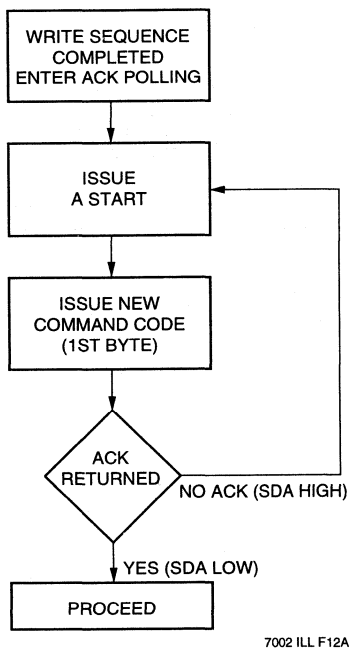
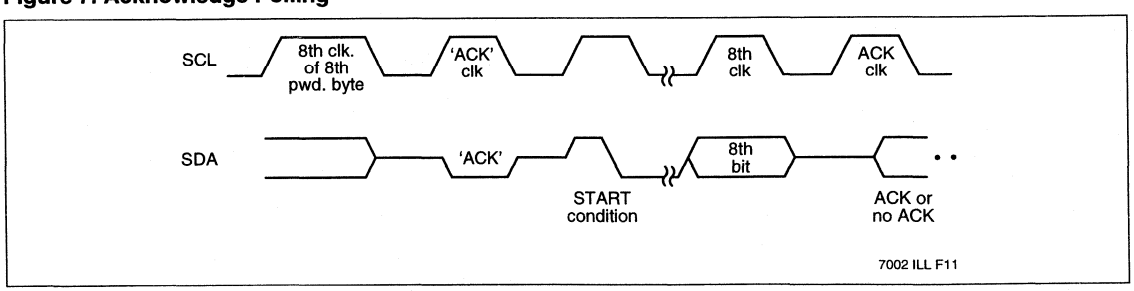


Figure 7. Acknowledge Polling



After a password sequence, there is always a nonvolatile write cycle. In order to continue the transaction, the X76F041 requires the master to perform an ACK polling with the specific code of C0h. As with regular acknowledge polling the user can either time out for 10ms, and then issue the ACK polling once, or continuously loop as described in the flow.

As with regular acknowledge polling, if the user chooses to loop, then as long as the nonvolatile write cycle is active, a no ACK will be issued in response to each polling cycle.

If the password that was inserted was correct, then an "ACK" will be returned once the nonvolatile write cycle is over, in response to the ACK polling cycle immediately following it.

If the password that was inserted was incorrect, then a "no ACK" will be returned even if the nonvolatile write cycle is over. Therefore, the user cannot be certain that the password is incorrect until the 10ms write cycle time has elapsed.

READ OPERATION

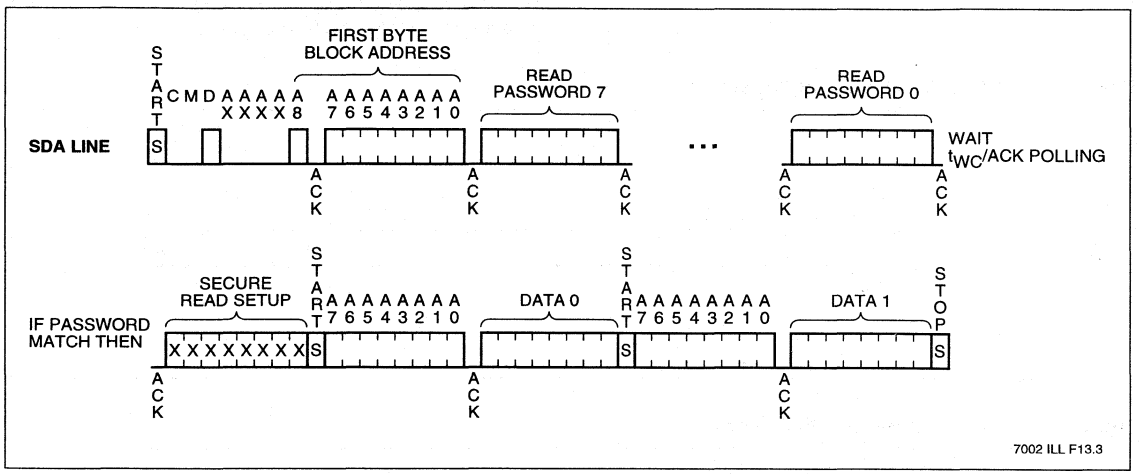
Random Read with Password

Random read with password operations are initiated with a START command followed by the read command and the address of the first byte of the block in which data is to be read:

Block 0 = 000h
Block 1 = 080h
Block 2 = 100h
Block 3 = 180h

This is followed by the eight byte read password sequence which includes the 10ms wait time and the password acknowledge polling sequence. If the password is accepted an "ACK" will be returned followed by eight bits of "secure read setup" which is to be ignored. At this point a START is issued followed by the address and data to be read within the original 1K block. See figure 8. Once the first byte has been read, another start can be issued followed by a new 8-bit address. Random reads are allowed only within the original 1K-bit block. To access another 1K-bit block, a stop must be issued followed by a new command/block address/password sequence.

Figure 8. Random Read with Password



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Random Read without Password

Random read operations without a password do not require the first byte block initiation address. To perform a random read without password, a START is followed by the read command plus address location of the byte to be read. This is followed by an "ACK" and the eight bits of data to be read. Other bytes within the same 1K-bit block may be read by issuing another START followed by a new 8-bit address as shown in figure 9.

Sequential Read

Once past the password acceptance sequence (when required) and "secure read setup", the host can read sequentially within the originally addressed 1K-bit array. The data output is sequential, with the data from address n followed by the data from address n+1. The address counter for read operations increments the address, allowing the 1K memory contents to be serially read during one operation. At the end of the address space (address 127), the counter "rolls over" to address space 0 within the 1K Block and the X76F041 continues to output data for each acknowledge received. Refer to figure 10 for the address, acknowledge and data transfer sequence. An acknowledge must follow each 8-bit data transfer. After the last bit has been read, a stop condition is generated without a preceding acknowledge.

Figure 9. Random Read without Password

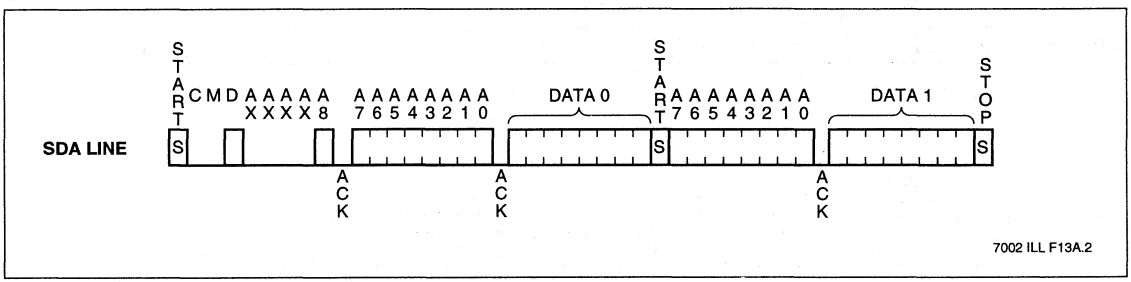
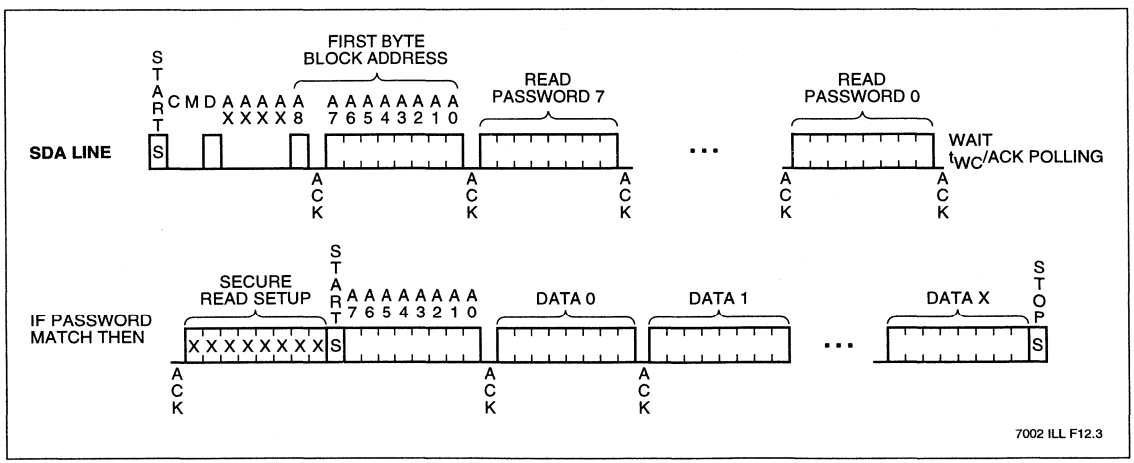


Figure 10. Sequential Read with Password



CONFIGURATION OPERATIONS

Configuration commands generally require the configuration password. The exception is that programming a new read/write password requires the old read/write password and not the configuration password. In most cases these operations will be performed by the equipment manufacturer or end distributor of the equipment or card.

Configuration Read/Write

Configuration read/write allows access to all of the nonvolatile memory arrays regardless of the contents of the configuration registers. Access includes sector writes, random and sequential reads using the same format as normal reads and writes.

In general, the configuration read/write operation enables access to any memory location that may otherwise be limited. The configuration password, in this sense, is like a master key that can override the limits caused by the control partitioning of the arrays.

Figure 11. Configuration Write

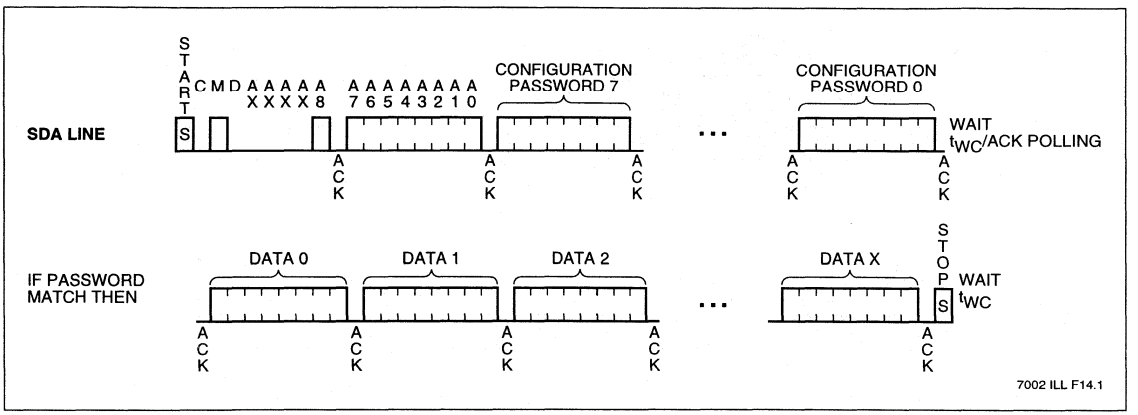
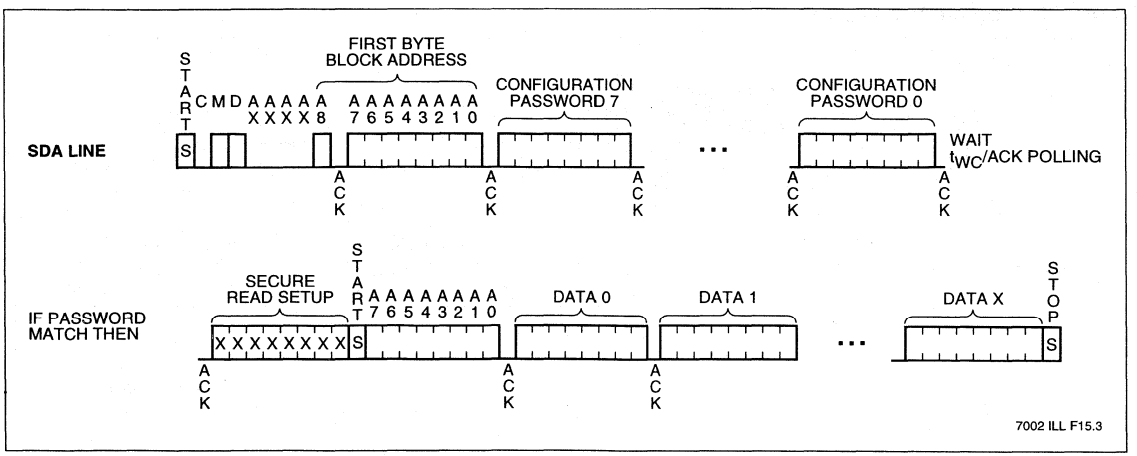


Figure 12. Configuration Sequential Read



Configuration of Passwords

The sequence in figure 14 will change (program) the write, read and configuration passwords. The programming of passwords is done twice prior to the nonvolatile write cycle in order to verify that the new password is consistent. After the eight bytes are entered in the second pass, a comparison takes place. A mismatch will cause the part to reset and enter into the standby mode and a "no ACK" will be issued.

There is no way to read the Read/Write/Configuration passwords.

Program Configuration Registers

This mode allows programming of the five configuration/control registers using the configuration password. The retry counter must be programmed with a value less than the retry register. If it is programmed with a value larger than the retry register there will be a wrap around.

Read Configuration Registers

This mode allows reading of the 5 configuration/control registers with the configuration password. It may be useful for monitoring purposes.

Figure 13. Configuration Random Read

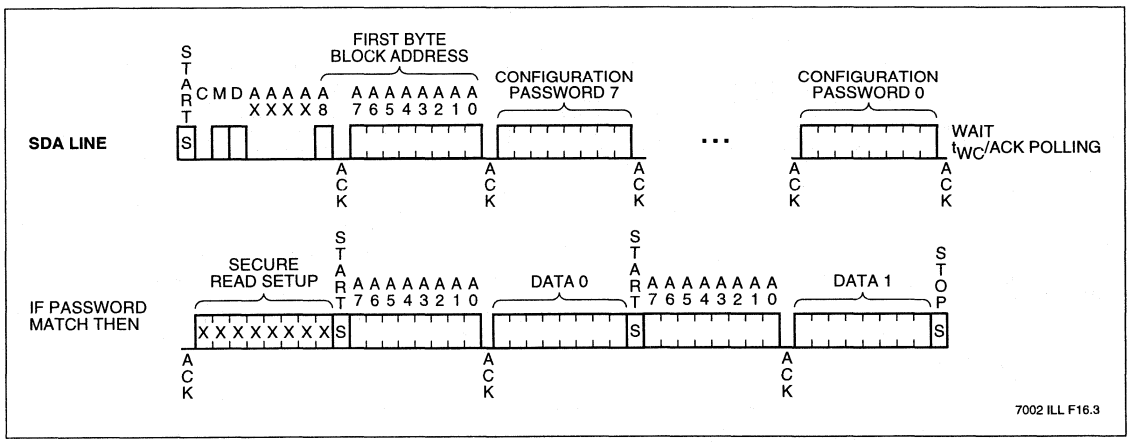
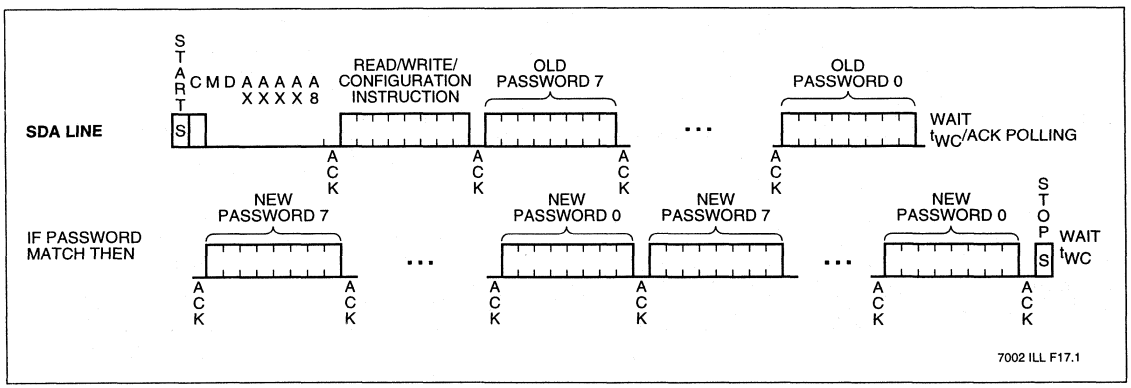


Figure 14. Program Passwords



Read Password Reset

This mode allows resetting of the READ password to all "0"s in case re-programming is needed and the old password is not known.

Write Password Reset

This mode allows resetting of the WRITE password to all "0"s in case re-programming is needed and the old password is not known.

Mass Program

This mode allows mass programming of the array, configuration registers and password to all "0"s using a special configuration command. All parts are shipped mass programmed.

Mass Erase

This mode allows mass erase of the array, configuration register and password to all "1"s using a special configuration command.

Figure 15. Program Configuration Registers

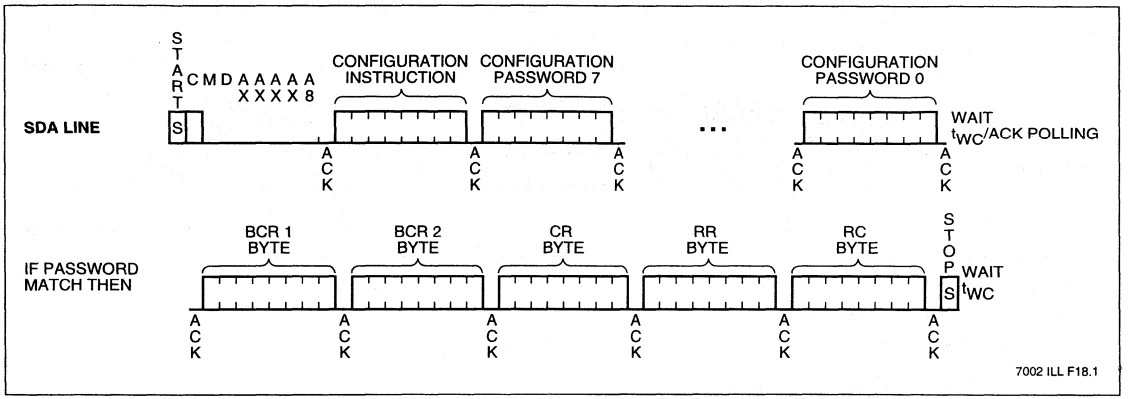


Figure 16. Read Configuration Registers

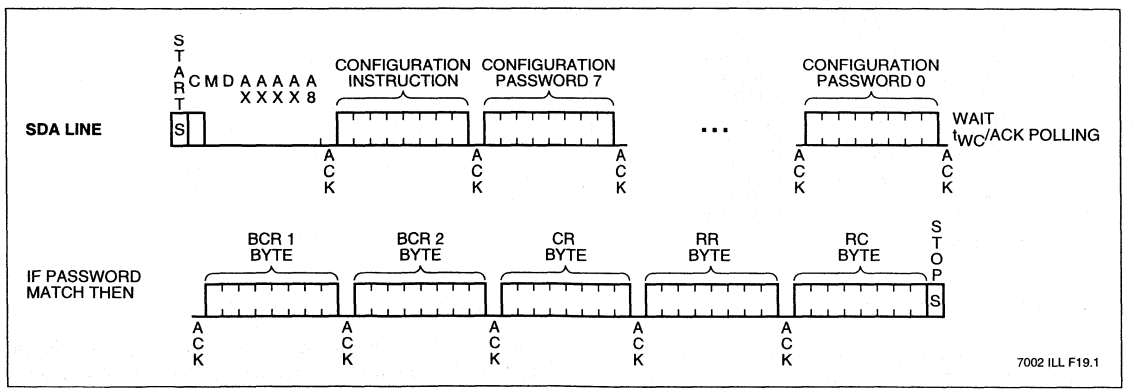


Figure 17. Read/Write Password Reset

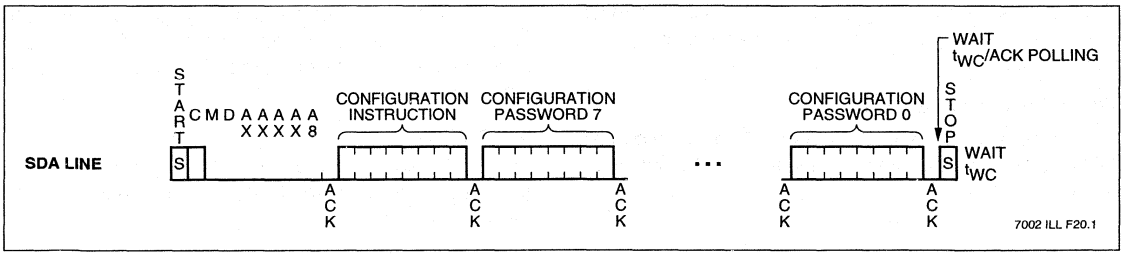
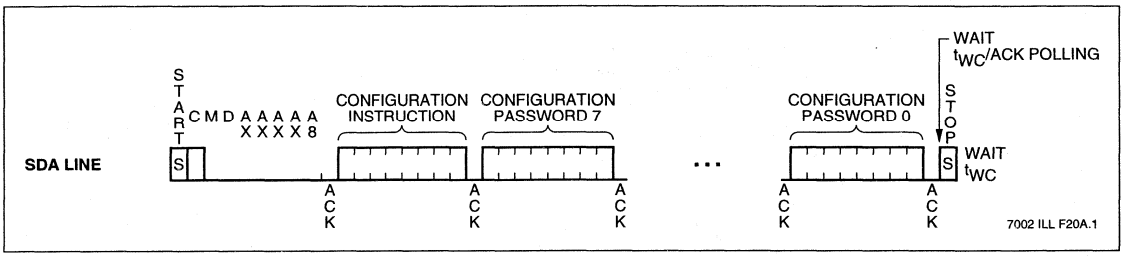


Figure 18. Mass Program/Erase



SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

ABSOLUTE MAXIMUM RATINGS*

Temperature under Bias ..... –65°C to +135°C
Storage Temperature ..... –65°C to +150°C
Voltage on any Pin with
Respect to V_{SS} ..... –1V to +7V
D.C. Output Current..... 5mA
Lead Temperature
(Soldering, 10 seconds) .....300°C

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temp	Min.	Max.
Commercial	0°C	+70°C
Extended	–20°C	+85°C

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Supply Voltage	Limits
X76F041	4.5V to 5.5V
X76F041 – 3	3V to 3.6V

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D.C. OPERATING CHARACTERISTICS (Over the recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
I_{CC1}	V_{CC} Supply Current (Read)		2	mA	$f_{SCL} = V_{CC} \times 0.1/V_{CC} \times 0.9$ Levels @ 1MHz, SDA = Open, RST = $\overline{CS}$ = V_{SS}
I_{CC2}(3)	V_{CC} Supply Current (Write)		3	mA	$f_{SCL} = V_{CC} \times 0.1/V_{CC} \times 0.9$ Levels @ 1MHz, SDA = Open, RST = $\overline{CS}$ = V_{SS}
I_{SB1}(1)	V_{CC} Supply Current (Standby)		100	µA	SCL = V_{SS}, $\overline{CS}$ = V_{CC} – 0.3V, SDA = Open, RST = V_{CC} = 5.5V
I_{SB2}(1)	V_{CC} Supply Current (Standby)		50	µA	SCL = V_{SS}, $\overline{CS}$ = V_{CC} – 0.3V, SDA = Open, RST = V_{SS}, V_{CC} = 3V
I_{LI}	Input Leakage Current		10	µA	$V_{IN} = V_{SS}$ to V_{CC}
I_{LO}	Output Leakage Current		10	µA	$V_{OUT} = V_{SS}$ to V_{CC}
V_{IL1}(2)	Input LOW Voltage	–0.5	$V_{CC} \times 0.3$	V	V_{CC} = 5.5V
V_{IH1}(2)	Input HIGH Voltage	$V_{CC} \times 0.7$	$V_{CC} + 0.5$	V	V_{CC} = 5.5V
V_{IL2}(2)	Input LOW Voltage	–0.5	$V_{CC} \times 0.1$	V	V_{CC} = 3.0V
V_{IH2}(2)	Input HIGH Voltage	$V_{CC} \times 0.9$	$V_{CC} + 0.5$	V	V_{CC} = 3.0V
V_{OL}	Output LOW Voltage		0.4	V	I_{OL} = 2mA
V_{OH}	Output HIGH Voltage	$V_{CC} – 0.8$		V	I_{OH} = –1mA

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CAPACITANCE T_A = +25°C, f = 1MHz, V_{CC} = 5V

Symbol	Test	Max.	Units	Conditions
C_{OUT}(3)	Output Capacitance (SDA)	10	pF	$V_{I/O}$ = 0V
C_{IN}(3)	Input Capacitance (RST, SCL, $\overline{CS}$)	10	pF	V_{IN} = 0V

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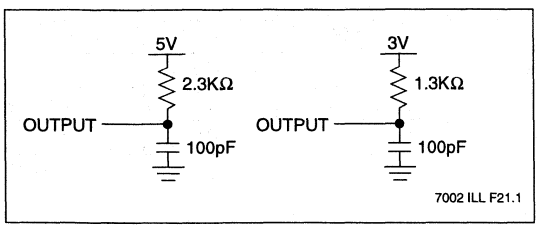
NOTES: (1) Must perform a stop command after a read command prior to measurement
(2) V_{IL} min. and V_{IH} max. are for reference only and are not tested.
(3) This parameter is periodically sampled and not 100% tested.

EQUIVALENT A.C. LOAD CIRCUIT



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A.C. TEST CONDITIONS

Input Pulse Levels	$V_{CC} \times 0.1$ to $V_{CC} \times 0.9$
Input Rise and Fall Times	10ns
Input and Output Timing Level	$V_{CC} \times 0.5$
Output Load	100pF

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A.C. CHARACTERISTICS (Over recommended operating conditions, unless otherwise specified)

Read & Write Cycle Limits

Symbol	Parameter	Min.	Max.	Units
f_{SCL}	SCL Clock Frequency		1	MHz
TI	Noise Suppression Time Constant at SCL & SDA Inputs		20	ns
t_{DV}	SCL HIGH to SDA Data Valid		450	ns
t_{LOW}	Clock LOW Period	500		ns
t_{HIGH}	Clock HIGH Period	500		ns
t_{STAS1}	Start Condition Setup Time to Rising Edge of SCL	150		ns
t_{STAS2}	Start Condition Setup Time to Falling Edge of SCL	150		ns
t_{STAH1}	Start Condition Hold Time to Rising Edge of SCL	50		ns
t_{STAH2}	Start Condition Hold Time to Falling Edge of SCL	50		ns
t_{STPS1}	Stop Condition Setup Time to Rising Edge of SCL	150		ns
t_{STPS2}	Stop Condition Setup Time to Falling Edge of SCL	150		ns
t_{STPH1}	Stop Condition Hold Time to Rising Edge of SCL	50		ns
t_{STPH2}	Stop Condition Hold Time to Falling Edge of SCL	50		ns
$t_{HD:DAT}$	Data in Hold Time	10		ns
$t_{SU:DAT}$	Data in Setup Time	150		ns
t_{RSCL}[4]	SCL Rise Time		90	ns
t_{FSCL}[4]	SCL Fall Time		90	ns
t_R[4]	SDA, $\overline{CS}$, RST Rise Time		90	ns
t_F[4]	SDA, $\overline{CS}$, RST Fall Time		90	ns
t_{DH}	Data Out Hold Time	0		ns
t_{HZ1}	SCL LOW to High Impedance		150	ns
t_{LZ}	SCL HIGH to Output Active	0		ns
t_{VCCS}	V_{CC} to $\overline{CS}$ Setup Time	5		ms
$t_{SU:CS}$	$\overline{CS}$ Setup Time	200		ns
$t_{HD:CS}$	$\overline{CS}$ Hold Time	100		ns
t_{HZ2}	$\overline{CS}$ Deselect Time		150	ns
$t_{SU:SCL}$	SCL Setup Time to $\overline{CS}$ LOW after Power Up	200		ns
t_{RST}	RST HIGH Time	1500		ns
$t_{SU:RST}$	RST Setup Time	500		ns
$f_{SCL:RST}$	SCL Frequency During Response to Reset		1	MHz
$t_{LOW:RST}$	SCL LOW Time During Response to Reset	500		ns
$t_{HIGH:RST}$	SCL HIGH Time During Response to Reset	500		ns
t_{PD}	SCL LOW to SDA Valid During Response to Reset		450	ns
t_{NOL}	RST to SCL Non-Overlap	500		ns
t_{WC}	Nonvolatile Write Cycle		10	ms

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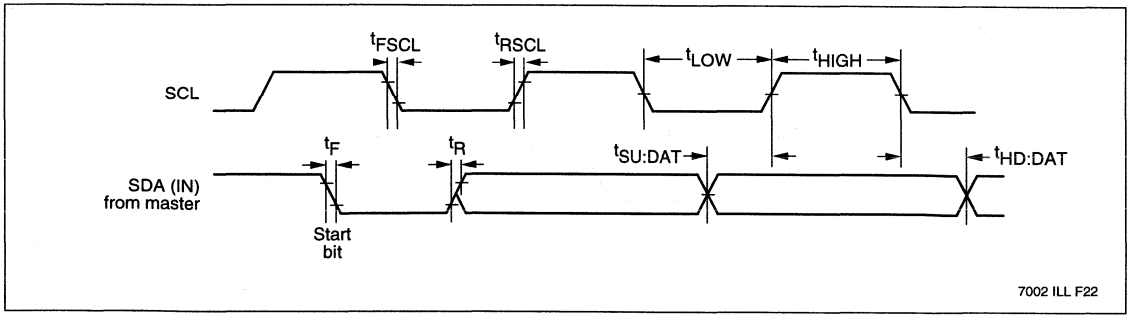
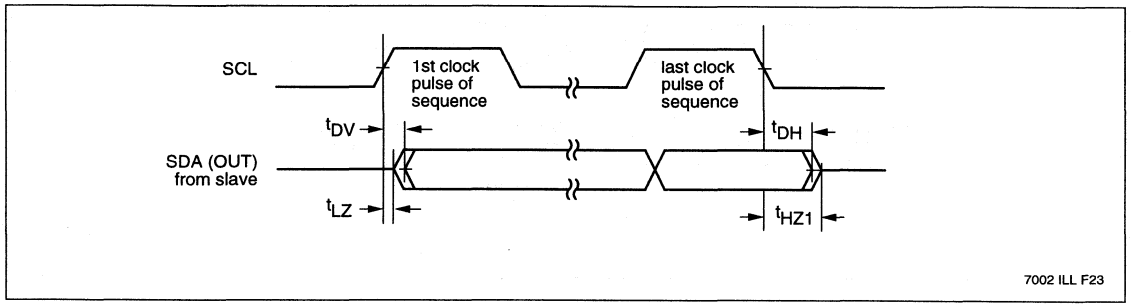
NOTES: (4) This parameter is periodically sampled and not 100% tested.

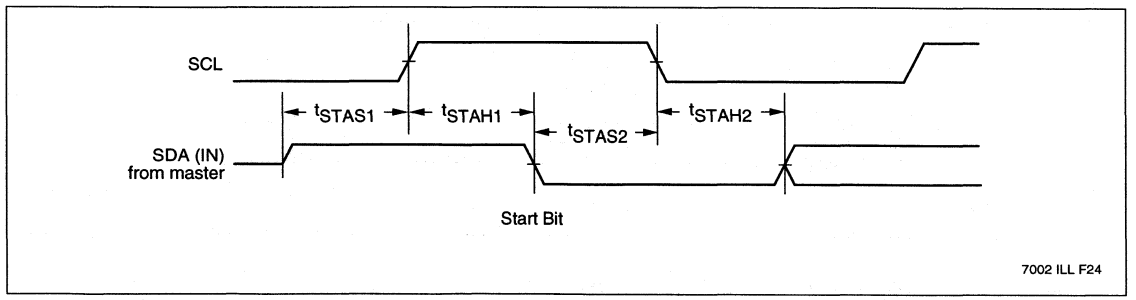
Bus Timing(1) — SDA Driven by the Bus Master



Bus Timing(2) — SDA Driven by the Slave



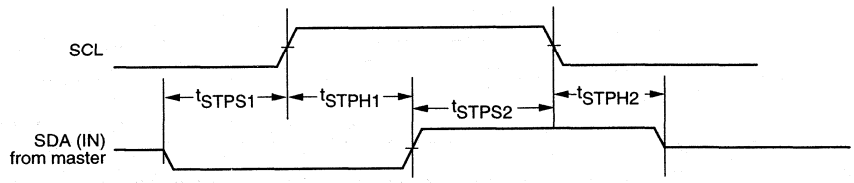
START Condition Timing



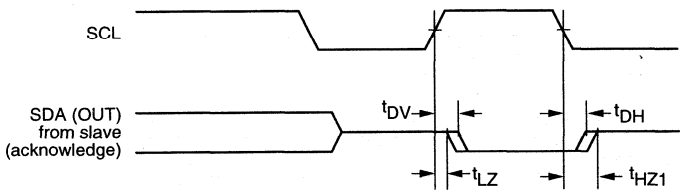
NOTES: (1) The master may issue a STOP condition at any given time in which it is driving the SDA line. In other words, when the part is sending ACK or data the master may NOT issue a STOP condition. The part will not respond to any such attempt which also causes bus contention. At any other time, a STOP condition will cause the part to reset and stop (enter a stand-by mode). Write operations will terminate prior to entering the stand-by mode.

(2) When the part drives the SDA line, it will tri-state the bus only after the last bit of the sequence. In other words, after the 8th bit of a byte that is read or after ACK between incoming bytes. In all other cases when the part drives the bus (between successive bits) it will continue to drive the bus also during the clock LOW periods.

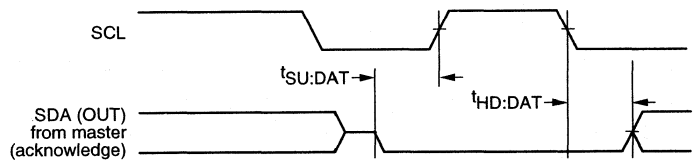
STOP Condition Timing



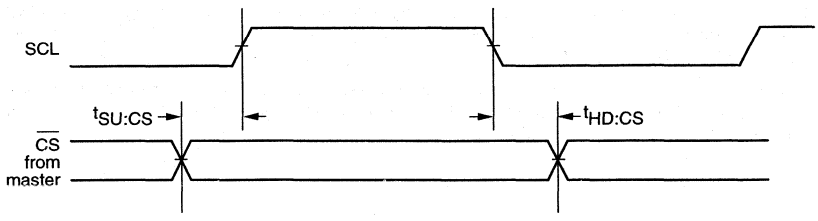
Acknowledge Response from Slave (Same Timing as Data Out)



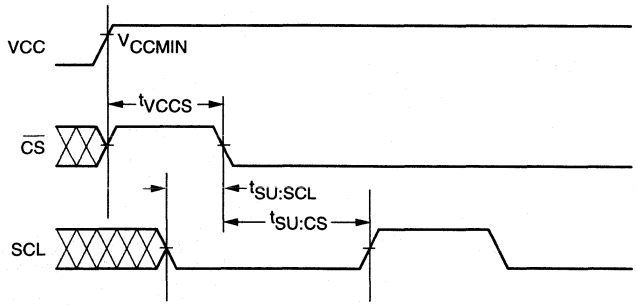
Acknowledge Response from Master



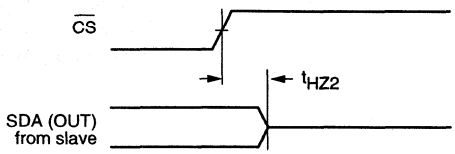
$\overline{CS}$ Timing Diagram (Selecting/Deselecting the Part)



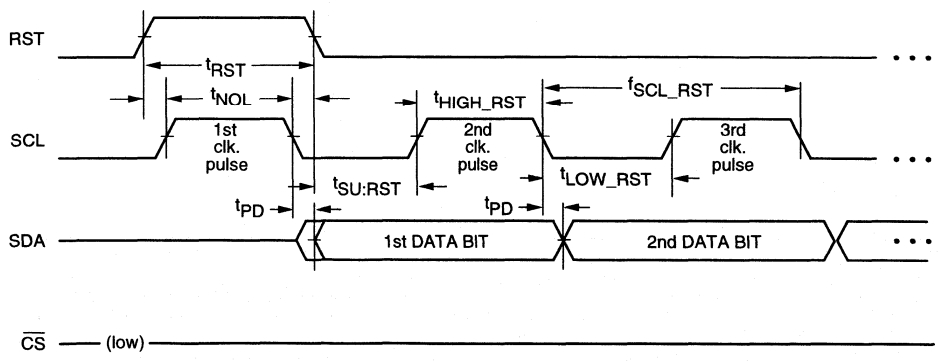
V_{CC} to $\overline{CS}$ Setup Timing Diagram



$\overline{CS}$ Deselect



RST Timing Diagram — Response to a Synchronous Reset (ISO)



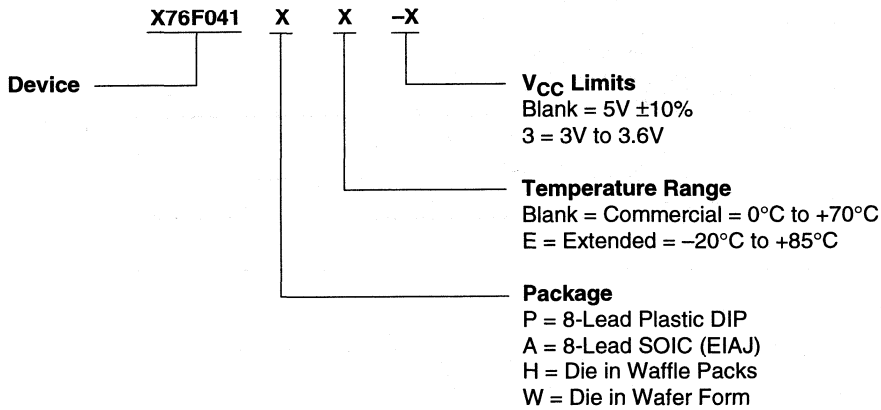
NOTES: (1) The reset operation results in an answer from the part containing a header transmitted from the part to the master. The header has a fixed length of 32 bits and begins with two mandatory fields of eight bits : H1 and H2.

(2) The chronological order of transmission of the information bits shall correspond to bit identification b1 to b32 with the LEAST significant bit transmitted first.

(3) The current values are:

H1 : 19 h
H2 : 55 h
H3 : AA h
H4 : 55 h

ORDERING INFORMATION



3807-2.3 12/4/95 T12/C0/D0 NS

XK68 SLIC® E²

68HC11/X68CXX SLIC E²PROM Development System

FEATURES

- 68HC11 Microcontroller
- 8MHz system clock
- 8Kx8 intelligent E²PROM (X68C64 SLIC E² or X68C75 optional)
- DOS based XSLIC communication/configuration software diskette
- Serial communication port (RS232 DB-9)
- Extended memory support
- Emulation mode
  - —Expansion connectors for 68HC11
  - —ROM emulator
  - —Interface option to target system
- Prototype area
- 4" x 5.5" form factor
- Power source alternatives: Battery/Power Jack/ Target system

SOFTWARE DISKETTE INCLUDES:

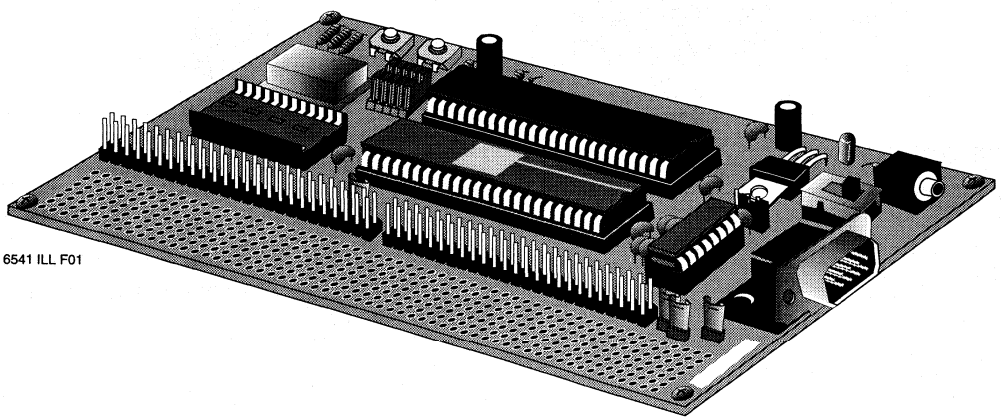
- README
- XSLIC.EXE
- SLIC.AS
- SLIC.HEX
- SLIC.DOC
- SLICNOTE.DOC
- XK68.SCH (ORCAD SCHEMATICS)
- XICOR.LIB (ORCAD LIBRARY)

DESCRIPTION

The XK68 is an 68HC11 based development system for the X68C64 and X68C75 SLIC (Self-Loading Integrated Code) E² products. The system allows users to easily integrate their code into the X68CXX SLIC E² product and speed up the design process. The prototype area on the board is ideal for small custom circuit design. Three power source options are available: external power jack, single 9-Volt battery, or from the target system. Two push-button switches are used to reset the 68HC11 or to generate an external interrupt.

The XK68 system can operate in two modes: stand-alone, and ROM emulation. In stand-alone mode the XK68 internally generates all of the necessary signals and operates independently.

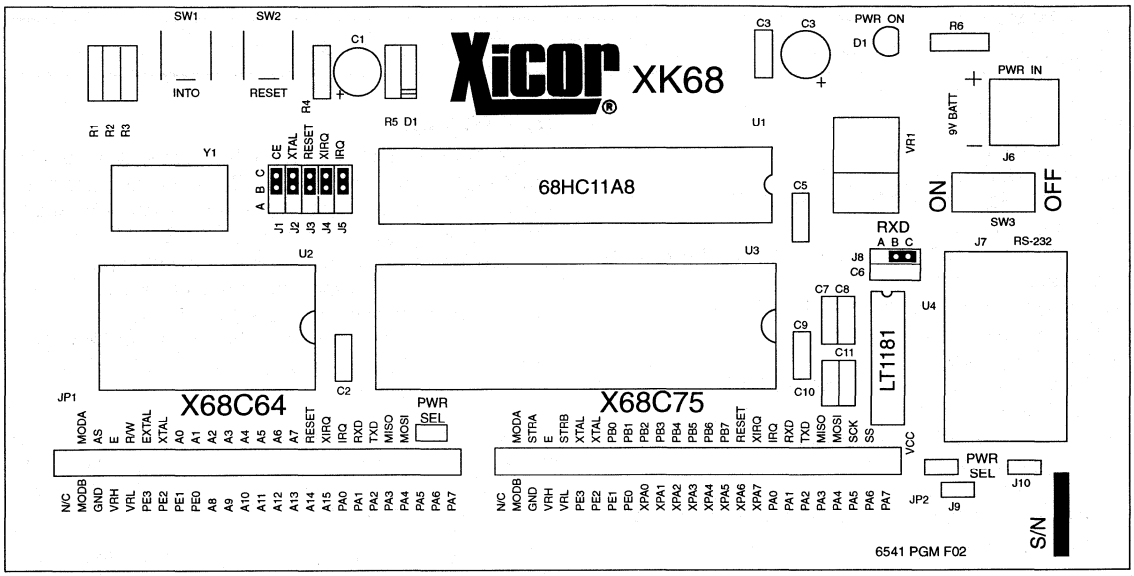
The ROM emulation mode employs one of the two 50-pin headers (J1 and J2) to interface to the target system. The headers carry all of the microcontroller signals. Depending on the SLIC E² type integrated on the board, one of the appropriate connectors is used to plug into the microcontroller socket on the target system through the 50-pin shielded flat ribbon cable provided with the XK68 system.



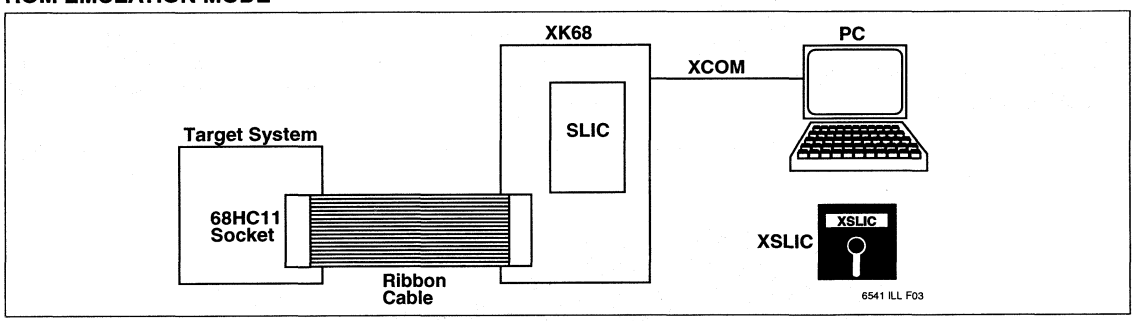
6541 ILL F01

8

SLIC® E² and CONCURRENT READ WRITE™ are trademarks of Xicor, Inc.



ROM EMULATION MODE



XSLIC SCREEN SHOWN FROM MONITOR

```
XSLIC Rev. 3.6
   X68C64 SLIC* E² Rev. 1.0 * SLIC is a
   trademark of Xicor, Inc. copyright © 1993
   by Xicor, Inc. Milpitas, CA
         Download
         BPR
         Verify
         Filename " "
         Reset
         ReLocate
         Setup
         Quit
         Please make selection
```

The XSLIC is a DOS based application program with a built in user interface and communication driver. It manages the programming of the SLIC E² devices by converting the user's file from Intel HEX or Motorola S formats to Xicor XCOM format and downloads them to the SLIC E² device.

XK76

X76F041 Development System (General Purpose Version)

CONTENTS

- **3.5" Diskette, PC Format, Double Density**
  - **—Executable Development System Software**
  - **—Source C Interface Routines**
- **Development Board**
- **Interface Cable**
- **Users Guide**
- **Two X76F041 DIP Parts**

FEATURES

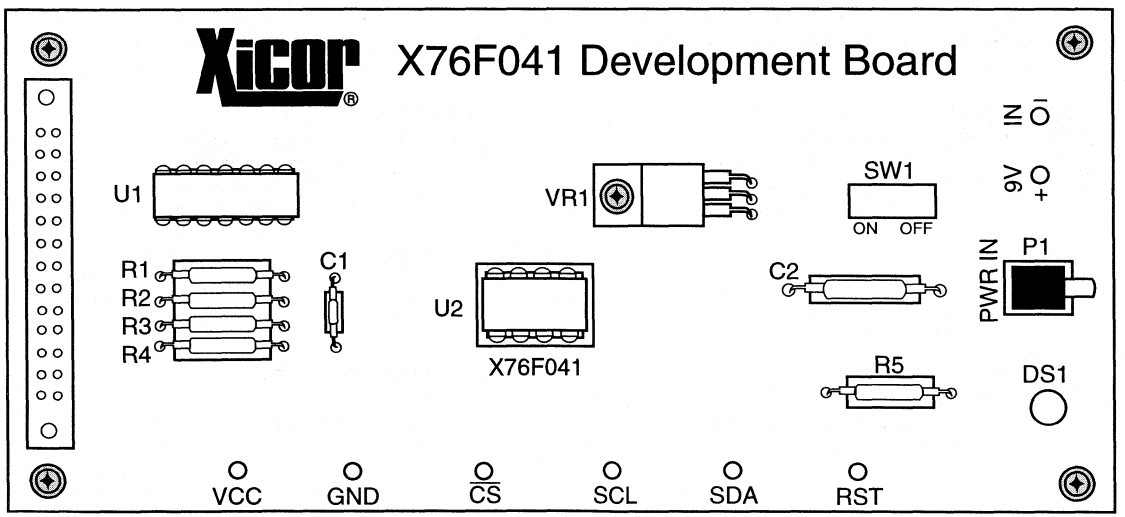
- **Simple PC Based Platform**
- **Menu Driven User Interface**
- **Programming Editor for Memory Arrays**
- **Provides Complete Control of PASS™ SecureFlash Operation**
  - **—Password Entry and Programming**
  - **—Configuration Registers Programming**
- **Simplifies Design and Debug Process**
- **Supports Three Modes of Operation**

Evaluation Mode—uses an X76F041 mounted on the development board to demonstrate the capabilities and suitability of the part for a particular application. Provides an understanding of the part in minutes not hours.

Prototype Mode—does not use the X76F041 on the development board, but rather controls an X76F041 placed in the Target System (Prototype PC board or ISO Card Reader). Connections between the development board and the Target System are made through the SDA, SCL, $\overline{CS}$, and RST terminals provided. This mode provides an effective debug capability. Memory array and register values of X76F041s residing in the Target Systems can be monitored and set by the designer.

Programming Mode—this provides a capability for programming parts mounted on the development board or residing in the Target System.

Development Board Layout



2609 ILL F01.1

PASS is a trademark of Xicor, Inc.

DESCRIPTION

The XK76 Development System has been designed to be a tool that significantly reduces development time of applications using the Xicor X76F041 PASS SecureFlash. It greatly simplifies the task of understanding, evaluating and designing-in the part.

The development system consists of a circuit board, two feet of flat ribbon cable with adjacent connectors, two X76F041's, and a 3.5" software diskette. It is easy to use and simple to set-up, operating with any PC compatible computer that is equipped with a parallel printer port. The development board is powered using a standard 9-Volt battery, power jack or DC power supply.

The XK76 is a tool that enables users to quickly and easily understand the capabilities of the X76F041. It provides an ideal platform for evaluating the suitability of the part for a particular application. The development system demonstrates the various levels of security available on the X76F041 by enabling the user to configure the part and then attempt to access it using one or none of the passwords.

The XK76 simplifies debug by controlling an X76F041 residing externally in a Target System (Prototype PC board or ISO Card Reader). Register and array values can be monitored and preset in-system by connecting the SDA, SCL, $\overline{CS}$, and RST terminals on the development board to the X76F041 in the Target System. The XK76 also provides the designer with the option of pre-programming parts before use in the Target System.

The status and values of the X76F041's registers and four memory arrays are represented on the PC using two graphical user interfaces. The MAIN interface is used to display the ISO identification number; enter, display, reset and program passwords; display and program configuration registers; and mass program/erase memory. The ARRAY interface is used to read the four memory arrays and enter the array programming editor. The various options in each interface are displayed using menus and selected using a single key input.

Development System's MAIN interface screen format

X76F041 PASSWORD ACCESS SECURITY SUPERVISOR

Configuration (Hex)	Write (Hex)	Read (Hex)
563A–89C3–2084–5760	6576–E798–251A–6554	3945–4890–03D4–4F9B

ACR1 (Hex)

D8

1st 1K – Read & Write
W & No R Password
2nd 1K – Read & Program
R & W Password

ACR2 (Hex)

F0

3rd 1K – Read & Write
No R or W Password
4th 1K – No Read or Write
R & W Password

CR (Hex)

2C

Device Kill – Off
Counter Reset – On
Counter Enable – On

RR (Dec)

3

RC (Dec)

1

ISO (Hex)

19-55-AA-55

W – Write Arrays
R – Read Arrays
C – Configuration Registers Program
E – Enter Password

P – Program Password
M – Mass Mode
S – Reset Password
Q – Quit

2609 ILL F02.3

Development System's ARRAY user interface screen format

X76F041 FOUR 128 x 8 MEMORY ARRAYS

	Write Password WRITE			Read Password READ	
000	C2989850573C69F6	A3C72153B7648910	35DA265237898422	84D5178A43321898	0lF
020	4897328F73543212	9379421598084765	E764569B74365355	A58682270647662F	03F
040	7419784A632764EF	897458952765E527	525A3267659785B6	532658659808563B	05F
060	73579899596CBF83	2098B95959880798	90A678568D9086B9	08909039357659C7	07F
080	----------	----------	----------	----------	09F
0A0	----------	----------	----------	----------	0BF
0C0	----------	----------	----------	----------	0DF
0E0	----------	----------	----------	----------	0FF
100	8867864F7D798798	78C2956766543292	B6362843290665D6	457627F237983427	11F
120	5798723665AF4798	6325675459983292	5433209985746492	7849332611326329	13F
140	7433005278194627	2191654D6D8C7257	1873662143219945	6436342833451901	15F
160	5347978D77657676	5A73268F72968765	78983276545C5762	32588C7253EB6786	17F
180	3267104576543875	43756FD76C678765	32908BDF79878FAD	6432DA776C980D30	19F
1A0	32139045E7578598	17630385A8653421	56479034215C8A6A	E21679D419859876	1BF
1C0	DF4A78754589435F	9847265793259806	65F980498FCFA679	806459787FE90237	1DF
1E0	6543987392537898	2FA786987A698257	6278F79865298273	2852F6686DA23429	1FF

Options : — ← ↑ ↓ → Move V - Verify M - Main Menu

2609 PGM F03.1

The software diskette contains two files; the development system's executable file and the basic source interface routines. The development system's executable file can run with any PC supporting DOS 3.0 or higher. The documented C source routines used to interface the PC with the X76F041 are provided to simplify the designers task of generating interface code and may be modified to match a particular application.

NOTES

XK76C

X76F041 Development System (Card Reader Version)

CONTENTS

- **Card Reader with Interface Cable**
- **3.5" Diskette, PC Format**
  - **—Executable Development System Software**
  - **—Source C Interface Routines**
  - **—Card Reader Schematic**
- **User Guide**
- **Two X76F041 Smartcards**

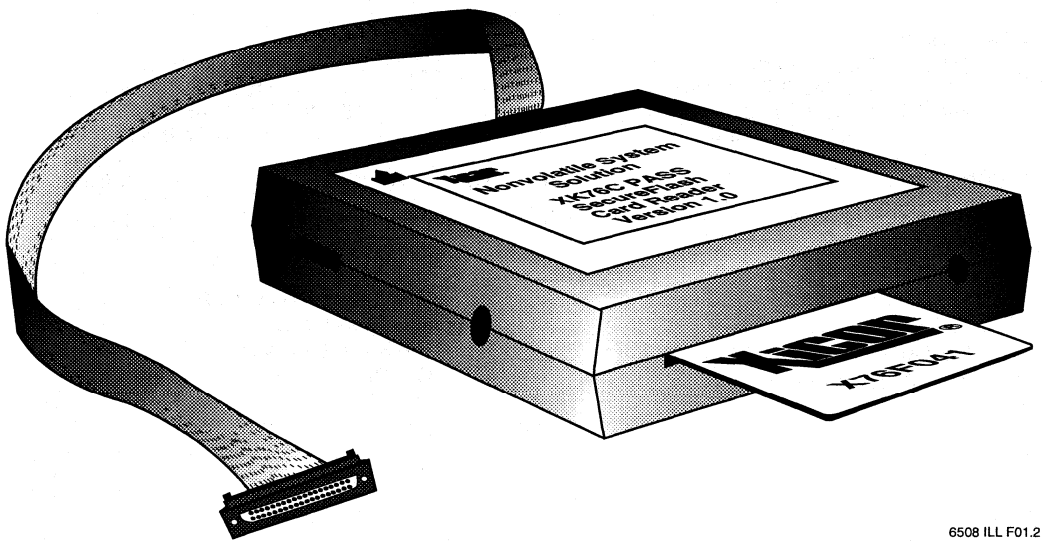
FEATURES

- **Simple PC Based Platform**
- **Menu Driven User Interface**
- **Programming Editor for Memory Arrays**
- **Provides Complete Control of PASS™ SecureFlash Device Operation**
  - **—Password Entry and Programming**
  - **—Configuration Registers Programming**
- **Simplifies Design and Debug Process**
- **Supports Three Stages of Development**

Evaluation—the System provides a comprehensive platform for evaluating the suitability of the X76F041 for a smartcard application. It allows for a complete understanding of the device in minutes not hours, by utilizing the card reader and graphical user interface software.

Appraisal—the Development System contains the hardware and generic software routines required to appraise the "smartcard solution". It saves the associated costs (time and money) of developing small numbers of hardware units and writing device interface software for the application.

Prototype—the XK76C System simplifies design by supplying card reader schematic and application code. The Development System is invaluable during debug for presetting and verifying the X76F041 configuration and data.



6508 ILL F01.2

PASS is a trademark of Xicor, Inc.

6508-1.3 1/10/96 T10/C0/D4 NS

DESCRIPTION

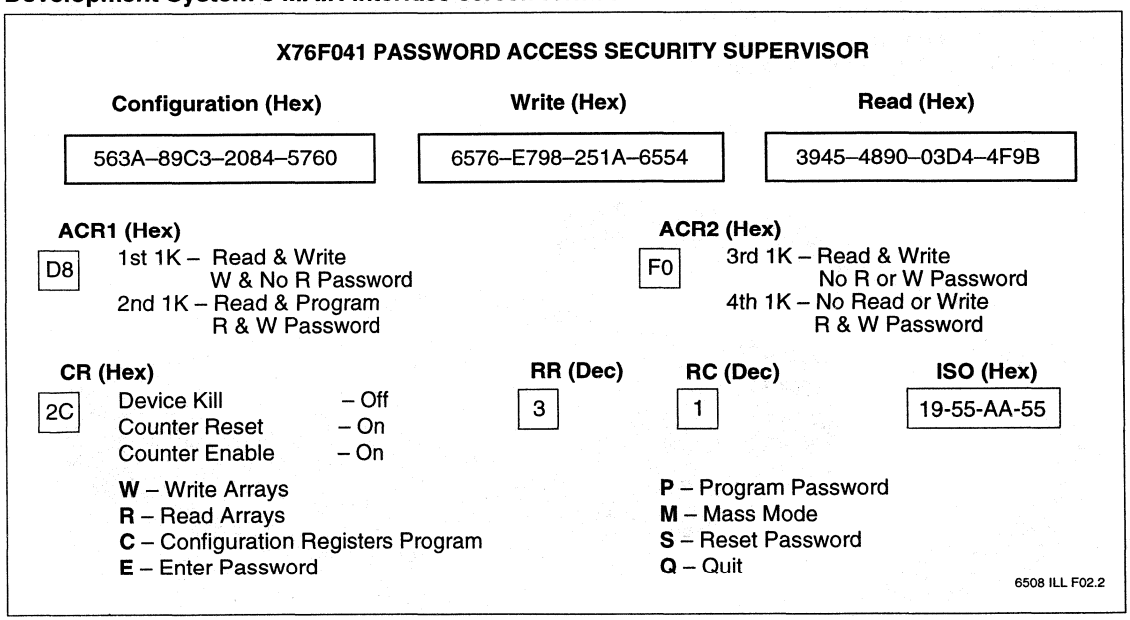
The XK76C Development System significantly reduces the time involved in understanding, evaluating and designing in the Xicor X76F041 smartcard. It provides comprehensive hardware and software support that includes a card reader and development system software.

The System is designed to enable users to quickly and easily understand the capabilities of the X76F041. It is an ideal platform for evaluating the suitability of the device for a particular application. The development system software, used to program and configure the device, enables various levels of security to be set and tested by attempting to access memory arrays using one or none of the passwords. The XK76C provides the hardware and application alterable software required to appraise the X76F041 smartcard solution, saving the designer from building an evaluation card reader and writing code from scratch. It also serves as an effective debug tool during prototype by providing a programming and verifying capability.

The status and values of the X76F041's configuration registers and four memory arrays are represented by the development software using two graphical interfaces. The MAIN interface is used to display the device's ISO identification number; enter, display, reset and program passwords; display and program configuration registers; and mass program/erase memory. The ARRAY interface is used to read the four memory arrays and to enter the array programming editor. The various options in each interface are displayed using menus and selected using a single key input.

The System consists of a card reader, two X76F041 smartcards, and a 3.5" software diskette. It is easy to use and simple to set up, operating with any IBM

Development System's MAIN interface screen format



Development System's ARRAY user interface screen format

X76F041 FOUR 128 x 8 MEMORY ARRAYS

	Write Password WRITE			Read Password READ	
000	C2989850573C69F6	A3C72153B7648910	35DA265237898422	84D5178A43321898	0lF
020	4897328F73543212	9379421598084765	E764569B74365355	A58682270647662F	03F
040	7419784A632764EF	897458952765E527	525A3267659785B6	532658659808563B	05F
060	73579899596CBF83	2098B95959880798	90A678568D9086B9	08909039357659C7	07F
080	----------	----------	----------	----------	09F
0A0	----------	----------	----------	----------	0BF
0C0	----------	----------	----------	----------	0DF
0E0	----------	----------	----------	----------	0FF
100	8867864F7D798798	78C2956766543292	B6362843290665D6	457627F237983427	11F
120	5798723665AF4798	6325675459983292	5433209985746492	7849332611326329	13F
140	7433005278194627	2191654D6D8C7257	1873662143219945	6436342833451901	15F
160	5347978D77657676	5A73268F72968765	78983276545C5762	32588C7253EB6786	17F
180	3267104576543875	43756FD76C678765	32908BDF79878FAD	6432DA776C980D30	19F
1A0	32139045E7578598	17630385A8653421	56479034215C8A6A	E21679D419859876	1BF
1C0	DF4A78754589435F	9847265793259806	65F980498FCFA679	806459787FE90237	1DF
1E0	6543987392537898	2FA786987A698257	6278F79865298273	2852F6686DA23429	1FF

Options : — ← ↑ ↓ → Move V - Verify M - Main Menu

6508 PGM F03

compatible PC that is equipped with a parallel printer port. The hardware is powered using either a 9 volt battery or standard DC power plug. The software diskette contains three files: the development system executable file, the source C interface routines, and the OrCAD schematic of the card reader. The executable file can run with any PC supporting DOS 3.0 or higher.

NOTES

XK84

X84041 MPS™ E² Development System

DESCRIPTION
CONTENTS:

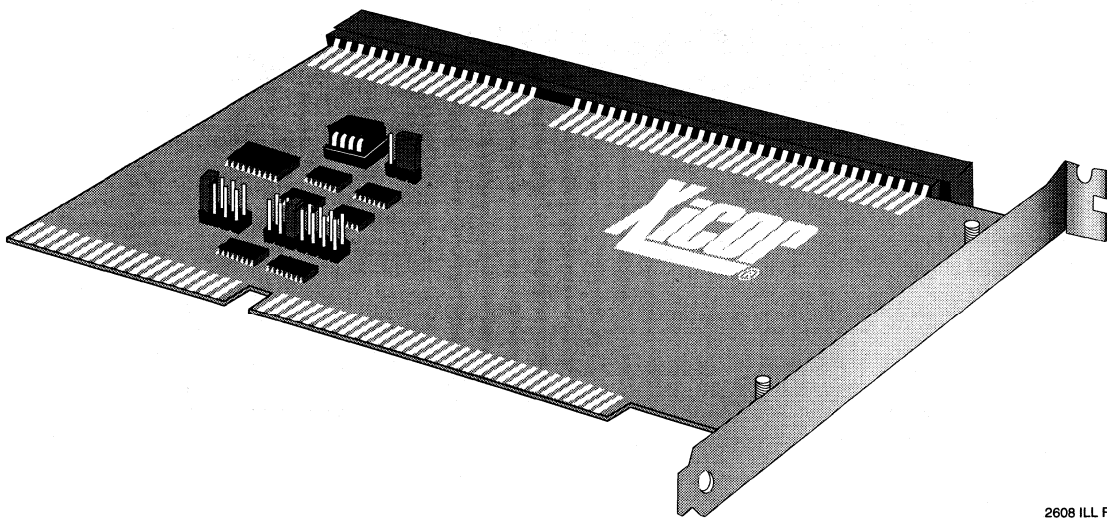
- **XK84 software on diskette (PC format)**
  - **—XK84 development system software**
  - **—X84041 software routines (ANSI C compatible)**
- **XK84 add-in card**
- **XK84 user's guide**
- **Three X84041P DIP parts**

FEATURES:

- **PC based development system platform**
- **XK84 add-in card doubles as PC Bus extender**
- **Full feature E²PROM development system software**
  - **—complete "programmer" software for XK84**
  - **—ready-to-use C routines for MPS™ E² interfacing**
- **Add-in card maps into an I/O port address block ($300 -$31F) under user control**
- **Optional $\overline{CE}$ from target system**
- **$\overline{WP}$ controllable by user**

2608 XXX F01

Development Board



2608 ILL F02

MPS is a trademark of Xicor, Inc.

2608-1.2 6/2/95 T0/C2/D0 TD

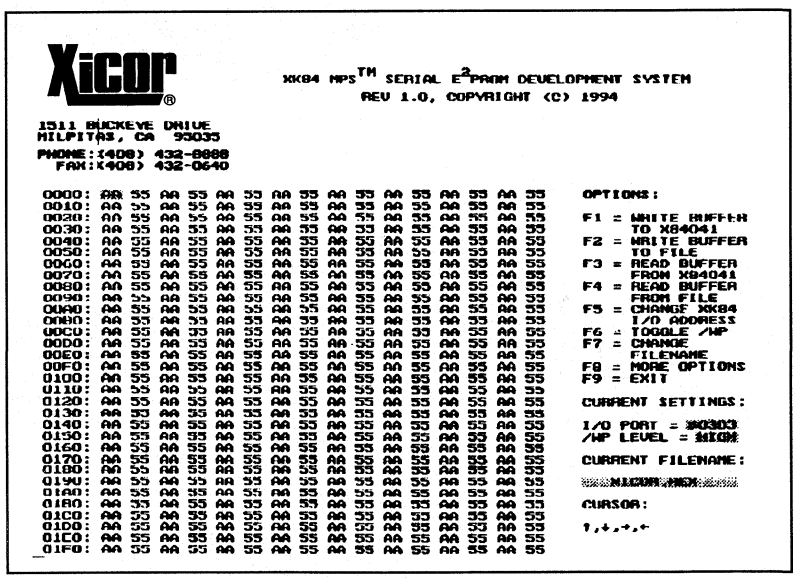
The XK84 development system is intended to demonstrate the simplicity of interfacing an MPS™ E² to a parallel bus system. To this end, Xicor produces an add-in card (the XK84) for PCs that includes enough I/O port bus decoding to interface to the X84041. However, if a designer needs to verify the use of an X84041 with an existing prototype add-in card, the XK84 also functions as a PC Bus extender socket so that the prototype card can be "piggybacked" on top of the XK84. Additionally, the decode circuitry on the XK84 can be bypassed in favor of $\overline{CE}$ decoding from the prototype card. In order to guarantee that there are no I/O port address mapping conflicts, the address of the XK84 can also be chosen from among a block of possible addresses. The MPS™ E² is socketed so that the card can be used to program any number of parts directly. A designer could also connect commonly available flat ribbon cables to this socket and to an externally socketed X84041 in order to expedite the process of programming a large number of parts.

Included with this development kit are routines that can be used directly in existing ANSI C programs simply by adding an "#include" statement and calling either the read_X84041 or write_X84041 subroutines.

When using the XK84 as a prototyping tool, the designer would use the "programmer" software under PC control to help debug both the software and hardware of the target system, since this kit allows great flexibility when reading from or writing to an MPS™ E².

The development system's executable program includes the ability to load the contents of the device into a buffer. That buffer, in turn, will be displayed on the PC screen. Also, the designer determines whether to save this buffer to disk for later use, to edit any number of bytes in the buffer, or to write the buffer back into the device. This buffer can also be loaded from ASCII compatible files stored on disk, allowing greater flexibility when the programming of multiple parts is required. In addition, there are several commonly desired test patterns that can easily be loaded into the buffer through the menu options.

The XK84 is also intended as a development system for future MPS™ E² devices and as such should prove to be a useful prototyping and debugging tool for any designer interested in Xicor's unique new interface. The XK84 software requires at least a VGA, MCGA, or IBM8514 compatible monitor in order to run in the graphics mode shown.



2608 PTO F03.1

XK88 SLIC® E²

80C31 / X88C75 SLIC E²PROM Development System

FEATURES

- **80C31B MICROCONTROLLER**
- **11MHz system clock**
- **8Kx8 intelligent E²PROM (X88C64 SLIC E² or X88C75)**
- **DOS based XSLIC communication/configuration software diskette**
- **Serial communication port (RS232 DB-9)**
- **Extended memory support**
- **Emulation mode**
  - **— Expansion connectors for 80C31 or 80C51**
  - **— ROM emulator**
  - **— Interface option to target system**
- **Prototype area**
- **4" x 5.5" form factor**
- **Power source alternatives: Battery/ Power Jack/Target system**

SOFTWARE DISKETTE INCLUDING

- **README**
- **XSLIC.EXE**
- **SLIC.ASM**
- **SLIC.HEX**
- **SLIC.DOC**
- **SLICNOTE.DOC**
- **XK88.SCH (ORCAD SCHEMATICS)**
- **XICOR.LIB (ORCAD LIBRARY)**

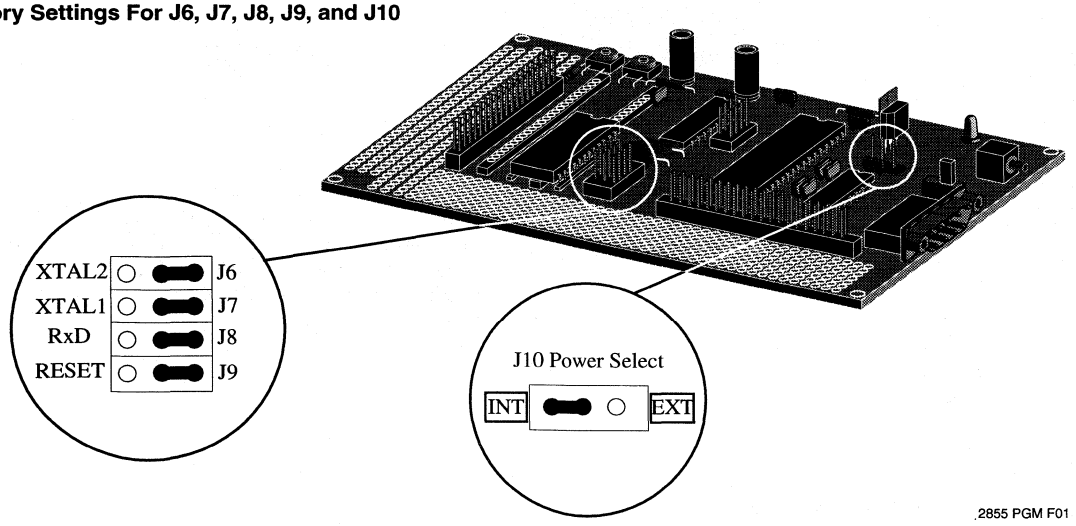
DESCRIPTION

The XK88 is an 80C31 based development system for the X88C64 and X88C75 SLIC (Self Loading Integrated Code) E² products. The system allows users to easily integrate their code into the X88CXX SLIC E² product and speeds up the design process. The prototype area on the board is ideal for small custom circuit design. Three power source options are available: external power jack, single 9-Volt battery, or from the target system. Two push-button switches are used to reset the 80C31 or generate an external interrupt.

The XK88 system can operate in two modes: stand-alone, and ROM emulation. In stand-alone mode the XK88 internally generates all the necessary signals and operates independently.

The ROM emulation mode employes one of the two 40-pin headers to interface to the target systems; they carry all of the microcontroller signals, J1/80C31 and J2/80C51. Depending on the SLIC E² type integrated on the board, one of the appropriate connectors is used to plug into the microcontroller socket on the target system through the 40-pin shielded flat ribbon cable provided with the XK88 system.

Drawing shows XK88 Development Board. Detail Views Show Default Factory Settings For J6, J7, J8, J9, and J10



.2855 PGM F01

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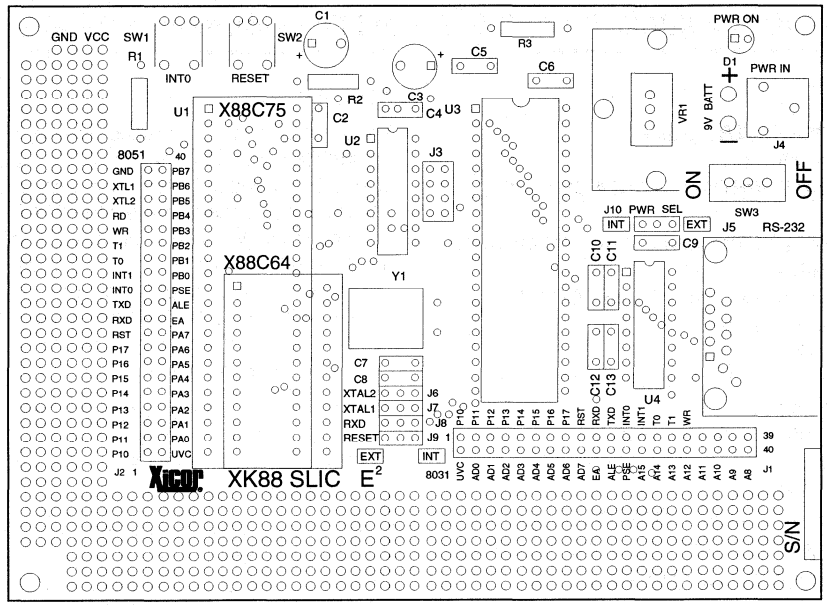
PC BOARD LAYOUT



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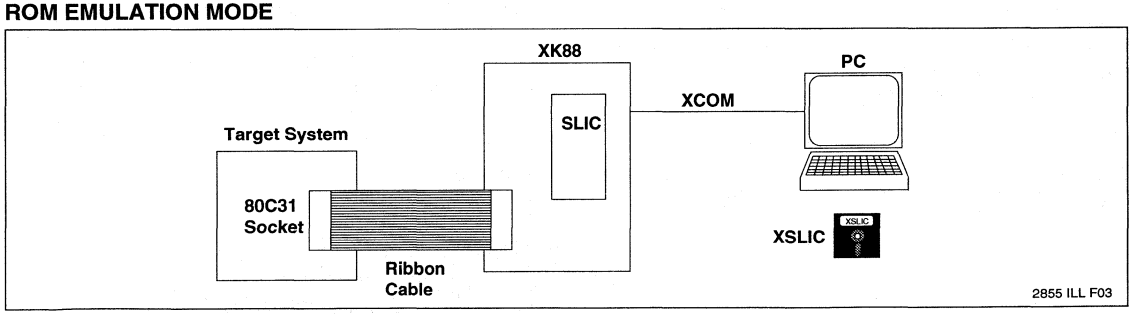
ROM EMULATION MODE



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XSLIC SCREEN SHOWN FROM MONITOR

```
XSLIC Rev. 3.5
X88C75 SLIC* E² Rev. 1.0 * SLIC is a trademark of
Xicor, Inc. copyright © 1994 by Xicor, Inc. Milpitas, CA

      Download
      BPR
      Verify
      Filename" "
      Reset
      ReLocate
      Setup
      Quit

      Please make selection
```

The XSLIC is a DOS based application program with a built-in user interface and communication driver. It manages the programming of the SLIC E² devices by converting the user's file from either Intel HEX or Motorola S19 formats to Xicor XCOM format and downloads them to the SLIC E² device.

XK9241

X9241 Development System

CONTENTS

- 3.5" Diskette, PC Format, Double Density
- Development Board
- Interface Cable
- Users Guide
- Two X9241W DIP Parts

FEATURES

- Simple PC Based Platform
- Menu Driven User Interface
- Provides for Complete Control of Quad E²POT Operation
  - —Register Values
  - —Configuration
  - —Wiper Position
- Supports Multiple Quad E²POTs
- Simplifies Design and Debug Process
- Provides a Complete Calibration/Adjustment System for Systems Utilizing the X9241
- Supports Two Modes of Operation

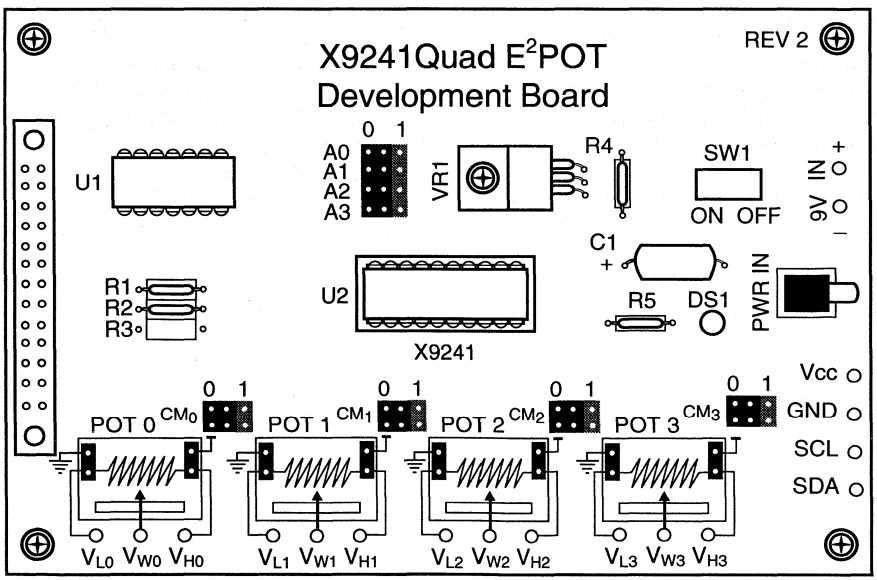
DESCRIPTION

The Quad E²POT Development System has been devised as a tool to significantly reduce development time of applications using the Xicor X9241. It greatly simplifies the task of evaluating the part and enables multiple X9241s to be simultaneously programmed via a standard PC. The System enables the user to quickly become familiar with the operation of the Quad E²POT and aids a designer by demonstrating the benefit of the device in the Target System.

The Development System consists of a circuit board, two feet of flat ribbon cable with adjacent connectors, two X9241s and a software diskette. It is easy to use and simple to setup, operating with any IBM compatible PC that is equipped with a parallel printer port.

The System allows the user to evaluate a part using the terminal voltage outputs mounted on the board and assist design by making available the two-wire serial

Development Board Layout



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data bus for controlling several external X9241s. The PC is interfaced to the development board using any of the hosts parallel ports.

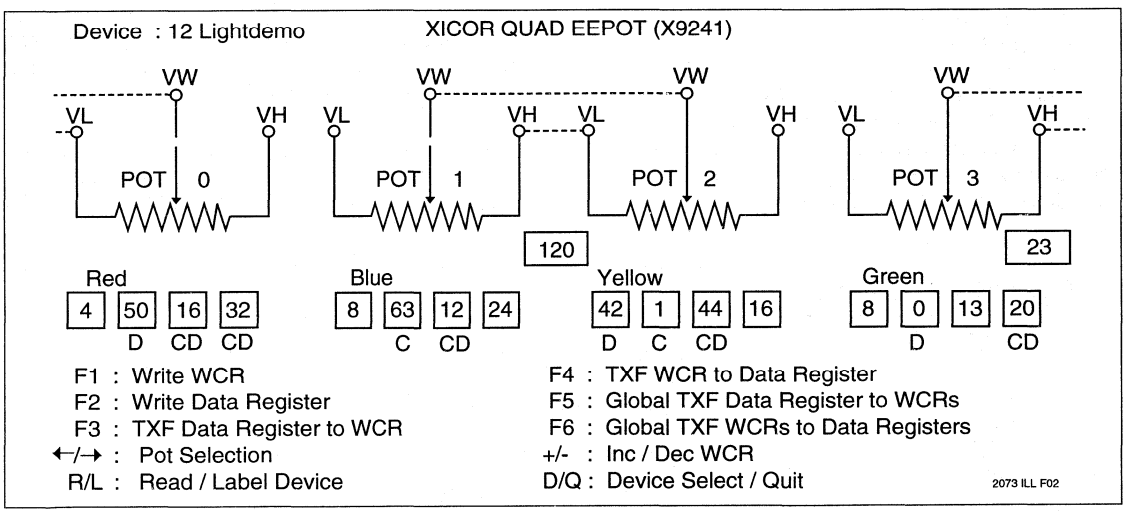
The status and values of the Quad E²POT are represented using a single screen output. Various options are available and are selected using a series of menus.

MODES OF OPERATION

Insertion Mode—uses an X9241 mounted on the development board to provide the Quad E²POT terminal voltage outputs for use by the Target System. Connections are made from the development board's resistor terminals (V_H,V_W, V_L) to the analog circuitry in the Target System. This allows the user to quickly and effortlessly evaluate the suitability of the X9241 in their circuit.

Bus Mode—does not use an X9241 mounted the development board, but rather controls X9241s placed in the Target System. Connections between the development board and the Target System are through the SDA and SCL lines, which enable the Development System to send control signals to multiple Quad E²POTs. This mode is useful in providing off-board control in applications where a microcontroller or microprocessor is not present at time of manufacture or at subsequent service or adjustments.

Development System's User Interface Personal Computer Screen Format



ORDERING INFORMATION

PART NUMBER	DESCRIPTION
XK9241W	Quad E^2POT PC Based Development System
XK76	PASS™ E^2 PC Based Development System
XK76C	PASS™ E^2 PC Based Card Reader Development System
XK88	X88C64/X88C75 SLIC E^2PROM Development System for 80C51 Target System
XK68	X68C64/X68C75 SLIC E^2PROM Development System for 68HC11 Target System
XK84	X84041 MPS Serial E^2 Device Development System

NOTES

Xicor®

3807-2.3 12/4/95 T12/C0/D0 NS

Variable Gain using E²POTS to alter Bias Currents of Transconductance Amplifiers

by Gray Creager, January 1994

One of the more widespread uses for Xicor's E²POT digital potentiometers in mixed signal applications is to vary the gain of an operational amplifier stage. To this end, these devices have the advantage of easy digital interfacing, nonvolatility, small package size, and low cost. However, the E²POT's internal charge pumps (operating between 800KHz - 5MHz) can couple noise onto the analog signal in some applications. Minimizing this noise requires extra care during the design stage as well as the inclusion of passive components for an RC filter.

A noiseless alternative would be to use an E²POT as a rheostat in order to vary the input bias current of a transconductance amplifier, such as the LM3080. Linear Technology produces a combination current feedback amplifier with DC gain control that lends itself well to such an application. For the LT1228, both a transconductance amplifier and a current feedback amplifier are included in the same package. For the single-ended amplifier circuit in Fig. 1, the designer is able to control gain by simply altering the wiper position of the E²POT. Using this scheme to vary the bias current is a much better solution than using a voltage output DAC in conjunction with a voltage to current circuit. The corresponding voltage gain for this circuit is given by:

$$A_v = \frac{(R_f + R_g)(R_{gf} + R1)}{R_g(R_{gf} + R_f + R_g + R1)}\left[\frac{(10)(R1)(R2)(I_{set}) + R_g}{(R1 + R_{in})}\right]$$

Furthermore, I_{set} for this E²POT configuration can be approximated as the following function of tap position, where V_γ is the voltage drop across a diode, V_{s-} is the negative Op Amp rail voltage, V_Z is the drop across the Zener diode used to prevent VH from becoming more negative than -5V, and R_{eepot} is the end to end resistance of the E²POT:

$$I_{set} = \left[\frac{(5 - 2V_g - V_{s-} - V_z)}{R_{set} + 40 + \left[1 - \frac{TAP}{99}\right](R_{eepot})}\right]$$

A resistor (R_{set}) is required to limit the wiper current in the E²POT. For the component values of Table 1, the frequency response of Fig. 2 is obtained. The use of components R_{gf}, C_{gf}, and C2 may be necessary for stability when other component values are used. However, if R_{gf} is omitted, the voltage gain simplifies to:

$$A_v = \left[1 + \frac{R_f}{R_g}\right]\left[\frac{(10)(R1)(R2)(I_{set})}{(R1 + R_{in})}\right]$$

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R1	R_{in}	R2	R_g	R_f	R_{gf}	R_{set}	C2	C_{gf}
19Ω	8450Ω	1100Ω	100Ω	5000Ω	-----	1820Ω	-----	-----

Table 1

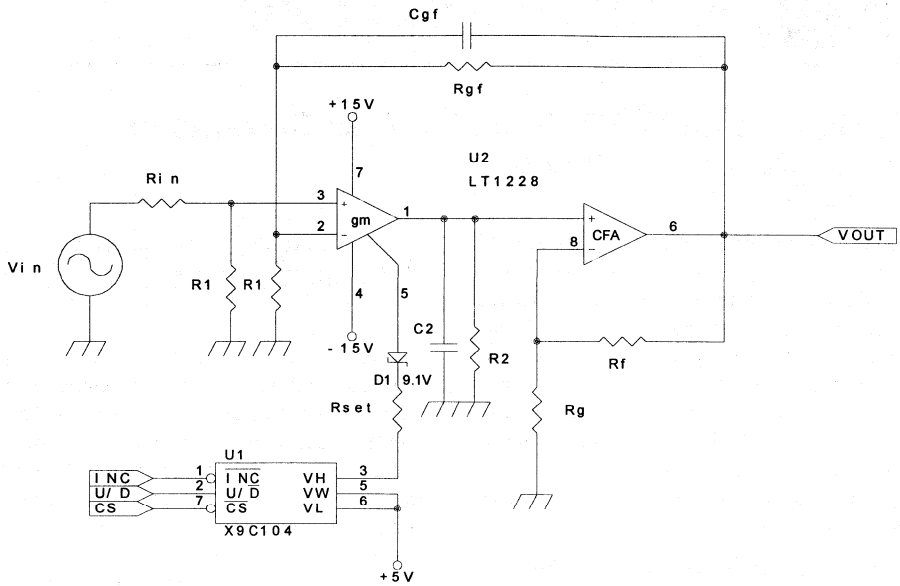

Figure 1

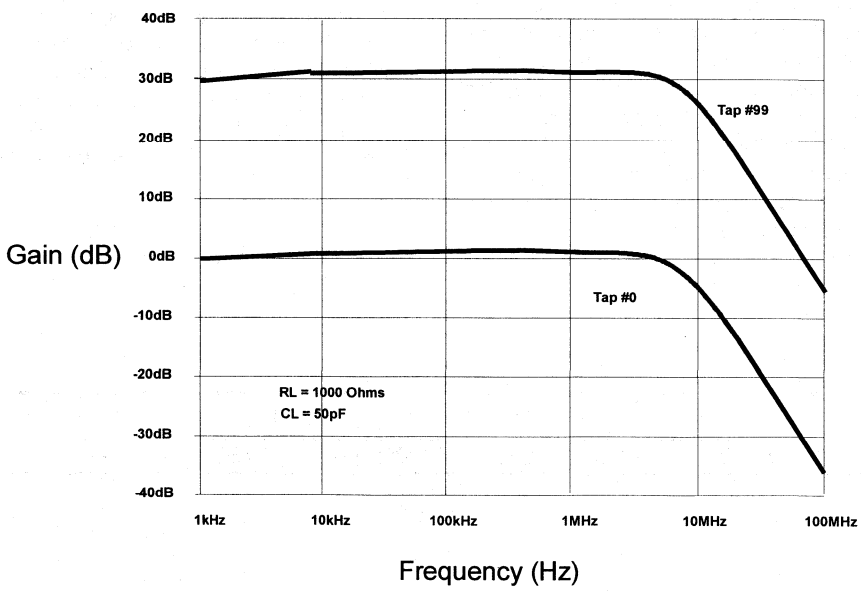

Figure 2

Software Implements a High Resolution Nonvolatile Digital Potentiometer

by Gray Creager, October 1994 (from a design idea published in EDN magazine (June 8, 1995))

In some applications (e.g. dynamic biasing of LASER diodes), the use of digital potentiometers or trimDACs to control voltage levels is limited by resolution, accuracy, or interface difficulties. Using the simple, but not so obvious, Vernier scheme in Fig. 1, which consists of an X9241 quad E^2POT and a little bit of software, an 8001-tap position nonvolatile digital pot can easily be implemented that exhibits a typical tap-to-tap resolution of 0.008%.

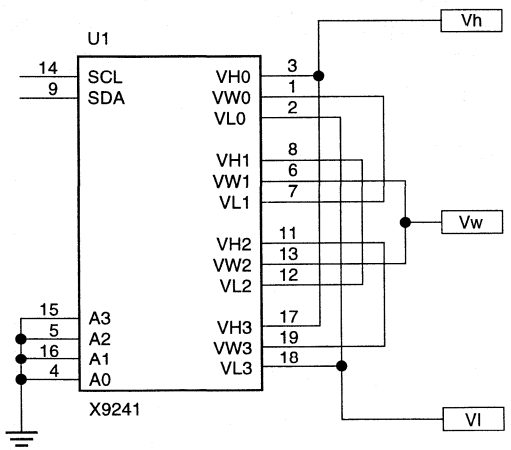

Figure 1

The X9241 includes four separate 64-tap nonvolatile E^2POTs with a mechanism to serially cascade adjacent POTs, allowing up to 253 distinct tap positions. However if only two POTs are cascaded together and the remaining two POTs are used to set the levels of VHcasc and VLcasc, then a much higher degree of resolution can be attained. Since the wipers of the POTs that set VHcasc and VLcasc must always be 1 position apart, there will be 63 distinct voltage intervals applied to the remaining cascaded POTs. This software neglects one redundant tap position per interval when VW is set to tap 64. Ideally, there should be another redundant tap position when transitioning between tap 127 of a particular voltage interval and tap 0 of the next voltage interval, however these tap positions are not actually redundant and their use can improve the linearity. With 127 distinct outputs for each of 63 distinct intervals, there are 8001 distinct VW outputs available between VH and VL. Fig. 2 illustrates the concept behind this scheme.

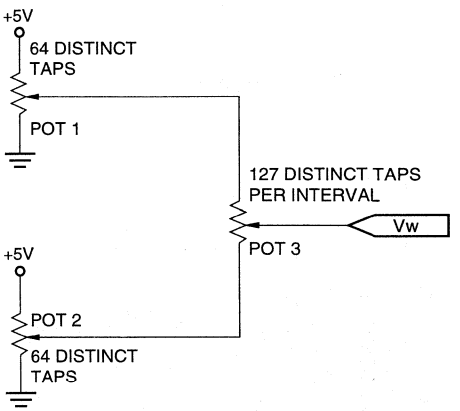

Figure 2

POT0 and POT3 set the voltage interval for POT1/2. As the wiper position of POT1/2 moves up and down, the wiper positions of POT0 and POT3 adjust when necessary. If the wiper of POT1/2 is incremented beyond tap 127, then the wipers of POT0 and POT3 will be incremented and the wiper of POT1/2 will be returned to tap 0. Likewise for decrements of the wiper of POT1/2 below tap 0, the wipers of POT0 and POT3 will be decremented and POT1/2 will be set to tap 127. The X9241 is nicely suited for this implementation since tap positions can be directly changed in software without the need to transition through each intermediate position.

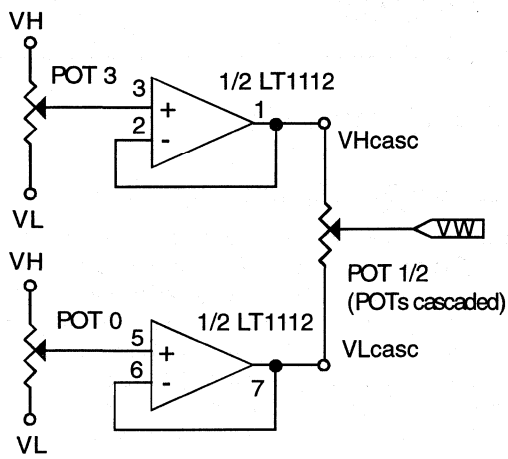

Figure 3

Due to wiper MOSFET loading and variations in the resistive elements of each pot, a piecewise linear behavior appears when transitioning between voltage intervals. By testing a circuit with a sample X9241U (49.37KΩ, 49.38KΩ, 49.32KΩ, 49.24KΩ) device, the representative resolutions between adjacent taps are found and shown in Fig. 4. The use of low offset unity gain buffers as shown in Fig. 3, as well as X9241 devices with both POT1 and POT2 well-matched can improve the linearity at the expense of monotonicity. To guarantee monotonicity for any X9241 device at the expense of resolution, software range transitions could be adjusted to occur between tap 127 and tap x (x > 0). The finer resolution within each voltage interval would provide sufficient precision, however connecting another pot as a rheostat between VH and the VH terminals of POT0 and POT3 will add a variable voltage drop for "trimming" the output of VW even further and would be an alternate method to the use of buffers.

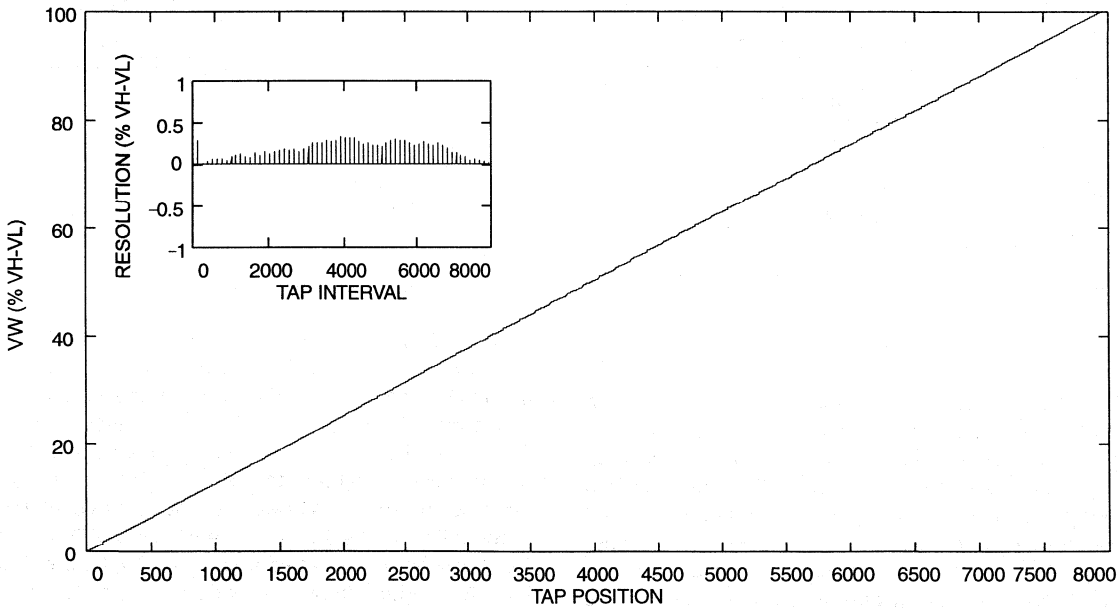

Figure 4 - Wiper Voltage Per Tap Position as a Percentage of Total Applied (VH-VL). Inset Graph Shows Resolution Between Adjacent Taps as a Percentage of Total Voltage Applied. Measurements Taken with 7940 Tap Implementation (x=1), but without LT1112 Buffers.

```
*************************************************************************/
*
* The following routines implement a high resolution EEPOT with the X9241.
* This C code can be adapted to any system since it is written at a
* high level.  The low level I2C routines will be processor/controller
* specific and can be extracted from the Xicor BBS (800-258-8864).
* For example, the required low level routines may as simple as:
*
*      start(), stop(), SDA_high(), SDA_low(), SCL_high(),
*      SCL_low(), ack(), nack(), send_byte(), & get_byte()
*
* Since C code exists on the Xicor BBS to drive the X9241, only those
* functions relating to this Vernier scheme are included here.  This
* code was written and debugged using Borland Turbo C. To use these
* routines, just include them into a larger program and call any of
* these five routines as desired.
*
*      eepot_8000_read()        returns integer value between 0 and 8000
*                               corresponding to current wiper position
*      eepot_8000_write(n)      changes wiper position to that specified by n
*                               where 0 <= n < = 8000
*      eepot_8000_inc()         increments wiper position by one tap
*      eepot_8000_dec()         decrements wiper position by one tap
*      eepot_8000_store()       performs a nonvolatile store of current wiper
*                               position
*
* All necessary record keeping for this scheme is handled automatically by
* software.
*
* Modified: 11/20/95                                          GHC IV
*************************************************************************/
#include <stdlib.h>             /* used for "div" function */
#include "c:\tc\x9241sub.c"     /* set of I2C subroutines, from */
                                /* Xicor BBS for example! */

void eepot_8000_move() {
       start();                 /* set VHcasc */
       send_byte(0x50);         /* slave address A3A2A1A0 = 0000 */
       nack();
       send_byte(0xaf);         /* WCR instruction for POT3 */
       nack();
       send_byte(wiper_range + 1);   /* 00xxxxxx into WCR */
       nack();
       start();                 /* set VLcasc */
       send_byte(0x50);         /* slave address A3A2A1A0 = 0000 */
       nack();
       send_byte(0xa0);         /* WCR instruction for POT0 */
       nack();
       send_byte(wiper_range); /* 00xxxxxx into WCR */
       nack();
       start();                 /* set wiper position */
       send_byte(0x50);         /* slave address A3A2A1A0 = 0000 */
       nack();
       if (wiper_cascade > 63) {     /* is wiper position in POT2 ? */
             send_byte(0xa8);        /* WCR instruction for POT2 */
             nack();
             send_byte(wiper_cascade - 64);  /* 00xxxxxx into WCR */
             nack();
             start();
             send_byte(0x50);  /* slave address A3A2A1A0 = 0000 */
             nack();
```

```
            send_byte(0xa4);  /* WCR instruction for POT1 */
            nack();
            send_byte(0x40);  /* 01xxxxxx into WCR (DW=1) */
            nack();
            stop();
      }
      else {                  /* otherwise, wiper is in POT1 */
            send_byte(0xa4);  /* WCR instruction for POT1 */
            nack();
            send_byte(wiper_cascade);     /* 00xxxxxx into WCR */
            nack();
            start();
            send_byte(0x50);  /* slave address A3A2A1A0 = 0000 */
            nack();
            send_byte(0xa8);  /* WCR instruction for POT2 */
            nack();
            send_byte(0x40);  /* 01xxxxxx into WCR (DW=1) */
            nack();
            stop();
      }
}

void eepot_8000_inc() {
      wiper_cascade = wiper_cascade + 1;     /* inc wiper */
      if (wiper_cascade == 128) {            /* change range? */
            wiper_cascade = x;
            wiper_range = wiper_range + 1;
      }
      if (wiper_cascade == 64)               /* redundant tap? */
            wiper_cascade = 65;
      if (wiper_range == 63) {               /* out of range? */
            wiper_cascade = 127;
            wiper_range = 62;
      }
      eepot_8000_move();                     /* implement move! */
}

void eepot_8000_dec() {
      wiper_cascade = wiper_cascade - 1;     /* dec wiper */
       if ((wiper_range > 0) && (wiper_cascade == x - 1)) {
            wiper_cascade = 127;             /* change range? */
            wiper_range = wiper_range - 1;
      }
      if (wiper_cascade == 64)               /* redundant tap? */
            wiper_cascade = 63;
      if (wiper_cascade < 0)                  /* out of range? */
            wiper_cascade = 0;
      eepot_8000_move();                      /* implement move! */
}

int eepot_8000_read() {          /* read the current wiper position */
int temp1,temp2,temp3,temp4;

      start();
      send_byte(0x50);           /* slave address A3A2A1A0 = 0000 */
      nack();
      send_byte(0x90);           /* read WCR instruction for POT0 */
      nack();
      temp1 = get_byte();        /* WCR of POT0 */
      ack();
      start();
```

```
        send_byte(0x50);        /* slave address A3A2A1A0 = 0000 */
        nack();
        send_byte(0x94);        /* read WCR instruction for POT1 */
        nack();
        temp2 = get_byte();     /* WCR of POT1 */
        ack();
        start();
        send_byte(0x50);        /* slave address A3A2A1A0 = 0000 */
        nack();
        send_byte(0x98);        /* read WCR instruction for POT2 */
        nack();
        temp3 = get_byte();     /* WCR of POT2 */
        ack();
        stop();
        temp1 = temp1 & 0x3f;                   /* remove CM and DW bits */
        if (temp1 != 0) {                       /* is wiper_range = 0? */
              if ((temp2 & 0x40) != 0) {        /* no, is wiper of POT1 disabled? */
                    temp2 = 64 - x;             /* yes, then wiper_cascade > 63 - x */
              }
              else {
                    temp2 = (temp2 & 0x3f) - x + 1; /* no, wiper_cascade <= 63 */
                    temp3 = 0;
              }
              temp4 = 126 + ((temp1-1)*(127-x)) + temp2 + (temp3 & 0x3f);
        }
        else {                                          /* yes, wiper_range = 0 */
              if ((temp3 & 0x40) == 0)                  /* is POT2's wiper disabled? */
                    temp4 = 63 + (temp3 & 0x3f);        /* yes */
              else
                    temp4 = (temp2 & 0x3f);             /* no  */
        }
        return (temp4);
}

void eepot_8000_write(int position) {       /* change wiper to any position */
div_t temp;
        if (position > 126) {               /* if wiper_range > 0 */
              temp = div(position-126,127-x);     /* gets quotient, remainder */
              wiper_range = temp.quot + 1;
              if (temp.rem + x > 64)                /* is wiper in POT1 or POT2? */
                    wiper_cascade = temp.rem + x;       /* POT2 */
              else
                    wiper_cascade = temp.rem + x - 1;   /* POT1 */
              if (wiper_cascade < x) {              /* case when x=0 and temp.rem = 0 */
                    wiper_cascade = 127;
                    wiper_range = wiper_range - 1;
              }
        }
        else {                          /* wiper_range = 0 */
              wiper_range = 0;
              if (position < 64)
                    wiper_cascade = position;
              else
                    wiper_cascade = position + 1;
        }
        if (wiper_cascade == 64)        /* account for redundant tap 64 */
              wiper_cascade = 65;
        eepot_8000_move();
}

void eepot_8000_store() {       /* nonvolatile store of wipers */
```

```
        start();
        send_byte(0x50);        /* slave address A3A2A1A0 = 0000 */
        nack();
        send_byte(0x80);        /* global XFR WCRs to REG0s */
        nack();
        stop();
        delay(10);              /* 10ms delay to complete store */
}
```

Wien Bridge Oscillators using E²POTs

by Applications Staff, October 1994

Wien Bridge Oscillators

In 1939, William R. Hewlett (later of Hewlett-Packard fame) first combined the network described by Wien in 1891 with a gain stabilizing element in a bridge configuration, to produce an oscillator based on a 6J7 vacuum tube. Few circuit designs can match the low distortion, good amplitude stability, ease of tuning, and circuit simplicity offered by the Wien bridge oscillator.

The Wien bridge oscillator is based upon an amplifier with two feedback paths, making up the two arms of the bridge. One arm of the bridge is the Wien network, which provides the frequency tuning elements, and another arm which establishes amplitude equilibrium. Figure 1 shows the configuration using an Operational Amplifier. Positive feedback is provided by the Wien network comprised of equal-valued C1, R1, C2, and R2 elements. Negative feedback is provided by R3 and R4.

To understand how the Wien bridge oscillator works, assume that at power-up, the negative feedback is made less than the positive feedback. Oscillation will start to occur at the frequency where the phase shift and amplitude attenuation in the Wien arm is a minimum. Figure 2 shows the response functions for magnitude and phase from the amplifier output to the noninverting (+) input with C=0.01µF and R=10KΩ. Notice that when the phase equals zero degrees, the magnitude of the positive feedback is a maximum and equal to 1/3. The oscillator amplitude will continue to increase until the amplifier saturates (and produces horrible square waves) or until amplitude equilibrium is maintained below saturation by adjusting the ratio of R3 and R4. Hewlett did this by taking advantage of the positive temperature coefficient of an incandescent lamp. It is interesting to note that when equilibrium is reached, the negative feedback factor will also be 1/3 (in a practical circuit, due to non-ideal components, the negative feedback will be slightly less).

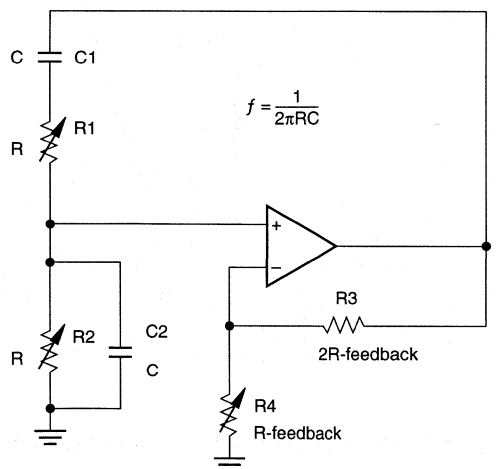

Figure 1. Wien Bridge Oscillator

A Wien bridge Oscillator with E²POTs

Notice that to change frequency, it is necessary to either change both Rs or both Cs of the network and that the Rs or Cs have to change by the same amount or "track" each other. Hewlett accomplished this by using a pair of ganged air-variable capacitors mechanically linked to a tuning knob. You could get similar results by using a pair of ganged potentiometers instead.

However, ganged variable capacitors and resistors are rather bulky and expensive mechanical items that require manual adjustment to change frequency. Since a pair of Xicor E²POTs can be electronically ganged together, they can provide a solid state solution and eliminate the need for any mechanical mounting considerations involved with the air-variable capacitors or the ganged mechanical pots. The benefit of using these digital pots is that the control circuitry can be located remotely from the actual oscillator since the pots are controlled digitally, you don't have to worry about the frequency being inadvertently bumped out of adjustment.

Circuit description

Figure 3 shows the Xicor X9C103 E²POT in a Wien bridge circuit along with remote pushbutton control circuitry. The frequency is determined by the combination of C1, C2, R1+U1, and R2+U2. Assuming that C1=C2 and R1+U1=R2+U2, the frequency is:

$$f = \frac{1}{(2\pi C1(R1+U1))}$$

The negative feedback is set by the combination of R3, R4A, R4B, and Q1. Q1 in parallel with R4B, plus R4A, forms the shunt elements in the negative feedback path. The channel resistance of Q1 is controlled by the amplitude detector circuit comprised of CR3, U3B, R11, and C7. U3B compares the positive peaks of the oscillator output detected by CR3, to the voltage reference established by R11 and R12. The amplitude detector scheme automatically sets the negative feedback so that the peak output just equals the reference voltage. This limits the oscillator voltage swing so that U3A does not saturate and maintains the amplitude equilibrium, which is important when generating sine waves. To ensure that cycle by cycle limiting is not occurring, the time constant of R11 and C7 is much longer than the lowest frequency which the oscillator can be tuned.

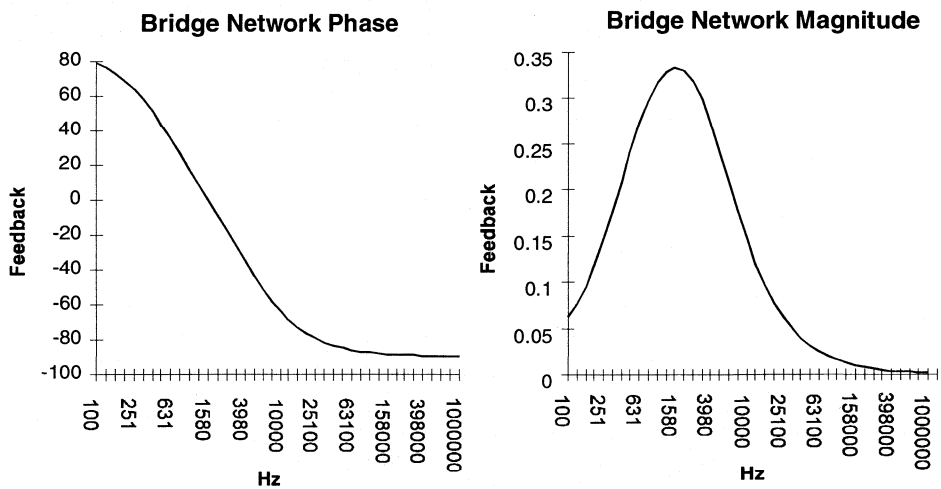

Figure 2. Bridge Network Phase and Magnitude

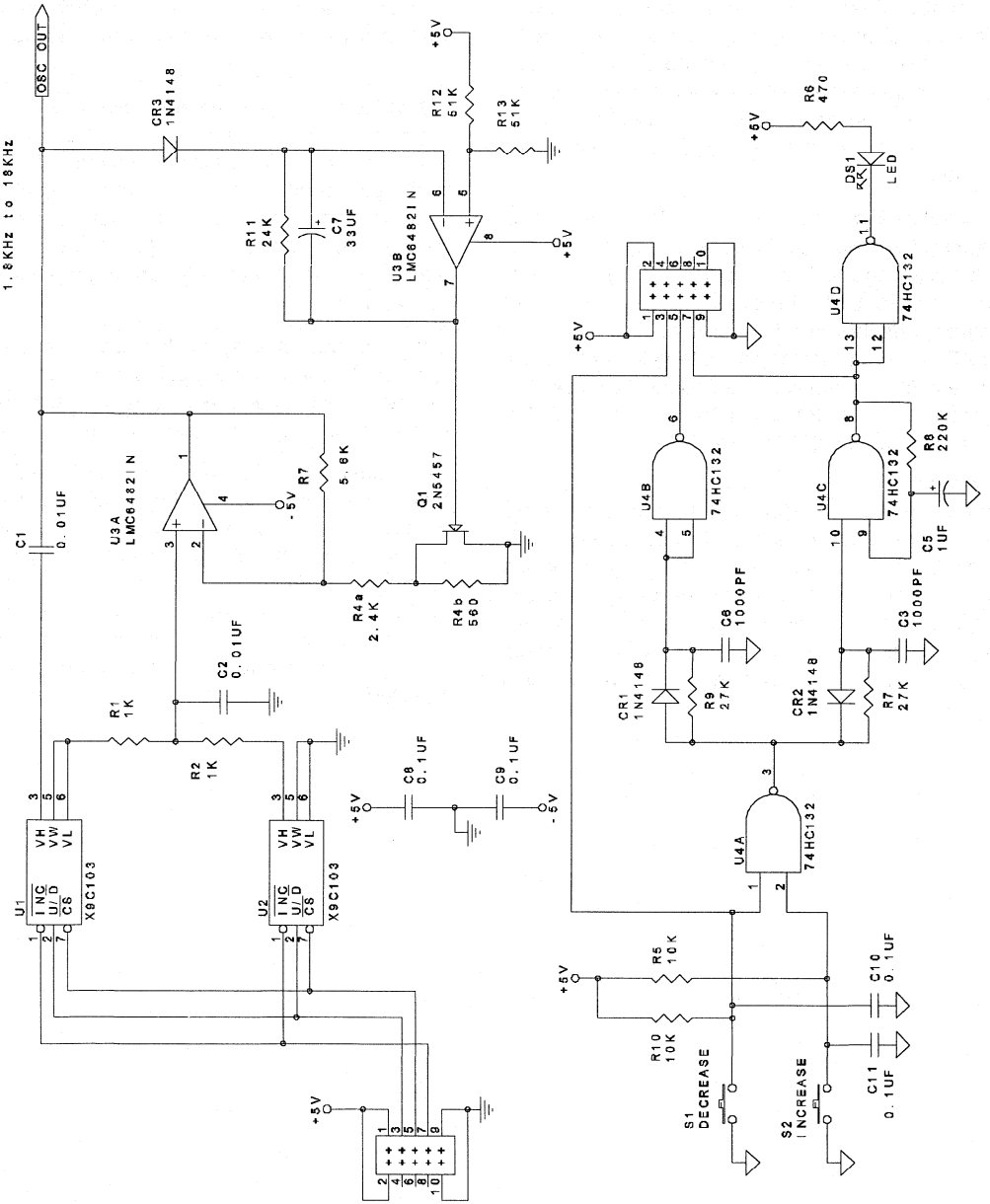

Figure 3. Xicor X9C103 Wien Bridge

Beyond the fact that equal valued Rs and Cs must be used in the Wien arm of the oscillator, there is nothing critical about the components used. Any Op Amp can be used as long as the input or output common mode voltage ranges are not exceeded. The FET can be most any N-channel device as long as R11 and C7 are optimized to keep the gain control loop stable.

This circuit design can be modified to suit just about any application. For example, you may wish to add an additional Xicor E^2POT in place of R13 in order to control the output amplitude. You could also implement digital range selection by using a MOSFET switch to select alternate values of C1 and C2 in decade increments. This should allow selection of decade ranges of 20Hz to 200Hz, 200Hz to 2KHz, 2KHz to 20KHz, and 20KHz to 200KHz.

Performance

Naturally, for the oscillator to work properly, the two digital pots have to be initially ganged together. This is accomplished simply by holding either of the controller pushbuttons down for at least 100 steps. After this procedure is performed, the pots will always "track" and the frequency can be set as desired. Figure 4 shows the output frequency verses step number. With the values used in the schematic the frequency range should be approximately 2KHz to 20KHz in 100 steps. The output amplitude is $2.2V_{RMS}$.

The total distortion and noise of this circuit was measured to be approximately 0.5% and most of the distortion products are second harmonics. This second harmonic is caused by the channel resistance of the gain control FET, Q1, being modulated by the oscillator frequency. You can further reduce the distortion by adding a small amount of Q1 drain signal onto the gate with an appropriate resistor divider network.

The amplitude stability of this oscillator is excellent with no change in output being perceptible over the full range. No doubt, this is why these oscillators proved to be so useful in test application.

Remember, one of the advantages of the E^2POTs is their nonvolatility, so the frequency will always be maintained, even if the oscillator and controller is powered-down. In fact, after the frequency is set, the controller can be removed. This circuit could prove useful in embedded built-in test equipment (BTE) applications where it is desirable to have a programmable oscillator with low distortion and good amplitude stability.

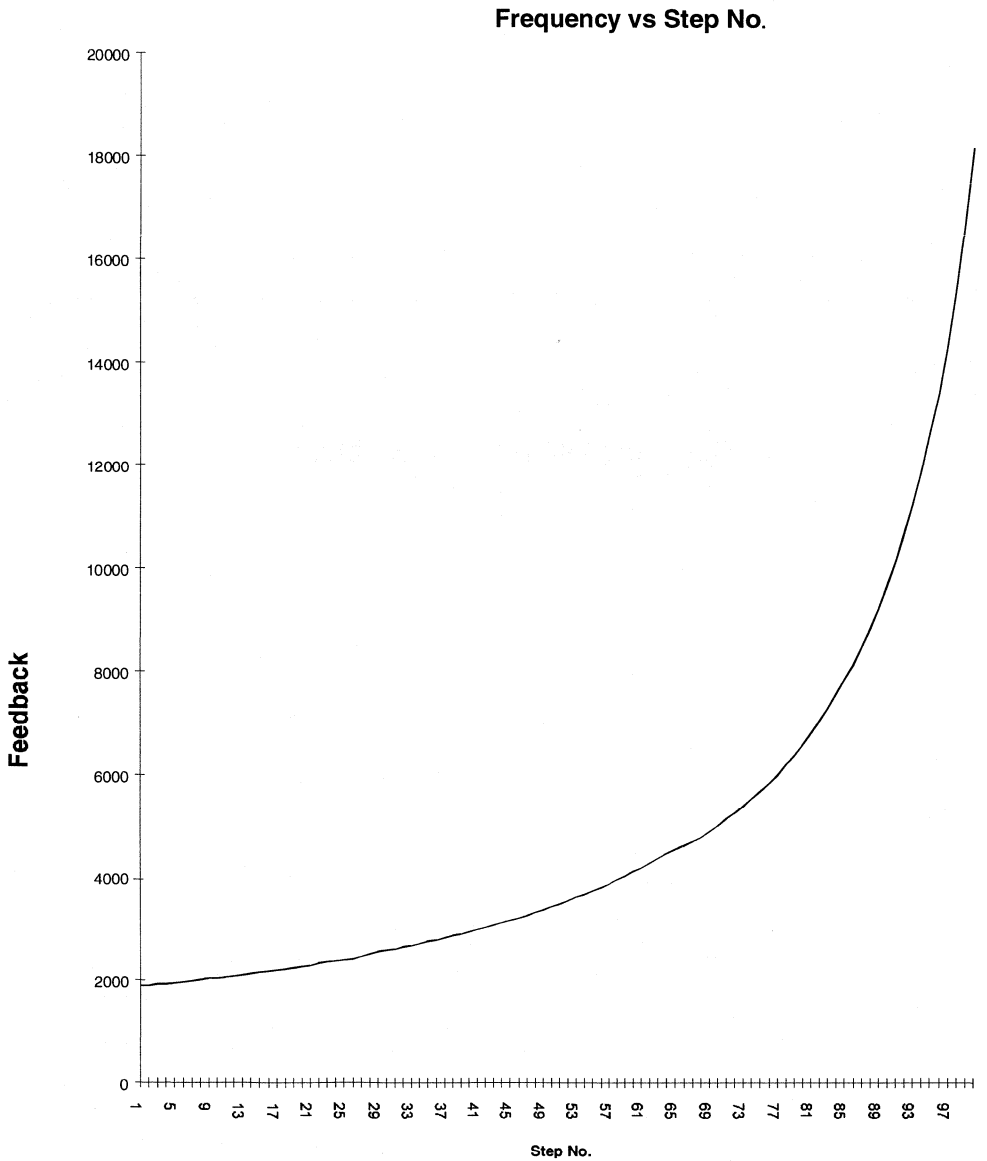

Figure 4. Oscillator Tuning

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Remotely Adjustable Voltage Regulators using E²POTs

by Applications Staff, October 1994

This note shows how an X9312 can be used to implement a remote, adjustable regulator. The LM317 is probably the most common adjustable three-terminal voltage regulator in use today. Often it would be desirable to adjust these regulators remotely, but extending the adjustment rheostat any distance introduces noise and instability. Xicor's X9312 E²POT can provide a simple solution. By using this E²POT, the voltage output of the LM317 can be set using a simple 3-wire digital interface over practically any distance.

Figure 1 shows the LM317's usual adjustment resistor replaced with the 10KΩ version of the X9312. The pushbutton control circuitry would be located remotely (on a separate board). The adjustment range can be set remotely to fit an application by changing R7, just remember not to exceed the V_H or V_L maximum limit of +15 volts.

The standard formula for output voltage naturally still applies:

$$V_{out} = V_{ref} + V_{ref}\left[\frac{R_{pot}}{R_{ref}}\right] + I_{adj}(R_{ref})$$

where Vref = 1.25V

Rref = R7

Rpot = 0 to 10KΩ value for U1 in 99 steps.

Iadj = approx. 50µA of current from the adjustment pin of the LM317

Figure 1 shows the control circuitry connected via a 10-pin connector. This allows an LM317 voltage regulator to be set and then for the control circuitry to be removed. In this configuration, it's a good idea to include a pull-up resistor on all of the control lines (R9, R10, and R11) to assure that inadvertant E²POT changes do not occur.

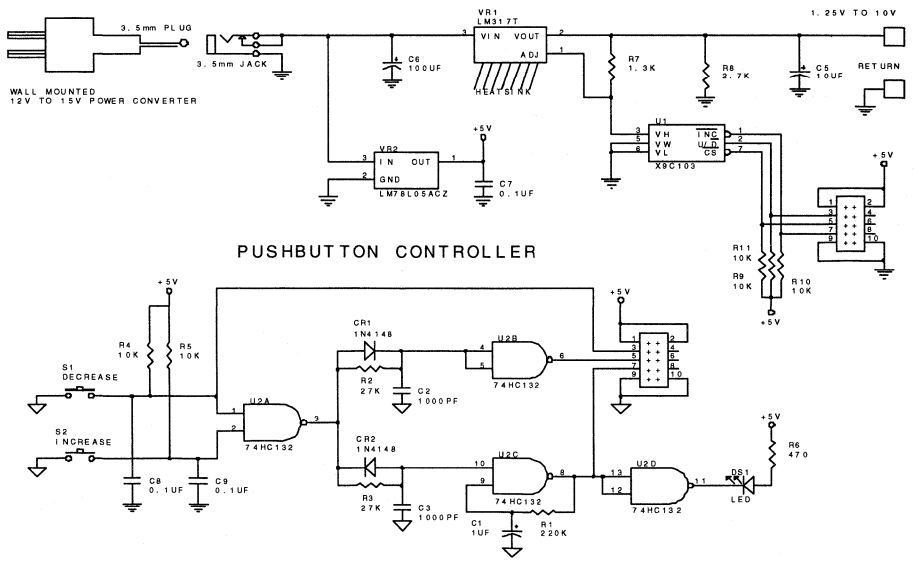

Figure 1. 1.25V to 10V DC Supply

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Controlling an LM555 Astable Oscillator using E²POTs

by Applications Staff, October 1994

An E²POT can be used for control in any of the standard LM555 timer/oscillator circuit configurations. These nonvolatile digital potentiometers allow the frequency of an astable oscillator (for example) to be conveniently adjusted without the need to manually twist a screwdriver adjustment on a potentiometer. A typical application might be one which requires an adjustable frequency source as part of some built in test equipment.

Figure 1 shows the typical connection for the astable mode of operation. Typically, in this mode, the timing is given as:

$$T_{high} = 0.693(R_a + R_b)C, \text{ and}$$

$$T_{low} = 0.693(R_b)C.$$

The problem with this setup is that a 50% duty cycle can only be approached when R_b is much greater than R_a.

Figure 2 shows another astable oscillator configuration which takes advantage of the versatility of these Xicor E²POTs. Notice here that R_b consists of U1 in series with R1, and that no R_a is used. Instead R_b is connected to the output of the LM555 timer (U2). This configuration now has a nearly 50% duty cycle with;

$$T_{high} = T_{low} = 0.693(R1 + U1)C.$$

or

$$f = \frac{1}{T} = \frac{0.722}{(R1+U1)C}$$

In this circuit, a CMOS ICM7555 timer is used because it has very similar source and sink capabilities, and with the component values shown produced a 50% ±4% duty cycle over a range from 900Hz to 30KHz.

TYPICAL ASTABLE OSCILLATOR

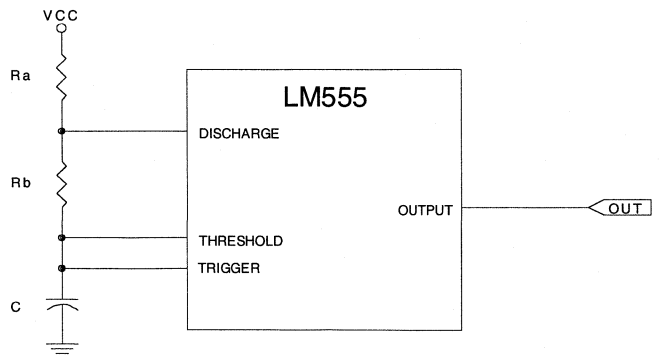

Figure 1. Typical Astable Oscillator Circuit

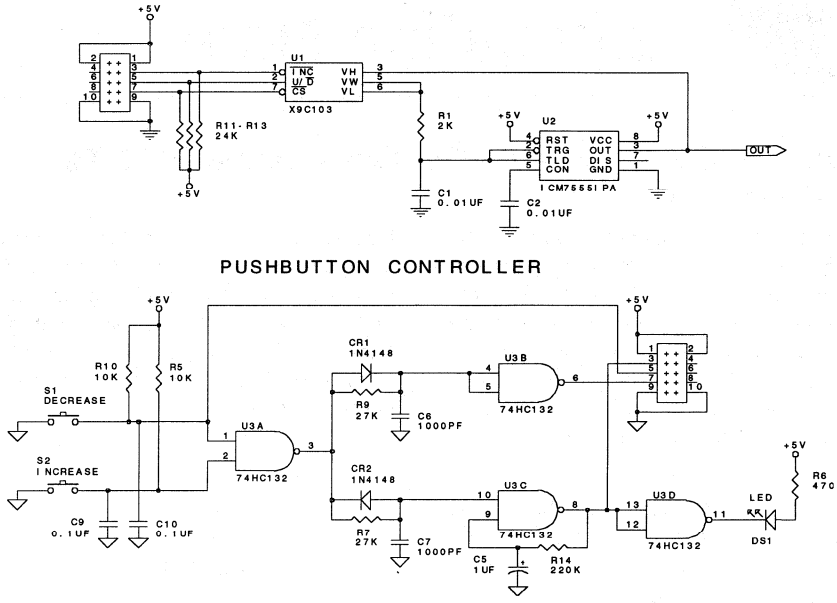

Figure 2. X9C103 Astable Oscillator Configuration

Shaft Encoder Drives Multiple E²POTs

by Applications Staff, October 1994

Suppose a circuit design requires the sprinkling of a significant number of control potentiometers around, but there is only enough room on the front panel for one knob. Alternately, for aesthetic reasons or due to other design considerations, it is only desired to have one control for a number of seldom adjusted, but essential control functions. A shaft encoder, some simple circuitry, and Xicor E²POTs can provide a versatile and unique solution for these types of issues.

Shaft angle encoders are available at low cost from a number of manufacturers. Many of these devices can output two signals in phase quadrature (90 degrees) with typically from 1 to 10,000 pulses available per revolution. By counting the number of transitions on both phases, the shaft angle of the control can be electronically resolved. By using one of the phases as a reference, the direction that the shaft was turned can also resolved.

The particular shaft encoder shown in Figure 1 is capable of encoding sixteen positions per revolution, though other encoders can be selected with different angular resolutions. Each channel of the encoder has four electrical cycles per revolution, or in other words, the electrical phase goes through 360 degrees for every 90 degrees of mechanical rotation. In any complete rotation of the shaft, there are a combined total of 16 level transitions (8 transitions per phase).

In the Figure 1, U7A and U7B are used as Schmitt-trigger buffers for the two phase channels out of the Grayhill shaft encoder. The XOR gate (U6B) essentially adds these two phases to produce an 8-cycle per revolution signal. U6C along with delay network R1/C2 form a one-shot which produces one pulse for every HIGH to LOW or LOW to HIGH transition from U6B. There are now 16 position pulses per revolution, with only the direction of the shaft rotation to be determined. This is accomplished by U6A and delay network R7/C4. If the shaft were being rotated at a constant velocity, say by a motor, the R7/C4 delay network would not be required since the U6A output would always be in a defined direction-indicating state, on the LOW going edge of the one-shot output formed by U6C. Since the shaft is going to be rotated by hand, and erratic direction changes could take place, there exists the possibility for direction ambiguity. This is solved by the delay network R7/C4 which stores the direction that the shaft was going at the time that the one-shot pulse was produced. Notice that the time constant for the direction delay is much longer than the one-shot time, ensuring that the direction will be valid on the falling edge of the increment pulse coming from the output of U6C.

Because the E²POTs should remember the last setting on power-down, it is required that $\overline{INC}$ be HIGH before $\overline{CS}$ goes HIGH. This is ensured by two timing networks consisting of the increment-invert network (CR2, R12, C7, U10A, U10B, and U10C), and the chip-select network (CR1, R2, C6, and U6D). The increment-invert circuit is essentially an increment pulse detector that holds U10B in the non-inverting state whenever an increment pulse is detected. The non-invert period is approximately ten times as long as an increment pulse. This allows the $\overline{INC}$ input on the selected E²POT to return to a HIGH state after the last falling pulse edge has incremented the pot. Since the time constant of the chip-select network is even longer, the $\overline{CS}$ input on the pot will be the last to return to a HIGH state after the increment pulse, thereby ensuring that the pot's current wiper setting is stored. Close inspection reveals that U10B is a follower when an increment pulse is present or recently received, but becomes an inverter after the increment pulse is gone, thus returning $\overline{INC}$ to a HIGH state.

A 4-bit shift register is formed by U8 and U9 which is clocked by the pushbutton switch included in the Grayhill shaft encoder. The shift register is preset on power-up by U7D with "1000", this selects the first E²POT. Whenever a $\overline{CS}$ pulse is generated by U6D, it is NANDed with the output of the shift register by

U5 and determines which pot will be selected. Subsequent button pushes on the shaft encoder will select the next pot in the sequence. The length of the shift register can be extended as desired. Naturally, a variety of shift register schemes will work as well as the one shown, the only problem being the ability to determine which pot is active. Here, the use of the four LEDs serves as a simple index pointer to indicate the active pot.

The schematic shows an application using four X9C103 type E^2POTs. Also notice that the Vh and Vl pot terminals are connected to supply and ground merely for the purpose of this application, however these terminals can be connected to any voltage levels, as long as the maximum terminal voltages are not exceeded.

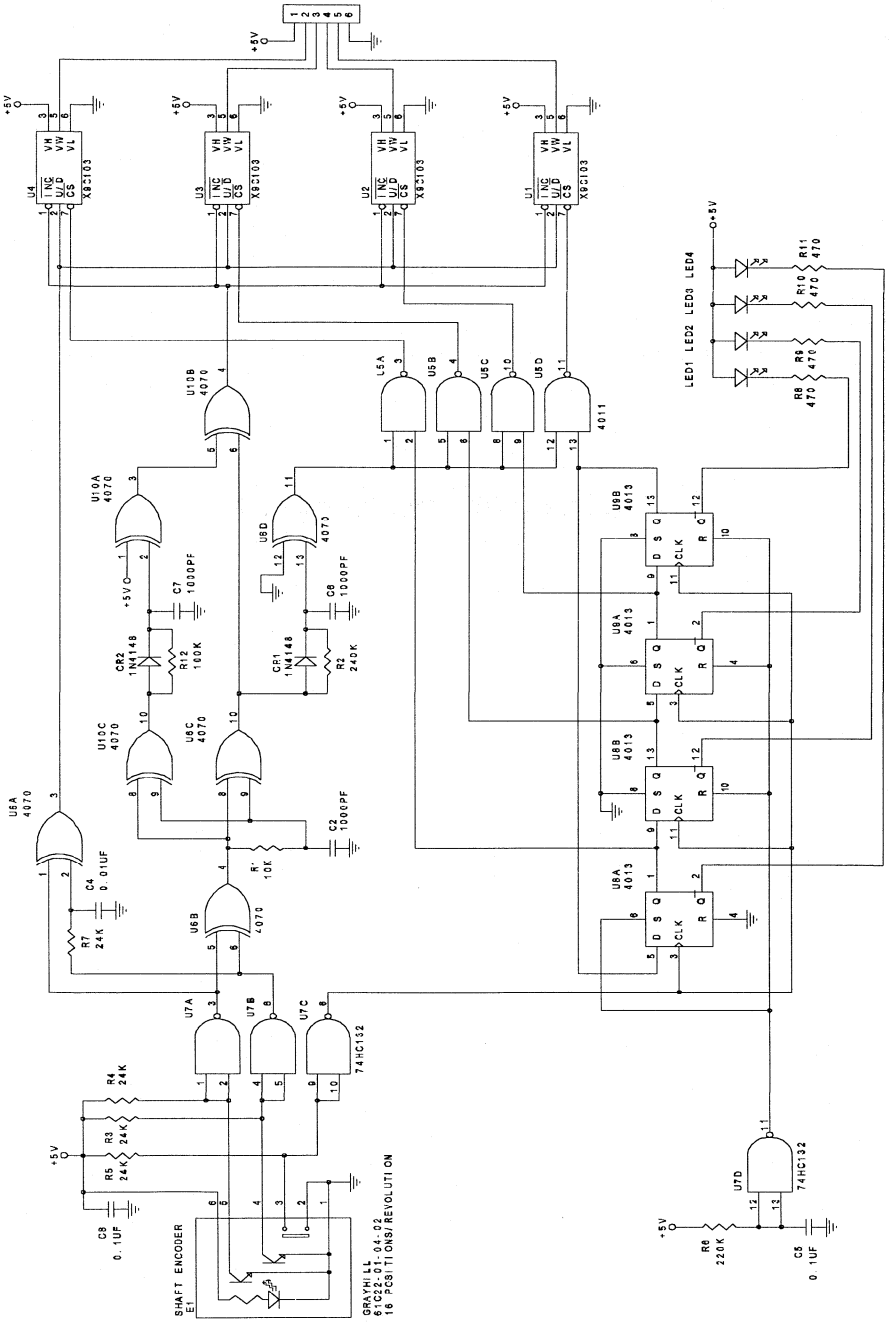

Figure 1. Shaft Encoder Driving Multiple E²POTs

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Digital Audio Amplifier Gain Control using Logarithmic E²POTs

by Applications Staff, January 1994

Often the power amplifier stage of a communications device is located some distance from the control panel. The typical solution is to mount the volume control on the front panel and run a pair of shielded cables back to the power amplifier stage. A better solution is to use the Xicor X9314 logarithmic taper digitally controlled potentiometer. This completely eliminates the need for shielded cables since the digital pot can be located on the printed circuit board near the low level input stages of the power amplifier. The up/down volume switches can be located yards away as these are merely low speed TTL signals.

Circuit Description

Figure 1 shows the X9314 with the low voltage LM386 power amplifier. This circuit will produce 250mW of audio power with only a 5V DC source. Figure 2 is a similar circuit that uses the higher power LM380 and is capable of delivering over 1W of audio if a 12V DC source is available. Either circuit will provide plenty of sound for intercom, communications, or monitoring applications. The 1W circuit would be preferred when higher ambient noise is present, such as in an automobile.

A 74HC132 quad Schmitt nand gate (U2) plus a few discretes are all that are required to interface to U1, the X9314W 10KΩ E²POT. When either pushbutton switch, S1 or S2, is depressed, U2A output will be HIGH. This immediately brings U2B output LOW which enables the E²POT. After a short delay determined by R3 and C3, the astable multivibrator (U2C) will begin generating increment pulses. The frequency of the oscillation (and consequently the speed at which the volume can be controlled) is determined by C1 and R1. The values shown will advance the X9314 through all 32 wiper taps in about 5 seconds. R1 can be changed from 5KΩ to 1MΩ to suit your preference. When the pushbutton switches are released, R2 and C2 delay the release of the X9314 chip select in order to ensure that the last increment pulse is written.

The X9314W needs little else to apply it to most audio circuits, but C9 has been included here to remove any DC component that may be present on the input signal. Also, lowpass filter R7 and C8 removes residual high frequency noise from the digital pot's internal charge pumps.

The LM380 and LM386 power amplifiers have fixed gains of 34dB and 26dB respectively. The gain of the LM386 can be increased to 46dB (X200) by connecting a 10uF capacitor from pins 1 to 8. The positive pole of the capacitor should be connected to pin 1. The output snubber network (R6 and C5) is required for stability and should be located close to the output pin of the power amplifier. These amplifiers have fairly high gain and wide bandwidths, so be careful with PCB trace lengths. All connections to these amplifiers should be as short and direct as possible.

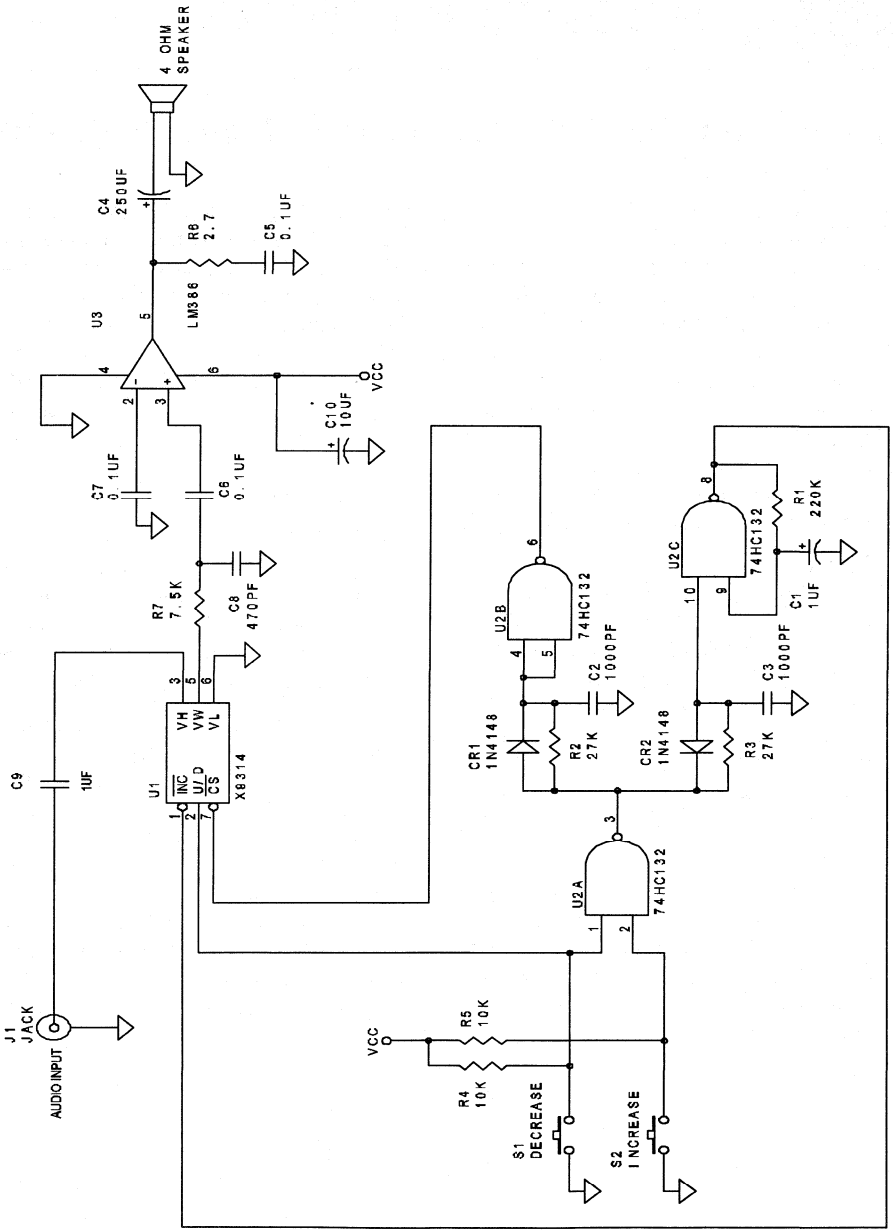

Figure 1. Low Voltage Audio Amplifier

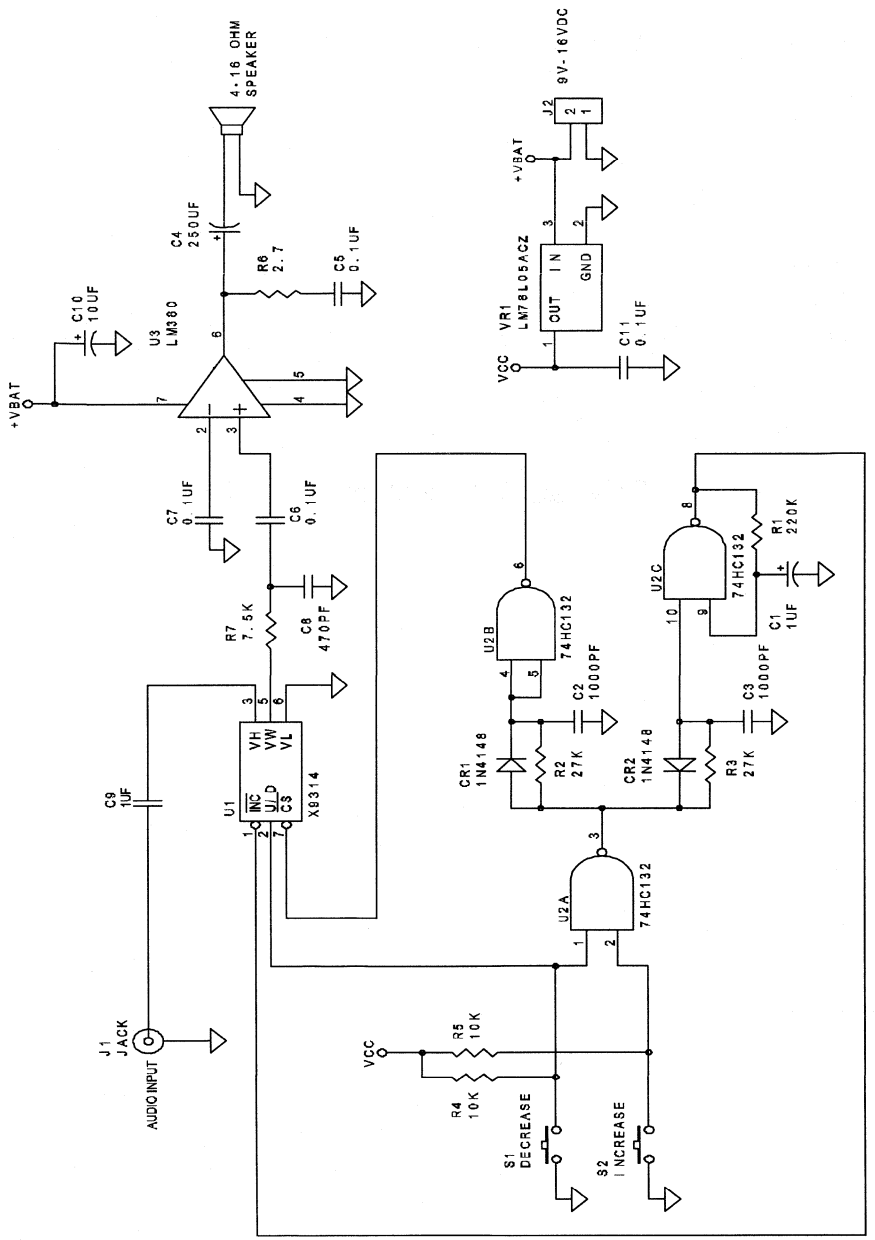

Figure 2. 1 Watt Audio Amplifier

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Op Amp Gain and Offset Trim using E²POTs

by Applications Staff, October 1994

Many system configurations require multiple transducers to be normalized for gain or offset, prior to further A to D conversion or signal processing. The Xicor X9241 quad E²POTs can provide an elegant and efficient solution for performing these tasks under microprocessor control.

The configuration in Figure 1 shows two dual Op Amps being controlled by a single quad E²POT. The gain range in this configuration can be trimmed between -0.5 to -2.0 over 64 steps. Increasing R5 and R6 (the feedback determining network in U2a for example) to 100KΩ will change the gain trim range to between -0.91 to -1.1. The inverting configuration shown is particularly suitable as this allows inputs signals to vary from ±10V without violating the digital pots terminal voltage specifications of ±5V.

An offset trimming configuration is shown in Figure 2 for the same pair of dual Op Amps. This configuration yields an offset trimming range of ±400mV over 64 steps. The offset range can be increased or decreased by changing the value of R13 (in amplifier U2a for example). Changing R13 to 1MΩ will decrease the offset range to ±40mV if finer resolution, but less range is desired. This configuration also ensures that the X9241 is operating within the specified terminal voltage range of less than ±5V.

Potpourri Amplifier

Figure 3 illustrates a microprocessor controlled circuit that can provide adjustable gain from -1 to infinity with two of the pots of the quad X9241W E²POT. The other two pots can be ganged together using the cascade mode for extended offset range. The purpose of this circuit is not to solve a particular analog signal processing problem, but rather to demonstrate the analog control flexibility that can be attained with the X9241.

With R2 set to 0 and R1 set to 63, the overall gain from input to output will be -1. Gain values in the range 0 to -1 can be set over 64 steps by incrementing the value of R1. Setting R1 back to 0 and setting R2 to 32 results in an overall gain of +1. Increasing R2 to 63 yields a gain of plus infinity. This is essentially a positive comparator with the threshold level being set by the cascade combination of R0 and R3. The National Semiconductor's LMC6482 is nice amplifier for this application because of its rail-to-rail input and output range.

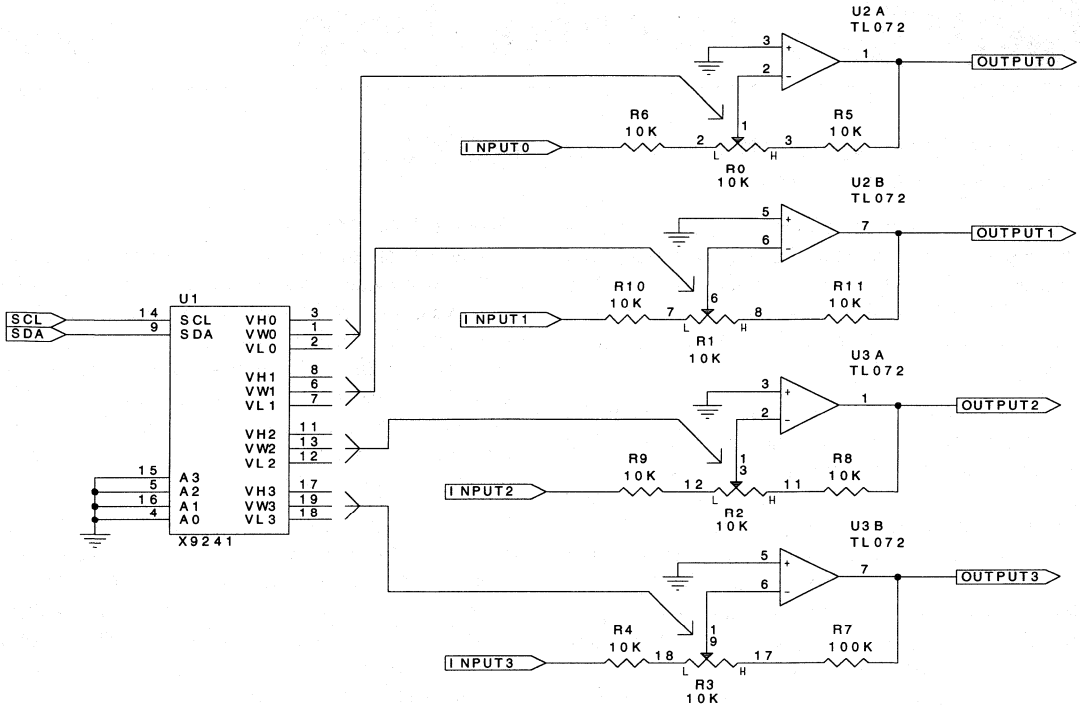

Figure 1. X9241 Controlled Gain Adjust

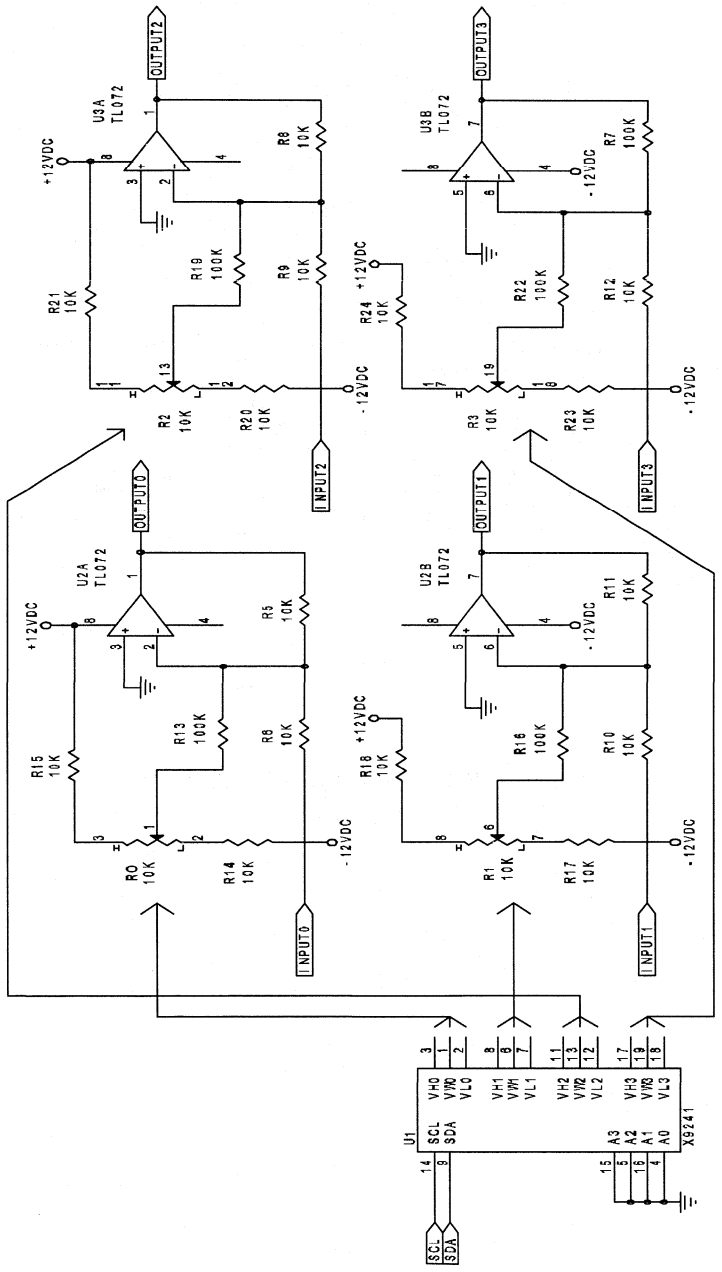

Figure 2. X9241 Controlled Offset Adjust

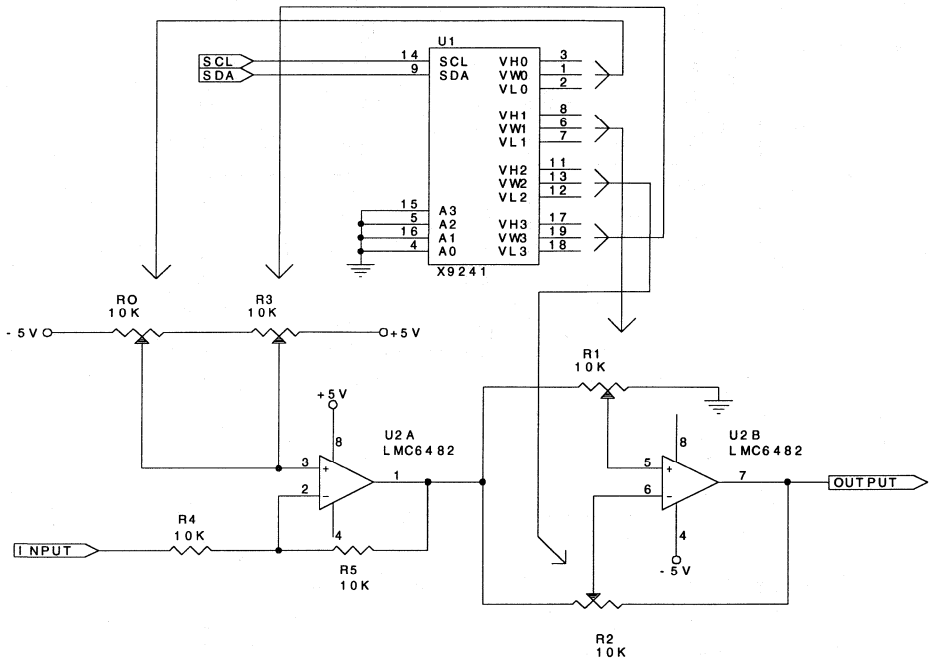

Figure 3. Extended Range Gain Adjust

Tone, Balance, and Volume Control using a Quad E²POT

by Applications Staff, October 1994

Imagine the possibilities of being able to integrate full audio tone, balance, and volume control into your multimedia computer product, without having to resort to any manual knobs. Naturally you could do that with a bunch of DACs all running under microprocessor control, but what happens if the audio amplifiers and sound generators come alive before the processor has had a chance to reload the preset values into the DACs. You could get blasted before the initialization sequence is complete.

Fortunately Xicor has solved this problem with the X9241 E²POTs. These devices can store the last position set by control and automatically reload these values into the pot tap registers upon power-up. Shown in the figure is the Xicor X9241U quad 50KΩ E²POT used to control the treble, bass, balance, and volume parameters of the LM1035 stereo audio processor. Unlike a conventional DAC, the Xicor devices can reload the last value, or a preset value, into the tone/balance and volume registers upon power-up, so you get predictable sound level conditions without any danger of over-driving the power amplifier.

The two channel stereo circuit shown provides approximately ±15dB of bass and treble boost (or cut) along with a 70dB balance and volume control range with the values shown (consult the LM1035 data sheet for full details and other configurations). It's a good idea to run the X9241 from an analog power supply in order to minimize noise picked-up from any digital circuits. The circuit shown uses the current source from within the LM1035 to provide power to the X9241. It would be nice to use the internal zener voltage regulator on the LM1035, but it is rated typically at 5.4V and the maximum supply voltage for the X9241 is 5.5V. An external shunt regulator (VR1) is used to maintain the supply voltage input to X9241 at a nominal 5V.

The full functionality and performance of the LM1035 is not impaired in any way by using E²POTs. The audio processing possibilities using the combo are many and varied, just remember to use good grounding and shielding techniques to minimize hum and noise.

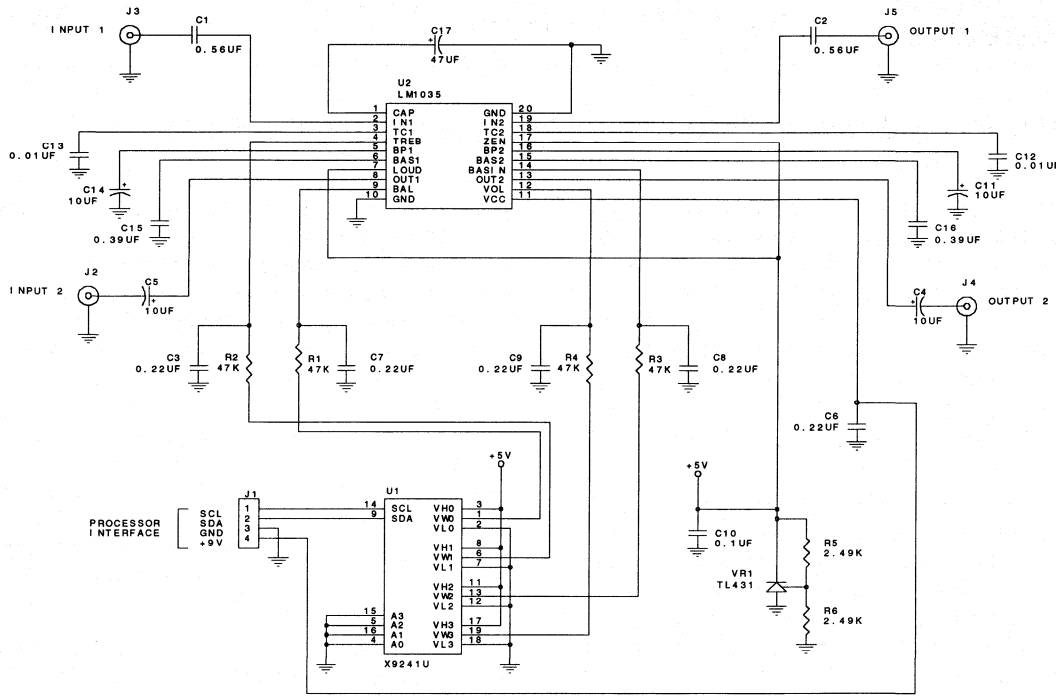

Figure 1. X9241 Dual Tone/Balance/Volume Controller

Power Supply and DC to DC Converter Control using E²POTs

By Richard Downing, October 1994

Introduction

The output voltage of power supplies and DC to DC converters is regulated by dividing down the output, comparing it with a stable reference, amplifying the error, and then using this error signal to control the input to output power transfer. Many applications use an expensive and unreliable mechanical potentiometer in the divider to precisely set the output voltage, as shown in Figure 1.

For fixed output supplies, manually adjusting the mechanical pot is a costly and time consuming operation that is prone to error. Physical access to the pot must be provided, which often requires less than optimal PCB layout and additional access holes in the chassis of enclosed units. Though initially set during production, the mechanical pot is subject to shock and vibration, incurring wiper position changes. Humidity and moisture can result in resistive changes and the prying hands of service technicians or end users can also affect accuracy. For variable output supplies, mechanical pots prevent the option of automated or remote adjustment.

To overcome these problems, a potentiometer would have to be electronically programmable in order to eliminate costly and potentially inaccurate manual settings, nonvolatile so as to power-up at the proper setting, and reprogrammable for testing in the factory or for adjustments in the field.

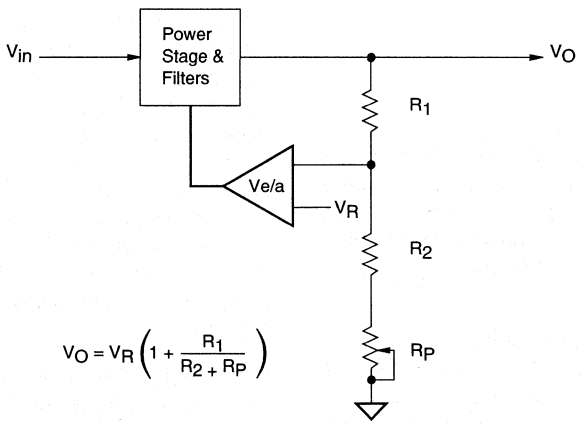

Figure 1

9

Implementing Designs with E²POTs

An example of a part that meets all of these requirements is the X9CMME from Xicor, shown in Figure 2. This electrically erasable, programmable nonvolatile potentiometer (E²POT) greatly simplifies manufacturing and test, and with a wiper position retention in excess of 100 years, can significantly increase field reliability.

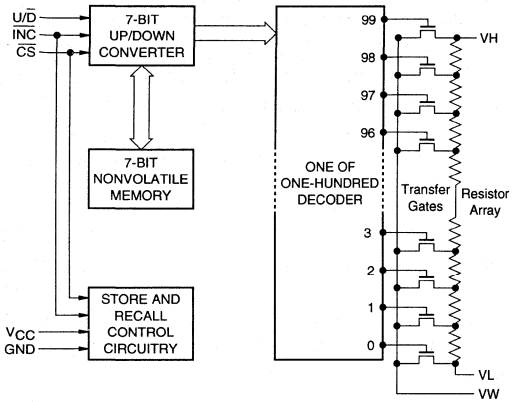

Figure 2.

Available in 8-pin DIP or SOIC packages, the 100 wiper position X9CMME is easily implemented into a circuit. Terminal connections are made in the same way as a mechanical pot. The part's three control lines can be brought out through a connector to automate programming and to test equipment, as shown in Figure 3.

$\overline{INC}$, U/$\overline{D}$, and $\overline{CS}$ pins control the setting of the wiper. Pulling $\overline{CS}$ LOW enables the part. Each HIGH to LOW transition on the $\overline{INC}$ line increases or decreases (depending on the state of U/$\overline{D}$) the resistance of the pot. After reaching the desired output voltage, the final wiper setting can be stored in nonvolatile memory by bringing $\overline{CS}$ HIGH while $\overline{INC}$ is HIGH. This ensures that the X9CMME powers-up at the last setting. It may appear that this is the only operating sequence for power supply applications, but there is at least one important scenario where wiper position storage is not required.

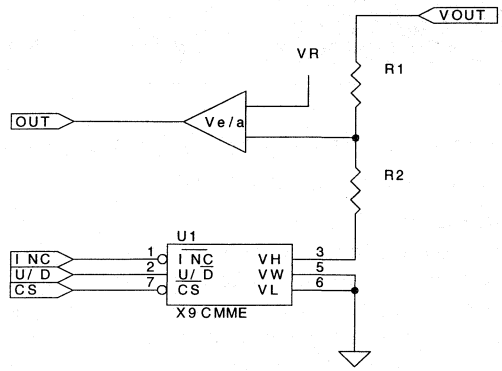

Figure 3.

Overvoltage Testing

Overvoltage (OV) testing has always presented a challenge to the manufacturing engineer. If a mechanical potentiometer is available, it must be adjusted manually to test the OV protection circuitry and then readjusted to reset the output voltage. If there is no potentiometer in the system, or even if there is one that is not easily accessible, an external power supply must be connected to the unit under test (UUT). The voltage on the external supply is then raised while monitoring the UUT, to determine the point at which it shuts-down. This often requires observation of waveforms internal to the UUT that are also difficult to access, compounded by the fact that the UUT control circuitry may obscure the response of the OV protection circuitry. This cumbersome procedure can be eliminated through the use of E²POTs.

If the output voltage in Figure 3 is 5V, with a 2.5V reference, and R1 is 10KΩ and R2 is 4.99KΩ, a good choice of E²POT for voltage regulation and overvoltage testing would be the X9C103 (10KΩ version of the X9CMME.) Having adjusted the output voltage to meet spec. at some nominal line and load, and after storing this setting in nonvolatile memory by deselecting the part with $\overline{INC}$ HIGH, the testing of the power supply can begin. When the OV portion of the test is reached, the output voltage is increased by toggling the $\overline{INC}$ pin of the E²POT while holding U/$\overline{D}$ LOW. Upon reaching the OV trip point and the supply shutting-down, the final value of the output voltage can be automatically recorded and compared to a maximum allowable value. The automatic test

equipment (ATE) could then generate a pass/fail response. Provided $\overline{CS}$ does not transition from HIGH to LOW with $\overline{INC}$ HIGH, the OV trip point wiper position will not be stored and the E^2POT will return to the previously calibrated regulation voltage upon power-up. This approach provides an accurate, automated means of overvoltage testing.

The X9CMME provides 100 tap positions for terminal voltages of ±5V and is available in 1KΩ, 10KΩ, 50KΩ, and 100KΩ versions. The X9312 gives an extended 0 to 15V terminal voltage capability and the X9313 provides an inexpensive 32 tap alternative. All single E^2POTs share the same pinout and are available in DIP and SOIC packages.

Quad E^2POT

For multiple output power supplies or in applications where resolution greater than 100 wiper positions is required, Xicor offers the X9241 Quad E^2POT, shown in Figure 4. Designed to interface directly with a microcontroller, the X9241 can be directly programmed with a wiper position or incremented/decremented tap-by-tap like the X9CMME.

The Quad E^2POT contains four 64 wiper position pots in a single 20 pin package. Each pot has a wiper counter register (WCR) that controls the wiper position and four nonvolatile registers that store wiper settings. The part provides four pins for device addressing, allowing as many as 16 devices to share the same bus, using an instruction oriented protocol. Registers and wiper positions can be read and written by the ATE using a two-wire bidirectional serial interface.

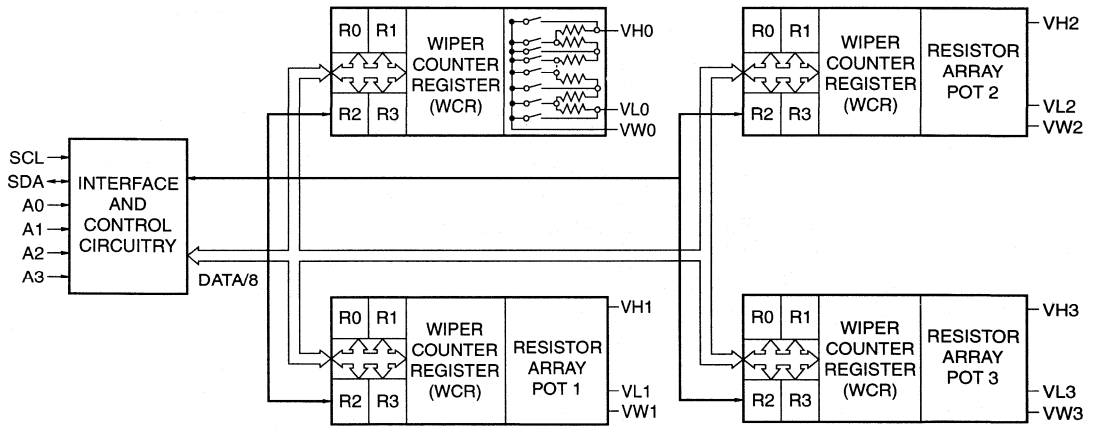

Figure 4.

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Internal support is available for cascading pots together in series or parallel to increase resolution and provide larger or smaller potentiometer values. These cascading configurations can be implemented in any number of ways using two or more pots. For example, using the X9241M (2KΩ, 10KΩ, 10KΩ, 50KΩ combo version), two pots to can be used to give a fine and course adjustment for setting the regulated output voltage and testing the overvoltage circuitry. This configuration is shown in Figure 5. Pot 3 can be used to provide course adjustment with 800Ω (50KΩ/63) steps and pot 0 to rpovide fine adjustment with 32Ω (2KΩ/63) steps. The wiper position is changed using the increment/decrement or write WCR commands. Wiper settings are stored in nonvolatile memory by directly writing to data registers or transferring data from WCRs to data registers. Each pot's WCR is loaded with contents of data register 0 upon power-up.

The X9241 is a ±5V terminal device available in 2KΩ, 10KΩ, 50KΩ, and combination versions, with either DIP or SOIC package options. This digitally controlled IC greatly simplifies and automates manufacturing and test. Like the X9CMME, nonvolatile storage retention of the X9241 is at least 100 years, providing a significant increase in field reliability.

Conclusion

Nonvolatile digitally controlled E²POTs provide significant advantages over mechanical potentiometers for power supplies in both manufacturing and in the field. Automated assembly and test provide labor savings, while increasing repeatability and eliminating human error. Immune to shock and vibration, and with superior resistance to environmental stress, E²POTs increase long term reliability. In the never ending struggle to cut costs and increase quality, Xicor E²POTs are a major enhancement in the design of power supplies and DC to DC converters.

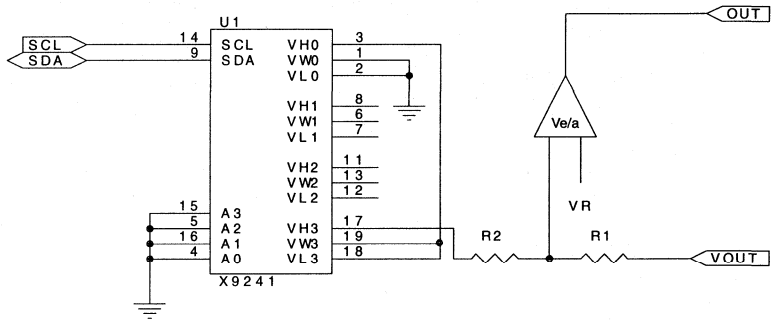

Figure 5

Designing with Xicor E²POTs

by Gray Creager, December 1994

Introduction

The use of Xicor's nonvolatile digital potentiometers (E^2POTs) can simplify and/or solve many mixed signal design problems, however in some applications, a deeper understanding of E^2POT technology may be required during the design process. In this note, additional information is provided relating to resolution, wiper noise, temperature coefficients, wiper current limitations, wiper leakage current, terminal voltage limitations, independent linearity, frequency response, hysteresis, reliability failure rates, NMOS and CMOS device differences, and logarithmic tapers. A summary of available E^2POTs and associated parameters is also included to aid the designer in choosing the correct device. Using the information and tips provided, a designer should be able to overcome most design problems that could be encountered.

Resolution

Simply put, the resolution of a potentiometer is a measure of the difference between adjacent tap positions. In a ratiometric application, this would correspond to a voltage step, whereas in resistive applications, the resolution more closely corresponds to an incremental resistance. A theoretical resolution can be defined as a measurement of the sensitivity to which the output ratio may be adjusted and is equivalent to the reciprocal of the number of taps (neglecting tap zero) expressed as a percentage. The precision with which this can be set is often called the adjustability or settability. On standard E^2POTs, either 100, 64, or 32 taps are available to the hardware designer, providing resolutions of 1.01%, 1.59%, and 3.23% respectively. These resolutions are approximately constant from tap to tap (though the relative linearity is more conservatively specified to be 20%) and the potentiometer exhibits monotonic behavior as the wiper is moved. With quad devices (i.e. X9241), internal cascading can be implemented with software commands, allowing up to 253 taps (0.39% resolution). On the newer generation E^2POTs, even higher resolutions will be possible using dual 128 tap and dual 256 tap devices. However, with standard E^2POTs, extremely high resolutions are already possible with external hardware or the use of certain software schemes (see Xicor application note AN43 "Software Implements a High Resolution Nonvolatile Digital Potentiometer"). A similar analysis will hold for E^2POTs connected as rheostats, however it should be noted that there will always be a small MOSFET channel resistance in series with the wiper terminal, due to the NMOS wiper transistor switch, which limits the minimum possible resistance in those applications. This wiper resistance can even manifest itself to a lesser extent in ratiometric applications by adding a term to the voltage divider expression. A simple formula to determine the channel resistance of these long channel NMOS wiper transistors (operated in the triode region) on is given in Eq. (1.1), along with the conditions for the triode region of operation in (Eq. (1.2)).

$$R_{DS} = \left[\left(\frac{\mu\varepsilon}{t_{ox}}\right)\left(\frac{W}{L}\right)(V_{GS} - V_t)\right]^{-1} \qquad \textbf{(1.1)}$$

$$V_{GS} - V_t > V_{DS} > 0 \qquad \textbf{(1.2)}$$

It can be seen from Eq. (1.1) that the MOSFET channel resistance is inversely proportional to V_{GS}. Since the source of the transistor is connected to the wiper terminal (which can have a varying voltage), the gate voltage of the wiper transistor in an E^2POT must be maintained at a high enough voltage to guarantee operation in the triode region. Internally, this is accomplished with another charge pump (which generates between 10V and 18V depending on tap position and device). With appropriate substitutions, this resistance can be estimated from Eq. (1.3) with V_W as the wiper voltage in Volts and T in degrees Celsius, using the parameters from the chart in Fig. 4 on page 6 of this note.

$$R_W = [K_1]V_W + K_2 \quad \textbf{(1.3)}$$

Nominally, this resistance is 40Ω, but it increases as temperature increases and has been measured to be as high as 90Ω over the industrial temperature range (-40°C to +85°C). The voltage drop across this wiper transistor is equal to V_{DS} and can be approximated for various wiper currents using Eq. (1.4), which is an equation for I_{DS} of a MOSFET operated in the triode region.

$$I_{DS} = \left(\frac{\mu\varepsilon}{t_{ox}}\right)\left(\frac{W}{L}\right)\left[(V_{GS} - V_t)V_{DS} - \frac{(V_{DS})^2}{2}\right] \quad \textbf{(1.4)}$$

Using some substitutions based upon Xicor process and design parameters, this equation reduces to the expression in Eq. (1.5), where V_{DS} is in units of Volts.

$$I_W = (49.5 - 3.3V_{DS})(V_{DS}) \quad mA \quad \textbf{(1.5)}$$

Resolutions can also be expressed in terms of dynamic range (DR). At approximately 6dB/bit, a 100 tap E^2POT has an equivalent DR of 39dB. Similarly, DRs of 36dB and 30dB exist for the 64 and 32 tap E^2POTs respectively.

Wiper Noise

An E^2PROM cell requires a high voltage to initiate Fowler-Nordheim tunneling, the phenomenon upon which much of the industry bases its EEPROM technology. In order to generate such voltages (as high as 18V), Xicor devices use an internal charge pump. There are other aspects of Xicor's process that also require the use of charge pumps (e.g. to provide a negative substrate bias for the IC die). For each charge pump, there must necessarily be an associated oscillator. It is these oscillators which contribute high frequency noise to signals on the wiper of the potentiometer. However, with knowledge of the cutoff frequency and internal oscillator frequencies of a particular E^2POT, this effect can be minimized.

The most direct solution is to add a first order lowpass filter to the wiper terminal in order to attenuate all of these unwanted frequencies. Since there is a wiper resistance (see Eq. (1.1)) associated with every E^2POT, simply connecting a capacitor between the wiper and V_{SS} will implement a passive RC filter. This wiper resistance varies due to loading and temperature, so a more accurate way of connecting an RC lowpass filter is to add a known resistance in series with the wiper and use that value for calculating the size of the wiper capacitor. Using Eq. (1.6) and the information in Table 1, the appropriate value for the capacitor can be determined for either technique.

$$f = \frac{159 \times 10^3}{RC} \quad Hz \quad \textbf{(1.6)}$$

The units for Eq. (1.6) are Hz, Ω, and μF. Typically, a low cost, 20% monolithic capacitor of appropriate size connected between the wiper terminal and V_{SS} is sufficient to significantly attenuate the charge pump noise contribution. For example, with an X9C103, which has a -3dB frequency of 300KHz and an oscillator frequency of 2.5MHz, an approximate wiper capacitor is calculated to be between 0.013μF and 0.0016μF, assuming a wiper resistance of 40Ω. By choosing a 0.013μF capacitance, the wiper noise would be attenuated by -23dB compared to an unfiltered wiper. Unrelated to the charge pump are other inherent noise sources common to all CMOS devices. In particular, E^2POTs exhibit both thermal and flicker noise components. Overall, Xicor specifies a noise for an E^2POT which is equivalent to 1μV per square root Hz. An estimate of the total wiper noise from all sources in the E^2POT can be obtained from Eq. (1.7)

$$\text{noise amplitude} \leq \left(6.6\mu V_{p-p}\right)\left[\sqrt{f}\right] \quad \mu V_{p-p} \quad \textbf{(1.7)}$$

Where f (in Hz) is the bandwidth of interest for signals on the wiper. The result is a magnitude of peak to peak noise superimposed on the wiper voltage.

Temperature Coefficients

Often, the performance of a circuit over temperature is a crucial design consideration. For this reason, Xicor E^2POTs contain a unique compensation scheme to minimize the resistive drifts due to temperature variations. The principle here is similar to the operation of circuitry in a low drift voltage reference. In those references, different active devices (Zener diodes, BJTs, MOSFETs, etc...) have differing parameter drifts over temperature. By combining those that have negatively sloped drifts with those that have positively sloped drifts, in the right configuration, an output voltage drift can be held "flat" over the temperature range of interest. Though E^2POTs, utilize an entirely different implementation

(i.e. there are no active elements), the principle is the same. This can be very important when a highly accurate bias voltage needs to be maintained over extreme temperature swings. In Eq. (1.8), the standard definition for a temperature coefficient is given in equation form.

$$TC = \left[\frac{(R_1 - R_2)}{R_1(T_2 - T_1)}\right](10^6) \quad ppm/°C \quad \textbf{(1.8)}$$

The temperature coefficient expresses a resistive drift in parts per million per degree centigrade, where R_1 is the resistance at reference temperature T_1 and R_2 is the resistance at the test temperature T_2. For Xicor's E^2POTs, the ratiometric temperature coefficients are good (at 20-30 ppm/°C) due to the resistor ladder structure, however the end-to-end resistance temperature coefficients are typically an order of magnitude or more higher.

Wiper Current Limitations

An important specification on Xicor's E^2POTs is the 1mA wiper current limit. However, the motivation behind this specification is primarily historical. On Xicor's older NMOS processes, the 1mA limit was required due to electromigration concerns with the metallization process. This was an industry wide reliability concern that sparked considerable research several years ago. For semiconductor devices, high currents, coupled with small cross-sectional areas for Aluminum metal lines, can lead to early device failures due to the migration of the Al ions. These failures often occur as open circuits (and occasionally short circuits) on the IC itself. Since the electromigration issue relates to long term reliability, the concern here is to avoid continuous operation in a mode that could lead to a failure, consequently DC current levels are of primary concern. An expression for the predicted mean time before a failure is given by Eq. (1.9).

$$MTBF \propto \frac{1}{J^2}\exp\left(\frac{-E_a}{kT}\right) \quad \textbf{(1.9)}$$

This Arhennius relationship expresses how strongly related electromigration failures and current densities are on a chip. The exponential dependence upon temperature is exhibited as well. The constant of proportionality can be determined by experimentation, assuming an average E_a of 0.44eV.

Notice that a tripling of current density anywhere that electromigration exists will reduce the MTBF nine-fold! Though these effects have not been entirely eliminated, good design as well as the use of several fabrication tricks have made electromigration less problematic than it once was. In order to make the newer CMOS parts as compatible as possible to existing NMOS parts, this 1mA limit, which has always been related to long term reliability, was also adopted. Though Xicor now adds Copper ions to the Aluminum metallization to improve reliability, this 1mA limit has been retained. A more realistic, yet still conservative DC wiper current limit for the CMOS devices would be on the order of 3.5mA.

When larger currents must be controlled, many techniques can be used to boost the current supplied by a given wiper voltage. A straight- forward and practical example would use the buffering voltage follower Op Amp configuration in Fig. 1. If the current gain of the Op Amp is too small, then additional gain stages could also be added on the output of the Op Amp. A wiper capacitor is shown here to diminish wiper noise on the Op Amp input. However, there are many other possible circuits to accomplish current gains for the E^2POT wiper currents.

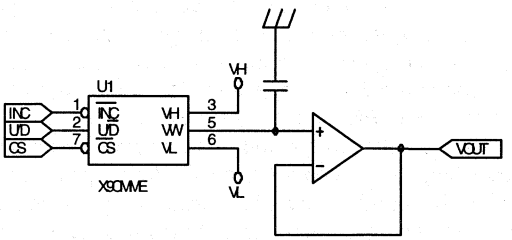

Figure 1 - Voltage Follower to Increase Output Current

Wiper Leakage Current

On E^2POTs which have differing f_{OSC1}, f_{OSC2}, and f_{OSC3} oscillator frequencies (see Table 2), slight voltage changes can appear on the wiper terminal depending on the whether $\overline{CS}$ is asserted or not (or whenever a nonvolatile store is being performed). This has often been misinterpreted as a DC leakage current, however, this is not the case! The

phenomenon that is actually being observed is the Body Effect, an inherent MOSFET mechanism which modulates a transistor's threshold voltage whenever the voltage between the bulk and the source is not exactly zero (i.e. $| V_{BS} | \neq 0$). Since the bulk (substrate) potential of an E²POT die is charge pumped down to a negative substrate voltage (V_{BB}), fluctuations in this substrate voltage will alter V_{BS}, thus changing the threshold voltage as well. Eq. (1.10) shows this relationship.

$$V_t = V_{t0} + \gamma\left[\sqrt{(\phi_S + |V_{BS}|)} + \phi_S\right] \quad \textbf{(1.10)}$$

Here, γ is a process parameter that is generally between 0.5 and 2 for any particular semiconductor manufacturer. This effect can cause $\Delta V_W \approx 5mV$ to 10mV in the worst case scenarios. Returning $\overline{CS}$ to the previous level will remove ΔV_W from the wiper as well.

Terminal Voltage Limitations

Occasionally, there is a need for a higher or lower tolerance on the terminal voltages of an E²POT. On typical devices, the limit is ±5V with respect to V_{SS}, however on the X9312, a range between V_{SS} and +15V is allowed. The issue limiting the terminal voltages has to do with specific breakdown mechanisms in the MOSFET structure. As the wiper decode logic attempts to maintain a steady voltage across the gate and source of the transistor, any increase in the voltage at the source must result in an increase of the voltage applied at the gate. Beyond a certain level, PN junction breakdown occurs. By limiting the voltages allowed at the source, as well as preventing the decode circuitry from generating excessive voltages, this breakdown can be avoided. Unfortunately, this limits the voltages allowed on the terminals (V_H and V_L). Since expansion of this range is limited by design and process considerations, external techniques must be employed to accomplish this task. Fig. 2 shows a simple configuration that can generate an output voltage with a larger swing than that from an individual E²POT. In this circuit, current gain can also be realized depending on the output of the Op Amp. Also, another technique is shown for reducing wiper noise. Here the capacitor is attached across the input terminals of an inverting Op Amp scheme.

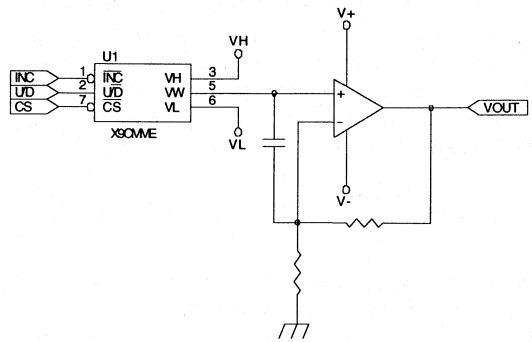

Figure 2 - Op Amp Circuit to Increase Output Voltage Range

Independent Linearity

With potentiometers, independent linearity is defined to be the maximum deviation from ideal behavior, expressed as a percentage of the voltage applied across the terminals. With E²POTs, similar information can be obtained using the absolute linearity specification. For this measurement, Xicor refers to a minimum increment (MI) unit that is defined in Eq. (1.11)

$$\frac{V_H - V_L}{\#TAPS - 1} = 1\ MI \quad \textbf{(1.11)}$$

Converting this absolute linearity specification (Eq. (1.12)) into an independent linearity, it is seen that all 100 tap E²POTs exhibit a 1.01% independent linearity.

$$V_{W(actual)} - V_{W(expected)} \leq \pm 1\ MI \leq \pm 1\ LSB \quad \textbf{(1.12)}$$

From these definitions, equivalent INL (integral non-linearity) and DNL (differential non-linearity) can be determined for E²POTs. The INL is 1 LSB and the DNL is 0.2 LSB.

Frequency Response

The frequency response of any E²POT will be limited by the response of its RC time constant. Xicor characterizes a typical -3dB point (½ power point) for a given end-to-end resistance by taking measurements when the wiper is set to a mid-range tap position. Due to variations in the end-to-end resistance of a given device (Xicor specifies ±20% on this parameter) and the likelihood that useful circuits

will require tap settings outside of mid-range, the frequency response of an E²POT will show some variance. However, for any fixed tap position, this -3dB point exhibits little dependence on fluctuations in V_{CC} or temperature. A summary of the expected -3dB point range for any given end-to-end resistance at 5V and +25°C and mid-range is shown (Table 1).

Table 1 - E²POT Frequency Response (-3dB Point Ranges)

R_{TOT}	f_{-3dB}
1 KΩ	2400 - 2600 KHz
2 KΩ	1070 - 1600 KHz
10 KΩ	260 - 320 KHz
50 KΩ	52 - 68 KHz
100 KΩ	32 - 36 KHz

For tap positions other than mid-range, estimations for the frequency response can be carried out assuming between 20pF and 25pF for the total wiper capacitance to ground. Remember that the end-to-end resistance will vary from device to device, thus in critical designs the appropriate error margins must be considered. In the case of the logarithmic taper E²POTs, the mid-range tap positions do not correspond to mid-range of the end-to-end resistance, therefore the -3dB points will not correspond to those in Table 1. For example, the X9314W exhibits a mid-range -3dB point of approximately 180KHz, not 290KHz as predicted above.

Hysteresis

One interesting quirk in the behavior of mechanical potentiometers is that there is a sort of "hysteresis" effect on the wiper voltage when changing wiper positions. The potentiometer's electrical characteristics won't change until a certain amount of mechanical travel has occurred by the knob. This results in a "lurching" behavior that makes fine trimming rather tedious. With Xicor's digital potentiometers, this behavior is entirely avoided. Another measure of hysteresis would be the change in output voltage at a certain wiper tap when the wiper is moved to either full scale (or zero scale) and then returned to the original tap position. Since Xicor devices are strictly monotonic and avoid the mechanical behavior of traditional potentiometers, any movement of the wiper will result in a change to the wiper voltage and for any movement from an initial tap position to other tap positions and back to the initial tap position, it can be observed that E²POTs exhibit no hysteresis effects (i.e. the wiper returns precisely to the same voltage).

Reliability Failure Rates

With or without a knowledge of the number of transistors on a die, an MTBF can be calculated to determine the average lifetime of an IC. For the X9CMME family of E²POTs, internal qualification data has yielded an MTBF of 2154 years based on the number of failures (0 out of 353) during a 1000 hour dynamic life test at 150°C. This data could also be expressed as 53 FITs at 55°C for a 60% upper confidence limit. The number of FITs is equivalent to the number of failures per billion device hours (see Xicor reliability reports RR-520 and RR-515 for a more complete explanation of the FITs parameter). This data helps predict the reliability of the standard logic on an E²POT, but similar results would be obtained for the charge pump and E²PROM cell circuitry. However, some electromigration failures might occur on the resistor chain before anything else on the IC fails, particularly if the 1mA limit is not strictly observed. The exact lifetimes for various wiper current loads are not explicitly known, however similar results will be obtained in a reliability analysis for any of Xicor's E²POTs.

NMOS and CMOS E²POT Differences

Xicor introduced the first E²POTs in 1984 using an NMOS technology. When these devices were replaced by CMOS designs, an extra standby current mode was added that allowed for the power savings benefits of CMOS circuitry. To implement this extra mode, a NOR gate was added between the $\overline{CS}$ and $\overline{INC}$ inputs. When the output of this NOR gate is HIGH, the wiper transistor decoder is enabled and the wiper position can be moved. Consequently on power-up, if both of these pins are held LOW, then the wiper position will be recalled from the E²PROM and the wiper will move one additional position depending on the state of the U/$\overline{D}$ pin. Subsequent movements require that the output of this gate see a rising edge, thus either $\overline{CS}$ or $\overline{INC}$ must be "clocked" in order for the wiper to be moved any further. This

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behavior can cause the power-up wiper positions to be off by one tap position if precautions are not taken. The standby power mode is available on all CMOS E^2POTs. Another difference that exists between the NMOS wiper and CMOS wiper E^2POTs is the length of time it takes to deselect the previous wiper position and select the new wiper position, when changing taps. Because the switching of these FETs works in a "make-before-break" mode, the use of NMOS wiper E^2POTs in certain audio configurations may require extra precautions to avoid audible "clicking" sounds on the speaker while the wiper position is being adjusted. The differing device technologies are summarized in Table 2 along with several other pertinent parameters.

Logarithmic Tapers

With some E^2POTs, the option to have a logarithmic taper instead of a linear taper exists. The logarithmic version of the X9313 is the X9314, likewise the logarithmic version of the X9511 is the X9514. Currently, these devices are available in 1KΩ and 10KΩ end-to-end resistances. A typical logarithmic response is shown in Fig. 3.

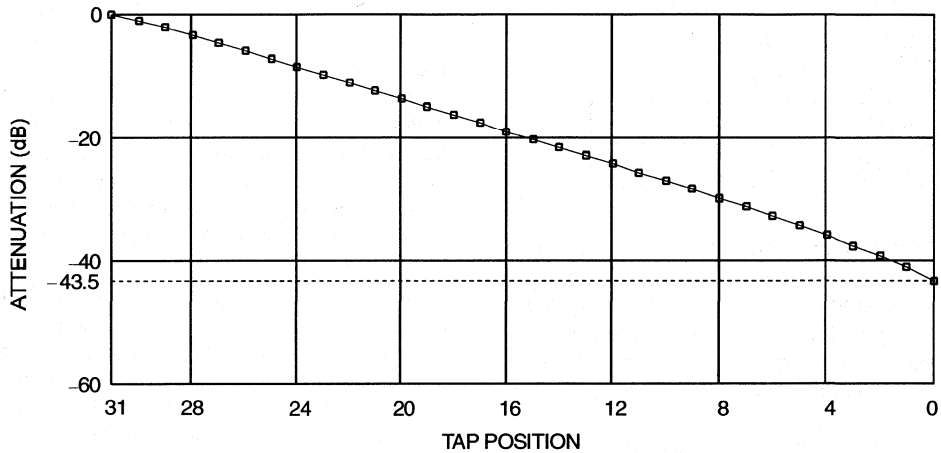

Figure 3 - Typical Logarithmic Taper Response of an X9514 or X9314

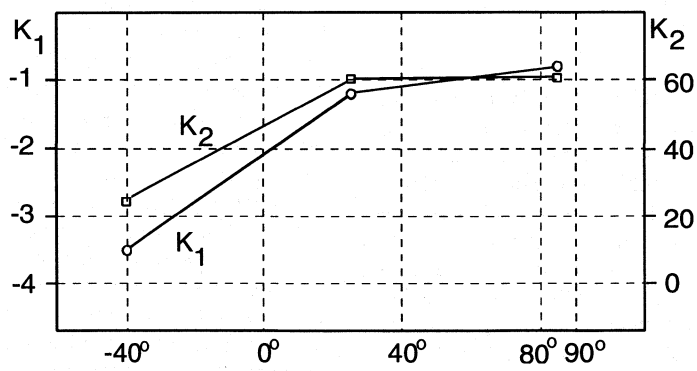

Figure 4 - K_1 and K_2 for use in equation (1.3)

Table 2. E²POT Parameter Summary

E²POT	PROCESS	f_{OSC1}	f_{OSC2}	f_{OSC3}	f_{-3dB}	TAPS	V_H, V_L	R_{TOT}
X9102[1]	NMOS	5.0 MHz	5.0 MHz	5.0 MHz	2.50 MHz	100	±5V	1 KΩ
X9103[1]	NMOS	5.0 MHz	5.0 MHz	5.0 MHz	0.30 MHz	100	±5V	10 KΩ
X9503[1]	NMOS	5.0 MHz	5.0 MHz	5.0 MHz	0.06 MHz	100	±5V	50 KΩ
X9104[1]	NMOS	5.0 MHz	5.0 MHz	5.0 MHz	0.04 MHz	100	±5V	100 KΩ
X9C102[2]	CMOS	2.5 MHz	2.5 MHz	2.5 MHz	2.50 MHz	100	±5V	1 KΩ
X9C103[2]	CMOS	2.5 MHz	2.5 MHz	2.5 MHz	0.30 MHz	100	±5V	10 KΩ
X9C503[2]	CMOS	2.5 MHz	2.5 MHz	2.5 MHz	0.06 MHz	100	±5V	50 KΩ
X9C104[2]	CMOS	2.5 MHz	2.5 MHz	2.5 MHz	0.04 MHz	100	±5V	100 K
X9311Z[1]	CMOS	5.0 MHz	5.0 MHz	5.0 MHz	2.50 MHz	100	+10V	1 KΩ
X9311W[1]	CMOS	5.0 MHz	5.0 MHz	5.0 MHz	0.30 MHz	100	+10V	10 KΩ
X9311U[1]	CMOS	5.0 MHz	5.0 MHz	5.0 MHz	0.06 MHz	100	+10V	50 KΩ
X9311T[1]	CMOS	5.0 MHz	5.0 MHz	5.0 MHz	0.04 MHz	100	+10V	100 KΩ
X9312Z	CMOS	2.5 MHz	2.5 MHz	5.0 MHz	2.50 MHz	100	+15V	1 KΩ
X9312W	CMOS	2.5 MHz	2.5 MHz	5.0 MHz	0.30 MHz	100	+15V	10 KΩ
X9312U	CMOS	2.5 MHz	2.5 MHz	5.0 MHz	0.06 MHz	100	+15V	50 KΩ
X9312T	CMOS	2.5 MHz	2.5 MHz	5.0 MHz	0.04 MHz	100	+15V	100 KΩ
X9313Z	CMOS	2.5 MHz	0.8 MHz	5.0 MHz	2.50 MHz	32	±5V	1 KΩ
X9313W	CMOS	2.5 MHz	0.8 MHz	5.0 MHz	0.30 MHz	32	±5V	10 KΩ
X9313U	CMOS	2.5 MHz	0.8 MHz	5.0 MHz	0.06 MHz	32	±5V	50 KΩ
X9313T	CMOS	2.5 MHz	0.8 MHz	5.0 MHz	0.04 MHz	32	±5V	100 KΩ
X9314W	CMOS	2.5 MHz	0.8 MHz	5.0 MHz	0.18 MHz	32	±5V	10 KΩ,
X9315Z	**CMOS[4]**	**N/A**	**N/A**	**5.0 MHz**	**2.50 MHz**	**32**	**+5V**	**1 KΩ ext. voltage**
X9315W	**CMOS[4]**	**N/A**	**N/A**	**5.0 MHz**	**0.30 MHz**	**32**	**+5V**	**10 KΩ ext. voltage**
X9511Z	CMOS	2.5 MHz	0.8 MHz	5.0 MHz	2.50 MHz	32	±5V	1 KΩ
X9511W	CMOS	2.5 MHz	0.8 MHz	5.0 MHz	0.30 MHz	32	±5V	10 KΩ
X9514W	CMOS	2.5 MHz	0.8 MHz	5.0 MHz	0.18 MHz	32	±5V	10 KΩ,
X9221Y	CMOS	2.0 MHz[3]	2.0 MHz[3]	5.0 MHz	1.33 MHz	64	±5V	2 KΩ, dual
X9221W	CMOS	2.0 MHz[3]	2.0 MHz[3]	5.0 MHz	0.30 MHz	64	±5V	10 KΩ, dual
X9221U	CMOS	2.0 MHz[3]	2.0 MHz[3]	5.0 MHz	0.06 MHz	64	±5V	50 KΩ, dual
X9241Y	CMOS	2.0 MHz[3]	2.0 MHz[3]	5.0 MHz	1.33 MHz	64	±5V	2 KΩ, quad
X9241W	CMOS	2.0 MHz[3]	2.0 MHz[3]	5.0 MHz	0.30 MHz	64	±5V	10 KΩ, quad
X9241U	CMOS	2.0 MHz[3]	2.0 MHz[3]	5.0 MHz	0.06 MHz	64	±5V	50 KΩ, quad
X9241M	CMOS	2.0 MHz[3]	2.0 MHz[3]	5.0 MHz	combo	64	±5V	combo, quad
X94xx family	**CMOS[4]**	**N/A**	**N/A**	**5.0 MHz**	**N/A**	**64-256**	**±5V**	**SPI and I²C ext. voltage**

boldface denotes devices to be introduced in 1995

f_{OSC1} = $\overline{CS}$ LOW, f_{OSC2} = $\overline{CS}$ HIGH, f_{OSC3} = during nonvolatile store

[1]obsolete part

[2]on older X9CMME devices, f_{OSC2} is 0.8MHz

[3]no $\overline{CS}$ on part, parameter is active at all times, except during nonvolatile stores

[4]newer devices utilizing a full CMOS pass transistor structure on the wiper

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E²PROM Programmer Vendors for Xicor Devices

by Gray Creager, March 1995

The following listing summarizes the most current information available to Xicor regarding external support of our products. Each manufacturer's listing has been condensed in order to provide a legible cross-reference between a part and the available programming support. For other information pertaining to a particular part and programmer (such as adapter, software revision, etc...), the third party manufacturer/representative or a Xicor sales office should be contacted.

Advantest Corporation of America
1100 Busch Pkwy.
Buffalo Grove, IL 60089
(708) 634-2552

A1 = TR4943/8, R4944/(A), R4949

American Reliance Inc.
11801 Goldring Rd.
Arcadia, CA 91006
(818) 303-6688

B1 = 9850, B2 = 9860

Aval Data Corporation
Shin-Yuri 21,
1-2-2 Manpukuji ASO-KU,
Kawasaki, Kanagawa 215
(44) 952-1311

C1 = PKW-1100/2100/3100/5100

BP Microsystems
1000 N. Post Oak Rd., Suite 225
Houston, TX 77055-7237
(713) 688-4600

D1 = BP-1200/1148/2100, D2 = CP-1128,
D3 = EP-1140, D4 = EP-1132, D5 = EP-1

Bytek Corporation
543 N.W. 77th St.
Boca Raton, FL 33487-1323
(407) 994-3520

E1 = 135H, E2 = 145H, E3 = MultiTRK
E4 = EZ-KF

Data I/O Corporation
10525 Willows Rd. N.E.
P.O. Box 97046
Redmond, WA 98073-9746
(206) 881-6444

F1 = 3900, F2 = Unisite, F3 = PSX

Logical Devices, Inc.
692 S. Military Trail
Deerfield Beach, FL 33442
(305) 974-0967

G1 = Allpro 40, G2 = Allpro 88, G3 = AP88XR
G4 = Shooter, G5 = Prompro 8X, G6 = Husky
G7 = Gangpro S, G8 = Gangpro 8+
G9 = Gangpro SII

Needham's Electronics, Inc.
4630 Beloit Dr., Suite #20
Sacramento, CA 95838
(916) 924-8037

H1 = EMP-20

Stag Microsystems, Inc.
1600 Wyatt Dr.
Santa Clara, CA 95054
(408) 988-1118

I1 = ORBIT, I2 = ECLIPSE, I3 = SOLAR
I4 = 41M111, I5 = 39M101, I6 = 4xM101
I7 = QUASAR 10xx

System General Corporation
1603A S. Main St.
Milpitas, CA 95035
(408) 263-6667

J1 = Turpro-1 (/FX/TX), APRO, multi-APRO
J2 = Turpro 840

Tribal Microsystems Inc.
aka **Hi-Lo Systems Research Co., Ltd.**
44388 S. Grimmer Blvd.
Fremont, CA 94538
(510) 623-8859

K1 = FLEX-700 or ALL-07

Xeltek
757 N. Pastoria Ave.
Sunnyvale, CA 94086
(408) 524-1929

L1 = SuperPro (/EM)

EE Tools
544 Weddell Dr., Suite 6
Sunnyvale, CA 94089
(408) 734-8184

M1 = Allmax(+)
M2 = ProMax (see H1 listing)

Link Instruments, Inc.
369 Passaic Ave, Suite 100
Fairfield, NJ 07004
(201) 808-8990

N1 = CLK 3100

Advin Systems Inc.
1050 - L East Duane Ave.
Sunnyvale, CA 94086
(408) 243-7000

O1 = U84/U40/U32
O2 = Pilot 145/144/143/142
O3 = Pilot-GCE, O4 = Pilot-832

NOVRAMs and Serial E^2PROMs

	Part	A 1	B 1	B 2	C 1	D 1	D 2	D 3	D 4	D 5	E 1	E 2	E 3	E 4	F 1	F 2	F 3	G 1	G 2	G 3	G 4	G 5	G 6	G 7	G 8	G 9	H 1	I 1	I 2	I 3	I 4	I 5	I 6	I 7	J 1	J 2	K 1	L 1	M 1	N 1	O 1	O 2	O 3	O 4
#	X2001					*	*	*	*						*	*		*	*	*																*								
#	X2002																																												
#	X2004					*	*	*	*						*	*		*	*	*								*								*								
	X20C04					*																						*							*	*		*					
	X20C05					*																						*							*	*							
	X20C16					*	*	*	*																			*							*	*		*					
	X20C17					*		*	*																			*							*								
#	X2201A					*	*								*	*																				*								
#	X2210					*	*	*	*							*		*	*	*															*	*		*					
#	X2210A					*	*	*	*																											*								
	X22C10					*	*	*	*							*												*							*		*		*				
#	X2212					*	*	*	*							*		*	*	*																*	*		*					
#	X2212A					*	*	*	*																																				
	X22C12					*	*	*	*																			*							*				*					
	X24C00					*	*	*	*																			*							*	*							
	X24C01					*	*	*	*						*	*		*	*	*								*							*	*		*	*	*	*	*	*
	X24C01A					*	*	*	*						*	*												*							*	*		*		*	*	*	*
#	X2402		*			*	*	*	*						*	*		*	*	*															*		*			*	*		
	X24C02					*	*	*	*						*	*		*	*	*								*							*	*		*	*	*	*	*	*
#	X2404		*			*	*	*	*						*	*		*	*	*								*							*			*		*	*		
	X24C04					*	*	*	*						*	*		*	*	*								*							*	*		*	*	*	*	*	*
	X24C08					*	*	*	*						*	*												*							*	*		*	*	*	*	*	*
	X24C16		*			*	*	*	*						*	*		*	*	*								*							*	*		*	*	*	*	*	*
#	X2444					*	*	*							*	*		*	*	*											*							*			*			
	X24C44					*	*	*										*	*	*								*							*			*					
	X24C45					*	*	*										*	*	*								*							*			*					
	X24001					*	*	*	*																			*							*			*					
	X24012					*	*	*	*																			*							*	*			*	*	*	*	*
	X24022					*	*	*	*																			*							*	*			*	*	*	*	*
	X24042					*	*	*	*																			*							*	*			*	*	*	*	*
	X24164					*	*	*	*																			*							*				*				
	X24645																											*							*								
	X25C02					*	*	*	*																			*							*	*							
#	X25010																											*							*	*							
	X25020					*	*	*	*						*	*												*							*	*							
	X25040					*	*	*	*																			*							*	*							
	X25043					*	*	*	*																			*							*	*							
	X25080																											*							*								
	X25160																											*							*	*							
	X25320																											*							*	*							
	X25401					*	*	*	*																			*							*								
	X25640					*	*	*	*																			*							*	*							
	X25642																											*							*	*							
	X25128																											*							*	*							

(#) = part is not currently being manufactured by Xicor
(*) = part is supported by this programmer

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Bytewide E^2PROMs and Special Function E^2 Devices

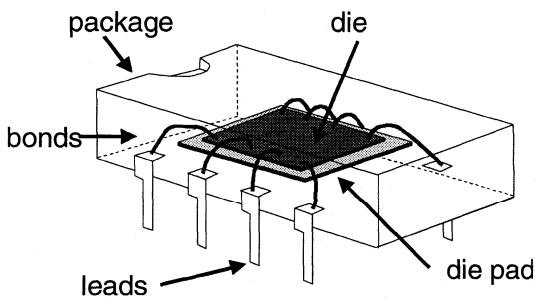
	Part	A1	B1	B2	C1	D1	D2	D3	D4	D5	E1	E2	E3	E4	F1	F2	F3	G1	G2	G3	G4	G5	G6	G7	G8	G9	H1	I1	I2	I3	I4	I5	I6	I7	J1	J2	K1	L1	L1	M1	N1	O2	O3	O4
#	X2804A		*	*		*	*	*	*	*	*	*	*	*	*	*	*	*	*	*		*	*	*			*	*	*	*	*	*	*	*		*	*	*	*	*		*	*	*
	X2804C																																												
#	X2816A	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*		*	*	*	*	*		*	*	*	*	*		*	*	*
#	X2816B	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*		*		*	*	*	*	*	*	*	*	*	*	*		*	*	*		*		*	*	*
	X2816C					*	*	*	*	*					*	*	*	*	*	*		*		*	*	*		*	*	*			*	*	*	*	*						
#	X28C16			*																							*	*	*		*	*	*			*		*	*						
#	X28HC16			*		*									*	*											*									*		*							
#	X2864A	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*		*	*	*	*	*	*	*	*	*	*	*	*	*		*		*	*	*		*	*	*
#	X2864B	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*		*	*	*	*	*	*	*	*	*	*	*	*	*		*		*	*	*		*	*	*
#	X2864H	*	*	*		*	*	*	*	*					*	*	*	*	*	*		*	*	*	*	*	*	*	*	*	*	*	*	*		*		*	*	*		*	*	*
	X28C64			*		*		*	*						*	*	*	*	*	*		*		*	*	*	*	*	*	*	*	*	*	*		*		*	*	*		*	*	*
	X28HC64			*		*		*	*						*	*	*										*		*							*		*	*	*		*	*	*
#	X28C64B														*	*																													
#	X28256	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*		*	*	*	*	*	*	*	*	*	*	*	*	*		*		*	*	*		*	*	*
	X28C256	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*		*	*	*	*	*	*	*	*	*	*	*	*	*		*	*	*	*	*		*	*	*
#	X28C256B														*	*	*												*		*		*		*		*	*						
	X28HC256			*		*		*	*	*					*	*	*										*									*	*	*	*	*		*	*	*
	X28VC256					*		*	*	*																	*									*	*	*	*	*		*	*	*
	X28TC256					*																					*									*	*							
	X28C512			*		*		*	*						*	*	*	*	*	*				*	*	*	*	*	*	*	*		*		*	*	*	*	*	*	*	*	*
	X28C513					*		*	*						*	*																							*	*		*	*	*
	X28C010			*	*	*		*	*						*	*	*	*	*	*				*	*	*	*	*									*	*	*	*	*	*	*	*	*
	X68C64					*									*	*											*									*		*						
	X68C75																										*									*								
	X76041					*																					*									*								
	X84041					*	*	*	*																		*									*								
	X86C64					*									*	*											*									*		*						
	X88C64					*		*	*						*	*		*	*	*							*									*		*		*	*			
	X88C75					*																					*									*								
	XM20C64																										*									*		*						
	XM20C64FR																																					*						
	XM20C64S																																											
	XM20C128S																																											
#	XM28C010			*		*		*	*		*	*	*	*	*	*	*							*	*	*	*	*									*		*	*	*			
	XM28C020			*											*	*			*	*							*									*	*	*						
	XM28C040			*																							*									*	*	*	*					
	XM28C4096																																			*	*	*						
	XM28C080S																																											

(#) = part is not currently being manufactured by Xicor
(*) = part is supported by this programmer

Summary and Use of θ_{JA} and θ_{JC} Parameters with Xicor Devices

by Gray Creager, January 1995

To determine the thermal heating characteristics of any Xicor device requires knowledge of both θ_{JA} and θ_{JC} for the package of interest. These parameters are collected in Table 1 by package type and number of leads. These values represent averages over a range of possible die sizes, however the margin of error when using average values is expected to be within ±5%. Each thermal resistance, θ_{JA} and θ_{JC}, is based on a typically sized die cavity pad for a package's leadframe and the assumption that the die is at an equivalent temperature at all points. Variations in die size for a given size die pad (e.g. different devices in equivalent packages) account for the margin of error on these thermal resistivities.



When basing a thermal analysis on average die junction temperatures and assuming that I_{CC} is constant (though in reality it is "pulsing" depending on mode of operation), several simple formulas can be developed. Using these formulas, calculations can be performed to determine an ambient vs. package temperature relationship.

$$T_J = T_C + \theta_{JC} P_{D(MAX)}$$
$$T_J = T_A + \theta_{JA} P_{D(MAX)}$$

T_J = die junction temperature
T_C = package (case) temperature
T_A = lead (ambient) temperature
θ_{JC} = thermal resistance between die junction and package
θ_{JA} = thermal resistance between die junction and leads
$P_{D(MAX)}$ = total maximum power dissipation of all die junctions (i.e. $P_{D(MAX)} = (V_{CC}I_{CC})_{(MAX)}$)

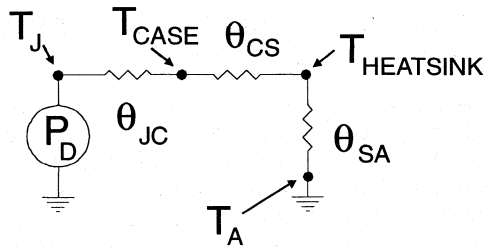
Generally, $P_{D(MAX)}$ increases for a device as V_{CC} increases and as the ambient temperature decreases. The important parameter to monitor is the die junction temperature (T_J). Typically, this should be limited to 150°C for both plastic packages (Xicor types P, S, J, T, L, or V) and ceramic/hermetic packages (Xicor types D, E, F, K, N, or R). Because Xicor's EEPROM fabrication processes are inherently more robust at high temperature (and since I_{CC} is never a fixed maximum DC current), certain Xicor devices can be fully functional at extended temperatures (e.g. the X28HT010 is fully operational at ambient (lead) temperatures up to 170°C), while many others will be functional for read-only operation. Since Xicor's characterization and burn-in programs verify device functionality based on ambient (lead) temperatures, the need to use the above equations to verify T_J is bypassed. Only packaging and ambient temperature range combinations for which the device is guaranteed to operate reliably are offered by Xicor.

As an example of how to use this information, assume that a design uses an X20C16EMB-55 at temperatures between -55°C and 125°C. For this 32 pad LCC package, T_{JA}=62°C/W and T_{JC}=15°C/W. Combining the q_{JA} and q_{JC} equations and calculating the worst case scenario for I_{CC} (i.e. T_A=-55°C, V_{CC}=5.5V, and I_{CC}=100mA),

$$T_C = T_A + (62°C/W - 15°C/W)(5.5V)(I_{CC})$$

shows that the package (case) temperature will be +0.258°C/mA (±8.5%) greater than the ambient temperature for a given I_{CC}. By device characterization over temperature and voltage, the actual $I_{CC(MAX)}$ is found to be about 60mA, thus the package (case) temperature will always be less than or equal to 141°C. Such calculations may be useful to a manufacturing engineer who has to do a thermal analysis of a system, though Xicor devices themselves don't require heatsinking.

More generally, the thermal transfer process of an integrated circuit can be modeled as the following electrical circuit:



Here, the inter-relationship between the thermal resistivities can easily be seen to be:

$$\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA}$$

Table 1 - θ_{JA} (°C/W) and θ_{JC} (°C/W) as a Function of Package Style and Number of Leads
(Note that θ_{JA} is Listed before θ_{JC} in each Box)

	8 leads	14 leads	16 leads	18 leads	20 leads	24 leads	28 leads	32 leads	36 leads	40 leads	44 leads	48 leads
P - PDIP alloy 42 leads				**97** **45**	**90** **42**	**78** **39**	**71** **36**	**65** **34**				**51** **29**
P - PDIP copper leads	**114** **38**	**81** **30**		**71** **27**	**68** **26**	**63** **25**	**59** **24**	**56** **23**				**50** **21**
D - CERDIP	**187** **24**			**82** **16**		**61** **14**	**52** **13**	**46** **13**				
S - SOIC	**164** **46**	**110** **27**	**101** **24**		**89** **19**	**81** **16**	**75** **14**					
J - PLCC								**56** **17**			**50** **15**	
E - LCC								**62** **15**				
N - LCC elongated								**NC** **NC**				
F - Flatpack							**33** **14**	**30** **12**				
K - PGA							**44** **9**		**NC** **NC**			
T - TSOP								**NC** **NC**		**NC** **NC**		
R - CERSOIC								**60** **10**				
L - TQFP											**NC** **NC**	
V - TSSOP		**NC** **NC**										

Note - Alloy 42 is a lead base material which consists of Fe/Ni in a 42% to 58% ratio. To determine the material used on a particular device, simply pass a magnet near the leads. NC is used for packages which have not yet been characterized for thermal analysis.

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NOVRAM AUTOSTORE Considerations

by Richard Downing, March 1994

Introduction

Xicor's NOVRAM (Nonvolatile RAM) devices are high-speed SRAMs overlaid bit-for-bit with a nonvolatile E^2PROM array. The AUTOSTORE (AS) feature available on these parts automatically saves the RAM contents to E^2PROM during power-down. AS typically requires some basic Vcc holdup circuitry to ensure successful completion.

Basic Autostore Circuit

The minimal components necessary to achieve an AS are a capacitor and diode which connect to the NOVRAM as shown in Figure 1. The "hold-up" capacitor must be capable of supplying the maximum AS current (I_{CC3} max.) for the maximum AS period (T_{ASTO} max.) as Vcc falls to a level between the AS threshold voltage (V_{ASTH} min.) and the AS end voltage (V_{ASEND} min.). The "hold-up" capacitor value (C_H) is calculated using the equation:

$$C_H = \frac{(I_{CC3}\text{max})(T_{ASTO}\text{max})}{V_{ASTH}\text{min} - V_{ASEND}\text{min}}$$

and is derived by taking the integral of:

$$i = C\frac{dV}{dt}$$

To use the circuit with a 5V supply requires that diode D_H to have low forward voltage drop V_F. A Schottky diode such as the 1N5817 (available from Motorola or Philips) is suitable with maximum V_F of 0.32V at 100mA. The cost of the component is around 20¢ in volume.

Power Supply Limitation

Xicor specifies a NOVRAM Vcc operating range between 4.5V and 5.5V. The diode in the AS circuit, however, results in a voltage drop (V_F) between the power supply and the NOVRAM's Vcc pin. A maximum V_F of 0.32V results in a possible AS at a supply voltage of 4.62V. For a reasonable margin of safety, the suggested AS circuit should be powered using a supply that operates above 4.75V. A 5V ±5%. power supply would be one way of ensuring correct AS operation.

Table 1. NOVRAM AUTOSTORE Device Summary

Part No.	V_{ASTH} (V) Min	V_{ASTH} (V) Max	V_{ASEND} (V) Min	T_{ASTO} (ms) Max	I_{CC3} (mA) Max	C_H (µF) Min
X24C45	4.0	4.3	3.5	5.0	2.0	20
X20C05	4.0	4.3	3.5	2.5	2.5	13
X20C16	4.0	4.3	3.5	2.5	2.5	13
X20C17	4.0	4.3	3.5	2.5	2.5	13

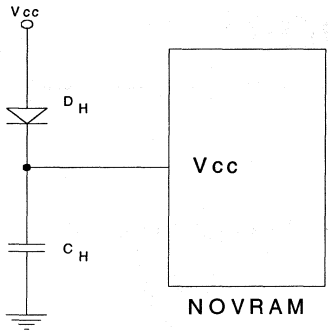


Figure 1.

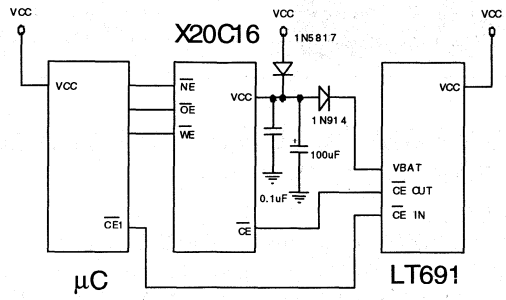


Figure 2.

Pre-AUTOSTORE Data Corruption

If the supply to a microcontroller interfacing to a parallel NOVRAM is lost while the NOVRAM remains powered, inadvertent writes to the SRAM can occur. The uncertain state of the microcontroller control lines during power-down may cause fluctuations in the status of CE, WE, and OE, which can result in a write condition. Invalid SRAM data may be transferred to the nonvolatile E^2PROM array if these changes occur before an AS. These inadvertent write conditions can be avoided using supervisory ICs available from manufacturers such as Linear Technology or Maxim. These devices control the CE of the NOVRAM so that below a set supply threshold voltage, CE is held HIGH and the NOVRAM is placed into a standby condition. An example of such a circuit is shown in Figure 2.

Conclusion

NOVRAMs combine the advantages of fast access RAMs and nonvolatility for E^2PROMs. The AUTOSTORE feature enables data integrity to be maintained during power-down. In most applications two additional components (a diode and capacitor) are all that is needed to ensure successful completion of an AUTOSTORE. A supervisory IC may also be useful to protect the part from inadvertent writes.

What is MPS E²?

by Gray Creager, May 1994

Introduction

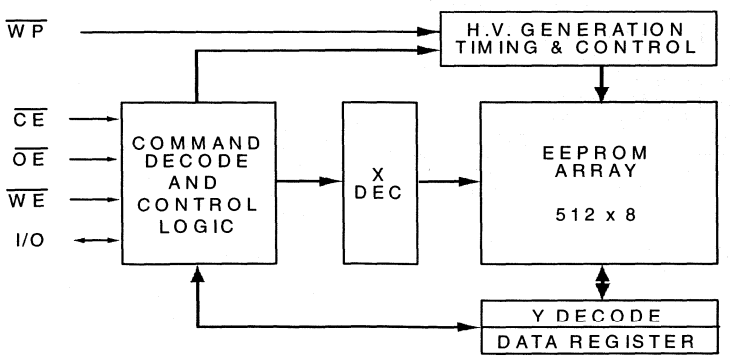
The X84041 MPS™ E² (Microprocessor Compatible Serial E²PROM) is a 4K-bit nonvolatile serial memory organized as 512 x 8. However, due to the sequential nature of the device, the use of consecutive reads or writes to the device also allows it to be used in 16-bit or 32-bit environments. This device supports an 8-byte page with a typical nonvolatile write cycle time of 5ms. Additionally, there is a write protect pin ($\overline{WP}$) to disable all nonvolatile writes to the device.

The unique feature of this device is its' ability to directly interface with a parallel data bus without glue logic. It's small size, low power, and low cost make it an ideal alternative to parallel access nonvolatile memory devices. System designers currently using parallel access devices to hold configuration data (e.g. motherboards, add-on cards, PCMCIA cards, Plug and Play cards, data recording systems, etc...) will especially benefit from the features of the X84041.

This CMOS device utilizes Xicor's proprietary Direct Write™ E²PROM cell technology which allows for an endurance of at least 100,000 write cycles per byte and a minimum data retention of 100 years.

X84041 Data Bus Cycles

An understanding of how the MPS E² serial interface works can be gained from the included bus cycle diagrams. The system designer accesses the X84041 using standard "read" or "write" activity on a parallel data bus. The interface is accomplished by directly connecting a single I/O pin from the data bus, as well as the $\overline{WE}$ and $\overline{OE}$ signals generated by the system processor and an address decoded $\overline{CE}$. When the X84041 is selected, the device will interpret each "read" or "write" on the data bus as a single bit in the serial interface protocol. Since the device is in standby mode when $\overline{CE}$ is HIGH, the serial interface scheme is fully static and can be interrupted at any time to perform other bus activities. At a later time, communications with the device can be resumed from the point when the communications were interrupted.

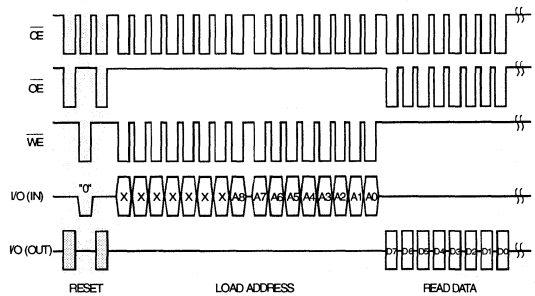


X84041 MPS™ E² Block Diagram

"Direct" Write and "MPS" are trademarks of Xicor, Inc.

In order to complete the interface, there are two additional unique sequences to reset the device and to initiate a nonvolatile write cycle. A RESET condition is recognized by the X84041 whenever the system processor issues the following sequence: "read", "write a zero", and "read". This 3-bus cycle sequence is used to initialize the part before a read or write sequence or to interrupt a sequence already in progress. An INITIATE NONVOLATILE WRITE CYCLE condition is recognized by the X84041 whenever the system processor issues the following sequence: "read", "write a one", and "read". This sequence is used to begin an internal write cycle after data has been loaded into the device. An additional feature of the device is the ability to determine the early completion of an internal nonvolatile write cycle. This can be accomplished by "polling" the level of the I/O pin during a nonvolatile write cycle. When the I/O pin can be read as a logic HIGH, then the cycle is complete and the part is again able to interact within the system.

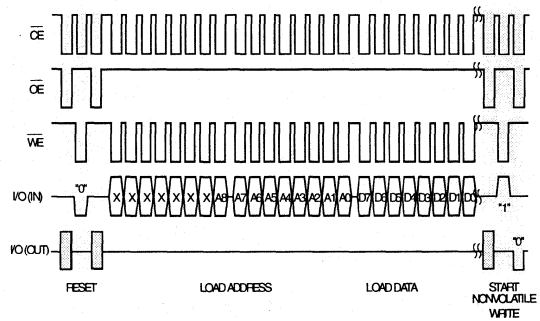
The X84041 read sequences should usually be initiated with a reset sequence, followed by 16 consecutive "writes" to the device without a "read". These 16-bits are for the address, of which the first 7 are don't cares and the remaining 9 are for the initial memory address to be accesssed (MSB first).



X84041 Read Cycle

At this point, the system processor can sequentially "read" any number of bits from the device beginning at the initial address.

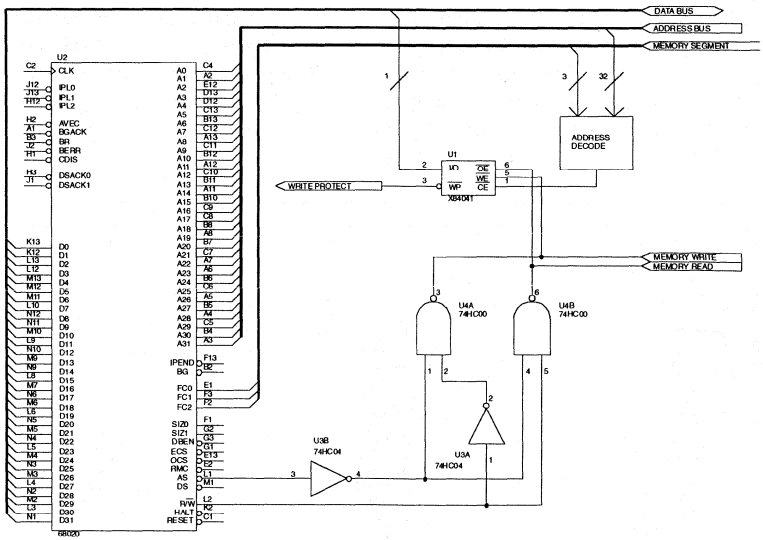
Write sequences follow the same format. Typically, the X84041 can be completely rewritten using page writes in less than 325ms when the technique of I/O polling for the early completion of each nonvolatile write cycle is used.



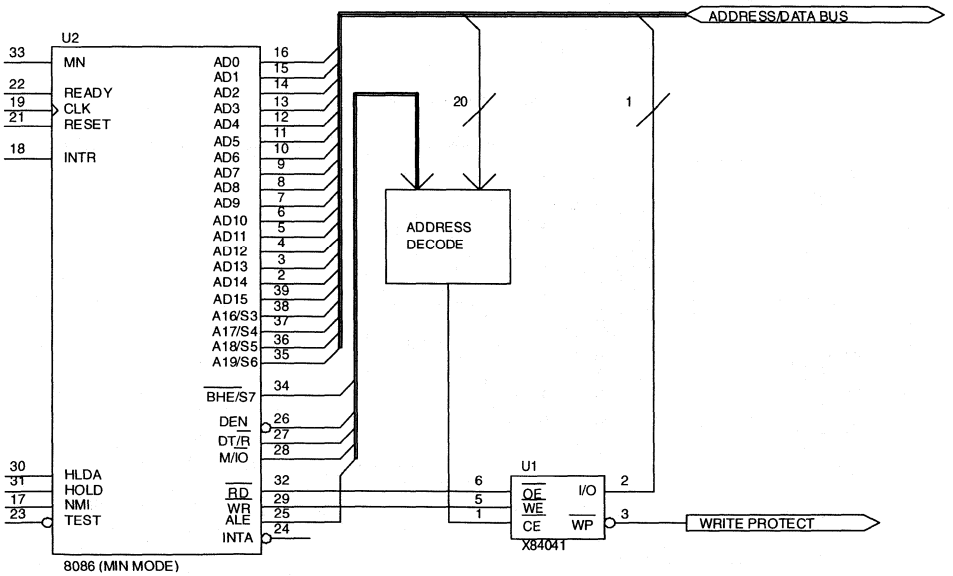
X84041 Write Cycle

Interfacing to the X84041

The X84041 is designed so that it is compatible with systems using either $\overline{CE}$ controlled write cycles (e.g. Motorola processors) or $\overline{WE}$ controlled write cycles (e.g. Intel processors). The following circuits show how simply the interfacing can be accomplished for different environments, such as the 68000, 80x86, 8051 microcontrollers, and TMS320 DSP processors.

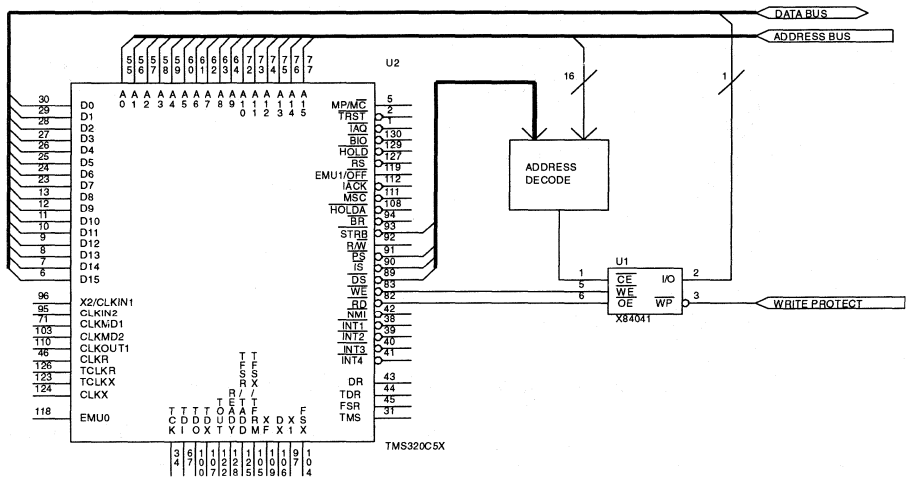


$\overline{CE}$ Controlled Write Cycle Environment (68000)

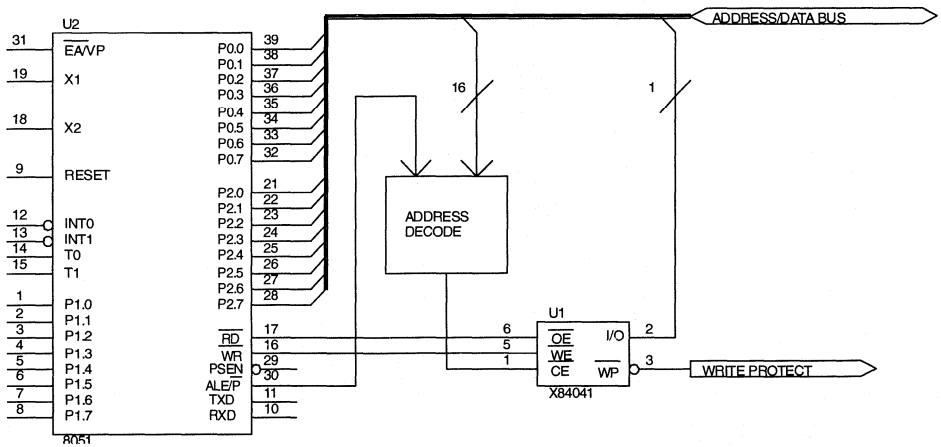


$\overline{WE}$ Controlled Write Cycle Environment (80x86)

Although the device is specified as requiring 300ns read cycle (t_{RC}) and write cycle (t_{WC}) times, there should be no problem interfacing to typical high speed busses. These cycle times are sums of the LOW pulse ($\overline{OE}$ or $\overline{WE}$) and the HIGH phase required before the next LOW pulse. As long as the LOW pulse minimum lengths are satisfied according to the bus timings of the X84041, then in software, a designer can accomodate the minimum cycle length requirement by issuing NOP instructions (or any instructions that will take sufficient time to execute).



DSP systems (TMS320)



Microcontroller Systems (8051)

The X84041 can also be an effective alternative for systems that otherwise have serial data port capabilities. For many microcontrollers, a designer is limited to only a few bit, addressable I/O port pins. Instead of using one of these pins strictly for E^2PROM communications, a designer can use the X84041. A commonly encountered circuit uses 2 I/O port pins of an 8051 microcontroller to interface to an I^2C E^2PROM. One previous circuit example shows how the X84041 frees up these port pins.

X84041 Software Routines

The following routines (taken from a design idea published in Electronic Design) are provided to minimize the design time for implementing an X84041 interface. This code is also available on the Xicor BBS at 1-800-258-8864 or 1-408-943-0655 (up to 19.2K baud, 8-bit word, 1 stop bit, no parity, and no local echo).

```
/*****************************************************************************************************************************/
/*
/*                                                Xicor X84041 MPS E2
/*
/* The following C subroutines are provided to interface with an X84041 that is memory mapped  into the I/O space of
/* an IBM PC or compatible environment.  With these subroutines, a designer can read multiple data bytes from the
/* X84041 by using the simple function call:
/*
/*                read_X84041(int no_bytes,int addr,int io_port,unsigned char *bytes)
/*
/* Any number of bytes (no_bytes) can be read sequentially from the starting address (addr) of the X84041 mapped into
/* a given I/O address (io_port).  The results are passed back sequentially to a series of system locations pointed to
/* by (bytes).  Care should be taken to provide enough locations for each data byte read.  Additionally, either a byte
/* write or page write to the X84041 can be initiated with the following call:
/*
/*                write_X84041(int no_bytes,int addr,int io_port,unsigned char *bytes)
/*
/* Up to 8 bytes (as specified by no_bytes) can be written to the X84041 at an I/O address (io_port) beginning at a
/* memory address (addr).  Sending more than 8 bytes will cause a "wrap-around" of data on the chosen page.  The
/* data to be written is contained in an array (pointed to by *bytes).  These routines can be appended to other ANSI C
/* code with the following (or similar) compiler directive:
/*
/*                #include "c:\xicor.c"
/*
/* Note that the source code should have an #include <dos.h> statement since the code (xicor.c) needs access to the
/* inportb() and outportb() functions.
/*                                                                                                                    GHC IV
/*****************************************************************************************************************************/

/*****************************************************************************/
/* Sends RESET sequence to the X84041 at io_port
/*****************************************************************************/
void x84reset(int io_port) {
        inportb(io_port);                       /* read bit from io_port */
        outportb(io_port,0x00);                 /* write a LOW bit to io_port */
        inportb(io_port);                       /* read bit from io_port */
}

/*****************************************************************************/
/* Writes a one to the X84041 at io_port
/*****************************************************************************/
void x84write_one(int io_port) {
        outportb(io_port,0xff);                 /* write a HIGH bit to io_port */
}
```

```
/*****************************************************************************/
/* Writes a zero to the X84041 at io_port
/*****************************************************************************/
void x84write_zero(int io_port) {
        outportb(io_port,0x00);                         /* write a LOW bit to io_port*/
}
/*****************************************************************************/
/* Reads a bit from the X84041 at io_port
/*****************************************************************************/
int x84read(int io_port) {
int bit_val;
        bit_val = inportb(io_port) & 1;                 /* read bit D0 from io_port */
        return(bit_val);                                /* return bit value to calling routine */
}

/*****************************************************************************/
/* Polls for the early completion of a nonvolatile write cycle in the X84041 at
/* io_port
/*****************************************************************************/
void x84poll(int io_port) {
int bit_temp;
        do {
                bit_temp=x84read(io_port);              /* continuously read bits until the bit is HIGH */
        } while (bit_temp == 0);
}

/*****************************************************************************/
/* Initiates and completes a nonvolatile write cycle in the X84041 at io_port
/*****************************************************************************/
void x84write_start(int io_port) {
        x84read(io_port);                               /* read bit from io_port */
        x84write_one(io_port);                          /* write a LOW bit to io_port */
        x84read(io_port);                               /* read bit from io_port */
        x84poll(io_port);                               /* poll the I/O pin for completion of write cycle */
}

/*****************************************************************************/
/* Sends all 16 required address bits, including don't cares, to the X84041 at
/* io_port
/*****************************************************************************/
void x84addr_send(int dont_care,int io_port,int addr) {
int addr_bit,mask_addr,addr_temp;
        for (addr_bit = 0; addr_bit < dont_care; addr_bit++) {
                x84write_zero(io_port);                 /* loop and send don't cares */
        }
        mask_addr = 256;                                /* bit mask to isolate address MSB */
        for (addr_bit = 0; addr_bit < (16-dont_care); addr_bit++) {   /* loop through all 9 address bits */
                addr_temp = addr & mask_addr;           /* mask to determine next required address bit */
                if (addr_temp == 0)                     /* if address bit is LOW, then ... */
                        x84write_zero(io_port);         /* write a LOW bit to io_port */
                else
                        x84write_one(io_port);          /* otherwise, write a HIGH bit to io_port */
                mask_addr = mask_addr >> 1;             /* shift bit mask right to get next bit */
        }
}
```

```
/*****************************************************************************/
/* Sends all 8 data bits to the X84041 at io_port
/*****************************************************************************/
void x84data_send(int io_port,int data) {
int mask_data,data_temp,data_bit;
        mask_data = 128;                                    /* bit mask to isolate data MSB */
        for (data_bit = 1; data_bit < 9; data_bit++) {      /* loop through all 8 data bits */
                data_temp = data & mask_data;               /* mask to determine next required data bit */
                if (data_temp == 0)                         /* if data bit is LOW, then ... */
                        x84write_zero(io_port);             /* write a LOW bit to io_port */
                else
                        x84write_one(io_port);              /* otherwise, write a HIGH bit to io_port */
                mask_data = mask_data >> 1;                 /* shift bit mask right to get next bit */
        }
}

/*****************************************************************************/
/* Reads 8 data bits from the X84041 at io_port and reconstructs the databyte
/*****************************************************************************/
int x84data_get(int io_port) {
int n,bit_temp[9];
bit_temp[0]=0;                                              /* clear array position 0, resetting previous sum */
        for (n=1;n<9;n++) {                                 /* loop through 8 data bits */
                bit_temp[n] = x84read(io_port)+2*bit_temp[n-1];  /* at the current position, shift the previous sum of */
                                                            /* data bits left, read the next bit, add it to previous */
        }                                                   /* sum, and store the result */
        return(bit_temp[8]);                                /* return the data byte value to the calling routine */
}

/*****************************************************************************/
/* General READ master routine that is called by the user in order to read a
/* number of bytes from the X84041 at io_port
/*****************************************************************************/
void read_X84041(int no_bytes,int addr,int io_port,unsigned char *bytes) {
int n;
        x84reset(io_port);                                  /* reset the X84041 */
        x84addr_send(7,io_port,addr);                       /* send the address bits (don't cares & addr) */
        for (n=0;n<no_bytes;n++) {                                  /* loop through all bytes to be read (no_bytes) */
                bytes[n]=x84data_get(io_port);              /* receive each byte and store sequentially */
        }
}

/*****************************************************************************/
/* General WRITE master routine that is called by the user in order to write a
/* number of bytes to the X84041 at io_port
/*****************************************************************************/
void write_X84041(int no_bytes,int addr,int io_port,unsigned char *bytes) {
int n;
        x84reset(io_port);                                  /* reset the X84041 */
        x84addr_send(7,io_port,addr);                       /* send the address bits (7 don't cares & addr) */
        for(n=0;n<no_bytes;n++) {                           /* loop through all bytes to be written (no_bytes) */
                x84data_send(io_port,*(bytes+n));           /* sequentially send each byte */
        }       x84write_start(io_port);                    /* initiate nonvolatile write cycle */
}
```

```
/*****************************************************************************/
/* Main listing example to utilize these functions
/*
/* When used in a larger program, the following include directives must be
/* included prior to compilation.  The example shows a page write of length
/* 4 bytes being initiated at address 0x000 of an X84041 memory mapped to
/* address 0x303. Data to be written is stored sequentially in send_buffer.
/* Similarly, 22 consecutive bytes are read from this X84041 starting at address
/* 0x01F and stored to receive_buffer.
/*****************************************************************************/

#include <c:\xicor.c>
#include <dos.h>
unsigned char send_buffer[8], receive_buffer[512];          /* maximum buffer sizes needed for X84041 protocol */
.
.
.

main () {
        write_X84041(4,0,0x303,&send_buffer);
        read_X84041(22,0x1F,0x303,&receive_buffer);
}
```

NOVRAM vs. Battery Backed SRAM: Latch-up Considerations for Nonvolatile Systems

by Gray Creager, September 1994

Nonvolatile memories come in many varieties (ROM, PROM, EPROM, etc..), however in-circuit reprogrammable nonvolatile memories are often significantly more useful. This second class includes devices that are nonvolatile due to underlying physical mechanisms available in a particular circuit technology (e.g. EEPROM, Flash EEPROM), as well as devices that rely on hybrid techniques (e.g. battery backed SRAM). A Flash EEPROM device typically allows for reprogrammability at 12V, while battery backed SRAM and EEPROM can be rewritten at the operating Vcc of the device, even during low voltage operation. Also, the endurance of flash type devices is typically 10,000 writes/byte, while full-feature EEPROMs usually offer 100,000 or more writes/byte. However, with a battery backed SRAM, there are essentially an unlimited number of writes/byte. Since this feature is an advantage in many applications (e.g. aircraft jet engine controllers, heating/air conditioning equipment, real-time data processing), Xicor produces NOVRAM (nonvolatile SRAM) devices which also allow for an unlimited number of writes/byte. These ICs consist of an SRAM array which is shadowed by an E^2PROM array (Xicor's preferred terminology for EEPROM). The unlimited writes/byte benefit of the SRAM array is realized, with the advantage that the entire contents of SRAM can be copied to (or retrieved from) the E^2PROM array whenever desired. An additional advantage of Xicor's NOVRAM technology is the 1,000,000 writes/byte specification for the E^2 array. Also, using Xicor's AUTOSTORE feature internally enables Vcc sense circuitry that will automatically initiate a transfer from SRAM to E^2PROM, whenever Vcc dips below an acceptable threshold, thus guaranteeing nonvolatile storage during power cycles.

With a battery backed SRAM, an externally attached Lithium battery discharges enough current into the SRAM array to keep it "ON" when power is removed, however, this type of solution will cause some unique problems for a designer. First, the packages are large due to the attached batteries. For example, Dallas Semiconductor's DS1220 encapsulated package size is 1.34" x 0.72" x 0.415". Compare this to a size of 0.484" x 0.314" x 0.04" for a Xicor NOVRAM of equal density (i.e. X20C16) in a TSOP package. The X20C16 TSOP occupies only 1.5% of the volume occupied by the DS1220!!! There are also increasingly strict regulations regarding the disposal of spent batteries that complicate matters and increase the cost to the customer. For battery backed devices, nonvolatility can only be guaranteed as long as the battery is good (usually specified as 10 years maximum). In contrast, Xicor's E^2 technology allows for a guaranteed data retention of at least 100 years (theoretically as many as 50 billion years at 50° C). When the battery dies, there is no way to replace it, hence for every chip that is discarded when the battery runs out, a perfectly good SRAM die is also discarded. In spite of these problems, designers often feel that battery backed SRAMs are an adequate solution for their needs, however there are still other considerations that can make battery backed SRAMs a poor choice.

One of these considerations is susceptibility to latch-up and latch-up related failures. Latch-up is a phenomena inherent in CMOS integrated circuits. Although it cannot be eliminated entirely, techniques exist to minimize the risk of latch-up when the IC is manufactured. In a CMOS process, parasitic bipolar transistors are created as shown in Fig. 1 (in this case an n-well process). Coupled with the inherent base resistances due to the substrate and the well doping levels, this NPN and PNP transistor combination forms a parasitic silicon controlled rectifier (SCR) circuit. Although normally reversed biased, if either or both BJTs are biased into the saturation region (and if the product of both betas is greater than unity!), a positive feedback circuit arises, causing both of these transistors to conduct heavily. Under

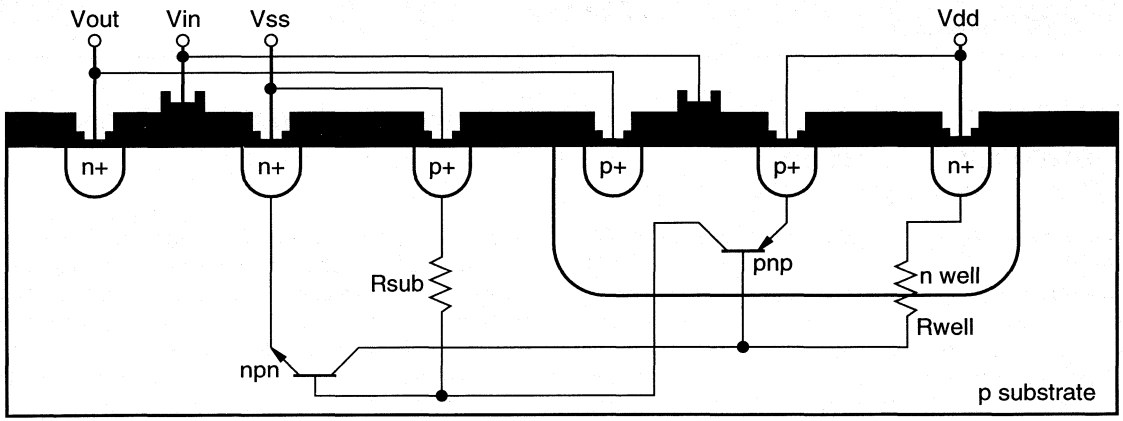


Figure 1 - Parasitic BJTs present in CMOS inverter structure

this condition, this parasitic circuit will draw a large DC current (80mA or more!) by causing a short circuit between the power and ground rails. The necessary voltage to cause this phenomena is called the triggering voltage. Sustained DC currents of these magnitudes could breakdown gate oxides or cause electromigration failures within the metal interconnects.

There are several causes of latch-up including internal transients during power-up, undervoltages or overvoltages applied to the I/O terminals, improper power supply sequencing, overvoltage on Vcc, or even radiation effects such as heavy ion single event upsets (SEU) or electromagnetic pulses (EMP). In the case of EMP, the cause of latch-up can be as seemingly benign an event as a nearby lightning strike!

To lessen the risk of latch-up, IC manufacturers use both design, layout, and manufacturing techniques. When BiCMOS processes are available, designers can use bipolar I/O structures to help eliminate latch-up sensitive structures. Layout designers minimize latch-up by a liberal use of substrate contacts to each well and throughout the substrate. These contacts can then be directly connected to a supply pad with a metal interconnect. The closer these contacts are to the source contacts of MOSFETs with direct rail connections, the smaller Rsub and Rwell will be, which in turn minimizes the chances of latch-up. Avoiding convoluted structures of intertwined NMOS and PMOS transistors also helps. Since latch-up is more likely to occur around I/O structures where large currents can flow, guard rings can also be used effectively. Processing tricks relating to the doping of the active devices with additional acceptors (e.g. Au) and controlling the thickness of the epitaxial layer have also been shown to help lessen latch-up susceptibility.

Unfortunately, even with the precautions taken by many IC manufacturers, care must also be taken when designing with CMOS circuitry in order to minimize the chance of latching-up the part. Input clamping diodes can be used to prevent overshoots and undershoots, but these add to the cost of the system. Current limiting resistors could also be used on each I/O pin, as well as current limited regulators for supplying power to the device. If the data busses are long enough, inductive ringing will cause overshoots and undershoots, so optoisolators can also be useful. Though these precautions can be taken, latch-up cannot be entirely eliminated. In certain environments or under extreme operating conditions, latch-up becomes a major reliability problem. Fortunately, latch-up is usually a nondestructive phenomena (assuming excessive DC currents are not allowed to flow for extended periods of time) and CMOS circuitry can be "reset" by simply cycling power. However, for battery backed devices, this will not always be possible! Once a battery

backed SRAM latches-up, the increased current draw of the device will drain the battery in a matter of several hours. Since many of these devices are designed such that the battery cannot be deactivated or removed, latch-up always becomes a destructive phenomena. The nonvolatile data will then be lost and the only recourse is to replace the part. This can mean expensive product recalls or technician field visits.

With Xicor's NOVRAM technology, even if a device latches-up, the system can usually be recovered by cycling power. In fact, data collected on Xicor's fabrication process from the various stress tests verify that Xicor products exhibit excellent latch-up immunity. Under absolute maximum ratings, this allows Xicor to specify NOVRAM pins at levels between -1V and +7V (with respect to Vss) without damaging the device. For Dallas Semiconductor's NVRAMs (battery backed SRAMs), the specification is between +7V and -0.3V. This limit is the most telling characteristic relating to latch-up susceptibility. With only 0.3V tolerance below GND, the ground bounce, noise, and ringing associated with today's high speed hardware systems can easily cause a battery backed SRAM to latch-up. For this reason, Xicor NOVRAMs are used extensively in systems where latch-up failures cannot be tolerated. With their low power, superior endurance, and advanced features, Xicor NOVRAMs provide a complete solution for nonvolatile systems with a need for high write endurance. Listed below are Xicor's currently available NOVRAM products, as well as the packaging options available for each device.

NOVRAMs	Density	Features	Packages
X20C04	512 x 8	150ns	DIP28,LCC32,PLCC32
X20C05	512 x 8	Autostore, 35ns	DIP28,LCC32,PLCC32
X20C16	2048 x 8	Autostore, 35ns	DIP28,SOIC28,LCC32,PLCC32,TSOP32
X20C17	2048 x 8	Autostore, 35ns	DIP24
XM20C64	8192 x 8	Autostore, 55ns	DIP28
XM20C128	16384 x 8	Autostore, 55ns	SIP36
X22C10	64 x 4	120ns	DIP18,SOIC16
X22C12	256 x 4	120ns	DIP18,SOIC20
X25401	32 x 8	Serial, SPI, Autostore	DIP8,SOIC8
X24C44	16 x 16	Serial	DIP8,SOIC8
X24C45	16 x 16	Serial, Autostore	DIP8,SOIC8

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Programmable Write Protection for High Density Serial E²PROMs

by Richard Downing, March 1994

One of the major considerations when designing with any form of memory is ensuring that data is adequately protected. This is particularly true of programmable memory which may be subject to inadvertent write conditions. To guard against this, serial E²PROMs have up to now been protected using either a single hardware write protect pin or some form of software block protection. The Xicor SPI family of devices (X25080/160/320/640/642/128) is the first that combines the advantages of both of these techniques to provide a Programmable Hardware Write Protection.

This hybrid form of write protection allows for selectable blocks of memory to be permanently protected via a hardware write protect pin that is enabled through software. The advantage of this scheme is that data can be downloaded to the device in-system and then be "secured" through hardware, without changing the status of any of the pins. Previously, devices using hardware protection have needed to be pre-programmed before being mounted onto a circuit board, thereby adding an additional manufacturing step. This new feature is particularly useful for systems utilizing surface mount devices, which are cumbersome to pre-program, and in applications where last minute programming may be required just prior to shipment.

The truth table for setting the various levels of protection available on the SPI devices is shown below. The WPEN (Write Protect Enable) bit is used to enable the hardware write protection and the BP0 and BP1 (Block Protect) bits are used to define the blocks of the E²PROM array to be protected. These bits are nonvolatile and can be read or written via the Status register. The status of the WEL (Write Enable Latch) is determined by reading the Status register and must be set before a write can occur. This latch also provides additional protection by being automatically reset on the completion of a write cycle or after power-down condition.

It should be noted that once hardware write protection has been enabled, it can only be disabled by changing the state of the write protect pin, and not through software.

$\overline{WP}$ Pin	WPEN Bit	BP0 and BP1 protected Memory Blocks	BP0 and BP1 Unprotected Memory Blocks	WEL	BP0/1 and WPEN bits	Type of Write Block Protection
L	1	Not Writable	Writable	Settable	Not Writable	Hardware
H	X	Not Writable	Writable	Settable	Writable	Software
X	0	Not Writable	Writable	Settable	Writable	Software

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What is SLIC E^2 ?

by Ray Kahidi, January 1995

Introduction

This application note discusses the features of Xicor's SLIC family of microperipheral products. Future families are planned to support other microcontrollers. Beginning with background information on the SLIC family, this note will provide a detailed discussion of the unique features of the SLIC E^2.

SLIC Background

Xicor continues to stay at forefront of advanced E^2 technology by employing its proprietary E^2PROM process to come up with new and innovative products. The SLIC gives design engineers a easy to implement interface with most popular microcontroller families.

Since the SLIC family is designed to directly interface to microcontroller families, it accepts a multiplexed ADDRESS/DATA bus from the microcontroller, eliminating an external address latch. Currently, microperipheral products exist for the 68HC11 and 8051 microcontroller families. The internal nonvolatile write cycle of a standard EEPROM device requires several milliseconds to complete. Once the internal programming cycle commences, the device tri-states its data bus and the microcontroller is unable to access the memory array. A second memory device is needed to hold the instructions (program) used by the microcontroller during the internal write cycle of the primary memory device.

The SLIC E^2 has two separate banks of memory. This allows one bank to be read while the microcontroller is writing data to the other bank. This Concurrent Read During Write feature eliminates any need for a separate ROM for program storage, while the microcontroller modifies the contents of E^2.

Block Lock Protection is another advanced feature of the SLIC devices. This allows the programmer to specify which of the eight 1K x 8 blocks will allow (or prevent) subsequent writes. This can be used to protect valuable data from accidental overwrites. On some of these microperipheral products, there are additional I/O port expanders. These devices have 2 on-chip ports, of which port B can be configured as an output latch for the lower byte of the addresses being clocked in by the address latch input signal. These port expanders also have internal programmable nonvolatile chip selects.

X68C75 and X88C75 SLIC Features

In addition to having all of the capabilities of the first generation devices (X68C64 or X88C64), the I/O port expander devices (X68C75 or X88C75) have additional features. They each have two memory mappable I/O expansion ports. The I/O lines can be configured as inputs or outputs and one of the ports can be programmed to output the demultiplexed A0 to A7 addresses. These devices also have a programmable interrupt controller and 16 bytes of SRAM. To control the operation of the X68C75 or X88C75 and to interface with the control registers, these devices have several Special Function Registers (SFRs). These registers can be mapped to one of sixty-four 1K-byte segments in the 64K-byte address range. Mapping is accomplished by writing a value to the SFR Map register. This allows address lines A10-A15 to specify the SFR base address. This on-chip programmable chip select logic eliminates the need for external address decoders.

Address[1]	Function
00	SFR Map register
08	Port B Data register
10	Port A Data register
18	Interrupt Control register
20	Configuration register
28	Port B Pin register
30	Port A Pin register
38	E2 Memory Map
200-20F	X68C75 or X88C75 SRAM

[1]Offset from base address. Base can be programmed on 1K-byte boundaries.

Figure 1. X68C75 or X88C75 SFR Memory Map

The E^2 Memory Map register controls the polarity of the RESET input, the mode of operation of port B (i.e. LAM mode), and the address of the program memory. Port B can be configured as an I/O port or it can be programmed to output the demultiplexed low address byte. The program memory can be mapped (by three bits) to be at one of eight 8K-byte boundaries. Both the SFR Map register and the Program Memory Map register are E^2 cells, so they must be programmed with a special sequence, similar to that required when programming the main block of E^2 memory. All other SFRs and the SRAM are volatile, so they can be written directly.

SLIC E^2 Operation

SLIC E^2 in a product name refers to devices with the SLIC code loaded at the factory. The SLIC is written to minimize intrusion in the 8K-byte memory space. Where possible, the SLIC routines are generic, allowing them to be re-usable by the application code.

The primary goal behind designing the SLIC was to facilitate modification and downloading of microcontroller code to the SLIC family of devices without a special purpose programmer. The SLIC is capable of downloading code, from a PC, through a microcontroller's UART. A special transmission protocol is used to handle this downloading process.

XSLIC is a driver program running on an IBM/PC compatible host machine. This program provides the user interface to the SLIC, through any of 4 COM serial ports (COM1-COM4). The XSLIC program converts Intel HEX or Motorola "S" files to the XCOM (Xicor Communication Protocol) format, supported by the SLIC, prior to downloading. The XSLIC also supports other features of the SLIC E^2 devices, these are explained in more detail in AN64.

The resident SLIC code has designated memory spaces allocated for its use. The user's application code should avoid using these areas as part of its code segments, otherwise it will overwrite the SLIC. Prior to downloading the application code, the application source files must be assembled and linked using information provided in Figures 2 and 3. Memory space taken by the SLIC can be used as run-time data storage if there is no further need to modify or download a new copy of the application code.

Application code can be written to replace the RESET vector with one that points to the application code instead of the SLIC. If this has been done, the system can be power cycled to begin execution of the user's code. Replacing the RESET vector requires that there be some way to re-invoke the SLIC. One way is to specify that the IRQ vector point to the SLIC MAIN routine. The SLIC can be restarted by generating an interrupt. Another way to get back to the SLIC is through a call to the SLIC MAIN routine from the application code. In this case, the RESET and IRQ vectors are free for other applications. This solution is hazardous; if the application code locks-up, the SLIC cannot be re-invoked.

Version 3.0 of the SLIC allows execution of either the application code or the SLIC E^2 code upon system power-up. If the SLIC receives any character from the UART other than "R" or "X", the application code will be executed on power-up. There is a two-byte entry reserved for the user's code address in the SLIC E^2 function table. The table entry can be changed to point to the start of the application program. When the system is powered-up, the SLIC will jump to the application program once it receives an unknown command.

The SLIC E^2 configures the serial port to a variable baud rate mode. In this mode, the timer reload value determines the system's baud rate. The default

setting for this constant is based on a system clock rate of 8MHz for the Motorola micros or 11.058MHz for the Intel micros, for a baud rate of 9600. If the target system is set up with other clock frequencies, then its timer constant value will be different than the default. A new timer constant value can be either programed into the SLIC E^2 using a programmer, or downloaded to it from the XSLIC setup menu.

Conclusions

These SLIC E^2 devices have multiplexed ADDRESS/DATA bus interfaces which eliminate an external address latch. They also offer a single chip solution, using their unique dual-plane architectures and eliminating the need for a separate device to hold instruction code during in-system reprogramming. Direct connection to a microcontroller's control pins provides for a "glueless" interface and the SLIC E^2 routines combine to make this a truly powerful solution. These on-chip SLIC E^2 routines facilitate in-system reprogramming during manufacture or during field BIOS upgrades. The port expander devices contain chip select logic that eliminates the need for external address decoders, as well as 2 byte-wide I/O ports that contribute an additional 16 valuable ports that are lost when interfacing a microcontroller to external memories. When operated in the LAM mode (Latched Address Mode), these I/O ports will allow for interfacing the microcontroller to any other byte-wide devices via the de-multiplexed ADDRESS/DATA bus.

ADDRESS	ADDRESS	
Rev. 2.0 (X68C64)	**Rev. 3.0 (X68C75)**	**Use**
E000H-E11FH	E000H-E14FH	SLIC Code
E120H-FEFFH	E150H-FEFFH	USER's Program
FF00H-FFBFH	FF00H-FFBFH	SLIC Code
FFC0H-FFFFH	FFC0H-FFFFH	ISR & RESET Vectors

Figure 2. 68HC11 System Memory Map

ADDRESS	ADDRESS	
Rev. 2.0 (X88C64)	**Rev. 3.0 (X88C75)**	**Use**
0000H-002FH	0000H-002FH	ISR & RESET Vectors
0030H-011FH	0030H-014FH	SLIC Code
0120H-1EFFH	0150H-1EFFH	USER's Program
1F00H-1FFFH	1F00H-1FFFH	SLIC Code

Figure 3. 8051 System Memory Map

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X88C64 SLIC Memory Expansion and Prototyping Techniques

by Ray Kahidi, August 1993

The X88C64 SLIC E^2PROM provides 8K-bytes of byte alterable program and data storage. For many applications, 8K-bytes is not sufficient, as a result, more memory capacity must be added. While larger versions of the SLIC family are in development, the only method to currently extend the memory capacity is to add an additional component. It would be advantageous to add this memory capacity utilizing additional X88C64 devices to retain the advantages of the architecture of the device.

In order to better understand the problem we must first look at how we control the chip select of the X88C64 when only one of the devices is to be used.

Hardware Issues

The 8051 reset and interrupt vectors reside in low memory. As a result, if the system is going to use a single X88C64, it must also be mapped into this area.

The X88C64 has a single active LOW chip select input and we can use any of the three most significant address lines (A15, A14, or A13) to control the X88C64 selection. A memory map for each of these possibilities is shown in Figure 1.

There are several approaches to adding additional X88C64 devices to a system. Since the device has only a single active LOW chip select, additional X88C64 devices cannot be simply connected to other address lines of the 8051. Some amount of address decoding must be added to the system. The problem with this approach is that it requires the addition of another component on the PC board. Using the output of one of the I/O ports from the 8051 as a chip enable signal is not recommended, since it might cause an asynchronous transfer of the read access between multiple devices, resulting in the misreading of the next opcode.

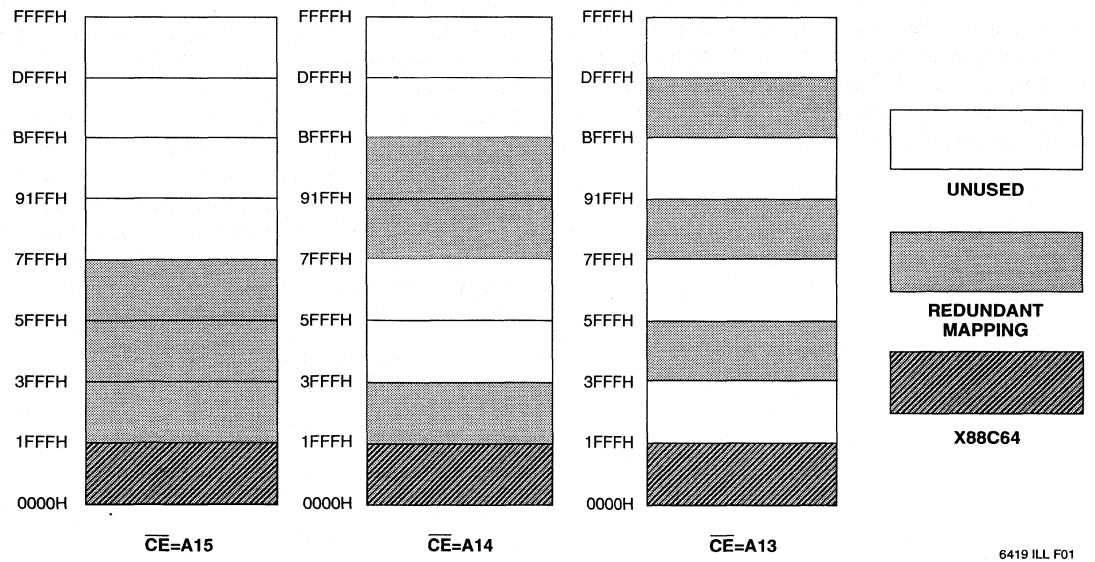

Figure 1. Single X88C64 Memory Map Options

The best option for adding additional memory capacity to an X88C64/8051 system is to utilize a X68C64 as the second memory device. The X68C64 is nearly identical to the X88C64, with the exception that several of the control lines have different names and that the polarity of the chip select is reversed, meaning that on the X68C64, chip select is active HIGH. The reason for using different input signal names on the X68C64 is to more closely match the signals on the 68HC11 microcontroller for which it was developed. The X68C64 will work perfectly well with an 8051 if the following connections are made:

Table 1.

X68C64 PIN	8051 PIN
SEL	PSEN
E	RD
R/W	WR
CE	A13
AS	ALE

In order to get a contiguous mapping of both the X88C64 and X68C64, A13 should be used to drive the chip select lines of each of the devices. This will result in the memory map shown in Figure 2. A14 or A15 could also be used, but the address mapping of the X68C64 would not be contiguous with the X88C64, possibly causing problems during code compilation and linking.

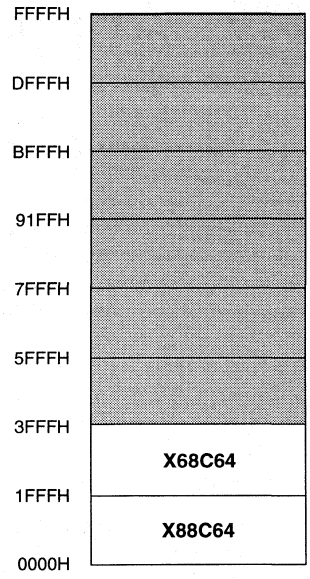

Figure 2. X88C64/X68C64 Memory Map Using A13 for Chip Select

Software Considerations

The X88C64 SLIC software is able to operate in the above configuration since it has been written with the capability for accessing E^2PROM memory throughout the entire 8051 address space. The only problem is that the X68C64 will be protected (by Software Data Protection) from being written to during the download. In order to get around this, first load a program through the SLIC which will disable Software Data Protection for the X68C64. The disable Software Data Protection is a command which is undocumented in the data sheet, since it is not advisable to use it during normal system operation. The sequence is as follows:

Data[AAH] ---> X555H
Data[55H] -----> XAAAH
Data[A0H] -----> X555H
Data[AAH] -----> X555H
Data[80H] ------> XAAAH

Wait 10ms

This software routine for disabling Software Data Protection on the X68C64 is shown below. The portion of the software which is contained in the box is the portion of software that actually performs the above write sequence to the X68C64, to disable Software Data Protection. It should be pointed out there is no 10ms wait routine at the end of the sequence. The reason for this is that the next instructions that the software will perform are to re-write the interrupt vector of the X88C64 to point back to the SLIC. Since this operation will require 10ms, we will use this interval also for timing the write cycle of the X68C64.

```
<<< ASM51 >> CROSS ASSEMBLER VER.3.0 ASSEMBLE LIST DATE: PAGE: 1
      LOC. OBJECT          LINE   STATEMENT     SLIC.ASM
                                  1
0000                              2             ORG     0000H
0000  02     01     30      3             JMP     DISABLE      ;Reset Vector
0130                              4             ORG     0130H
0130  90     25     55      5 DISABLE:MOV       DPTR, #2555H
0133  74     AA             6             MOV     A, #0AAH
0135  F0                     7             MOVX    @DPTR,A
0136  90     2A     AA      8             MOV     DPTR, #2AAAH
0139  74     55             9             MOV     A, #055H
013B  F0                     10            MOVX    @DPTR,A
013C  90     25     55      11            MOV     DPTR, #2555H
013F  74     A0             12            MOV     A, #0A0H
0141  F0                     13            MOVX    @DPTR,A
0142  74     AA             14            MOV     A, #0AAH
0144  F0                     15            MOVX    @DPTR,A
0145  90     2A     AA      16            MOV     DPTR, #2AAAH
0148  74     80             17            MOV     A, #080H
014A  F0                     18            MOVX    @DPTR,A
014B  12     1F     40      19            LCALL 01F40H ;Send_SDP_HDR_LO
014E  90     00     01      20            MOV     DPTR, #0001H
0151  74     00             21            MOV     A, #00H
0153  F0                     22            MOVX    @DPTR,A
0154  A3                    23            INC     DPTR
0155  74     30             24            MOV     A,#030H
0157  F0                     25            MOVX    @DPTR,A
0158  E0                    26 POLL:      MOVX    A,@DPTR
0159  F8                     27            MOV     R0,A
015A  E0                     28            MOVX    A,@DPTR
015B  68                     29            XRL     A,R0
015C  20 E6 F9 [0158]30          JB      Acc.6,POLL
015F  21 5F [015F] 31 LOOP:      AJMP    LOOP
```

The call to 01F40H is a call to the SDP_HDR_LO routine which is included in the SLIC software. After we re-write the RESET vector, we use Toggle Bit Polling to determine if the device is finished. The software will then enter an endless loop until a hardware reset occurs, at which time, SLIC will re-initialize itself and the applications software can be downloaded into both the X88C64 SLIC and the X68C64.

After we download the applications software, we must enable Software Data Protection on the X68C64. This can be done again through the loading of a small routine which writes a dummy value to the X68C64 using the SDP sequence. In order for the SLIC to be accessible after the downloading of the user's software, the RESET vector should not be overwritten. Only during the execution of the routine to enable SDP on the X68C64 should the RESET vector be updated to point to the beginning of the application's software. The following flow chart describes the entire process of disabling the SDP on the X68C64, the downloading of the applications software, and the enabling of the SDP on the X68C64.

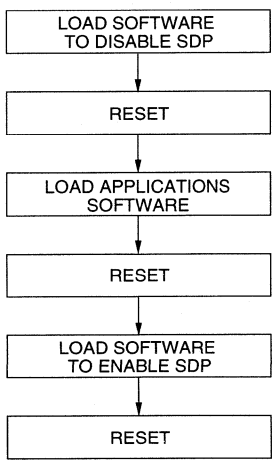

Figure 3.

Evaluation of the X88C64 (or X88C75)

The X88C64 SLIC is a powerful integration of a state-of-the-art product architecture and preloaded routines for the 8051 family of microcontrollers. The basic purpose that was planned for the X88C64 SLIC was to reduce complexity of manufacturing 8051 based systems by providing the capability of downloading the applications software through the 8051 UART. This download capability eliminates the need to initially program the memory device prior to board assembly. This built-in software also simplifies the task of upgrading the software in the field, after the system is shipped to the end-customer.

In addition, many engineers who have looked at the SLIC have thought that it would also provide an inexpensive development capability with which they can try out the various versions of their software in their target system. The only problem with this utilization of SLIC is if the applications software goes into an endless loop or hangs. Control will never be returned to the SLIC, therefore a new version of the applications software cannot be downloaded through the SLIC.

There is an easy "work around" for this problem. If the target system is not going to utilize both of the hardware interrupts (INT0 and INT1), one of them can be used to return control of the program to the SLIC routine. This can be done by including the following assembler directives in the application program:

For INT0

```
.ORG    03H
```

For INT1

```
.ORG    13H
```

Followed by the ISR routine that responds to the external interrupt and forces execution of the SLIC code.

```
        MOV     R0,SP           ;CURRENT VALUE OF THE STACK POINTER
        MOV     @R0,#00H        ;MSB OF THE SLIC ADDRESS
        DEC     R0              ;BACK UP ONE POSITION ON THE STACK
        MOV     @R0,#30H        ;LSB OF THE SLIC ADDRESS
        RETI                    ;POP THE SLIC ADDRESS FROM THE
                                ;STACK UPON RETURN
```

The initialization routine of the application program must include instructions to enable the external interrupt and set its level as edge-triggered.

```
        ORG     200H
APPS_MAIN:
        MOV     SP,#60H         ;SET THE STACK POINTER()
        SETB    IT0             ;SET THE INT0 AS EDGE SENSITIVE
        SETB    EA              ;ENABLE INTERRUPTS
        SETB    EX0             ;ENABLE EXTERNAL INT0

        ...                     ;YOUR CODE WILL GO HERE

END
```

If an engineer wants to include this capability in his system, he should make sure that the switch or button that he uses to generate the interrupt pulse on the 8051 is properly debounced and of sufficient duration to meet the specifications of microcontroller.

X88C64 (or X88C75) Demonstration Circuit

The following schematic shows the minimum number of components needed to build an X88C64 SLIC E^2PROM evaluation board, as well as the connections for evaluating a similar device with I/O ports (X88C75). The memory expansion techniques can be implemented with this circuit very easily, however this is sufficient to evaluate the use of the X88C64 in a user's system. The crystal for the 8051 is chosen to be 11.0598MHz, which will insure that the on–board UART will be initialized at 9600 baud. The LT1181 from Linear Technology is a 5V only RS–232 line driver. If +12V and –12V are available on the target PC board, the LT1181 can be replaced by a typical 1488 and 1489 combination.

The 9-pin RS–232 connector can be connected directly to the serial port of an IBM PC compatible system.

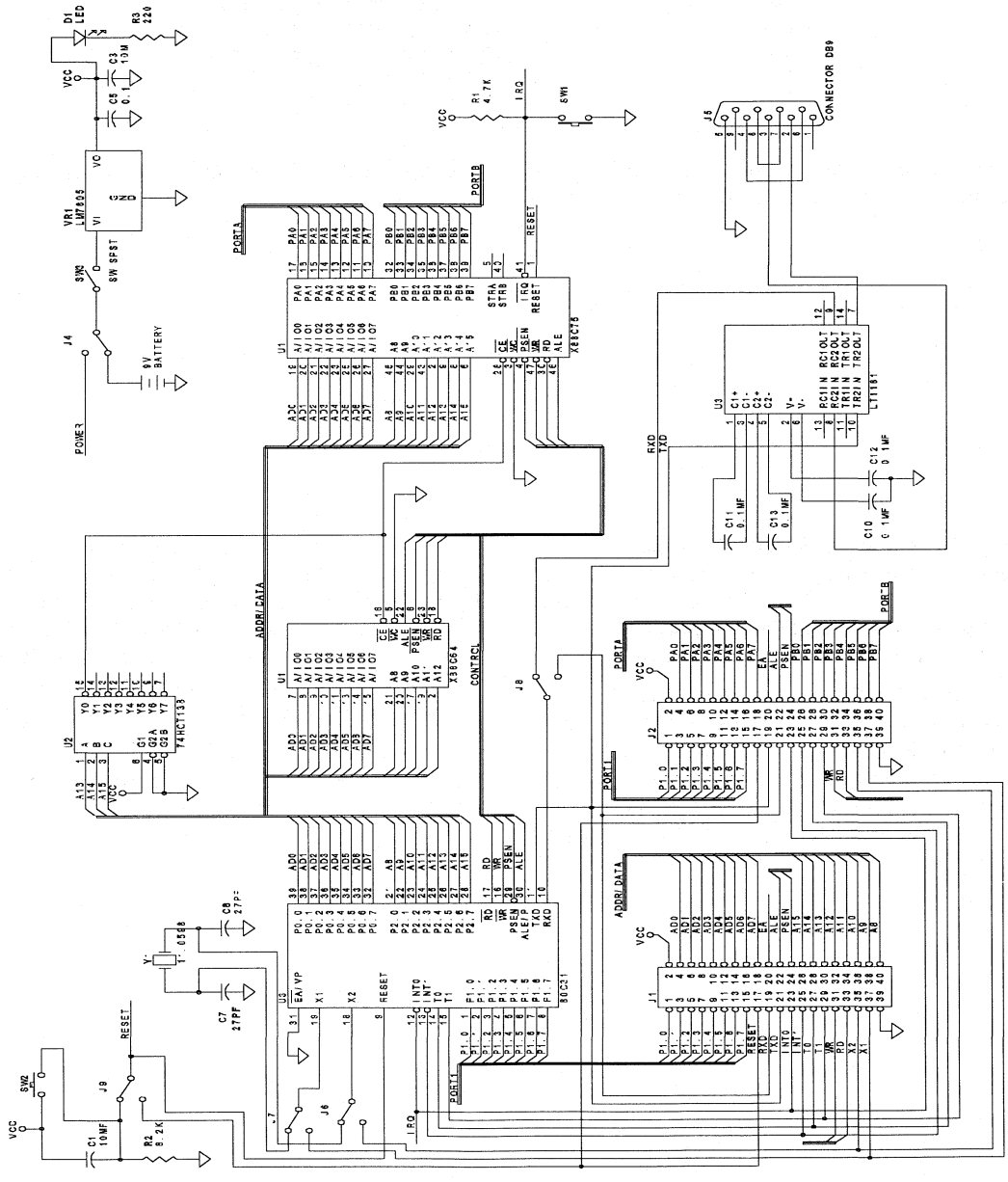

Figure 4. Evaluation Circuit for the X88C64 or X88C75

Using XSLIC and Xicor's XCOM Protocol

by Ray Kahidi, August 1993

The XSLIC driver uses the XCOM protocol format to communicate with the SLIC E^2. This application note lists and explains some commands in this protocol that the SLIC E^2 (version 3.0) recognizes.

Power-Up Sequence

When a microcontroller is reset, it begins fetching its initialization instructions from the SLIC E^2. The firmware initializes portions of the internal RAM, UART control registers, and some SFRs. At this point, the SLIC E^2, using the UART, transmits an acknowledge (ACK) character code 68 ("D") to the host system, indicating that it is ready to process commands.

The SLIC E^2 monitors the UART receive buffer for the ID request command "X". In response, the SLIC E^2 firmware transmits an ID sequence, the firmware version, and a carriage return code.

Device Programming

The program command contains a header field, consisting of four bytes which precede every block of data sent to the SLIC E^2 for programming. The bytes in the header are: a lead-in character used as command type identifier, the total number of bytes in the data block, and the starting memory address of the first byte in data block (with the lower address byte first). A data block refers to a string of packed hexadecimal bytes conveying code and data information.

The SLIC E^2 uses the page write mode in order to obtain shorter programming time. Hence, all data block content must belong to the same page. Address bits [12:5] of the start address specify the page number. The lower address bits [4:0] of the start address indicate an offset within the page. The offset value, plus the byte count, should not exceed the device page size of 32 bytes. After the SLIC E^2 completes the programming of a data block into the device, it transmits an ACK character to the host.

```
Host Command:                    X
SLIC E2:              D          X88C75: v <CR>
                      V = Current SLIC version number
```

```
Host Command:         M          XX    YYYY     Data
SLIC E2:              D
                      M          = Command Preamble
                      XX         = Byte Count
                      YYYY       = Start Address - bits [4:0] = offset
                                   [Byte Count + offset <= 32
```

BPR Programming

This command modifies the contents of the on-chip Block Protect register (BPR) before and/or after programming the part.

Content Verify

After programming the device with the desired data, the contents can be verified by sending data blocks in the same fashion as with the device programming command. The command identifier in the header field is changed, but the remaining parameters are identical. If the contents of the memory match the data block, a passed response is returned to the host (ACK character), otherwise a failed character (NACK "F") is returned.

System Reset

This command causes the SLIC E^2 firmware to restart by executing a software jump to the power-up routine. After initialization, the SLIC E^2 sends and ACK character to the host. It then begins monitoring the input for the ID request command "X". When the ID command is received, the SLIC E^2 responds with its ID string.

BPR Command

```
Host Command:        K          Data
DATA                 PROTECTED RANGE
0000 0001            [0000H-03FFH]
0000 0010            [0400H-07FFH]
0000 0100            [0800H-0BFFH]
0000 1000            [0C00H-0FFFH]
0001 0000            [1000H-13FFH]
0010 0000            [1400H-17FFH]
0100 0000            [1800H-1BFFH]
1000 0000            [1C00H-1FFFH]
```

Verify Command

```
Host Command:        V          XX    YYYY     Data
SLIC E2:             D          (Pass)
                     F          (Fail)
                     V          = Command Preamble
                     XX         = Byte Count
                     YYYY       = Start Address - bits [4:0] = offset
```

Reset Command

```
Host Command:        R          X
SLIC E2:             D          X68C64: v <CR>
                     V = Current SLIC version number
```

XSLIC Driver Overview and Command Interface

The XSLIC driver is a PC-based program that runs under MS-DOS 3.1 or later. It provides a menu driven user interface to the SLIC E^2 devices- through serial communications port in the PC. The in-system reprogramming feature of the SLIC E^2 devices are utilized to download application programs or to update existing code for de-bugging or upgrading purposes. The on-chip loader routines support the XCOM binary format, which is the communication protocol used by the XSLIC to issue commands or send data and information to the SLIC E^2.

XSLIC starts-up by sending a reset command "R" through the host COMx port to the SLIC E^2. If an ACK response is not received, an error message followed by the main menu is displayed. Following an ACK response, the XSLIC proceeds to issue the ID request command "X". The SLIC E^2 response contains

information such as the device type and firmware version currently programmed into the device. Next, the XSLIC searches in the current directory for its configuration file, the default name is "SLIC.CNF". Other filenames can be substituted by entering filename on the XSLIC command line. Detailed examination of the available options can be found in the following paragraphs.

Download

This option is used to program the application code into the SLIC E^2 device. The hexadecimal filename, including its path name if different from the current one, must be entered on the filename prompt line. Enter a blank line if the filename is previously specified using the FILENAME option. XSLIC reads and converts the contents of the file to the XCOM binary format prior to downloading. Each packet transfer concludes with the SLIC E^2 sending an ACK or NACK character back to indicate the success or failure of the operation. If an ACK character is received, the XSLIC prepares and transmits the next data block. The download process continues until either an EOF character is reached or a NACK character is received. The download option does not test if the data was properly stored into the device. The VERIFY option compares the contents of the device and contents of the file.

Filename

Use this option to specify the application program filename, including its path name, if different from the current path. The filename has to conform to the DOS specified file naming convention. When a valid filename is entered, the screen is repainted and the filename is displayed in the FILENAME option menu field. If the file is not found, an error message is displayed and main menu is displayed. The FILENAME option menu will contain either previously specified filename, or is blank if none was specified.

Verify

This option compares the contents of the SLIC E^2 with the contents of the specified disk file. When selected, it prompts for filename; if none is specified, the previously entered filename is substituted. If no valid filename is given, an error message is displayed and the program returns to the main menu. When a valid filename is specified, its contents are scanned and translated to the XCOM binary format before transmission to the SLIC E^2. If all bytes compare correctly, the SLIC E^2 sends an ACK character "D". All of the blocks are sent until either an EOF character is read or a NACK character "F" is received. If the contents do not match, the SLIC E^2 sends a NACK character.

Reset

This option sends a reset command to the SLIC E^2, forcing execution to resume from microcontroller RESET vector. The default reset vector points to the MAIN routine of the SLIC E^2 code. This routine initializes the stack, UART, receive buffer pointers, and other system parameters. An ACK character is then sent to the UART. The only commands that the SLIC E^2 will process at this stage are either the ID request "X", or another reset "R".

BPR Programming

This option allows for programming into the device the desired BPR value. The BPR is a nonvolatile register and it preserves its contents when the power to the device is removed. The BPR feature divides the E^2 memory into (8) 1K-byte blocks. Each block has its control bit within the BPR. Setting a control bit will protect the corresponding block against all write operations. To give SLIC E^2 write access to a memory block, the control bit of the memory block must be set to "0". After the programming of the memory block is complete, it can be protected. Refer to the BPR command table for a complete listing of the available BPR values and their corresponding memory blocks.

Relocate

This feature is used to reposition the portion of the code which occupies the lower memory block. The new location starts at either 80H or 100H (versus the old position 30H). A prompt is displayed for the destination address selection. The purpose of the move is to eliminate conflicts which may exist between extra ISR vectors and SLIC E^2 code space. Some enhanced 8051 derivatives include expanded ISR vectors. If the additional resources are not employed by the application, relocation is optional.

Setup

This option provides reconfiguration of the RS-232 communications parameters by the end user. The system baud rate can be customized to match the application's frequency requirements. The data length is fixed at eight, due to the nature of the XCOM binary format, and lower data lengths are not

supported. The stop and parity bits are also fixed. The default baud rate is set at 9600 bps.

Baud Rate

The default baud rate is set to 9600, however other values are supported. The timer constant value in the SLIC E^2 firmware controls the baud rate of the target system. The PC serial communications baud rate is determined by the values stored in high and low byte divisor registers. XSLIC always displays the error rate between the SLIC baud rate, calculated based on present timer constant value, and the PC baud rate. The value displayed in the BAUD rate field is desired and not the actual value. The PC divisor registers are programmed with the best estimates that will generate a rate closest to the selected value in the BAUD rate field. These values are copied to their respective hardware registers when the TEST or QUIT options are selected.

The baud rate of the application's system board is determined solely based on the Timer Constant (TC) value programmed into the SLIC E^2 and is independent of the value in the BAUD rate field. When the baud rate of the application board is calculated, if the TC value has not been modified, the result is based on the factory default TC value and the system clock frequency specified in the FREQUENCY field.

After the parameters have been modified to match your system requirements, use the TEST option to verify the operation. If communication is successfully established, the UPDATE option can be used to program into SLIC E^2 the new TC value.

System Clock

The system frequency of the unit equipped with the SLIC E^2 device can be specified using the SYSTEM CLOCK option. When entering desired values, use the "M" character to specify MHz and "K" for KHz for the frequency. The default parameters of the SLIC E^2 can not be initially modified without first establishing a communications link with it at the proper baud rate, which requires knowledge of the system clock frequency. If no entry is made for either the new baud rate or the system clock, the default values are used. The new system clock frequency is used to calculate the current baud rate of the SLIC E^2 system. The obtained baud rate is based on the timer constant value currently programmed into SLIC E^2 device. If the UPDATE, QUIT, or TEST options are selected, the host communication parameters are updated with the newly calculated values.

When new values are entered, the XSLIC first determines the current baud rate of the SLIC E^2 then it modifies default baud rate parameters of the SLIC E^2, resetting it so the new BAUD rate can take effect.

RTS/CTS

The RTS/CTS option field is used to directly disable the modem control lines. An "OFF" message in this option field indicates that the line's state is controlled via the BIOS function calls. If this field is set to "ON", then the modem control lines are disabled by the XSLIC. The XSLIC program assumes an 8250 compatible communications controller is being used, when writing to the modem control registers.

COMx

XSLIC supports up to four different serial communications ports. The selection is entered using the COMx port option field. A valid entry is a digit between 1-4. The base address of the ports are tabulated below:

COMx PORT	BASE ADDRESS
1	3F8
2	2F8
3	3E8
4	2E8

BIOS/Hardware

On some systems, the incoming characters are not buffered fast enough and are dropped. If this is the case, the communication interface experiences hang-ups or fails to get established.

The problem is eliminated by enabling the direct hardware access mode. This is controlled by the option field "Hardware/BIOS". When this field displays an "ON" message, the XSLIC will use direct hardware access to write or read from the UART. This feature only works on systems which are fully IBM PC compatible. If this option field displays an "OFF" message, the system BIOS calls are used to communicate with the UART. This will limit the baud

rate selection range to the values supported by the BIOS functions.

Test

After all communications parameters are set to desired values, the TEST RUN option should be used to establish communications with the SLIC E^2 device. An error message is displayed when communications fail due to an improper baud rate setting. At this point the baud rate should be changed and the TEST option selected until the interface passes the test.

Save Configuration, Recall Configuration

If the communications parameters have changed, the new values can be stored into a diskfile for future use. Select the SAVE CONFIG option if you want to save the current settings. Use the RECALL CONFIG option to reload the previously saved parameters.

When these options are selected, you are asked to enter the configuration file name. The default filename is used if the entry is omitted (SLIC.CNF). A List of the parameters saved to the configuration file are as follows:

Microcontroller type selected

The COMx port number

System clock rate

Actual operating baud rate

Timer constant value

Desired baud rate

Hardware or BIOS mode

Base address of SLIC (88Cxx SLIC)

Modem control lines (RTS/CTS)

E^2 memory map address (X88/68C75)

SFR memory map address (X88/68C75)

The application file name entered

Update

The UPDATE SLIC E^2 option allows for updating the SLIC E^2 code on the device. Modified communication parameters may require a different timer constant value than that currently programmed into the SLIC E^2 device. Invoking the UPDATE SLIC E^2 option sends a new timer constant value to the SLIC E^2 device. This option prompts for the base address of the current SLIC code. Skip this step when using the standard version, however, if the SLIC code is relocated to any location other than that used by the "ReLocate" option, the new location must be entered here. If the firmware version of the SLIC E^2 code is not current, XSLIC will prompt for permission to upgrade it.

Quit

Upon entering this option, the XSLIC program will exit to its main menu. The newly entered communications parameters will replace the default ones.

X88/X68C75 Support

When an X68/88C75 SLIC is installed, the set-up menu is expanded to include support for programming the EEM and SFRM registers on these parts. Selecting this option clears the screen and displays a new menu. If any of the default values are modified, the new value should be programmed into the SLIC E^2 device using the UPDATE option. The EEM/SFRM registers are updated by downloading a utility firmware to the SLIC E^2 device and executing the code. After the utilities perform their task of reprogramming the nonvolatile registers, by generating the required sequences, they reset the execution back to the SLIC E^2 MAIN routine.

E^2 MEMORY ADDRESS

This option is used to specify the E^2 memory mapped address range. Entering this option prompts for a number between 0 and 7. The corresponding memory range is shown below:

MAP VALUE	ADDRESS (HEX)
0	0000-1FFF
1	2000-3FFF
2	4000-5FFF
3	6000-7FFF
4	8000-9FFF
5	A000-BFFF
6	C000-DFFF
7	E000-FFFF

9

When CS is enabled and an address which falls within the chosen address map appears on the address bus, the E^2 memory is accessed. With the CS enabled, but the address outside of the E^2 memory range, access to the E^2 memory is denied, or vice-versa. A valid address will not be acknowledged if it does not accompany an active CS signal.

Special Function Registers (SFR) Address

This option is used to enter the SFR memory address map value. Upon entering this option, the system prompts for an entry between 0 to 32. These values and their corresponding memory map address ranges are tabulated below:

MAP VALUE	ADDRESS RANGE	MAP VALUE	ADDRESS RANGE
0	0000-03FF	10	4000-43FF
1	0400-07FF	11	4400-47FF
2	0800-0BFF	12	4800-4BFF
3	0C00-0FFF	13	4C00-4FFF
4	1000-13FF	14	5000-53FF
5	1400-17FF	15	5400-57FF
6	1800-1BFF	16	5800-5BFF
7	1C00-1FFF	17	5C00-5FFF
8	2000-23FF	18	6000-63FF
9	2400-27FF	19	6400-67FF
A	2800-2BFF	1A	6800-6BFF
B	2C00-2FFF	1B	6C00-6FFF
C	3000-33FF	1C	7000-73FF
D	3400-37FF	1D	7400-77FF
E	3800-3BFF	1E	7800-7BFF
F	3C00-3FFF	1F	7C00-7FFF

MAP VALUE	ADDRESS RANGE	MAP VALUE	ADDRESS RANGE
20	8000-83FF	30	C000-C3FF
21	8400-87FF	31	C400-C7FF
22	8800-8BFF	32	C800-CBFF
23	8C00-8FFF	33	CC00-CFFF
24	9000-93FF	34	D000-D3FF
25	9400-97FF	35	D400-D7FF
26	9800-9BFF	36	D800-DBFF
27	9C00-9FFF	37	DC00-DFFF
28	A000-A3FF	38	E000-E3FF
29	A400-A7FF	39	E400-E7FF
2A	A800-ABFF	3A	E800-EBFF
2B	AC00-AFFF	3B	EC00-EFFF
2C	B000-B3FF	3C	F000-F3FF
2D	B400-B7FF	3D	F400-F7FF
2E	B800-BBFF	3E	F800-FBFF
2F	BC00-BFFF	3F	FC00-FFFF

Port B Mode Selection

Port B can operate in two modes; general purpose I/O, or Latched Address Mode (LAM). This field toggles between the two modes. The bit which configures port B's operating mode is located in the E^2M register. When this field is modified, the UPDATE option has to be used to write the new selection into the E^2M register.

Update E^2M and SFRM Registers

Changes to the E^2M and SFRM registers are transferred to the SLIC device using the UPDATE option. When selected, it prompts for the register name to be updated; only one register can be updated at a time. If the SFRM and E^2M registers are both to be changed, then first update the SFRM.

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Introduction to Xicor's 80C51 SLIC E²PROM LapKit Chipset:

Simplifying the Tasks of Power Management, Keyboard Configuration, and LCD Control

by Gray Creager, July 1994

The constantly changing laptop computer marketplace requires solutions to several problems associated with bundling desktop computing power and configurability into systems of limited size and weight. With conventional designs, upgrading nonvolatile configuration information often requires the dismantling of the laptop unit and the swapping of parts, typically EPROMs. There are many obvious drawbacks to those designs. Now, Xicor introduces a chipset offering a much more flexible nonvolatile solution that is implemented in hardware, yet allows direct changes to BIOS firmware under software control. With this chipset, not only does the designer benefit from the advanced features of the 80C51SL architecture for keyboard control, but because of the use of E²PROM technology, any custom power management routines can be implemented in BIOS and updated whenever required. Such flexibility is essential for today's power hungry laptop and notebook computers. The LapKit chipset (Fig. 1) consists of an 80C51SL advanced keyboard microcontroller, an X88C75 E²Microperipheral, and an X9241 Quad E²POT. With these 3 chips, the problems associated with OTP based keyboard controllers are resolved. Since the contents of the X88C75 E² array can be updated in circuit, the problems and costs associated with the removal and replacement of EPROM memories are entirely avoided. The extra features and computation power of the 80C51SL also allow easy implementation of power management algorithms to extend battery life.

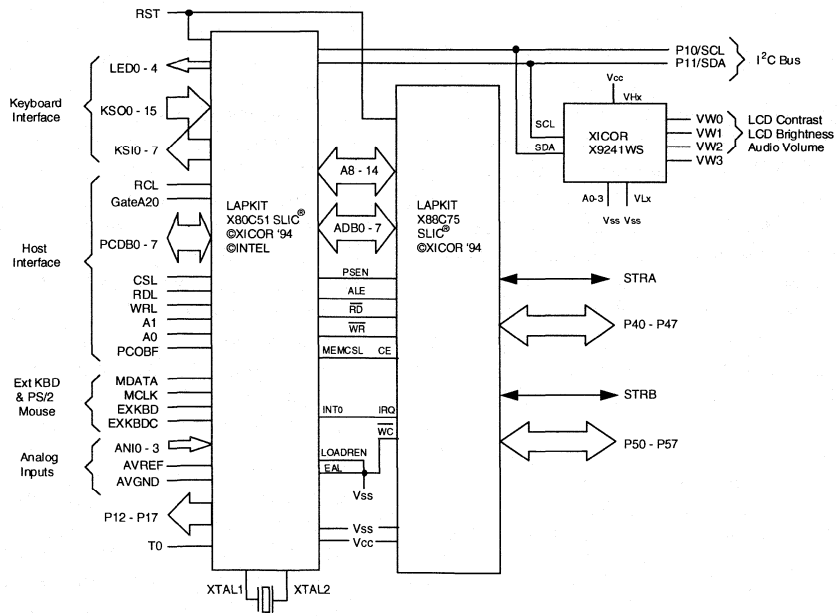


Figure 1 - LapKit chipset functional diagram

Finally, using just two E^2POTs of the X9241, LCD brightness and contrast are easily controllable. The remaining two E^2POTs can be used elsewhere in the system (e.g. volume control for a speaker, etc...).

The 80C51SL is a low power, universal keyboard controller specifically designed for use in laptop and notebook computer applications. Using the 80C51 architecture as it's core, this microcontroller has all of the functionality of the ubiquitous 8042 keyboard interface controller, yet with additional power management features. It is capable of operating at clocking frequencies up to 16MHz (at Vcc = 5V ±10%) and is packaged in a 100 pin PQFP. Among the more useful extra features integrated into this device is a 4-channel, 8-bit successive approximation A/D converter uniquely suited for power management duties. For interfacing, there are 4 high-drive, bidirectional port pins which can be configured into 2 standard serial interfaces, as many as 5 high-drive LED driver ports, up to 10 interrupts (including 6 definable external interrupts) with selectable priorities, and internal power-down/idle modes to increase battery life. When the 80C51SL is purchased as part of this chipset, the 16K-bytes of microcontroller ROM will contain Phoenix Technologies keyboard BIOS routines.

The X88C75 SLIC E^2Microperipheral is a highly integrated microcontroller peripheral intended to interface directly to (and to greatly enhance the capabilities of) 80C51 family microcontrollers. It has 8K-bytes of E^2PROM organized in a dual plane architecture (4K-bytes each), allowing concurrent read during write ability. As with other Xicor devices, Software Data Protect logic is provided to prevent undesired writes to the E^2 array, as well as the more advanced Block Lock data protection schemes for configuring the array in 1K-byte sections. This configuration is stored in a nonvolatile register and will be retained, even after power is removed. The X88C75 contains vectors to BIOS routines in the microcontroller that allow the CPU to reprogram the device (e.g. to alter custom power management routines, to change the keyboard scan matrix, etc...). This device provides two general purpose bidirectional I/O ports, providing a total of 16 additional bit addressable port pins. The X88C75 also features internal programmable address decoding, a multiplexed address/data bus, and 16-bytes of general purpose SRAM. The other important feature of the LapKit is the SLIC (Self Loading Integrated Code) pre-programmed into the 80C51SL ROM. These executable routines are customized for use by the 80C51SL to establish a reprogramming interface between the CPU and the X88C75. Effectively, the E^2 array of the X88C75 can be altered under CPU control (i.e. from a special DOS or Windows program).

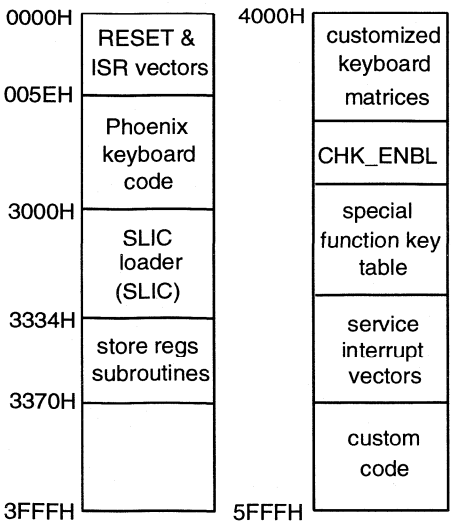
The X9241 Quad E^2POT is a nonvolatile, digitally controllable potentiometer which recognizes several different software commands passed on an I^2C compatible bus. These CMOS E^2POTs each have 64 wiper taps, with the ability to cascade any adjacent E^2POTs for longer tap lengths. The wiper position for each E^2POT can be stored in any of 4 associated nonvolatile registers for later recall. On power cycles, these four E^2POTs will return to the tap positions that were previously stored in each respective initial register.

There are several advantages of this chipset over the alternatives. The LapKit isolates power management from the CPU, and instead implements it with the excess computing power of the 80C51SL. This alleviates vendor incompatibility problems that surface when second sourcing a CPU with a different implementation for system management mode (not all manufacturers adhere to a common set of tasks to be performed when a CPU enters SMM) . Transferring the power management task to the microcontroller could be problematic for a designer who needs alot of BIOS code or needs to regularly upgrade this code. However, the Xicor LapKit is ideally suited for just such a task! With the 80C51SL's 16K-bytes of ROM and 8K-bytes of external memory in the X88C75, even the most ambitious power management schemes can be implemented. As upgrades are required, software executing on the CPU will allow direct in-circuit reprogrammability of the nonvolatile E^2 array.

With a trend toward longer product life for high performance laptops, expandability becomes an important issue to the consumer. However, the consumer will not want to sacrifice battery life because of these enhancements. Consequently, the addition of new components to the system will require different power management schemes. With the LapKit, the vendor can allow for appropriate changes

simply by providing reconfiguration software for consumer use. Also, as NiCd batteries become outdated by newer and better technologies, a laptop computer could be reconfigured for other battery types simply by altering the power management BIOS. In this manner, the LapKit can be used to make a laptop nearly as expandable as a conventional desktop PC, where power management requirements are not normally of concern.

Other uses for the X88C75 code space include the ability to re-map the scanning matrix of the keyboard at any time. This feature would be useful when switching between incompatible keyboards at separate locations. These BIOS and "custom" routines are interrupt driven, allowing greater flexibility to enable/disable certain routines using the vector redirection table included on the X88C75. The ROM includes the RESET and ISR vectors, SLIC routines, Phoenix keyboard BIOS, and generic I^2C interface routines. Using these I^2C routines, a System Management Bus (see the Intel and Duracell Smart Battery specification) or an ACCESS.bus could also be implemented. The X88C75 E^2 array includes the previously mentioned interrupt redirection map, "custom" keyboard matrix, a command redirection map, and any other "custom" code. This provides for efficient and powerful software control of the 80C51SL microcontroller. The segmentation of the 80C51SL memory map is shown below.



Finally, the X9241 Quad E^2POT can be used for a variety of tasks in the laptop environment, including control of the LCD. In the backlighting circuitry of the LCD, it is of great benefit to manipulate the brightness of the display screen. Intelligent control will decrease the current draw on the battery and extend it's life before recharge. Consequently, this is an important part of power management. The X9241 will allow several different brightness settings under digital control, since it is often a nuisance to have the LCD go dark when not in constant use. Using an E^2POT is identical to a conventional mechanical pot or slider switch, but with the additional advantages of digital control. Similar uses can be found for contrast control, volume control, etc...

Clearly, the Lapkit will be a significant enhancement of the features of the workhorse 80C51 microcontroller family. In comparison to other keyboard controllers, Xicor's LapKit will provide greater functionality and more nonvolatile features. With flexible power management, keyboard, and LCD control, this chipset will be a complement to any laptop or notebook design. There is a 5V (±10%) chipset available designated LapKit 51, as well as a 3.3V (±10%) version designated LapKit 51LV. At the time of this databook's publication, the LapKit 51LV chipset's economical price of $25 for 10,000 units or more, with the previously described functionality, is unprecedented in the laptop world.

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Using SLIC Devices with NEC 78K2 Microcontrollers

by Carlos Martinez, August 1994

Introduction

This application note discusses the design of a system that combines an NEC uPD782xx (78K2) microcontroller with a Xicor X88C64 or X88C75 E^2PROM, however with minimal changes, the firmware can also support members of the K3 family. The design requires no glue logic, uses only a single memory device, and utilizes firmware available from Xicor to implement the SLIC (Self Loading Integrated Code) interface to a host PC.

SLIC E^2PROM Basics

The X88Cxx E^2PROM family members are nonvolatile memory devices accommodating a multiplexed ADDR/DATA bus. Their dual plane architecture allows writing to one plane while continuing to read from the other. Current family members include the X88C64 and X88C75. Both have 8K-bytes of on-chip storage. The X88C75 adds two, byte-wide, bidirectional I/O ports (capable of providing DEMUXed address outputs), 16-bytes of SRAM, a programmable address decoder, and an intelligent interrupt controller.

The purpose of the SLIC firmware is to provide a means of loading application software into the program memory through the 78K2 UART. This ability eliminates the need to pre-program the application code to the device prior to PCB board assembly. It also facilitates repetitive software downloading in various stages of manufacturing, when making changes during program development, and when managing firmware upgrades to systems in the field.

The ability to run code out of the X88Cxx device, while loading new code, is a unique feature of the device. With two independent arrays of E^2PROM, the microcomputer can execute code from one array, while writing to the other. This feature is called Concurrent Read During Write.

When the board is powered-up, the 78K2 microcontroller begins to execute code out of the E^2PROM. The code initializes the microcomputer and establishes communication with the host through the serial port. The host uses the SLIC firmware to program the Block Protect register (BPR) and download the user's application software. Control can be transferred to the user's application software by performing a hardware or software reset. The SLIC routines can stay resident in the E^2PROM. Whenever subsequent downloads are desired, the application software can change the RESET vector to return to the SLIC firmware on the next system reset. Alternately, an external interrupt vector can be used to re-invoke the SLIC firmware. This is especially useful when the application software has become lost or "hung-up". The SLIC firmware for the 78K2 device uses 511 bytes of the E^2PROM and is split between the two planes. The firmware also uses 38 bytes of the 78K2 internal RAM.

The host PC connects to the RS-232 port on the board and communicates with the SLIC firmware. The host PC controls the download of the application software and other operations. Prior to loading application code, the host computer converts the application firmware object code into the Xicor communications (XCOM) format. Xicor has developed a program called XSLIC that will perform this function on an IBM compatible computer. A copy of the XSLIC program is available.

In addition to the download command, the SLIC will recognize other commands from the host computer: Verify, Reset, Setup, Set BPR, and Quit. The XSLIC program also has a Relocate command that is not used by the 78K2.

78K2 SLIC E²PROM Implementation

Figure 1 shows a minimal implementation of the 78K2 and either the X88C64 or the X88C75. This design assumes no other circuitry and no additional memory, hence there is no need for additional address decoding. The SLIC firmware code is pre-loaded into the X88Cxx. When the board powers-up, the SLIC code will initialize the 78K2 and establish communications with the host. Host commands will direct the SLIC firmware to save into the E²PROM application program code received over the serial link.

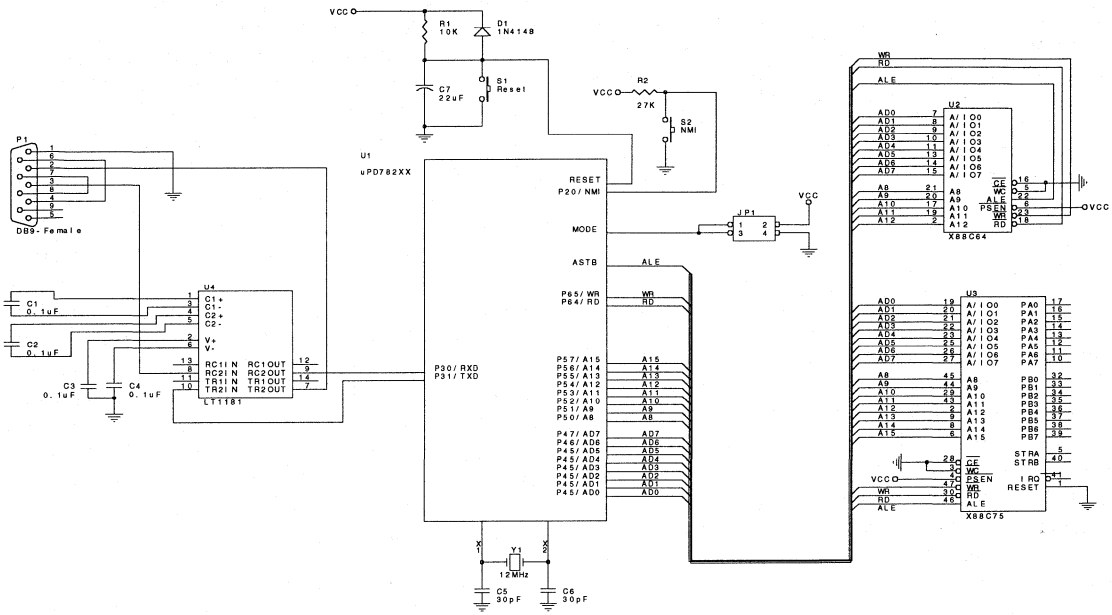

Figure 1. 78K2/X88Cxx Schematic

In order to write application code, it is necessary to know which areas of memory the SLIC firmware uses. This is documented in Figure 3. From 0H to 7FH are 78K2 RESET, Interrupt, and CALLT vectors. The SLIC code uses locations 0H and 1H for a reset vector and location 7EH and 7FH for a CALLT vector. If the application code over-writes the RESET vector, the code must be able to re-invoke the SLIC program. If code over-writes the CALLT vector, the SLIC code will not work.

Space is available on the X88Cxx for the user's application program from 180H to 1EFFH (7552 bytes). For programmers not familiar with the 78K2, the CALLT vector area can also be used for application programs, if not being used for call vectors.

The 78K2 does not provide address signals to the external world when addressing internal RAM or SFR areas, except for an external SFR area between 0FFD0H and 0FFDFH. Because of this restriction, and to provide maximum flexibility, the X88C75 SFR registers are mapped at location 0F800H. This is set by writing to the X88C75 SFR Map register. Locating these registers at 0F800H reduces the maximum code space by 1K bytes, but the design will be usable by all members of the 7821x and 7823x families.

Since the address/data lines take up ports 4 and 5, and since port 4 and 5 registers reside in the SFR area (0FF04H and 0FF05H), writing data to port 4 or port 5 registers can not activate the I/O expansion of the X88C75. It is necessary to relocate these ports to the X88C75 SFR area. To do this, the application code must write to 0F804H or 0F805H instead of writing to ports 4 and 5. In this way, data meant for port 4 goes to the X88C75 Port A and data meant for port 5 goes to the X88C75 Port B.

Writing 78K2 Application Code

Writing application code for use with the SLIC firmware is very easy. By using assembler directives for locating code and data space, there will be little problem with application code disrupting SLIC routines.

Some of these techniques are shown in the SLIC listing. For example, to locate the SLIC code to address 01F00H, the directive:

```
UPR_BNK    CSEG     AT      01F00H
```

is used. Similarly, RAM is reserved for SLIC firmware use by implementing the directive:

```
SLICDATA   DSEG     AT      0FE9CH
```

Addr	USE	Comments
00000H–0003FH	ISR Vectors	0000-0002 SLIC Reset Vector
00040H–0007DH	CALLT Vectors	Also available for user's code
0007EH–0017FH	SLIC Code	007E-007F SLIC CALLT Vector
00180H–01DFFH	USER's Program	
01F00H–01FFFH	SLIC Code	
02000H–0F7FFH	USER's Program	Other memory devices
0F800H–0F838H	X88C75 Internal SFRs	[See Figure 3]
0FA00H–0FA0FH	X88C75 RAM	
0FB00H–0FDFFH	USER's RAM	Internal to 78K2Size depends on choice of 78K2
0FE00H–0FE1FH	STACK RAM	Used by SLIC, but can also be used by application
0FE20–0FE9BH	USER's RAM	Internal to 78K2
0FE9CH–0FEC1H	SLIC RAM	Can be used by application, if no SLIC routine used
0FEC2H 0FFFFH	Macro Service General Purpose Special Function Registers	

Figure 2. 78K2/X88C75 Memory Map

Address	Function
0F800	SFR Map Register
0F808	Port B Data Register (Port 5)
0F810	Port A Data Register (Port 4)
0F818	Interrupt Control Register
0F820	Configuration Register
0F828	Port B Pin Register
0F830	Port A Pin Register
0F838	Program Map Register
0FA00-0FA0F	X88C75 RAM block

Figure 3. X88C75 SFR Memory Map

When moving between a 78K2 ROM part and a 78K2/X88C75 with I/O expansion, writing to Ports 4 and 5 is handled differently. To prevent a great deal of code modifications, conditional assembly directives can be used. In this way a single line change will accommodate either hardware configuration (see Figure 4).

```
;$          SET     (SW1);ROM devices
$           RESET   (SW1);ROMless devices
$           IF      (SW1)
PORT4       EQU     0FF04H
PORT5       EQU     0FF05H
$           ELSE
PORT5       EQU     0F808H
PORT4       EQU     0F810H
$           ENDIF
            :
            :
            MOV     A,PORT4
            MOV     PORT5,A
```

Figure 4. Selecting Port access ROM v. ROMless

Other limitations in fully emulating a 78K2 ROM device are the loss of two I/Os and the need to add X88C75 I/O port setup routines to existing "ROM" code. The I/Os are lost since the read and write lines share pins with Port 6 I/O. These cannot be re-created by the X88C75.

The port I/O software needs to modify the SFR Map register of the value 03FH to map the X88C75 SFRs to address 0F800H. As a default, the SFRs are mapped to address 0FC00H. Those members of the 78K2 family with 1K internal RAM cannot utilize the X88C75 features with default SFR mapping. Once the SFRs are mapped, configuration information is loaded into the Interrupt Status register (ISR) and to the Configuration register (CR). These are located at 0F818H and 0F820H, respectively. This configures the operation of the ports and interrupts.

XSLIC Command interface

The XSLIC program is a DOS based software driver, designed to facilitate communication with the SLIC E^2PROM. The XSLIC program can download programs to the SLIC E^2PROM devices by converting the files from either Intel Hex or Motorola 'S' formats to the Xicor XCOM format, supported by the SLIC firmware.

Listed below are the commands available at the XSLIC main menu:

Option Name	Function
Download	Download the specified file
BPR	Modify the BPR contents
Verify	Verify SLIC contents match the file
Filename	Application Hex filename
Reset	Software reset for the SLIC
ReLocate	Relocate the SLIC code
Setup	Setup new communication parameters
Quit	Exit the SLIC

Figure 5. XSLIC Menu Commands

The XSLIC Download option does not verify the programmed code. The verify option is used after programming, to check that the download has been successful.

XCOM Format

XCOM is the protocol format that is used to communicate with the SLIC E^2PROM. The following lists explain some of the commands in the protocol.

Power-Up Sequence

After RESET, the SLIC E^2PROM initializes portions of the internal RAM, UART control registers, and some SFRs. The SLIC firmware eventually sends a 'D' character over the serial link to the host indicating that it is ready to receive a command. The SLIC firmware monitors the UART receive buffer for a request command 'X'. In response, the SLIC firmware transmits an ID sequence, the firmware revision, and a carriage return code.

Device Programming

A header field, consisting of four bytes, must precede every block of data sent to the SLIC E^2PROM for programming. The bytes in the header are a lead-in character used as a command identifier, the total number of bytes in the data block, and the starting address of the first byte in the data byte (lower byte first). A data block refers to a string of packed hex bytes conveying code and data information.

The SLIC E^2PROM uses the X88Cxx page write mode in order to obtain a shorter programming time. Hence, the data block content must belong to the same page and bits [12:5] of the start address must specify the page number. The lower address bits [4:0] of the start address indicate an offset within the page. The total offset value, plus the byte count, should not exceed the X88Cxx page size of 32 bytes.

After the SLIC E^2PROM firmware programs the data block into the device, an ASCII 'D' is transmitted to the host.

BPR Programming

This command modifies the contents of the on-chip Block Protect register (BPR) before and/or after programming the part.

Content Verify

After programming the device with the desired data, the contents can be verified by sending data blocks in the same fashion as in the device programming command. The header field specifies a different command identifier, but all other parameters are the same. If the contents of the memory match the data blocks being verified, a block passed response is returned, otherwise a block failed message is returned.

System Reset

This command causes the SLIC E^2PROM firmware to restart by jumping to the power-up start routine.

SLIC Firmware discussion

The SLIC software that is loaded to the X88C64 or X88C75 occupies about 512 bytes of the 8K-byte capacity of the device. It is not possible for the SLIC firmware to download software to completely replace these 500 bytes, but care should be taken when writing application code to avoid overwriting any part of the SLIC code. The user's application code could intentionally over-write the SLIC code, however it is recommended that the SLIC code be left resident to facilitate future downloads.

Note: There are two routines in the SLIC code that are not currently used by the XSLIC program. These are available to the application code. The first of these routines is "proc_sfr". This is used to send a byte to the SFR Map register. This byte maps the X88C75 SFR registers to a 1K-byte segment. The second routine is "proc_eem". This is used to send a byte to the EEM Register of the X88C75. This byte is used to program the operation of Port B (either I/O or the low address byte), the polarity of the RESET pin, and the mapping of nonvolatile memory to an 8K-byte segment.

Code Listing

The entire code listing for this 78K2 SLIC firmware is available on the Xicor BBS at (800) 258-8864, operating at up to 19.2K baud.

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What is PASS SecureFlash™ ?

By Richard Downing, March 1994

Introduction

The X76F041 PASS SecureFlash is a high security device containing four flash memory arrays. The level of protection, against unauthorized access, given to each array is highly configurable, with access being restricted using three 64-bit programmable passwords: the Read, Write, or Configuration Password. The Configuration Password is the "master key" that allows unlimited access to the memory arrays and is required to configure the security options. The Read and Write Passwords are used to provide limited access to the otherwise protected array memory.

The X76F041, whose block diagram is shown in Figure 1, uses a standard ISO pinout with the serial communication interface consisting of a clock line (SCL) and a bidirectional data line (SDA). Each part is accessed through a chip select input ($\overline{CS}$) and identified using the response to reset (RST) pin that initiates a predefined 32-bit data stream.

This CMOS device uses Xicor's proprietary flash cell technology to provide four 128x8 nonvolatile SecureFlash memory arrays, with an endurance of 100,000 cycles per page and a minimum data retention of at least 100 years.

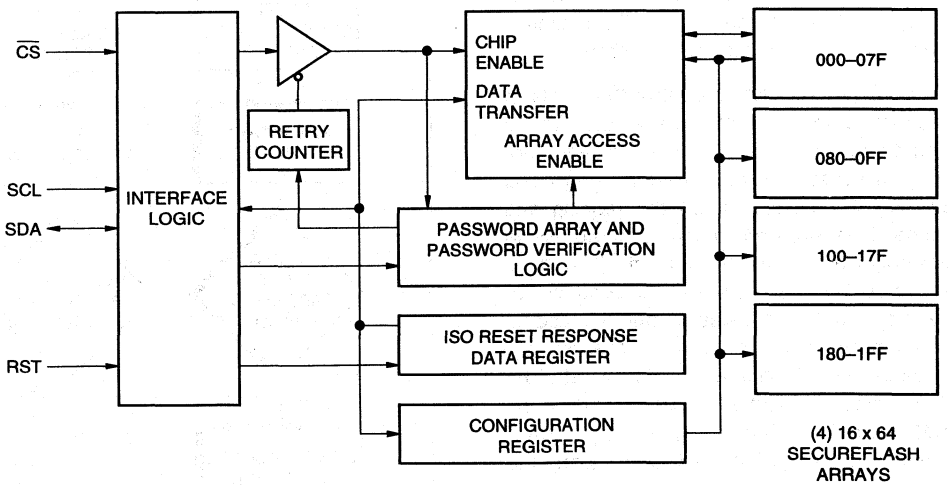

Figure 1.

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Password Protected

The three 64-bit passwords, used to safeguard the integrity of the X76F041, provide a high level of security. These passwords are reprogrammable and can be encrypted on the fly to enhance security. The probability of guessing a correct password is one in 18 quintillion (2^{64} = 18,446,744,073,700,000,000).

Access to a protected array is achieved by sending the appropriate password as part of the operation sequence, waiting 10ms and polling to check the validity of the password. This password "checking" delay ensures that large numbers of access attempts can not be tried in a short period of time and results in the minimum amount of time required to try all possible combinations being well over 5.8 billion years.

Configurable Security

The X76F041 uses five nonvolatile configuration registers, that are programmed using the Configuration Password to configure the levels of security required by an application: Array Control register 1, Array Control register 2, Configuration register, Retry register, and Retry Counter register.

The two Array Control registers control the levels of protection given to the four memory arrays. These registers determine which passwords, if any, are required to gain access to the individual arrays and define any restrictions imposed on the reading and writing of data. One such restriction, allowing bits to be changed only from "1" to "0" and not "0" to "1" is particularly useful in debit-type applications where credits are required to be deleted, but not added. These restrictions do not apply when the arrays are accessed using the Configuration Password. The Configuration register, Retry register and Retry Counter and are used to limit the number of invalid password attempts. The Retry register stores the maximum number of permitted password attempts, the Retry Counter counts the number of invalid attempts, and the Configuration register configures the operation of the Retry counter and defines the consequences of the Retry Counter being equal to the Retry register—access to the arrays may be restricted to configuration operations only or permanently terminated by "killing" the device.

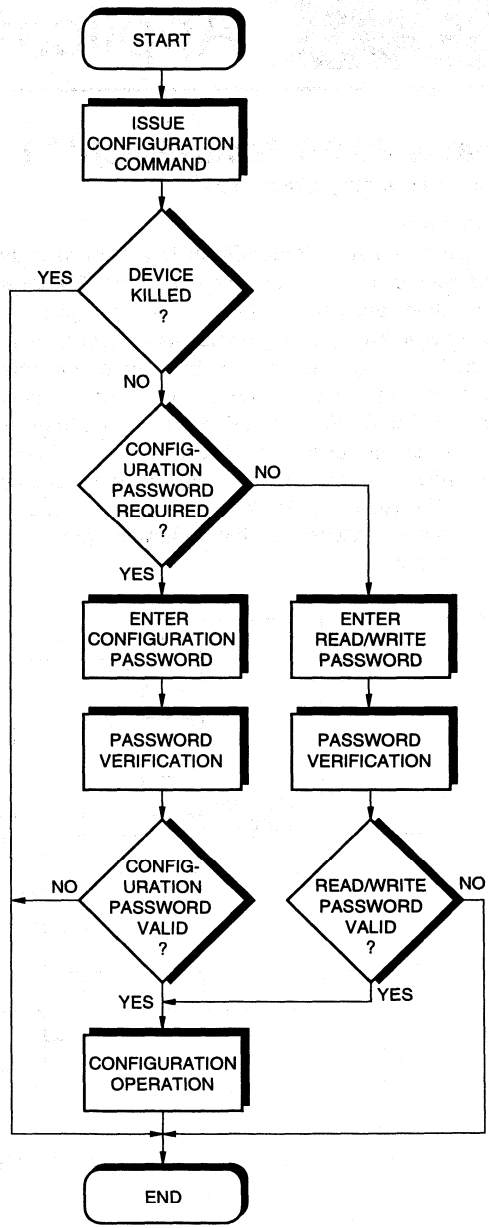

Figure 2. Configuration Command Flow

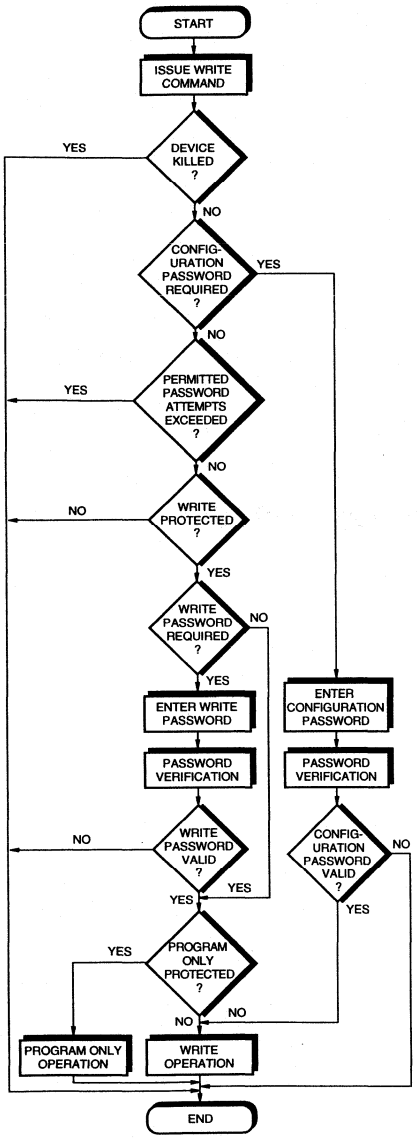

Figure 3. Write Command Flow

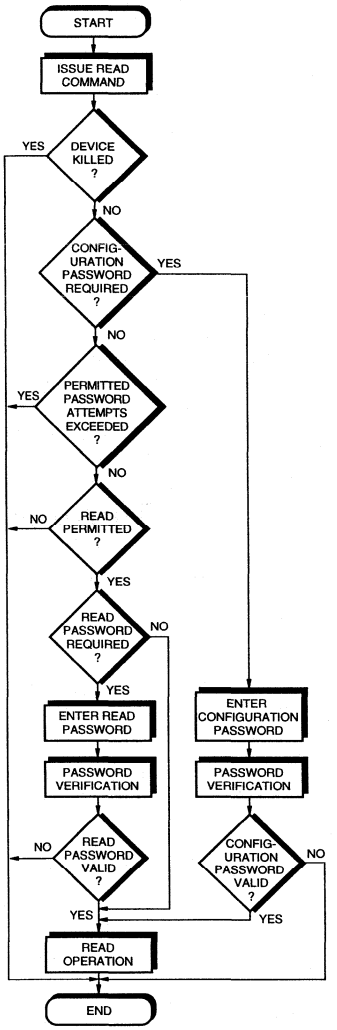

Figure 4. Read Command Flow

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Customizing Communication Parameters on the SLIC E^2

by Ray Kahidi, August 1993

The X88C64 SLIC E^2 configures the 8051 UART to operate at a 9600 baud rate. In many applications it is desirable to change the baud rate to a different value. For a temporary change in the baud rate, update the timer1 reload constant in register TH1 at run time and after the SLIC E^2's initialization of the UART. To permanently set a new default baud rate, one must modify the section of SLIC E^2 code that holds this parameter value. The location is 00FDH in the current versions of the SLIC E^2 code (revisions B.2.0 and B.2.1). The new timer1 constant can be either programmed into the SLIC E^2, using an EEPROM programmer, or downloaded to the SLIC E^2 from the XSLIC setup menu.

One can obtain new timer1 reload constants using the following equation:

$$BAUDrate = \frac{2(CRYSTALfrequency)}{(32)(12)(256 - TC)}$$

BAUDrate: the desired baud rate.

CRYSTALfrequency: The frequency of the external crystal/oscillator or clock connected to the microcontroller.

TC: Is the Timer Constant (single byte quantity).

The table below gives some timer1 reload constants for commonly used baud rates and crystal/oscillator values. Again, the SLIC E^2 sets the default baud rate of the 8051's serial communication port to 9600. However, with this information, the user's application program may elect other values as the power-up baud rate.

Table 1.

BAUD rate	TC (f = 11.058MHz)	TC (f = 12MHz)
9600	FAH	F9H
4800	F4H	F3H
2400	E8H	E6H
1200	D0H	CCH

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The X24C44 NOVRAM Teams up with 8051 Microcontrollers

by Rick Orlando, January 1990

Introduction

The X24C44 is a 256-bit serial NOVRAM internally configured as sixteen 16-bit words of RAM overlaid bit for bit with a nonvolatile E^2PROM. The X24C44. has the standard hardware RECALL and STORE inputs plus the ability to perform these same operations under software control, thereby freeing two microcontroller port pins for other tasks. The serial interface allows the X24C44 to be packaged in a low cost space saving 8-pin mini DIP. When teamed with the 8051 family of microcontrollers (Figure 1), the X24C44's small physical size, software instruction set, and serial interface make it an ideal parameter storage and scratch pad memory, while maintaining full use of the 8051 serial port as a UART.

Scope

This application note describes interfacing the X24C44 with the 8051 family of microcontrollers. Emphasis will be placed on the timing considerations of the interface and explaining the modifications to the instruction words for normal device operation. This note assumes the reader has access to a Xicor Data Book and an Intel Microcontroller Handbook.

Serial Port Operation

Port 3 on the 8051 provides a serial port that can be used in two basic configurations, full duplex and half duplex. This note examines the half duplex (mode 0) operation when interfacing to the X24C44. Port 3 pin 1 (P3.1) is the clock output for both transmit and receive modes and port 3 pin 0 (P3.0) is used for bidirectional data transfers. The clock output frequency is 1/12 of the XTAL oscillator input frequency. To simplify timing calculations, this note will assume an input frequency of 12MHz resulting in a symmetrical 1MHz output on P3.1.

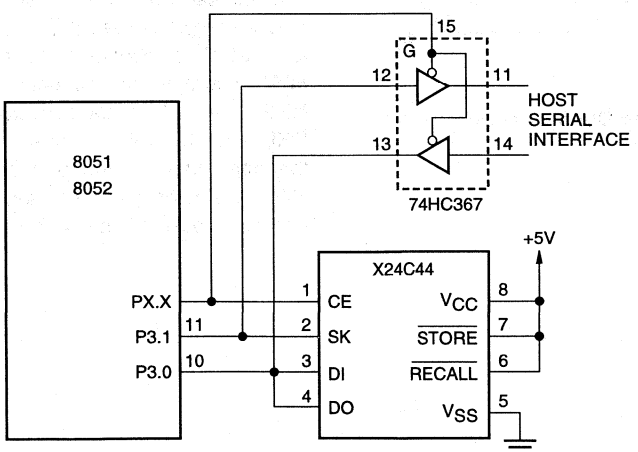

Figure 1. 8051 and X24C44 Interface Adds Scratch Pad RAM and Nonvolatile Parameter Storage via the 8051 Microcontroller Serial Port and Still Maintain Full Use of the Serial Port as a UART.

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The P3.1 and P3.0 pins, when inactive (neither transmitting nor receiving) are always a logic "1" (HIGH). When a data transfer commences, P3.1 will be LOW during machine cycle states S3, S4, and S5 and will be HIGH during states S6, S1, and S2. When transmitting, data is shifted out on P3.0 during S6P2 (state 6 phase 2) LSB first. When receiving, data is sampled during S5P2. Refer to Figure 3 for the basic 8051 serial port timing.

Hardware Connections

The X24C44 directly interfaces with the 8051 with no external circuitry required. DI and DO of the X24C44 are both tied to P3.0, SK is tied to P3.1, CE is tied to any free port pin configured as an output, and STORE and RECALL are tied to V_{CC} (see Figure 2).

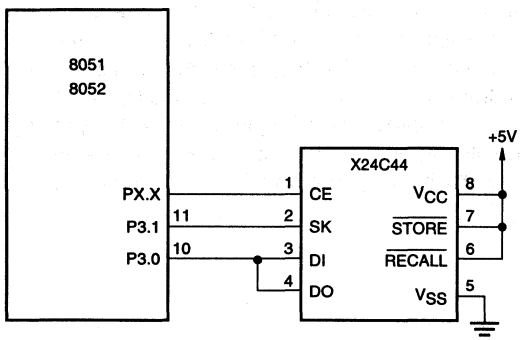

Figure 2. Basic Configuration

X24C44 Operations Review

The X24C44 is a serial device and in this application, all chip functions are handled via the software instructions. The 8051 transmits data LSB first, but the instruction format for the X24C44 shows the instruction to be transmitted MSB first. This requires a simple transposition of the instruction, MSB for LSB. The memory is effectively a FIFO, so the data to be stored need not be transposed.

Internally the X24C44 increments a bit (clock) counter. This is used to indicate the end of an instruction and, if a read or write instruction is received, to increment a bit position pointer. This pointer enables individual RAM cells for writing and reading. The counter for the pointer increments from zero to fifteen. If CE remains HIGH and SK continues to clock, the counter will rollover from fifteen to zero. The word address does not increment, therefore during a write operation, if SK continues to clock and CE is HIGH, a 25th rising clock edge (8 edges for instruction + 16 edges for the data word + 1) would cause bit position zero to be overwritten.

System Characteristics

Under normal operating conditions, the X24C44 expects CE to transition LOW to HIGH when SK is LOW in order that the first bit of data can be clocked into the X24C44 on the first rising edge of SK. The data is sampled to see if it is "0" (a don't care state) or a "1" which is recognized as an instruction start. The 8051, however, places both P3.1 and P3.0 in the HIGH state when not actively transmitting. THIS IS OK! The X24C44 internally gates CE and SK; therefore, toggling the port pin controlling CE to a HIGH effectively generates the first rising edge of SK, and also clocks in the HIGH present at P3.0 (DI).

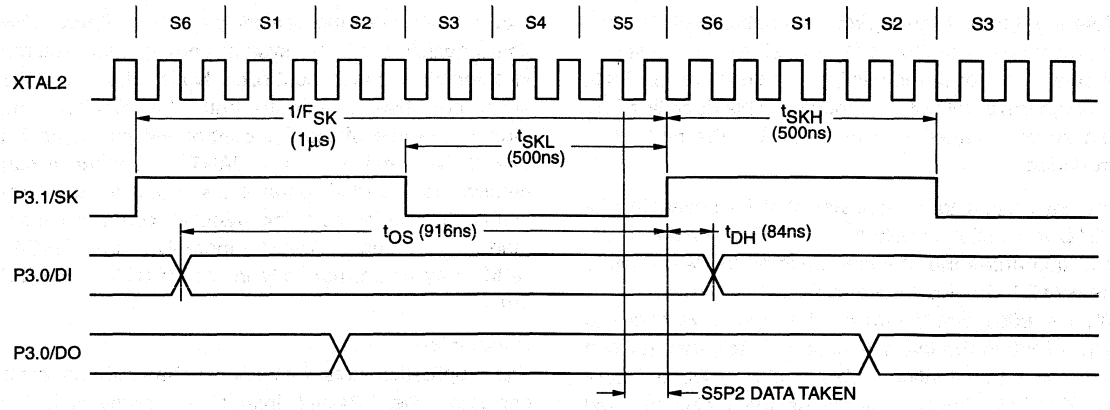

Figure 3. 12MHz 8051 Serial Port Mode 0 and X24C44 Timing

What this does is clock a "1" into the X24C44 indicating the start of an instruction prior to any shifting operation by the 8051 serial port. This will require dropping the leading "1" from the instruction. See Table 1 for the WAS/IS conditions for the equivalent instructions to be used by the 8051.

The 8051 will still generate eight rising clock edges on P3.1 for each byte loaded into the shift register (SBUF), effectively providing the X24C44 with nine clocks for the first byte. For the single byte instructions, the ninth clock and data are ignored by the X24C44. Refer to Figure 4 for the single byte instruction timing.

Writing

Writing to the RAM array is straightforward. The write instruction is issued by the 8051 in the same manner as the single byte instructions. The MSB (eighth bit) of the instruction byte is clocked in on the equivalent ninth clock rising edge. This bit is recognized as the first data bit of the transfer and is initially written into the addressed word's bit position zero. The 8051 will continue to transmit two more bytes of actual data. The LSB (bit zero) of the first byte will be physically located in bit position one and all subsequent bits will also be offset by one. The MSB (sixteenth data bit) of the word will be written into bit position zero, overwriting the last bit of the instruction byte. Refer to Figure 5 for the sequence of operations.

Reading

Reading data back from the RAM array is quite similar. The X24C44 begins to shift data out during the instruction cycle (more on this later). After the instruction is shifted out, the 8051 must turn around P3.0 and configure it as an input. CE and SK are static during this period and the DO output will remain unchanged until after the rising edge of the first 8051 receive data clock. Therefore, the first data shifted into the 8051 will be from bit position one, equivalent to the LSB originally written. Refer to Figure 5 for the sequence of operations.

Bus Contention

There will not be any bus contention for single byte instructions or the WRITE command. However, for the READ command there could be contention. While the 8051 is still shifting out the instruction byte, the X24C44 begins to output data on the same line. Refer to figure 5, just aftre the falling edge of clock eight.

The 8051 shifts out data at S6P2. If the data changes state from "0" to "1" a high current enhancement FET is turned on for two 8051 system clock cycles. This is used to provide a fast rise time. At the end of this two cycle period, the enhancement FET is turned off and the output is held HIGH by a depletion mode FET that essentially looks like a resistor pull-up (refer to Intel's Microcontroller Handbook [1984] pages 6-6 and 6-7).

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Note that the high drive circuit is enabled only for data state changes from "0" to "1"; therefore, if the output is already a "1" and another "1" is shifted out on P3.0, the high drive will not be turned on. This depletion FET can source a maximum of 250 µA if the port pin is grounded.

The instruction table indicates that bit seven for the READ instruction should be a "1". The reason for this is to guarantee that the high drive period is off before the X24C44 begins to output data. If bit seven were a "0", the 8051 would turn on the high drive circuit to return P3.0 to the inactive state, possibly generating a high current contention problem with the DO output of the X24C44. Figure 6 illustrates the timing involved during clock eight. The high drive period of the 8051 is turned off well before the X24C44 begins to output data.

Versatility

The DO output of the X24C44 is always in the high impedance state unless it is outputting data in response to a READ command. Therefore, the serial port of the 8051 need not be dedicated solely to a serial memory interface.

Figure 1 illustrates the versatility that this affords. This figure depicts the basic system components required in a remote location controller. Notice that the 8051 serial port has access to both the X24C44 and through the use of the CE control line maintains full use of the serial port as a UART. Therefore, it can receive downloaded parameters from a host, re-enable the serial port for X24C44 communication, then store the data either temporarily in the X24C44 RAM array or permanently in the X24C44 E^2PROM array.

Conclusion

This application note has shown that with no extra hardware, the X24C44 interfaces directly with the 8051 family of microcontrollers, providing a nonvolatile memory storage and scratch pad memory, while maintaining full 8051 UART capabilities. It is the ideal solution for applications where extra memory is required but few port pins are available for implementation.

Table 1. Reconfigured Instruction Format

INSTRUCTION	WAS									IS							
	7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0
WRDS	1	X	X	X	X	0	0	0		X	0	0	0	X	X	X	X
STO	1	X	X	X	X	0	0	1		X	1	0	0	X	X	X	X
RESERVED	1	X	X	X	X	0	1	0		X	0	1	0	X	X	X	X
WRITE	1	A	A	A	A	0	1	1		X	1	1	0	A	A	A	A
WREN	1	X	X	X	X	1	0	0		X	0	0	1	X	X	X	X
RCL	1	X	X	X	X	1	0	1		X	1	0	1	X	X	X	X
READ	1	A	A	A	A	1	1	X		1	X	1	1	A	A	A	A

*Note: bit 7 of the READ command should be a "1" to avoid bus contention.

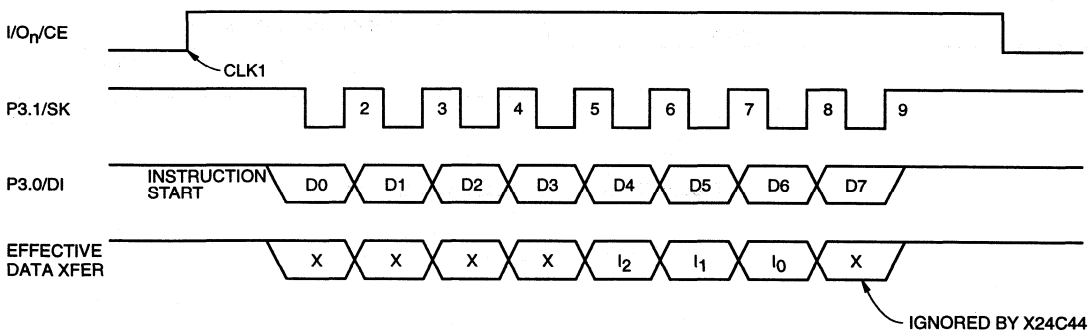

Figure 4. Single Byte Instructions

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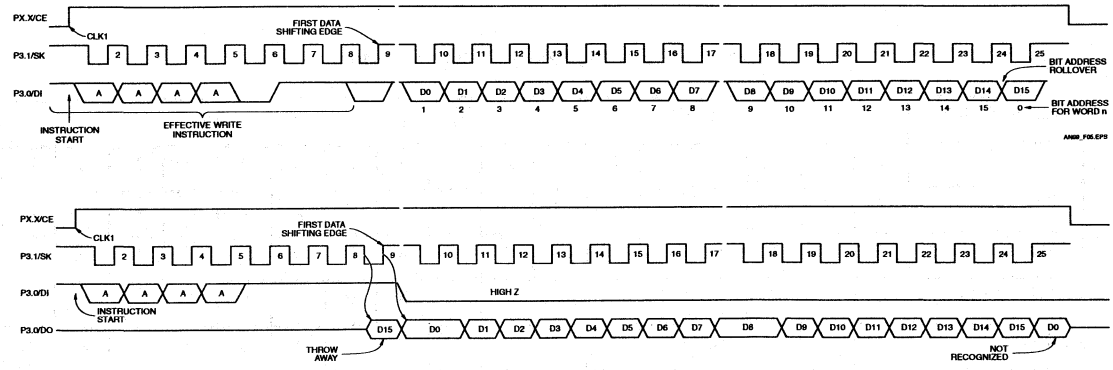

Figure 5. Read Cycle Sequence

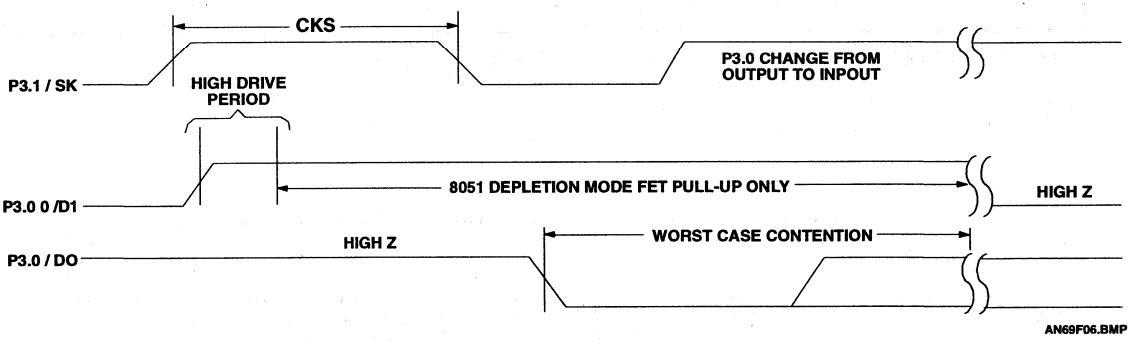

Figure 6. Worst Case Bus Contention

Recent Trends in Embedded Control Memory

by Cliff Ziltlaw, January 1991, Presented at WESCON 1991

Introduction

The proliferation of embedded controllers into new environments has led to a second generation of application specific memories. Memory manufacturers have developed devices with architectural and operational characteristics that address specific design requirements. The new devices complement or even replace on-board ROM, RAM, or E^2PROM memories found with most microcontrollers.

This paper will briefly describe several memory families suited to specific embedded control environments and then focus on a "controller-specific" E^2PROM device recently released by Xicor Inc.

Memory Overview

SERIAL MEMORIES: The majority of controllers sold for embedded applications are ROM based and offer different densities of on-board RAM and E^2PROM for data storage. Off-board serial memories often provide a more cost effective solution than designing in a controller with extended on-board data memory. Serial memories based on E^2PROM, ferro-electric, SRAM, or DRAM technology are now available with features tailored to specific environments.

Most serial devices provide an interface to one of the standardized serial busses offered on many microcontrollers. These standard busses provide an effective means of moving data back and forth between the microcontroller and a serial memory. Three of the more popular busses include the MICROWIRE™ bus (National Semiconductor), SPI bus (Motorola), and the I^2C bus (Philips Semiconductor).

If a standardized bus is not available, general purpose I/0 port lines can be used to communicate with a serial device. This implementation uses software to emulate the bus protocol. While there is added software overhead, this is the only method possible when a controller without a standardized serial port is used.

Portable applications are demanding that components consume less current and operate at lower voltages. Therefore, many manufacturers are offering devices that operate at supply levels of 3V or below and consume less than 1mA of current when in active mode.

EMERGING TECHNOLOGIES: Two technologies that have recently been introduced may have a place in embedded control environments.

Ferro-electrics offer many of the nonvolatile storage features provided by E^2PROMs and battery backed SRAMs. While process development is still underway, ferro-electrics should eventually become a significant technology for nonvolatile memory devices.

A new twist on E^2PROM technology has led to the development of a device capable of storing analog signals. Each bit in these E^2PROMs store an analog level instead of the "1" or "0" stored in traditional memory devices. This new family of devices is well suited to applications where analog data logging is to be performed.

HIGH SPEED MEMORIES: High performance products, such as laser printers, are using controllers with processing capabilities unheard of a few years ago. These high performance applications require much more sophisticated memories than those used by traditional microcontrollers. Parallel EPROM devices with cache-like features have emerged to keep up with the requirements of newer high performance controllers.

DATA AND PROGRAM STORAGE: ROM-less controllers operate by accessing off-chip program memory stored in parallel memory devices. External memory requirements include program and often data storage. Recently introduced E^2PROM based products address the needs of both program and data

storage in low-end controller environments. The X88C64 from Xicor, Inc. provides E²PROM program and data storage for microcontrollers in a single package.

External Memory for Microcontrollers

The time and expense required to implement program changes in ROM based microcontrollers often makes external program memory an attractive alternative. EPROM based controllers are available at a substantial price increase but they do not address applications where additional data storage is required. In situations where on-board data memory is inadequate, an interface to external memory becomes a design requirement. Therefore, most 8-bit microcontrollers offer the ability to access off-board memory for program and data storage. An external memory interface is implemented by redefining I/0 ports as the address, data, and control busses.

Microcontrollers with the ability to access external memory usually have a multiplexed address and data bus to reduce the number of pins required for the external interface. Figure 1 shows how an EPROM can be interfaced to a microcontroller to increase program storage. The implementation shown effectively increases the program and permanent data storage of the circuit, but does not change the amount of programmable data memory.

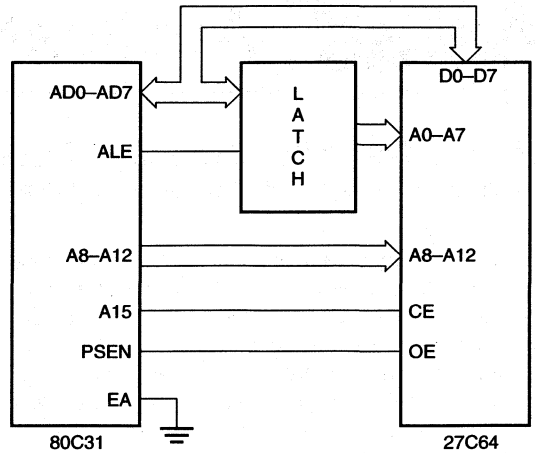

Figure 1. External Memory Configuration

To increase the amount of alterable data storage, a second memory device must be added as shown in Figure 2. E²PROMs are often chosen for data storage due to their nonvolatile characteristics. The addition of programmable data storage can be implemented by using a parallel device, as shown, or with a serial E²PROM.

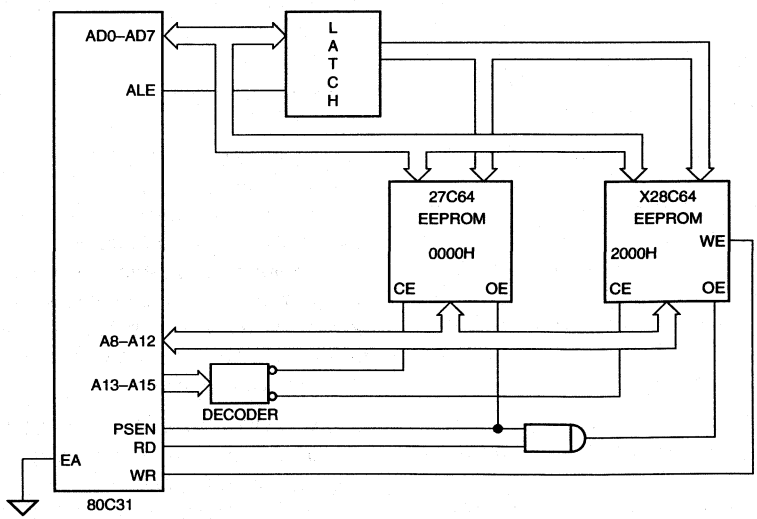

Figure 2. Two External Memory Devices

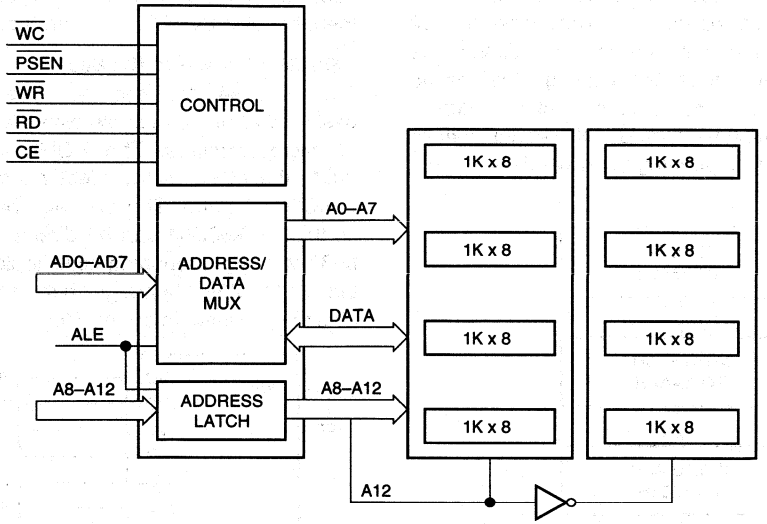

Figure 3. X88C64 Functional Block Diagram

One advantage of using a parallel device is that part of the program code can reside in E^2PROM, which allows for in-circuit program updates. However, one of the problems that must be solved when using E^2PROMs for program storage is that during a programming cycle, taking up to 10ms, data cannot be read from the device. Because data cannot be read during an E^2PROM write cycle, processor fetches must take place from a second memory device. The lack of a "read during write" feature makes it awkward or often impossible for a traditional E^2PROM to be used as the only external memory device.

X88C64 Description

To solve the "read during write" dilemma, Xicor developed the X88C64. The X88C64 is the first in a family of devices offered by Xicor that are designed specifically for microcontroller environments. Figure 3 shows the block diagram of the X88C64. The X88C64 provides an architecture consisting of 2 independent 4K x 8 E^2PROM memories. Because each half plane is independent of the other, a write cycle can take place in one plane while opcode fetches are being performed from the opposite plane. The ability to read while a write is taking place is a unique feature that allows the X88C64 to fill the external program and data requirements in many microcontroller applications.

Most microcontrollers provide a multiplexed address and data bus to reduce the number of pins required for an external memory interface. The X88C64 supports this multiplexed bus structure by latching an address when the ALE input makes a HIGH to LOW transition and transferring data while ALE is LOW. The multiplexed bus feature eliminates the need for the external address latch required when a traditional byte-wide (parallel) memory is used.

The ability to ensure data integrity in an E^2PROM has been a design concern for as long as E^2PROMs have been available. Inadvertent writes during power-up and power-down are especially difficult to prevent in microcontroller based environments. The X88C64 provides 2 different software methods of ensuring that inadvertent writes do not occur.

The first method required a 3-byte write sequence to occur immediately before new data is written into the X88C64 (Figure 4). This method is similar to the industry standard Software Data Protection (SDP) algorithm used on newer generation E^2PROM devices. Each write operation in the 3-step sequence uses a different address/data combination. This unique combination of writes to the device before

data is transferred, virtually eliminates the possibility of inadvertent write operations. The state of A12 defines where data will be written during the SDP/data transfer sequence. Having A12 define which plane is to be written means that the address sequence used during the 3-step SDP sequence must be modified slightly depending upon which half plane is being altered.

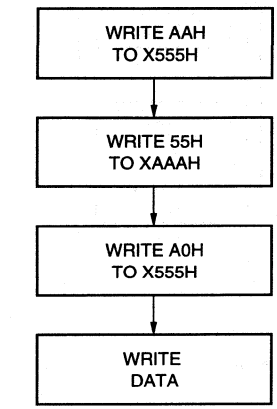

Figure 4. SDP Sequence

A second level of Software Data Protection has been provided with the nonvolatile Block Protect register (BPR). The BPR is an internal byte of E^2PROM memory, with each bit controlling the write protect status of one of the eight 1K x 8 blocks. While a block is protected, the data in that segment can no longer be changed. If a protected block needs to be modified, its write protect bit in the BPR must first be reset before the block can be written.

Modifying the BPR is performed with a 6-byte sequence similar to the SDP sequence described earlier. Each bit in the BPR controls the write status in a different 1K x 8 block. Bit 0 controls the write protect status of addresses 0000H-03FFH, bit 1 controls addresses 0400H-07FFH, etc.

In addition to the software controlled write protect mechanisms on the X88C64, a hardware write control pin (WC) has been provided. Writes to the X88C64 will be inhibited while the WC input is held at a HIGH level. If a write cycle is in progress when the WC pin goes HIGH, the write will be allowed to complete and then the X88C64 will enter a protected state.

X88C64 Interface to the 8051

The X88C64 features an interface specifically designed to be compatible with the Intel 8051 family of microcontrollers. The ROM-less version of the 8051, the 8031, is the ideal microcontroller for an X88C64 interface. The interface has been designed so that an X88C64 can be directly connected to the 8031 with no supporting glue logic (Figure 5). The pins on the X88C64 are given the same names as the pins they connect to on the 8031.

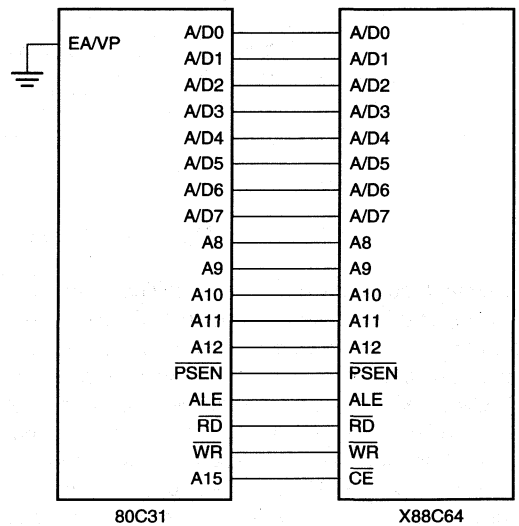

Figure 5. 80C31 and X88C64 Interface

The 8031 memory space is broken into separate program and data areas. Read/write data memory is accessible with the $\overline{WR}$ and $\overline{RD}$ outputs on the 8031. Program memory is read-only, with access controlled by the 8031 $\overline{PSEN}$ line. Direct in-circuit program modification is not possible because the 8031 does not provide any way to write to the program memory space. The traditional work-around, to allow writes into program space, uses glue logic to map a memory device into both the data and program spaces. The X88C64 maps both program and data memory into the same 8K x 8 address space to provide write capability to both memory spaces. Because of the dual plane architecture, program execution can continue out of one plane while a write is done in the

other plane. This Concurrent Read Write™ feature makes the X88C64 an ideal choice when in-system program updates are required.

The multiplexed address/data bus interface on the X88C64 is designed to connect directly to the 8031. Data transfer protocols on the AD lines and the ALE polarity match the requirements of an 8031. The X88C64's multiplexed bus eliminates the external address latch required when traditional byte-wide memories are used.

If the 8K x 8 E^2PROM density of the X88C64 is adequate for external memory requirements, the interface to an 8031 requires no glue logic. The $\overline{CE}$ input is connected to the A15 pin of the 8031, which maps the X88C64 into the memory space between 0000H and 1FFFH. All other pins are connected directly to the pins with the same names on the 8031. This 2-chip solution provides all of the functionality of the 6-chip circuit shown in Figure 2.

The reduced parts count made possible by the X88C64 provides several advantages over the multichip external memory configuration. The most obvious advantage is that circuit complexity decreases as the number of devices decreases. A second improvement is in the reduced printed circuit board space required to implement similar circuit functions. Manufacturing rework rates should drop as the number of devices on a PCB goes decreases. System reliability will also be improved because there are fewer components to fail on the PCB. The advantages provided by the X88C64 make it an attractive alternative to byte-wide memories in ROM-less controller applications.

Conclusion

As microcontrollers proliferate into new environments, niches will continue to develop for peripheral memory devices to support specific design requirements. Memory manufacturers are becoming increasingly responsive to the application requirements of the embedded control market. This trend will quite possibly continue until traditional byte-wide memories are displaced by devices targeted at specific microcontroller environments.

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Implement a Nonvolatile Latch with E²POTs

by Cliff Zitlaw, January 1993

Many applications exist for nonvolatile event detection circuits. Circuits needing to sense an over/under-voltage condition often must remember that an event occurred, even after a power-down has taken place. These applications typically use latching relays when the input is automated, or switches when manual input is appropriate. Both latching relays and switches are forms of nonvolatile memory that can often be replaced with the circuit described here.

The circuit shown in Figure 1 demonstrates how the 32-tap X9313 E²POT can be configured to act as a single-bit nonvolatile latch. Any HIGH to LOW transition on the event detect input will change the output of the circuit to the HIGH state. This event detect input can be driven by a switch, as shown, or by the output of a transducer circuit. A manual reset is provided to allow the circuit to be returned to the LOW state.

The circuit is designed around the X9313 nonvolatile digital potentiometer, but other Xicor E²POTs could be used. This device stores the "state" of the circuit by moving the wiper from one end of the potentiometer to the other. With the wiper moved to V_H, the circuit outputs a logic "1", and when the wiper is moved to V_L, a logic "0" is output. Once the wiper has been moved from one end of the resistor array to the other, the wiper position is stored in a nonvolatile E²PROM register. Moving the wiper is accomplished with a circuit that uses a Schmitt-triggered inverter and several discretes. The driver circuitry assures that when a HIGH to LOW transition occurs at the event detect input, the wiper of the X9313 will move from tap position 0 to tap position 31. Much of the circuitry is used to generate a one-shot pulse that allows the $\overline{CS}$ and $\overline{INC}$ pin circuitry to move the wiper through full-scale.

This provides a cost effective method of implementing a nonvolatile latching function, using a low cost E²POT and a little bit of "glue" circuitry. The circuit can be especially attractive when an expensive micro-controller implementation cannot be justified.

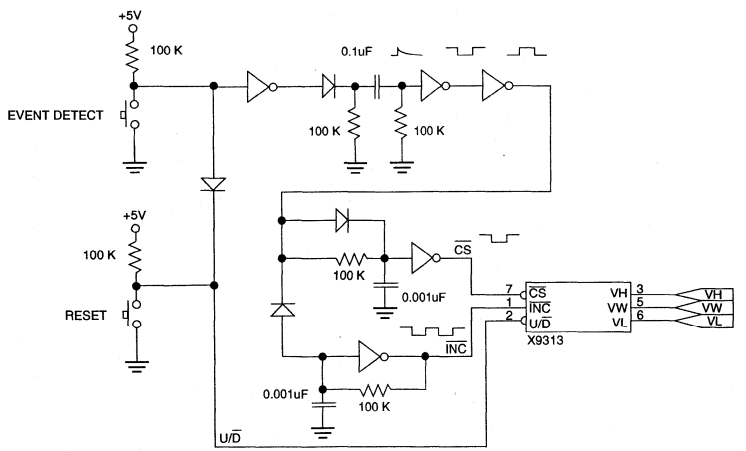

Figure 1. Schematic for the Nonvolatile Latch

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Serialization using Small E²PROMs

by Mark Rutledge, June 1992

Introduction

One of the most common applications for small serial E²PROMs is for the solid state storage of serial numbers in microcontroller/microprocessor based systems. These devices are ideal for such applications because they are easily programmable, very small in physical size, and are very low cost. Moreover, by taking advantage of the features offered by E²PROMs, many other types of logistical data can be stored that cannot be accomplished with other serialization methods such as labels, bar codes, imprints, etc. Xicor offers three products which are ideally suited for these applications, the X24C00, X24001, and X24C01.

Why E²PROM?

The advantages of E²PROM over other methods of serializing circuit boards or enclosed units are numerous. The assignment process is easier, there is more versatility offered by the retrieval process, and the entire system can be more secure.

The serial number and other logistical information can be written to the E²PROM at any time in the manufacturing process. It can be written at any test step by Automatic Test Equipment or into the component prior to board insertion. In addition, the X24001 device can be programmed by Xicor prior to shipment.

The use of solid state devices also expands the capabilities for data retrieval because the data does not have to be seen or scanned. Information can be read and recorded from test equipment (such as a bed-of-nails tester or a PC) in a factory environment. The integrity of the units need not be violated as the data can be extracted via the connector without having to open the unit. The unit need not be brought back to the factory or service location as the data can be retrieved over existing communication links such as a modem, RF link, or remote PC. None of these things can be accomplished with bar-codes, labels, or imprinting.

A solid state method of storing logistical data is also more secure than other methods. Information cannot be stripped-off or altered without intelligence and insight into the inner workings of the system. In systems where a serialized unit is designed to interface with another unit, serial or ID numbers can be made to match, before the unit will function properly. This could make the unit, such as a car radio, inoperable if stolen or used with system components that were improperly obtained.

Standard Implementation

The most common application is to simply store a serial number or a device ID number where each unit must have a unique "address" or identifier, such as LAN applications. Devices such as the X24C00 and X24001 are ideal for these applications due to their size and cost. Both devices are 128 bits in density, internally configured as 16x8.

The X24001 is especially well suited to this application because it provides an added security level for the data. The X24001 operates from a standard 5V supply and can be read at 5V like any other serial E²PROM. However, the data line must be raised to 12V to perform a write operation. This ensures that the E²PROM could not be modified in a 5V-only system and could only be modified in a laboratory environment where 12V can be applied.

Additional Capabilities

Most serial numbers and ID numbers take up only 5 to 10 bytes of memory. The remaining memory in the serial device can be used for many additional things. A circuit board revision letter could be stored in one byte. A software version identifier could be stored in another one or two bytes. A data code for manufacturing date, final test date, ship date, etc. could be stored in four bytes. Memory can also be allocated for future usage, such as repair history, modification upgrade logs, and so on. Each of these entries can be defined such that only a few bytes are used.

For these applications, where the E^2PROM device contains more than a serial number and revision letter, a device larger than the 16-byte X24C00 or X24001 becomes necessary. Xicor offers a low cost serial E^2PROM at the 1K-bit density, the X24C01 which is internally configured as 128x8. If still more memory is required, 2K-bit, 4K-bit, 8K-bit, and 16K-bit devices are available with similar features.

Reliability Enhancements

The serial E^2PROM can also be used to help monitor the reliability of the overall unit. Locations can be allocated as counter registers which are updated whenever a particular event occurs. These can include power cycles, whether a particular button was pushed or a specific mode entered, etc. Data from these locations may provide clues to a repair/maintenance center and provide information about what the common causes of system failures are or where the "weak links" are. In an age where quality is paramount, this type of data is extremely valuable.

Memory Map

Here is an memory map example for a X24C00/X24001-type device which is used to store standard logistical data:

Location	Data
00H-09H	10-digit serial number
0AH	Hardware revision level
0BH	Software revision level
0CH-0DH	Manufacturing date - work week
0EH-0FH	Manufacturing date - year

Here is an memory map example for a X24C01-type device which is used for standard logistical data plus historical reliability monitoring data.

Location	Data
00H-1FH	Modification/upgrade log (six bytes per entry) -one byte for type of modification -four bytes for date code -one byte for how implemented
20H-4FH	Repair/maintenance log (six bytes per entry) -four bytes for date code -one byte to identify performing entity -one byte for activity type
50H-5FH	Reliability monitoring information (one byte registers)
60H-69H	10-digit serial number
6AH	Hardware revision level
6BH	Software revision level
6CH	Test procedure revision
70H-71H	Manufacturing date - work week
72H-73H	Manufacturing date - year
74H	Manufacturing location
75H-76H	Operator/line code
77H-7BH	Customer code

Summary

This applications note has shown the versatility that a serial E^2PROM would provide for the storage of logistical information. These devices can be thought of as permanent routers for the circuit boards or units in which they are used. These serial E^2PROMs also provide capabilities that cannot be provided as cost effectively when using other methods.

Improving Analog Signal Monitors with E²POTs

by Mark Rutledge, July 1994

Introduction

This application note describes a unique implementation for the Xicor X9241 E²POT in a process control or process monitoring environment. This implementation is made possible by some of the features of X9241, many of which have not been available on E²POT devices prior to the introduction of the X9241.

Implementation

Imagine a process control system or any other system where an analog voltage from a transducer needs to be monitored. The ideal method of monitoring such signals is to have an "alarm" in place for when the signal drifts out of its acceptable operating range, and to have the absolute value of the signal accessible to the processor so that intelligent decisions can be made about how to address the new condition. There are several ways of accomplishing this task using A-to-D converters, resistor-divider networks, or similar techniques, but these solutions prove to be messy and/or costly.

Imagine achieving the requirements of the ideal monitor with nothing more than a potentiometer and a comparator! The potentiometer is used to set a reference voltage which will become the trip point at which an "alarm" is generated (Figure 1). A simple comparator is used to compare the reference voltage to a transducer output voltage. The comparator output is then used to signal the processor by means of an interrupt. The missing element is the means to read the value of the transducer voltage. This can be done by implementing an A-to-D converter, but this adds cost and complexity. A variable voltage reference is still required, which the A-to-D converter cannot provide. By using the X9241 Quad E²POT as the precision reference voltage potentiometer, the transducer voltage can be determined without adding any other components!

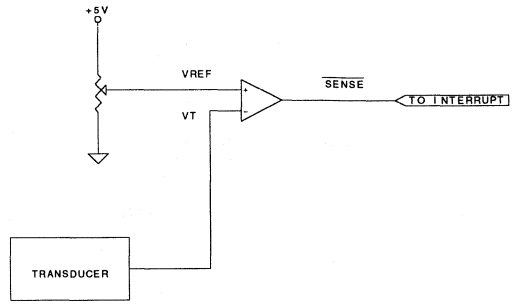

Figure 1.

The key to this scheme is a feature of the X9241 that allows direct reading of the contents of the Wiper Counter Registers (WCRs). Each of the four potentiometers on the X9241 has a WCR which contains the numeric position of the corresponding wiper. The processor can read the digital contents of the WCR via a 2-wire serial communications bus and, if necessary, easily calculate the actual wiper voltage. By adjusting the X9241 and reading the I/O bit assigned to the comparator output (after first disabling the interrupt!), the E²POTs wiper voltage is matched to the transducer voltage, which can be determined by reading the contents of the WCR (Figure 2). The reference wiper setting (or the trip point setting) is not lost since it had previously been stored in one of the E²POT's four nonvolatile data registers (R0-R3). The contents of the desired data register can be transferred into the WCR by giving the appropriate software command. The interrupt is then enabled to resume monitoring.

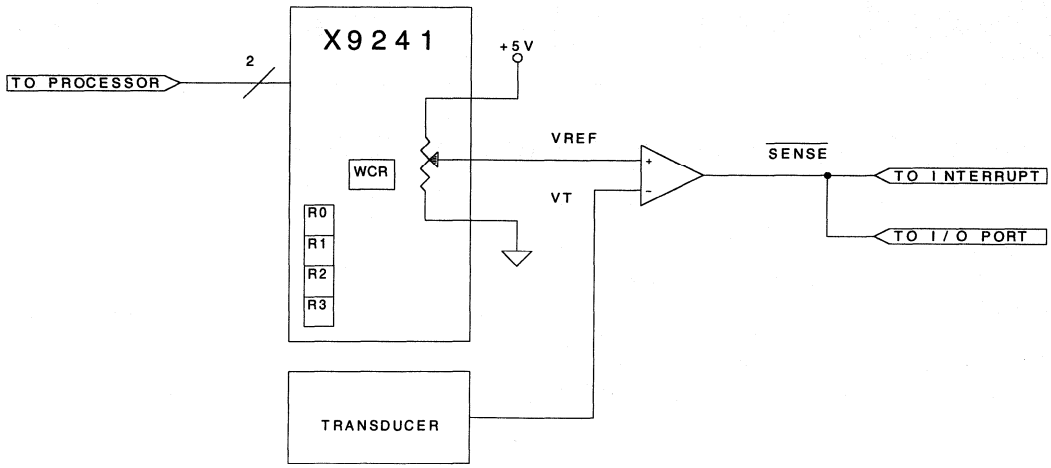

Figure 2. Smart Monitor using X9241 Quad E²POT

System Calibration

Calibration of the transducer and A-to-D conversion process can be easily achieved by storing the required constants in system memory and having the system processor perform the appropriate calculation. In this manner the total system is calibrated rather than calibrating the transducer and A-to-D converter individually.

Reference Voltage Resolution

The X9241 consists of four potentiometers with 63 resistive elements each, giving each potentiometer 64 steps or wiper positions. The resolution would thus be 1/63 or approximately 1.59%. The X9241 feature set includes a cascade mode where adjacent potentiometers can be connected in series, and the extra wipers disabled, resulting in potentiometers of 127, 190, or 253 steps with internal wiper transitions, allowing resolution levels of 0.79%, 0.53%, or 0.40% respectively. If higher resolution is required, vernier cascading techniques can be used. For a method of increasing resolution, see Xicor application note AN43 "Software Implements a High Resolution Nonvolatile Digital Potentiometer".

Application Example

Let's say that a liquid or chemical used in a process must be at least +65°C for the process to yield the desired results. The reference voltage is initially calibrated by adjusting the E²POT, so that its wiper voltage is the next increment below the actual voltage of the transducer at +65°C. The WCR contents are then stored into the desired E² register, (R0-R3.) If the temperature of the liquid drops below +65°C, the comparator changes state and an interrupt is generated. The processor can then adjust the potentiometer until the comparator output changes state again, at which point the WCR contents can be read to find the new transducer voltage level. The processor can then make a decision about what has happened. If the temperature had drifted a couple of degrees below +65°C, then warming heaters can be switched on (or intensity increased) to return the liquid to +65°C. The process can then continue uninterrupted and the event can be logged into the system's E²PROM or NOVRAM memory for future analysis. However, if the voltage read indicates a temperature dramatically below +65°C, then the process can be shut down and the appropriate "alarm" activated. This monitor can easily be set-up to maintain an operating window, for example +65°C ±1°C, by using dual comparators.

Conclusion

The advanced features of the X9241, especially the direct read capability of the WCRs, allow the user to simplify monitor controls by having a device that functions both as a variable reference voltage and an A-to-D converter. Additionally, the X9241 allows total

system calibration since correction factors may be stored in system memory and combined with the contents of the WCR as required for calibration. The 128-bits of nonvolatile memory in the data registers may be used for other purposes, if all four data registers are not required for use in transducer monitoring. The X9241 thus offers the user a simple, low cost, yet quite versatile solution for intelligent process monitoring and control.

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Xicor®

3807-2.3 12/4/95 T12/C0/D0 NS

Die Products

FEATURES

- **High Performance Advanced CMOS Technology**
- **0°C to 70°C Operating Temperature**
- **100 Year Data Retention**
- **95% Yield Excluding Assembly Related Losses**
- **Commercial Data Sheet Parameters (except input levels)**
- **Die Visually Inspected to MIL-STD-883, T/M 2010 Condition B**
- **Optional Die Element Evaluation per MIL-STD-883,T/M 5008, Class B**

DESCRIPTION

Xicor die products are fabricated with Xicor's Advanced CMOS Floating Gate technology. Like all Xicor programmable nonvolatile memories, they are 5V only devices.

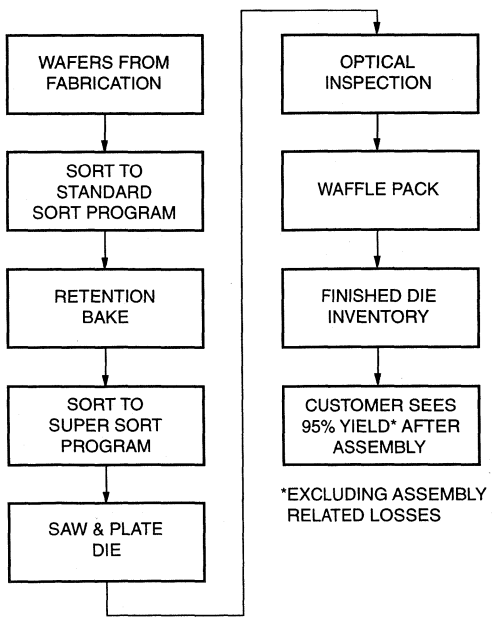
Xicor die products are designed and tested for applications requiring extended endurance. Data retention is specified to be greater than 100 years.

Products to be shipped in die form follow the flow shown below. This insures a 95% yield (excluding assembly related losses) to the commercial data sheet. The slowest datasheet access time is guaranteed. All A.C. parameters and D.C. parameters except input and output voltages are guaranteed.

For military applications, Xicor now offers die with element evaluation testing per MIL-STD-883. A description of the element evaluation testing can be found on the following page.

Bonding diagrams, die size/thickness and other information required for use of die can be obtained from your local Xicor sales representative.

TEST FLOW



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DIE ELEMENT EVALUATION

Test samples shall be taken from the same wafer lot as the production die, assembled and tested to the die element evaluation as specified in paragraph 3.2 of Test Method 5008, MIL-STD-883, Class B.

Subgroup	Test	Test Method	Quantity (Accept No.)
1	Internal Visual	2010, Condition B	10 (0)
2	Final Electricals[1]	Per Applicable Device Specification	10 (1)
3	Wire Bond Evaluation	2011, Condition C or D	10 (0) wires or 20 (1) wires

Notes: (1) Final Electricals to be performed at customer's specified temperature range.

DIE ORDERING INFORMATION

When ordering, please specify die in waffle pack or die in wafer form.

Part number suffix: H = Die in waffle pack
W = Die in wafer form

Xicor®

3807-2.3 12/4/95 T12/C0/D0 NS

Xicor Military Program Overview

INTRODUCTION

Xicor, Inc. is committed to supplying products that meet the demands of the Military and High Reliability marketplace. Xicor's high performance Textured Poly Floating Gate (TPFG) and Direct Write™ cell offer an intrinisic reliability, when combined with the screening requirements of MIL-STD-883 produces an extremely enhanced product.

The Xicor Quality Assurance Program has been designed to be carried out by all employees in order to maintain the highest standards in producing these products. The backbone of the system is a self-auditing SPC program that has been implemented throughout the company. This program influences product definition, product design, testability criteria, fabrication process, and final test philosophies.

Every Xicor product is designed to meet or exceed 100% functionality over the full military temperature range. This attention to detail in design has lead to the manufacture of the only floating gate 5V, byte alterable memories qualified for use by the oil industry in down hole drilling operations at 170°C for both read and write operations. In addition, Xicor's continued exploitation of its proprietary TPFG technology has allowed it to maintain a generation lead in die size for all product densities.

MIL-STD-883 and SMD Products

Xicor offers two different military category products. Most Xicor products are available with processing 100% compliant to paragraph 1.2.1 of MIL-STD-883. Secondly, a large number of products are available to the SMD (Standardized Military Drawing) program administered by DESC. These products are not only fully compliant with MIL-STD-883 but they are also screened to the electrical requirements set forth in the individual SMDs.

ADDITIONAL DATA AND SERVICES

Source Control Drawings

Customers may provide source control drawings for Xicor review and quotation. To reduce overall product cost to the customer and to assure full compliance with the requirements of MIL-STD-883, Xicor will, on occasion, respond with waiver requests. Xicor must review and accept a customer source control drawing prior to acceptance of an order. Orders to SCDs must be placed directly with the factory to assure compliance. A customer may, however, purchase standard Xicor product with REFERENCE ONLY to the SCD either directly from the factory or through one of Xicor's franchised distributor locations.

Quality Conformance Inspection Data

QCI Groups A and B are performed on each lot of devices as standard procedure for all MIL-STD-883 products. This data is available to the customer and should be requested at the time of quotation to insure its shipment with the product.

Generic QCI data for Groups C and D which qualify the product being shipped is also available.

Attributes data (copies of the the lot travelers) are also available for customer purchase. This requirement should be so noted prior order placement.

Customer Source Inspection

Customer Source inspection may be performed at final ship point at Xicor. This requirement must be specified and quoted prior to or placement. The standard source inspection is comprised of the following:

- Group A testing: Sample size based on Table I Method 5005 MIL-STD-883 and LTPD values in Table D-1 Appendix D of MIL-I-38535.
- Documentation review of all travelers, drawings and purchase orders.

The following sections contain: detailed screening and test methods performed for all MIL-STD-883 compliant products; reference tables listing compliant Xicor products, a SMD to Xicor part number cross reference table, a description of Xicor's Military Die Program and a white paper discussing the decassification procedures for Xicor's E^2PROMs.

MIL-STD-883 FLOWS

ASSEMBLY, ENVIRONMENTAL AND FINAL TEST SCREENING METHODS

Screen		Test Method	Application
Internal Visual		2010, Condition B	100%
Temperature Cycling		1010, Condition C	100%
Constant Acceleration (Centrifuge)		2001, Condition E, Y-Axis	100%
Seal:	Fine	1014, Condition A or B	100%
	Gross	1014, Condition C	100%
External Visual		2009	100%
Pre Burn-In Electricals		As Applicable	100%
Burn-In		1015, Condition D, Class B	100%
Post Burn-In and Final Electricals(1)		Per Device Data Sheet	
Static Tests		Subgroups 1, 2, 3	100%
Functional Tests		Subgroups 7, 8A, 8B	100%
Switching Tests		Subgroups 9, 10, 11	100%
Dynamic Tests		Subgroup 4 (Method 3012)	Periodically Tested
Solder Dip Lead Finish (As Applicable)		MIL-I-38535, Paragraph 30.5.6.3.4	100%
Seal:(2)	Fine	1014, Condition A or B	Sample
	Gross	1014, Condition C	Sample
External Visual		2009	100%
Quality Conformance Inspection (3)		5005, Class B	Sample

Notes: (1) Percent defective allowable (PDA) is 5% (Subgroups 1 and 7) for each lot.
(2) Sample tested in accordance with Method 5004.
(3) Sample tested in accordance with Class B requirements for Groups A, B, C and D.

QUALITY CONFORMANCE INSPECTIONS, METHOD 5005

The following Tables illustrate the Groups A, B, C and D Tests, Test Methods, Conditions and frequency of testing for all qualified products.

TABLE 1. GROUP A ELECTRICAL TESTS (Performed on each lot or sublot)

Test	Subgroup	LTPD*
Static Tests at +25°	1	116/0
Static Tests at +125°C	2	116/0
Static Tests at –55°C	3	116/0
Functional Tests at +25°C	7	116/0
Functional Tests at +125°C	8A	116/0
Functional Tests at –55°C	8B	116/0
Switching Tests at +25°C	9	116/0
Switching Tests at +125°C	10	116/0
Switching Tests at –55°C	11	116/0

TABLE 2. GROUP B ASSEMBLY INTEGRITY TESTS (Performed on each lot)

Test	Test Method	Conditions	LTPD*
Subgroup 2 Resistance to Solvents	2015	Top and Bottom Mark	3/0
Subgroup 3 Solderability	2003	Solder Temperature: +245°C ±5°C	22/0
Subgroup 5 Bond Strength	2011	Condition D	15/0

TABLE 3. GROUP C DIE RELATED TESTS (Performed periodically per MIL-STD-883, paragraph 1.2.1)

Test	Test Method	Conditions	LTPD*
Subgroup 1 Steady State Lifetest Endpoint Electricals	1005	Condition D Subgroups 1, 2, 3, 7, 8, 9, 10, 11 Per Applicable Device Specification	45/0

*LTPD=Quantity/Accept Number

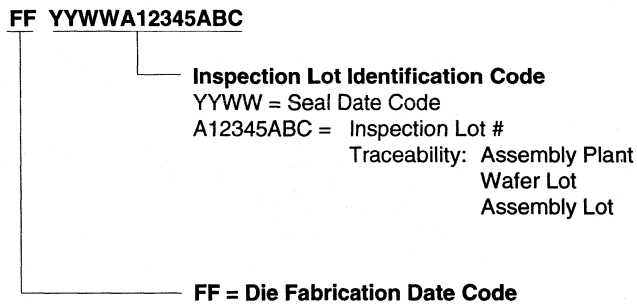
TABLE 4. GROUP D PACKAGE RELATED TESTS (Performed periodically per MIL-STD-883, paragraph 1.2.1)

Test	Test Method	Conditions	LTPD*
Subgroup 1			15/0
Physical Dimensions	2016	Per MIL-M-38510, Appendix C	
Subgroup 2			45/0
Lead Integrity	2004	Condition B2, Lead Fatigue	
Seal: Fine	1014	Condition A or B	
Gross	1014	Condition C	
Subgroup 3			15/0
Thermal Shock	1011	Condition B, 15 Cycles	
Temperature Cycling	1010	Condition C, 100 Cycles	
Moisture Resistance	1004	10 Cycles	
Endpoint Electricals	5005	Subgroups 1, 2, 3, 7, 8, 9, 10, 11	
Seal: Fine	1014	Condition A or B	
Gross	1014	Condition C	
Visual Examination	1010 and 1004		
Subgroup 4			15/0
Mechanical Shock	2002	Condition B, 1.5 kg at 0.5 ms	
Variable Frequency Vibration	2007	Condition A, 4 Cycles X, Y, & Z	
Constant Acceleration	2001	Condition E, 30 kg, Y1	
Seal: Fine	1014	Condition A or B	
Gross	1014	Condition C	
Visual Examination	1010		
Endpoint Electricals		Subgroups 1, 2, 3, 7, 8, 9, 10, 11 Per Applicable Device Specification	
Subgroup 5			15/0
Salt Atmosphere	1009	Condition A, 24 Hours	
Seal: Fine	1014	Condition A or B	
Gross	1014	Condition C	
Visual Examination	1009		
Subgroup 6			3/0
Internal Water Vapor Content	1018	5000 ppm at 100°C	
Subgroup 7			15/0
Adhesion of Lead Finish	2025	(LTPD Applies to Leads)	
Subgroup 8			5/0
Lid Torque	2024	Glass Frit Seal Packages Only	

*LTPD = Quantity/Accept Number

TOPSIDE MARK

The topside mark of each MIL-STD-883 compliant device provides complete wafer lot, assembly and inspection lot traceability. This marking appears as an alphanumeric code as shown below:

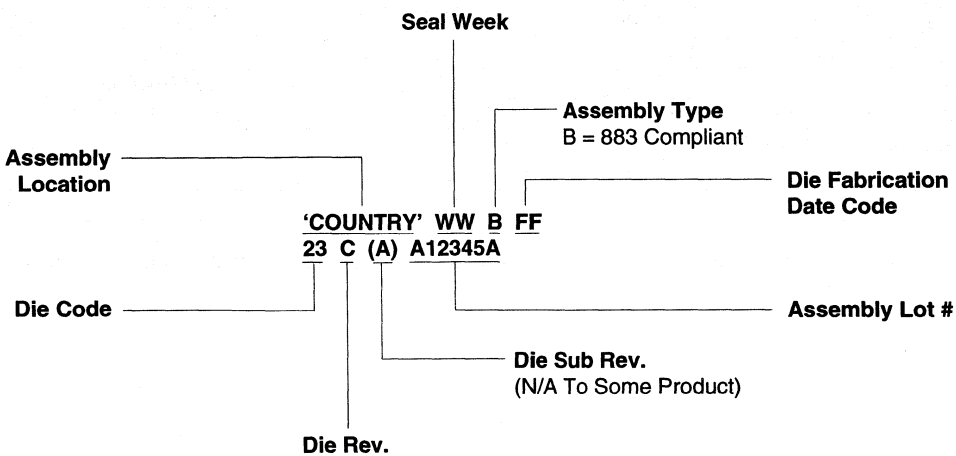


In addition, the following items will appear as part of the topside marking:
- Xicor Logo
- Xicor CAGE Code Number: 60395
- MIL-STD-883 Compliance Indicator: C
- ESD Identifier: ▽

Notes: On some packages, either the Xicor Logo *or* the CAGE Code number will apear, but not both.

BACKSIDE MARK

The backside mark provides wafer lot and assembly lot traceability. This appears in an alphanumeric code as follows:



MIL-STD-883 PRODUCT LISTING

Xicor Part Number	Organization	Speeds*	Package Style and Lead/Pin/PAD Count				SMD Number	Page Number
			CERDIP	LCC	FLATPACK	PGA		
NOVRAMs								
X22C10	64 x 4	120ns	18					1-1
X22C12	256 x 4	120ns	18					1-11
X20C04	512 x 8	200ns	28	32				1-21
X20C05	512 x 8	35ns	28	32				1-33
X20C16	2K x 8	35ns	28	32				1-47
Serial NOVRAMs								
X24C44	16 x 16	0–1MHz	8					2-1
X24C45	16 x 16	0–1MHz	8					2-13
Serial E²PROMs								
X24C04	512 x 8	0–100KHz	8				5962-89590	'92DB
X24C16	2K x 8	0–100KHz	8				5962-89667	'92DB
E²POT Digitally Controlled Potentiometer								
X9241	2/10/10/50KΩ	100KHz	20				5962-95525	4-69
X9C102	1KΩ	250KHz	8					4-1
X9C103	10KΩ	250KHz	8					4-1
X9C104	100KΩ	250KHz	8					4-1
X9C503	50KΩ	250KHz	8					4-1
5 Volt, Byte Alterable E²PROMs								
X28C64	8K x 8	150–250ns	28	32	28	28	5962-87514	3-25
X28HC64	8K x 8	55–120ns	28	32	28	28		3-41
X28C256	32K x 8	150–300ns	28	32	28	28	5962-88525	3-57
X28HC256	32K x 8	70–120ns	28	32	28	28	5962-88634	3-73
X28C512	64K x 8	120–250ns	32	32	32	36	5962-90869	3-105
X28C513	64K x 8	120–250ns		32			5962-90869	3-105
X28C010	128K x 8	120–250ns	32	32	32	36	5962-38267	3-147
Microcontroller Peripheral Memory								
X88C64	8K x 8	120ns	24	32				5-51
X68C64	8K x 8	120ns	24	32				5-1

* Speeds for parallel access devices is tAA in ns; for serial devices speed is min. to max. clock rate in Hz.

Standardized Military Drawing (SMD) Numeric Cross Reference Guide

SMD Number	MIL-STD-883 Part Number	Package Style	Page Number	Product Description
5962-3826701 MUX[1]	X28C010EMB-25	32 LCC	3-147	
5962-3826701 MXX	X28C010DMB-25	32 CERDIP	3-147	
5962-3826701 MZX	X28C010FMB-25	32 FLATPACK	3-147	
5962-3826703 MUX	X28C010EMB-20	32 LCC	3-147	
5962-3826703 MXX	X28C010DMB-20	32 CERDIP	3-147	**128K x 8**
5962-3826703 MZX	X28C010FMB-20	32 FLATPACK	3-147	**5V**
				Byte
5962-3826705 MUX	X28C010EMB-15	32 LCC	3-147	**Alterable**
5962-3826705 MXX	X28C010DMB-15	32 CERDIP	3-147	**E²PROM**
5962-3826705 MZX	X28C010FMB-15	32 FLATPACK	3-147	
5962-3826707 MUX	X28C010EMB-12	32 LCC	3-147	
5962-3826707 MXX	X28C010DMB-12	32 CERDIP	3-147	
5962-3826707 MZX	X28C010FMB-12	32 FLATPACK	3-147	
5962-8751403 XX	X28C64DMB-25	28 CERDIP	3-25	
5962-8751403 YX	X28C64EMB-25	32 LCC	3-25	
5962-8751403 ZX	X28C64FMB-25	28 FLATPACK	3-25	
				8K x 8
5962-8751404 XX	X28C64DMB-20	28 CERDIP	3-25	**5V**
5962-8751404 YX	X28C64EMB-20	32 LCC	3-25	**Byte**
5962-8751404 ZX	X28C64FMB-20	28 FLATPACK	3-25	**Alterable**
				E²PROM
5962-8751405 XX[2]	X28C64DMB-25	28 CERDIP	3-25	
5962-8751405 YX[2]	X28C64EMB-25	32 LCC	3-25	
5962-8751405 ZX[2]	X28C64FMB-25	28 FLATPACK	3-25	

1. UX = 32 PAD LCC for the 1Mbit Device
2. These devices are screeened for 100,000 write cycle endurance

LEGEND - SMD SUFFIX	
M = MIL-STD-883	XX = CERDIP
PX = CERDIP (8 Lead)	YX = LCC
UX = PGA	ZX = FLATPACK
VX = CERDIP (18 Lead)	

STANDARDIZED MILITARY DRAWING (SMD) NUMERIC CROSS REFERENCE GUIDE (Continued)

SMD Number	MIL-STD-883 Part Number	Package Style	Page Number	Product Description
5962-8852502 UX	X28C256KMB	28 PGA	3-57	
5962-8852502 XX	X28C256DMB	28 CERDIP	3-57	
5962-8852502 YX	X28C256EMB	32 LCC	3-57	
5962-8852502 ZX	X28C256FMB	28 FLATPACK	3-57	
5962-8852503 UX	X28C256KMB-25	28 PGA	3-57	
5962-8852503 XX	X28C256DMB-25	28 CERDIP	3-57	
5962-8852503 YX	X28C256EMB-25	32 LCC	3-57	
5962-8852503 ZX	X28C256FMB-25	28 FLATPACK	3-57	
5962-8852504 UX	X28C256KMB-20	28 PGA	3-57	
5962-8852504 XX	X28C256DMB-20	28 CERDIP	3-57	
5962-8852504 YX	X28C256EMB-20	32 LCC	3-57	
5962-8852504 ZX	X28C256FMB-20	28 FLATPACK	3-57	
5962-8852505 UX[3]	X28C256KMB-25	28 PGA	3-57	
5962-8852505 XX[3]	X28C256DMB-25	28 CERDIP	3-57	
5962-8852505 YX[3]	X28C256EMB-25	32 LCC	3-57	
5962-8852505 ZX[3]	X28C256FMB-25	28 FLATPACK	3-57	
5962-8852506 UX	X28C256KMB-15	28 PGA	3-57	
5962-8852506 XX	X28C256DMB-15	28 CERDIP	3-57	
5962-8852506 YX	X28C256EMB-15	32 LCC	3-57	**32K x 8 5 V Byte Alterable E^2PROM**
5962-8852506 ZX	X28C256FMB-15	28 FLATPACK	3-57	
5962-8852508 UX[3]	X28C256KMB-15	28 PGA	3-57	
5962-8852508 XX[3]	X28C256DMB-15	28 CERDIP	3-57	
5962-8852508 YX[3]	X28C256EMB-15	32 LCC	3-57	
5962-8852508 ZX[3]	X28C256FMB-15	28 FLATPACK	3-57	
5962-8852510 UX	X28C256KMB	28 PGA	3-57	
5962-8852510 XX	X28C256DMB	28 CERDIP	3-57	
5962-8852510 YX	X28C256EMB	32 LCC	3-57	
5962-8852510 ZX	X28C256FMB	28 FLATPACK	3-57	
5962-8852511 UX	X28C256KMB-25	28 PGA	3-57	
5962-8852511 XX	X28C256DMB-25	28 CERDIP	3-57	
5962-8852511 YX	X28C256EMB-25	32 LCC	3-57	
5962-8852511 ZX	X28C256FMB-25	28 FLATPACK	3-57	
5962-8852512 UX	X28C256KMB-20	28 PGA	3-57	
5962-8852512 XX	X28C256DMB-20	28 CERDIP	3-57	
5962-8852512 YX	X28C256EMB-20	32 LCC	3-57	
5962-8852512 ZX	X28C256FMB-20	28 FLATPACK	3-57	
5962-8852513 UX[3]	X28C256KMB-25	28 PGA	3-57	
5962-8852513 XX[3]	X28C256DMB-25	28 CERDIP	3-57	
5962-8852513 YX[3]	X28C256EMB-25	32 LCC	3-57	
5962-8852513 ZX[3]	X28C256FMB-25	28 FLATPACK	3-57	

3. These devices are screened for 100,000 write cycle endurance

STANDARDIZED MILITARY DRAWING (SMD) NUMERIC CROSS REFERENCE GUIDE (Continued)

SMD Number	MIL-STD-883 Part Number	Package Style	Page Number	Product Description
5962-8852514 UX	X28C256KMB-15	28 PGA	3-57	
5962-8852514 XX	X28C256DMB-15	28 CERDIP	3-57	
5962-8852514 YX	X28C256EMB-15	32 LCC	3-57	**32K x 8 5V Byte Alterable E^2PROM**
5962-8852514 ZX	X28C256FMB-15	28 FLATPACK	3-57	
5962-8852516 UX[3]	X28C256KMB-15	28 PGA	3-57	
5962-8852516 XX[3]	X28C256DMB-15	28 CERDIP	3-57	
5962-8852516 YX[3]	X28C256EMB-15	32 LCC	3-57	
5962-8852516 ZX[3]	X28C256FMB-15	28 FLATPACK	3-57	
5962-8863401 UX	X28HC256KMB-12	28 PGA	3-73	
5962-8863401 XX	X28HC256DMB-12	28 CERDIP	3-73	
5962-8863401 YX	X28HC256EMB-12	32 LCC	3-73	
5962-8863401 ZX	X28HC256FMB-12	28 FLATPACK	3-73	
5962-8863403 UX	X28HC256KMB-90	28 PGA	3-73	**32K x 8 5V Byte Alterable E^2PROM**
5962-8863403 XX	X28HC256DMB-90	28 CERDIP	3-73	
5962-8863403 YX	X28HC256EMB-90	32 LCC	3-73	
5962-8863403 ZX	X28HC256FMB-90	28 FLATPACK	3-73	
5962-8863405 UX	X28HC256KMB-70	28 PGA	3-73	
5962-8863405 XX	X28HC256DMB-70	28 CERDIP	3-73	
5962-8863405 YX	X28HC256EMB-70	32 LCC	3-73	
5962-8863405 ZX	X28HC256FMB-70	28 FLATPACK	3-73	
5962-8959001 PX	X24C04DMB	8 CERDIP	'92DB	**512 x 8 Serial E^2PROM**
5962-8966701 PX	X24C16DMB	8 CERDIP	'92DB	**2K x 8 Serial E^2PROM**

3. These devices are screened for 100,000 write cycle endurance

LEGEND - SMD SUFFIX	
M = MIL-STD-883	XX = CERDIP
PX = CERDIP (8 Lead)	YX = LCC
UX = PGA	ZX = FLATPACK
VX = CERDIP (18 Lead)	

STANDARDIZED MILITARY DRAWING (SMD) NUMERIC CROSS REFERENCE GUIDE (Continued)

SMD Number	MIL-STD-883 Part Number	Package Style	Page Number	Product Description
5962-9086901 MUX	X28C512KMB-25	36 PGA	3-105	
5962-9086901 MXX	X28C512DMB-25	32 CERDIP	3-105	
5962-9086901 MYX	X28C512EMB-25	32 LCC	3-105	
5962-9086901 MZX	X28C512FMB-25	32 FLATPACK	3-105	
5962-9086902 MUX[4]	X28C512KMB-25	36 PGA	3-105	
5962-9086902 MXX[4]	X28C512DMB-25	32 CERDIP	3-105	
5962-9086902 MYX[4]	X28C512EMB-25	32 LCC	3-105	
5962-9086902 MZX[4]	X28C512FMB-25	32 FLATPACK	3-105	
5962-9086903 MUX	X28C512KMB-20	36 PGA	3-105	
5962-9086903 MXX	X28C512DMB-20	32 CERDIP	3-105	
5962-9086903 MYX	X28C512EMB-20	32 LCC	3-105	
5962-9086903 MZX	X28C512FMB-20	32 FLATPACK	3-105	
5962-9086904 MUX[4]	X28C512KMB-20	36 PGA	3-105	
5962-9086904 MXX[4]	X28C512DMB-20	32 CERDIP	3-105	
5962-9086904 MYX[4]	X28C512EMB-20	32 LCC	3-105	
5962-9086904 MZX[4]	X28C512FMB-20	32 FLATPACK	3-105	
5962-9086905 MUX	X28C512KMB-15	36 PGA	3-105	**64K x 8 5V Byte Alterable E^2PROM**
5962-9086905 MXX	X28C512DMB-15	32 CERDIP	3-105	
5962-9086905 MYX	X28C512EMB-15	32 LCC	3-105	
5962-9086905 MZX	X28C512FMB-15	32 FLATPACK	3-105	
5962-9086906 MUX[4]	X28C512KMB-15	36 PGA	3-105	
5962-9086906 MXX[4]	X28C512DMB-15	32 CERDIP	3-105	
5962-9086906 MYX[4]	X28C512EMB-15	32 LCC	3-105	
5962-9086906 MZX[4]	X28C512FMB-15	32 FLATPACK	3-105	
5962-9086907 MUX	X28C512KMB-12	36 PGA	3-105	
5962-9086907 MXX	X28C512DMB-12	32 CERDIP	3-105	
5962-9086907 MYX	X28C512EMB-12	32 LCC	3-105	
5962-9086907 MZX	X28C512FMB-12	32 FLATPACK	3-105	
5962-9086908 MUX[4]	X28C512KMB-12	36 PGA	3-105	
5962-9086908 MXX[4]	X28C512DMB-12	32 CERDIP	3-105	
5962-9086908 MYX[4]	X28C512EMB-12	32 LCC	3-105	
5962-9086908 MZX[4]	X28C512FMB-12	32 FLATPACK	3-105	
5962-9086909 MYX	X28C513EMB-25	32 LCC	3-105	
5962-9086910 MYX[4]	X28C513EMB-25	32 LCC	3-105	
5962-9086911 MYX	X28C513EMB-20	32 LCC	3-105	
5962-9086912 MYX[4]	X28C513EMB-20	32 LCC	3-105	
5962-9086913 MYX	X28C513EMB-15	32 LCC	3-105	
5962-9086914 MYX[4]	X28C513EMB-15	32 LCC	3-105	
5962-9086915 MYX	X28C513EMB-12	32 LCC	3-105	
5962-9086916 MYX[4]	X28C513EMB-12	32 LCC	3-105	
5962-9552504MRX	X9241MDMB	20 CERDIP		Quad E^2POT 2/10/10/50KΩ
5962-9552503MRX	X9241UDMB	20 CERDIP		Quad E^2POT 50/50/50/50KΩ
5962-9552502MRX	X9241WDMB	20 CERDIP		Quad E^2POT 10/10/10/10KΩ
5962-9552501MRX	X9241YDMB	20 CERDIP		Quad E^2POT 2/2/2/2KΩ

4. Write Cycle Time = 5ms

Declassification Procedures For Xicor 5V Only E²PROMs

INTRODUCTION

With their introduction into the market place, 5V only E²PROMs were quickly designed into many military electronics systems. They provided a mechanism for easily updating data bases and software programs without the requisite board removal and component changes associated with other nonvolatile semiconductor memories. Because the E²PROMs might contain classified data, many OEMs were required to provide a means of erasure.

This paper will review the basics of the technology, two techniques employed for chip declassification and a complete description of Xicor's declassification experiments and results will be reviewed.

DEVICE OPERATION

Xicor E²PROMs employ Fowler-Nordheim tunneling to transfer charge onto or off of a floating gate. The voltages required to transfer charge are generated onboard the device.

Figure 1 is a cut away view of the cell structure. Poly 1 acts as both the cell ground isolation transistor and programming cathode; Poly 2 is the floating gate; and Poly 3 acts as both the select word line transistor and erase tunnel anode. Poly 2 is totally surrounded by an oxide electrically isolating it from all other device structures. Its channel region acts as both the floating gate charge-conditional current path for reading and the data conditional current path for writing.

A schematic representation is illustrated in Figure 2. Because the construction of the cell incorporates the poly 1 to 2 programming and poly 2 to 3 erase tunneling elements in a single structure, data storage is a direct, single pass operation, involving the following sequence. First the poly 1 line, common to the entire array, is brought low, cutting off the conduction path from bit line through the cell to array ground. Next, the bit lines are set up to either 0V for an erase operation or about 16V for a program operation. The poly 3 word line is ramped up to about 22V in 1ms to drive the nonvolatile charge transport. To erase, the bit line is grounded, whereupon the channel voltage under poly 2 capacitively steers the floating gate towards ground. This induces sufficient voltage across the poly 3/2 tunneling element to remove electrons from the floating gate. When the bit line is high for programming, the channel potential steers the floating gate positively. This induces sufficient voltage across the poly 2/1 tunneling element to inject electrons onto the floating gate.

Figure 1. Cell Cross Section

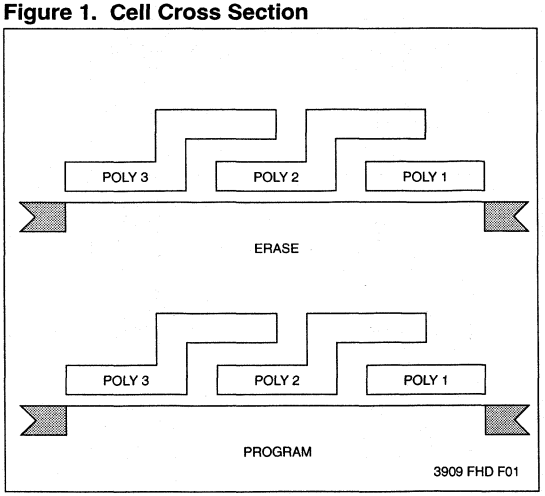
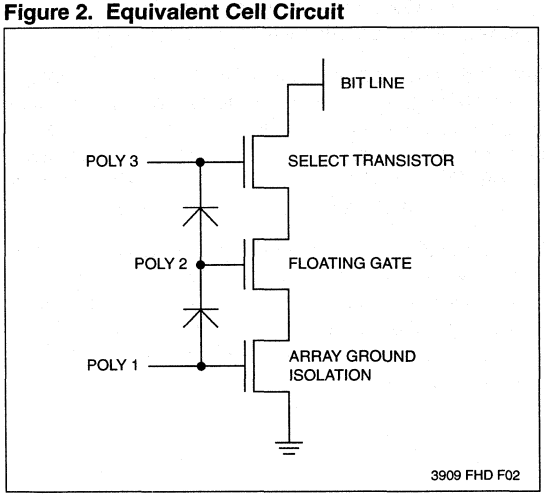


Figure 2. Equivalent Cell Circuit



11

During tunneling, charge will be trapped in the interpoly oxides. This trap-up is caused by the accumulation of trapped negative charge in the dielectric due to the repeated passage of current. These charges create a potential which is additive and opposite to that of the floating gate.

The basic cell operation and description of charge trap in the dielectric is fundamental background for understanding the experiments described in later sections. For detailed descriptions of device operation and endurance in floating gate memories refer to Xicor's 1988 Data Book.

First Generation Chip Clear Techniques

E²PROMs require a relatively long period of time to program/erase data on the floating gate. The maximum time generally specified for the first generation devices (X2816A) was 10ms per byte. In a manufacturing/test environment each byte must be programmed and verified with multiple patterns at all V_{CC} limits and temperature limits. With the X2816A, a 2K x 8 device, one rewrite of the entire array would take approximately 20 seconds. When multiplied times all the test variables, the test time would begin to take minutes per device.

In order to reduce test times most manufacturers incorporated test modes whereby the entire array could be erased (changed to all 1s) or programmed (changed to all 0s) in a single 10ms cycle.

This operation for Xicor devices is performed by raising the $\overline{OE}$ input to V_{OE} (a voltage higher than V_{CC}), setting the I/Os to a specified TTL level and strobing the $\overline{WE}$ and $\overline{CE}$ inputs LOW. This whole operation is similar to a standard write operation with the exception of V_{OE}.

It should be noted that V_{OE} is not coupled into the device. The high voltage on $\overline{OE}$ is detected by the input circuitry and conditions the internal logic for a chip mode operation (sometimes referred to as block mode or mass mode). The high voltage required for tunneling is generated by the device's on-board charge pumps.

The timing diagrams and input level requirements were shared with the OEMs requiring these functions. The chip erase (not chip program) function was subsequently specified on various Standardized Military Drawings and slash sheets; thereby, becoming de facto standard features.

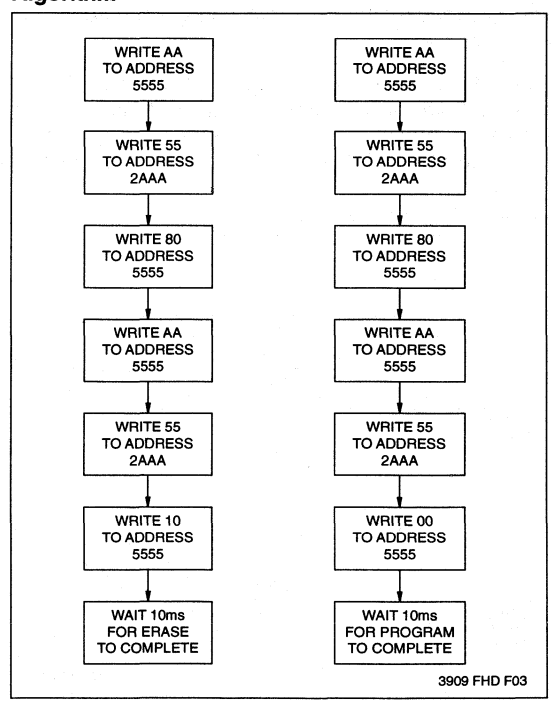
Second Generation Chip Clear Techniques

The X28256 was the first device to employ software data protection. This feature was developed to eliminate the most common design problem encountered with 5V only nonvolatile memories, inadvertent writes during power-up/-down cycling. During power transitions, positive control of E²PROM inputs cannot always be guaranteed before system stabilization. This can lead to inadvertently generating write conditions to the E²PROMs, resulting in corrupted data.

Based on Xicor's experience in resolving these system design issues, the company implemented software data protection. When employed by the end user, the device will ignore all attempts to write unless a specific three byte command sequence is issued (refer to Xicor Data Book).

Expanding on the three byte command sequence, Xicor implemented 5V only chip erase and chip program algorithms that may be employed to completely erase or program the device in a single 10ms operation. This is illustrated in Figure 3.

Figure 3. 5V Only Chip Erase and Chip Program Algorithm



Declassification Procedures for Xicor 5V Only E²PROMs

Classified Erase Experiment

Recently a number of our customers have requested data regarding the effectiveness of the chip erase modes. Their contractual requirements have specified declassification procedures that do not specifically encompass E²PROMs. The declassification procedures default to those reserved for ferrite core memories. This requires a minimum 100 erase/program cycles for secret and below data and a minimum 1000 erase/program cycles for top secret data.

In certain applications where data has to be declassified on a daily basis or end of work shift basis, the specified procedures would predominate over actual useful data writes as the end of life endurance mechanism.

Intuitively we understood the requirements to be far in excess of actual need. From daily test operation it was evident that after a chip erase or program operation the contents would be read back as all 1s or all 0s under normal operating conditons.

In order to prove no "residual" data could be read out under any conditions, Xicor proceeded with a study: first, to determine if there was a method of data recovery; secondly, if there was recoverable data, what was the optimum method of declassification.

Background

The tests performed for this report were done with the full knowledge of the device's internal and external operating characteristics, including all the device's proprietary test modes. Once the device is fully erased or programmed in a single pass there is no known method of scanning the die in a non-intrusive manner to detect latent or residual data patterns. Therefore a method had to be found which would make a read operation most sensitive to floating gate charge or other residual charge which might be a result of previously stored data.

Reading Data

A highly sensitive method of reading needed to be found to insure the results of the experiment were valid. The X28C256 has a proprietary test mode which allows measurement of individual cell currents. During the experiments, cell currents were recorded after declassification and downloaded to a computer. The data were passed through a software filter that emulated a self centering sense amplifier, approximately three times more sensitive than the on-chip sense amplifier.

Figure of Merit

A figure of merit rating was employed to determine the effectiveness of declassification tests. The figure of merit was derived by exclusive or'ing the erased pattern with the original pattern and summing the result over the array. This number is then divided by the total number of bits to give a figure of merit. A figure of 0.5 would mean the data has been totally scrambled, while less than 0.5 would mean the complement data is appearing, and for more than 0.5 would mean the original data is appearing. For example 0.8 means that 20% of the bits are randomly different from the original pattern. Therefore, a figure of merit of 0.5 would be the ideal result.

Moving Address Pattern

A moving address pattern was employed to eliminate any potential misinterpretation of data due to the physical proximity of cells to ground planes or voltage lines.

The Experiments

It was well known that under normal device operation, randomly changing the data pattern on a regular basis or infrequently performing software updates, a single chip erase operation would be sufficient to insure no data could be recovered. Therefore, based on knowledge of the device a worst case experiment was developed. Worst case would be iteratively writing the same data pattern to the device, maximizing traps in the interpoly oxides. It was known that latent charge (or lack of charge) on the floating gate after erasure would not be detectable, but the traps might modify the local electric fields enough to be detectable under laboratory conditions.

Experiment #1. Gathering A Baseline

The tests were originally performed on units provided from production after basic go/no-go tests without full screening. The test consisted of writing the moving address pattern to the device 4,000 times without any intervening pattern being written. After a single pass chip erase (all 1's) and chip program (all 0's) in the 5V only mode, the pattern was not detectable when reading under normal operating conditions. However, by employing the proprietary test mode under an extreme voltage condition on V_{CC} and using the computer analysis tool a latent pattern could be detected with a figure of merit of 0.79. This was not a read of the floating gate charge, but a detection of the traps caused by the iterative writing of the same pattern.

Experiment #2. Impact Of Standard Screening

The experiment was then continued to determine the effect of standard production precycling. This precycling is normally performed to screen infant mortality failures prior to shipment. The screen is repetitive erase/program cycles which would cause trap-up. Trapping is logarithmic; therefore, after precycling any additional writing would not add many traps, reducing the likelihood of data recovery.

After precycling, the devices were cycled 4,000 times with the moving address pattern. This was followed by five 5V only erase/program cycles, yielding a read back figure of merit of 0.53 under the special test conditions.

Experiment #3. Impact Of High Temperature During Declassification

In this experiment, devices were subjected to 2000 cycles of the same moving address pattern. 5V only erase and program was performed at + 125°C with the following results:

	Figure of Merit
Erase 1	.57
Program1	.55
Erase 2	.52
Program2	.52

Experiment #4. Chip Erase Only As A Means Of Declassification

Additional units were cycle 100,000 times with the moving address pattern. These units were then subjected to 5V only chip erasure. The results are as follows:

	Figure of Merit
Erase 1	.59
Erase 2	.55
Erase 3	.53

Recommendations—In most applications a single erase operation is sufficient, in worst case applications three to five erase/program cycles will render the data totally unrecoverable. Below are application examples and recommended methods of declassification.

Data logging—where monitored data are stored in sequential fashion as the data are generated. This is generally done by simply incrementing the address for each new data to be stored; when reaching the end of the allocated memory space recording begins at address zero. Single chip erase cycle (10ms) or single chip erase/program cycle (20ms).

Program storage—where the program is updated infrequently with data changing in a random manner. Single chip erase cycle (10ms) or a single chip erase/program cycle (20ms).

Program storage—where the data are frequently updated but only the data actually changed is being rewritten. Single chip erase cycle (10ms) or a single chip erase/program cycle (20ms).

Program storage—where the data are frequently updated, most of the data is unchanged and all addresses are rewritten for each update.

a. Perform a single erase/program cycle prior to each update. Then for declassification a single chip erase/program cycle (20ms) would be required.

b. If data are loaded at beginning of each work shift and data then declassified at end of each work shift; perform end of shift declassification utilizing a single chip erase/program cycle (20ms).

c. If data are frequently updated with no intervening erase/program cycles then declassify with three chip erase/program cycles (100ms).

Footnote:

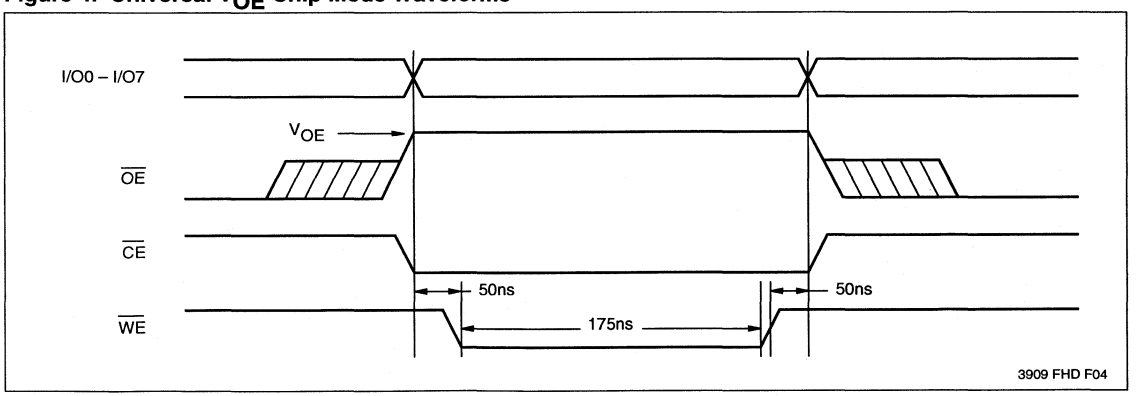
This report has shown the effectiveness of the 5V only Classified Erase Algorithm under various applications conditions. Because the internal mechanism is identical for the V_{OE} operating mode, the conclusions are valid for its use also.

It should be noted for applications where neither 5V only erase/program nor the V_{OE} method of erase/program are suitable; writing all "1"s in either byte or pag emode is equivalent to a chip erase operation and writing all "0"s is equivalent to a chip program operation.

Below is a cross matrix table indicating by product the method of chip erase/program employed. Where V_{OE} mode is defined the V_{OE} voltage and I/O conditions required are also defined.

	V_{OE} Chip Mode			
Xicor Device	**V_{OE}**	**I/O State for Program**	**I/O State for Erase**	**5Volt Only Mode Available**
X2816B	20V	00	FF	No
X28C64	14V	00	FF	Yes
X28HC64	14V	00	FF	Yes
X28C256	14V	00	FF	Yes
X28HC256	14V	00	FF	Yes
X28VC256	14V	00	FF	Yes
X28C512	14V	00	FF	Yes
X28C010	14V	00	FF	Yes

Figure 4. Universal V_{OE} Chip Mode Waveforms



Individual device timing requirements are available from Xicor. Address states are "don't care" for this operation. Once initiated, the operation (either chip erase or chip program) is self-timed and will complete within 10ms.

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Ordering Information

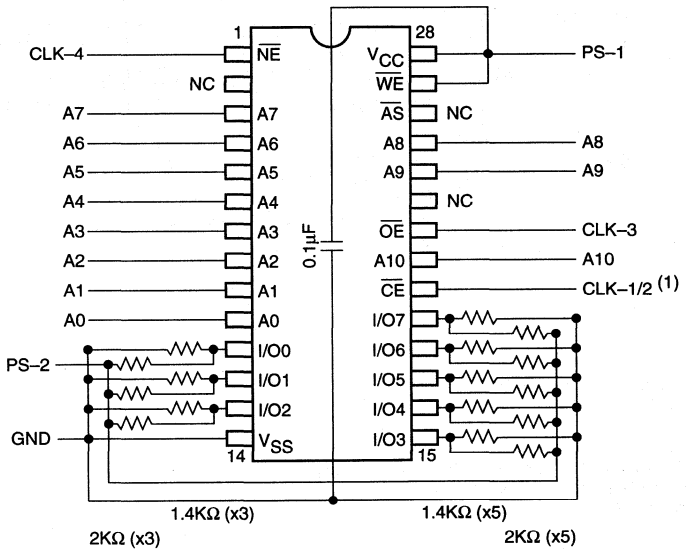
The required mode of declassification must be stated prior to ordering the applicable Xicor MIL-STD-883 device. Xicor does not guarantee declassification on "off-the-shelf" MIL-STD-883 product.

Please contact your local Xicor Sales Office for availability and ordering information.

NOTES

Military Product Burn-in Circuits and Timing

Figure 1. X20C04, X20C05, X20C16 Burn-In Circuit



Notes: (1) CLK-1: Rows 1, 3, 5... (odd rows $\overline{CE}$-A)
CLK-2: Rows 2, 4, 6... (even rows $\overline{CE}$-B)
CLK-2 = $\overline{CLK\text{-}1}$
(2) $\overline{WE}$ (Pin 27) must be hardwired to V_{CC} (Pin 28) at device as shown.
(3) I/O Pull Up: 2KΩ I/O Pull Down: 1.4KΩ
(4) All Resistors: 1% Metal Film, 1/4W
(5) Pin 24 (A9) and Pin 25 (A10) are no connects on the X20C04 and X20C05.
(6) Pin 26 ($\overline{AS}$) is a no connect on the X20C04.

3906 ILL F01.1

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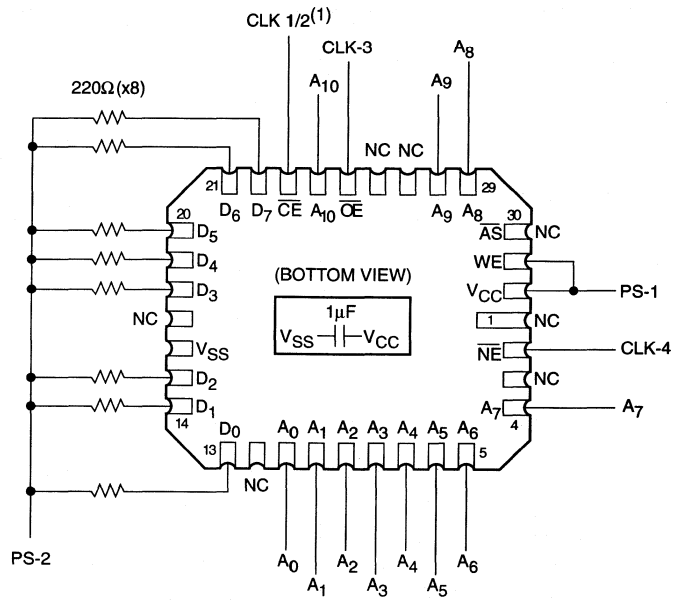
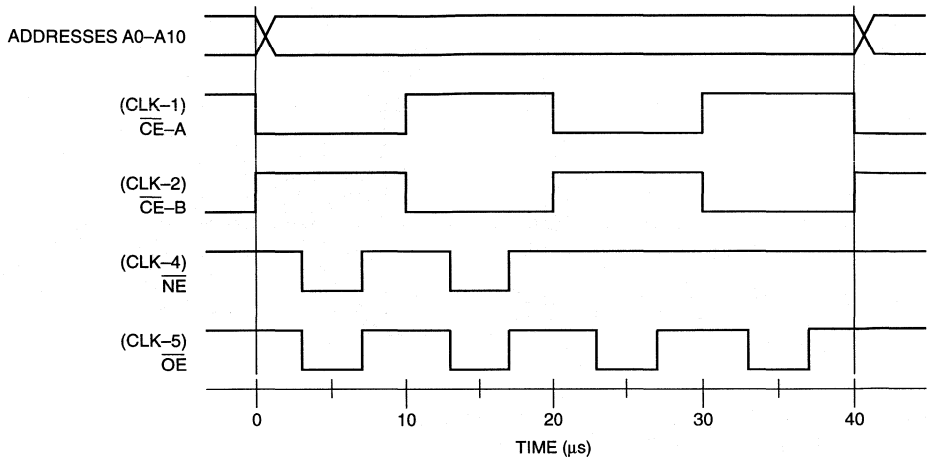
Figure 2. X20C16 Burn-In Circuit



Notes: (1) 'Chip Enable' Clock Assignments:
CLK-1: All Odd Rows
CLK-2: All Even Rows
Such that: CLK-2 = $\overline{\text{CLK-1}}$
(2) Pin 31 ($\overline{\text{WE}}$) must be hardwired to V_{CC} (Pin 32) at device.
(3) All resistors: 1% metal film, 1/4W
(4) I/O Isolating resistor = 220Ω

3906 ILL F17.1

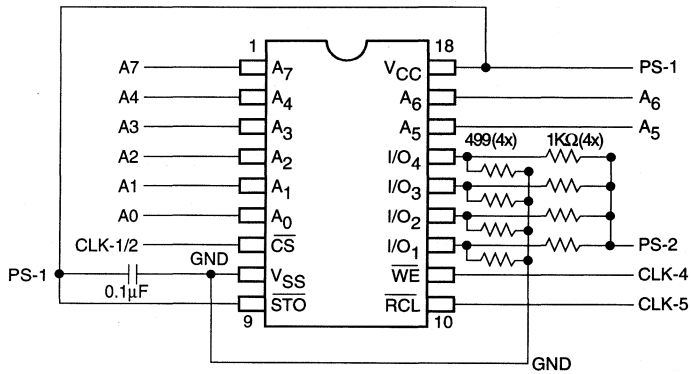
Figure 3. X20C04, X20C05, X20C16 Burn-In Timing



Notes: (1) ADDRESS Lines: 0-10
ADDRESS Cycle: 40µs
(2) $\overline{WE}$ Disabled (tied to V_{CC} at device)
(3) V_{IN} LOW: 0.4V, V_{IN} HIGH: 5V
(4) V_{CC}: 5.5V

3906 ILL F08

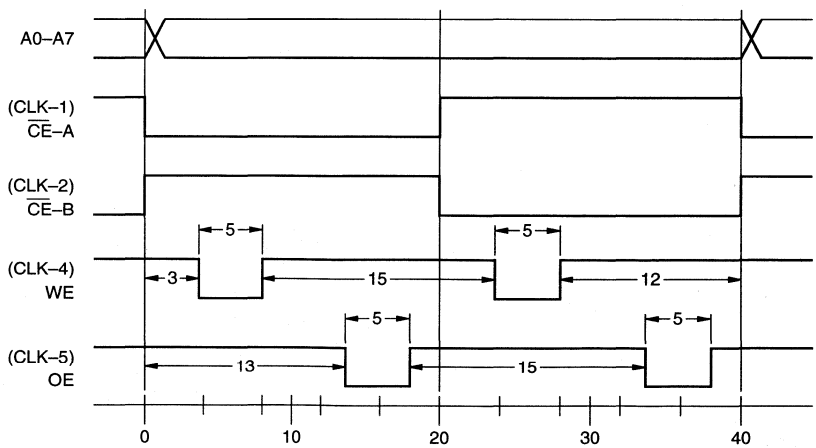
Figure 4. X22C10, X22C12 Burn-In Circuit



Notes: (1) Pin 1 (A_7) and Pin 17 (A_6) are no connects (NC) for the X22C10.
(2) $\overline{STO}$ must always be hardwired to V_{CC} (Pin 18) at device.
(3) I/O Pull Up: 1KΩ
I/O Pull Down: 499Ω
(4) All resistors: 1% metal film; 1/4W.
(5) Socket-to-Socket isolation as shown.
(6) CLK-1: Rows 1, 3, 5... (odd rows—$\overline{CS}$–A)
CLK-2: Rows 2, 4, 6... (even rows—$\overline{CS}$–B)
Such that: CLK-2 = $\overline{CLK}$-1

3906 ILL F12.1

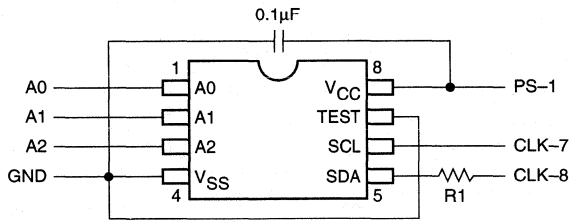
Figure 5. X22C10, X22C12 Burn-In Timing



Notes: (1) A0–A7: Binary Sequencing
Address Cycle: 40µs
(2) $\overline{WE}$ Disabled (tied to V_{CC} at device)
(3) V_{IN} LOW: 0.4V, V_{IN} HIGH: 5V
(4) V_{CC}: 5.5V

3906 ILL F07

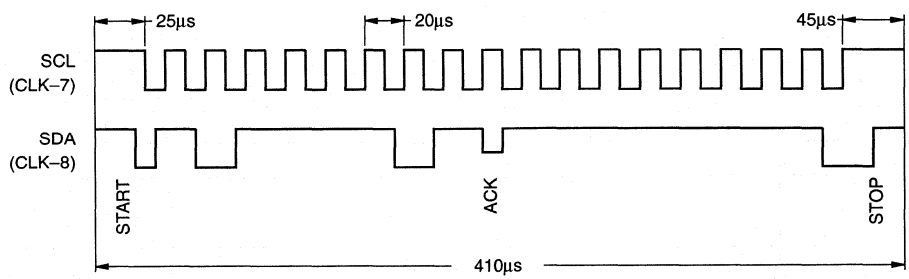
Figure 6. X24C04, X24C16 Burn-In Circuit



Notes: (1) Test (Pin 7) hardwired to V_{SS} (Pin 4) at socket.
(2) SDA (Pin 5) socket-isolated as shown—143KΩ (R1) resistor.
(3) Resistor: 1% metal film, 1/4W
(4) A0, A1, A2 must be set HIGH.

3906 ILL F02.1

Figure 7. X24C04, X24C16 Burn-In Timing



Notes: (1) All addresses: A0–A2 tied HIGH
(2) Voltage levels:
V_{IN} HIGH = 5V
V_{IN} LOW = 0.4V max.
(3) V_{CC} = 5.5V

3906 ILL F09.1

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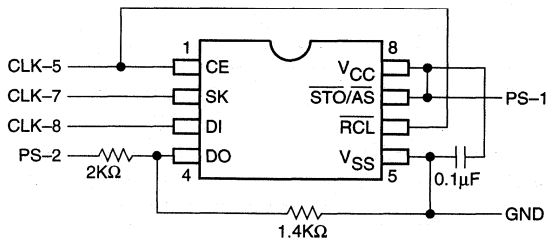
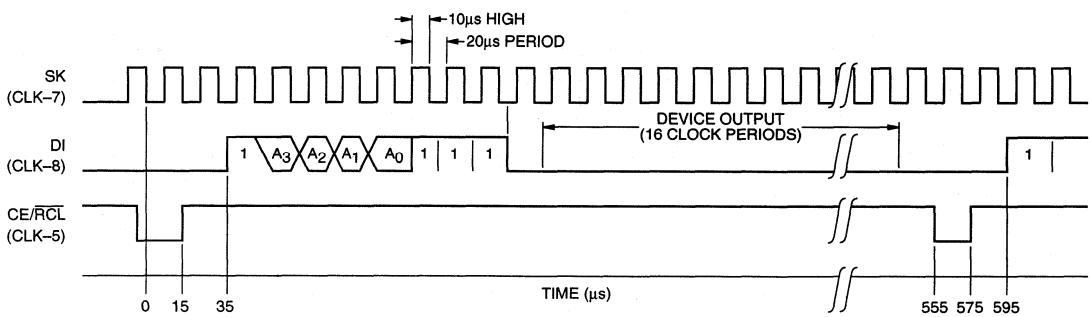
Figure 8. X24C44 and X24C45 Burn-In Circuit



Notes: (1) $\overline{STO}$ (Pin 7) must be hardwired to V_{CC} (Pin 9) at device as shown.
(2) All resistors: 1% metal film, 1/4W
(3) Socket-to-socket isolation as shown.

3906 ILL F18.1

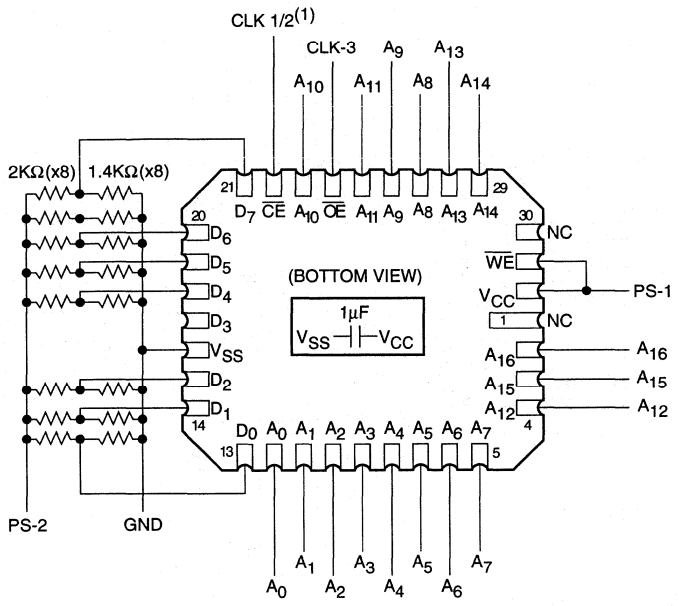
Figure 9. X24C44 and X24C45 Burn-In Timing



Notes: (1) A0 through A3 bindary count in data steam (10000111 through 11111111).
(2) All bits 20µs wide; 60µs between bytes.
(3) V_{CC} = 5.5V, V_{IN} HIGH = 5V, V_{IN} LOW = 0.4V max.

3906 ILL F19.1

Figure 10. X28C512, X28C010 Burn-In Circuit



Notes: (1) 'Chip Enable' Clock Assignments:
CLK-1: All Odd Rows
CLK-2: All Even Rows
Such that: CLK-2 = $\overline{\text{CLK-1}}$
(2) Pin 31 ($\overline{\text{WE}}$) must be hardwired to V_{CC} (Pin 32) at device.
(3) All resistors: 1% metal film, 1/4W
(4) I/O Pull Up: 2KΩ
I/O Pull Down: 1.4KΩ

3906 ILL F04.1

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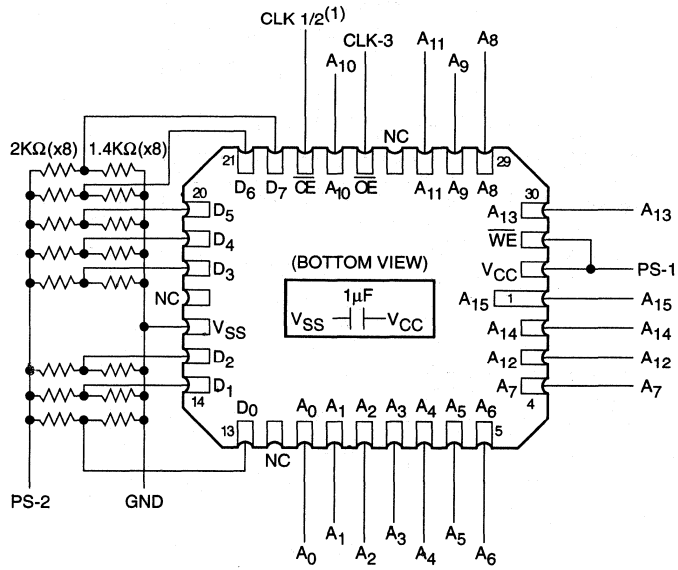
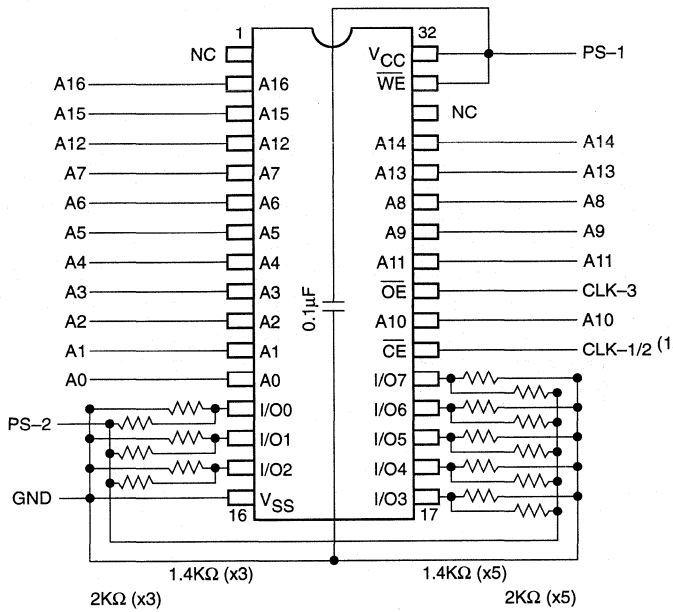
Figure 11. X2816C, X28C64, X28HC64, X28C256, X28HC256, X28C513 Burn-In Circuit



Notes: (1) 'Chip Enable' Clock Assignments:
CLK-1: All Odd Rows
CLK-2: All Even Rows
Such that: CLK-2 = $\overline{\text{CLK-1}}$
(2) Pin 31 ($\overline{\text{WE}}$) must be hardwired to V_{CC} (Pin 32) at device.
(3) All resistors: 1% metal film, 1/4W
(4) I/O Pull Up: 2KΩ
I/O Pull Down: 1.4KΩ

3906 ILL F05.1

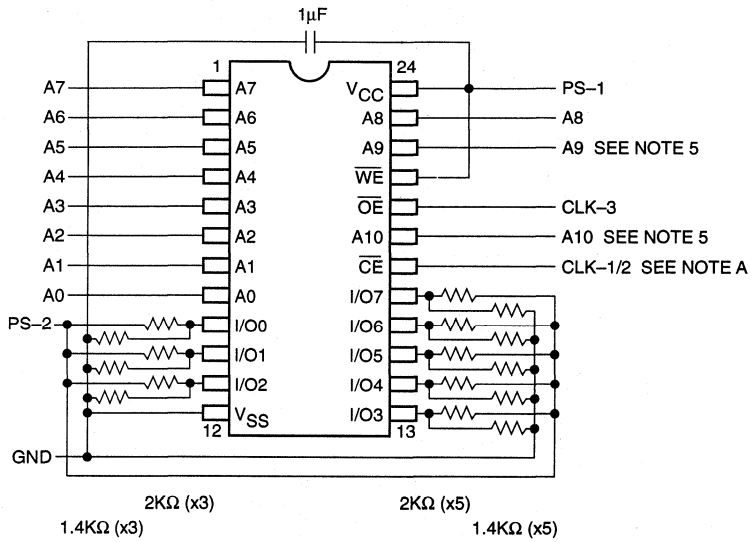
Figure 12. X28C512, X28C010 Burn-In Circuit



Notes: (1) 'Chip Enable' Clock Assignments:
CLK-1: All Odd Rows
CLK-2: All Even Rows
Such that: CLK-2 = $\overline{\text{CLK-1}}$
(2) Pin 31 ($\overline{\text{WE}}$) must be hardwired to V_{CC} (Pin 32) at device.
(3) All resistors: 1% metal film, 1/4W
(4) I/O Pull Up: 2KΩ
I/O Pull Down: 1.4KΩ
(5) Pin 2 (A16) is a no connect on the X28C512.

3906 ILL F03.1

Figure 13. X2816C Burn-In Circuit

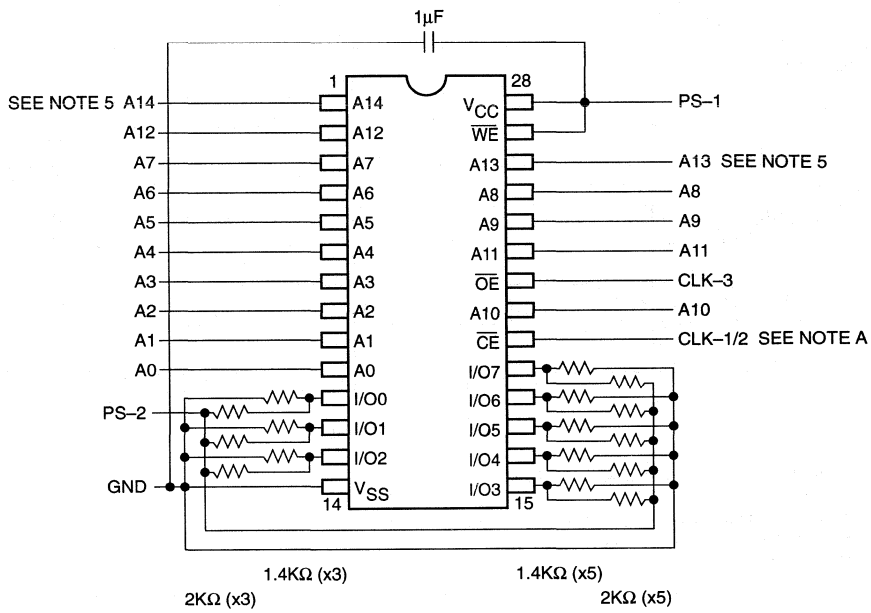


Note A: CLK–1: Rows 1, 3, 5 ... (odd rows—$\overline{CE}_A$)
CLK–2: Rows 2, 4, 6 ... (even rows—$\overline{CE}_B$)
Such that: CLK–2 = $\overline{CLK–1}$

Note B: (1) $\overline{WE}$ must always be hardwired to V_{CC} (Pin 24) at device as shown.
(2) All resistors: 1% metal film, 1/4W
(3) I/O Pull Up: 2KΩ
I/O Pull Down: 1.4KΩ
(4) Socket-to-socket isolation as shown.

3906 ILL F20.1

Figure 14. X28C64, X28HC64, X28C256, X28HC256 Burn-In Circuit



Note A: CLK–1: Rows 1, 3, 5 ... (odd rows—$\overline{CE}_A$)
CLK–2: Rows 2, 4, 6 ... (even rows—$\overline{CE}_B$)
Such that: CLK–2 = $\overline{CLK–1}$

Note B: (1) $\overline{WE}$ must always be hardwired to V_{CC} (Pin 28) at device as shown.
(2) All resistors: 1% metal film, 1/4 Watt
(3) I/O Pull Up: 2KΩ
I/O Pull Down: 1.4KΩ
(4) Socket-to-socket isolation as shown.
(5) Pin 1 (A14) and Pin 26 (A13) are no connects (NC) for the X28C64, X28HC64.

3906 ILL F21.1

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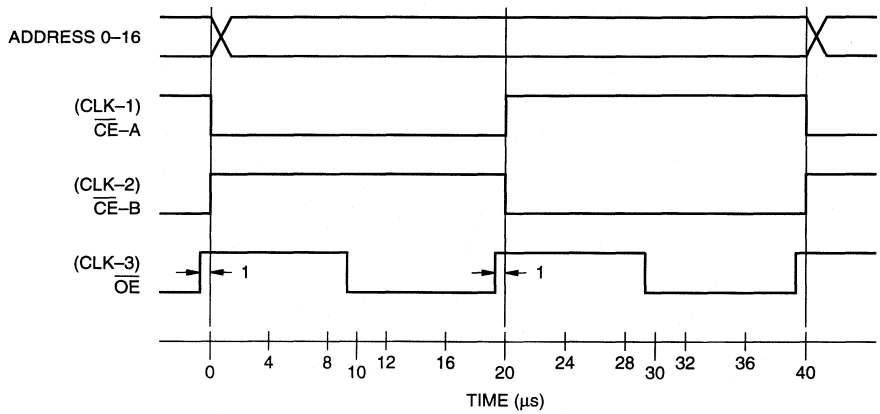
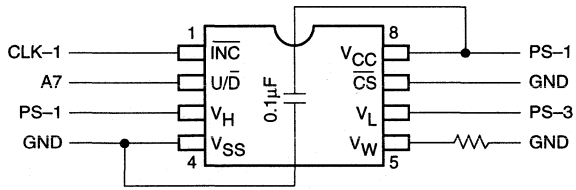
Figure 15. X2816C, X28C64, X28HC64, X28C256, X28HC256, X28C512, X28C513, X28C010 Burn-In Timing



Notes: (1) Address Lines 0–16: Binary Sequencing
Address Cycle: 40µs
(2) $\overline{WE}$ disabled (Tied to V_{CC} at device)
(3) V_{IN} Low: 0.4V, V_{IN} High: 5V
(4) V_{CC}: 5.5V

3906 ILL F10.1

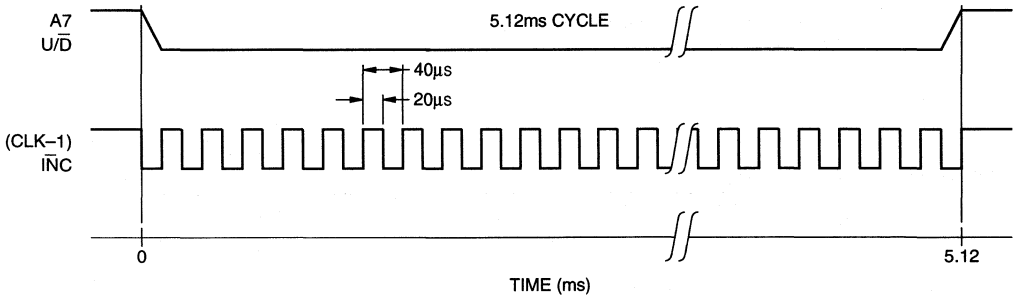
Figure 16. X9C102/103/104/503 Burn-In Circuit



Notes: (1) $\overline{CS}$ (Pin 7) hardwired to V_{SS} (Pin 4) at socket.
(2) V_W (Pin 5) is socket-isolated as shown—5KΩ resistor.
(3) Resistor: 1% metal film, 1/4W

3906 ILL F06.1

Figure 17. X9C102/103/104/503 Burn-In Timing



Notes: (1) Device U/$\overline{D}$ cycle: 5.12ms
(2) Device $\overline{INC}$ cycle: 20µs
(3) Low State: 0.4V max.
High State: 5V typ.
V_{CC}: 5.5V, V_L (PS–3): –5.5V

3906 ILL F11.1

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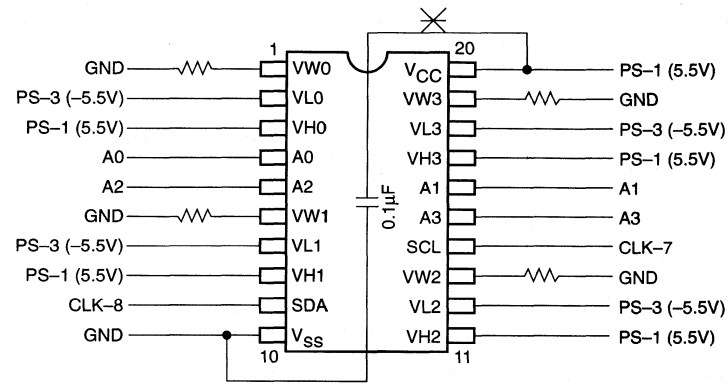
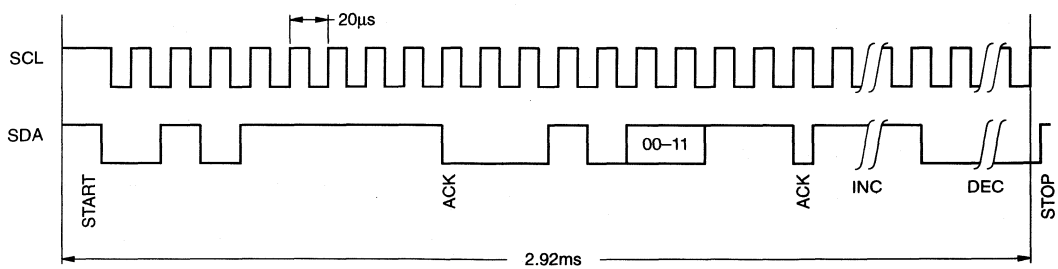
Figure 18. X9241 Burn-In Circuit



Notes: (1) All resistor values are 5KΩ, 1/4W, 1% metal film.
(2) Socket to Socket isolation as shown.

3906 ILL F22.1

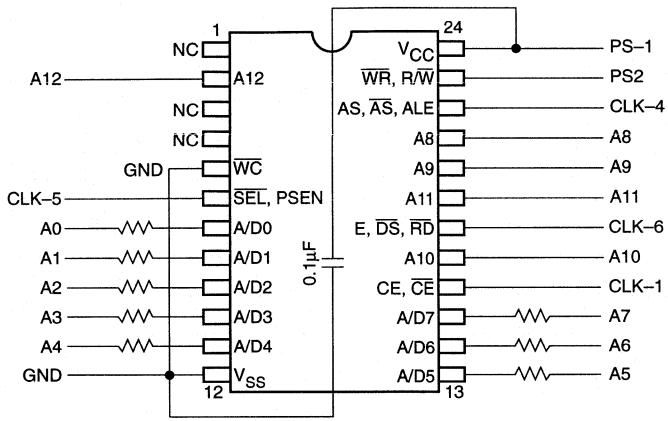
Figure 19. X9241 Burn-In Timing



Notes: (1) V_{CC} is @ 5.5V
(2) All Vh pins are @ 5.5V
(3) All Vl pins are @ –5.5V (PS3)
(4) All Vw pins are connected to Ground.
(5) A0, A1, A2, A3 are @ 5V

3906 ILL F23.1

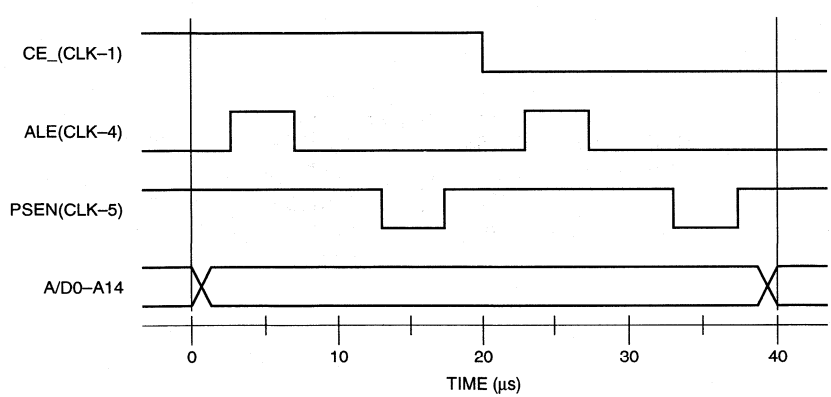
Figure 20. 88C64 Burn-In Circuit



Notes: (1) R/W (Pin 23) is tied to PS2 (5.0V).
(2) WC (Pin 5) is tied to V_{SS} at socket.
(3) Isolation resistors on A/D pins are 10KΩ.
(4) All resistors: 1% metal film 1/4W

3906 ILL F24.1

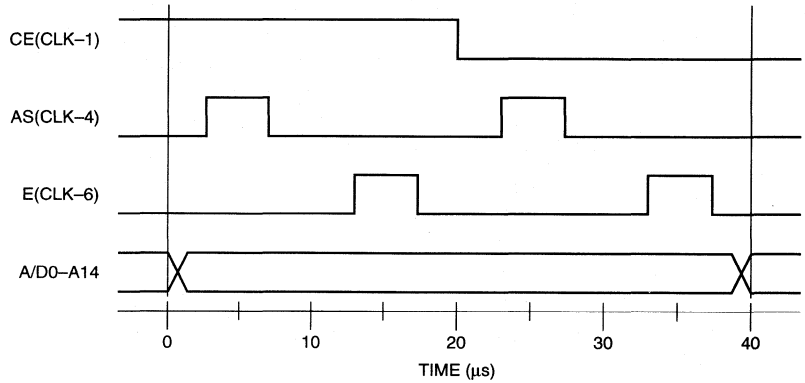
Figure 21. 88C64 Burn-In Timing



Notes: (1) Address lines: A/D0–A14 (A13, A14 88C257)
Address cycle: 40µs
(2) RD_(Clk.6) = 0V
(3) R/W_(PS2) = 5V
(4) Programs: "03" V_{CC} = 5.5V, "06" V_{CC} = 6V.
(5) Vin LOW: 0.4V, Vin HIGH: 5V

3906 ILL F25

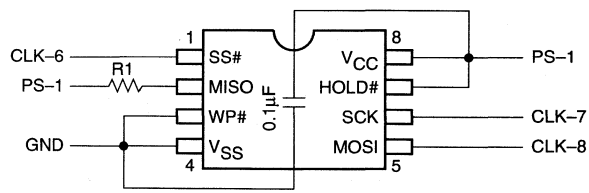
Figure 22. 68C64 Burn-In Timing



Notes: (1) Address lines: A/D0–A14 (A13, A14 68C257)
Address cycle: 40µs
(2) SEL_(CLK-5)
(3) R/W_(PS2) = 5V
(4) Programs: "0D" V_{CC} = 5.5V, "0E" V_{CC} = 6V.
(5) Vin LOW: 0.4V, Vin HIGH: 5V

3906 ILL F26

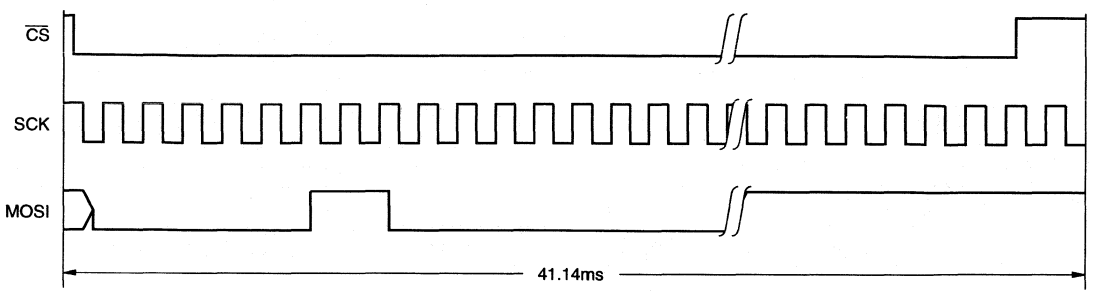
Figure 23. 25XXX Burn-In Circuit



Notes: (1) Hold# (Pin 7) hardwired to V_{CC} (Pin 8) at socket.
(2) MISO (PIN.2) Socket-Isolation; 1KΩ
(3) Resistor: 1% metal film 1/4W

3906 ILL F27.1

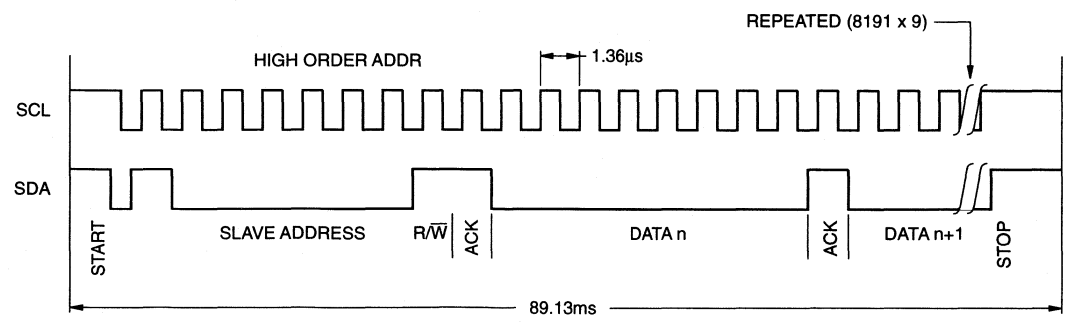
Figure 24. X25C02 Burn-In Timing



Notes: (1) SCK = 20µs cycle
(2) 41.14ms to read entire array
(3) Voltage levels:
Vin HIGH = 5V
Vout LOW = 0.4V max.
(4) V_{CC} = 5.5V

3906 ILL F28.1

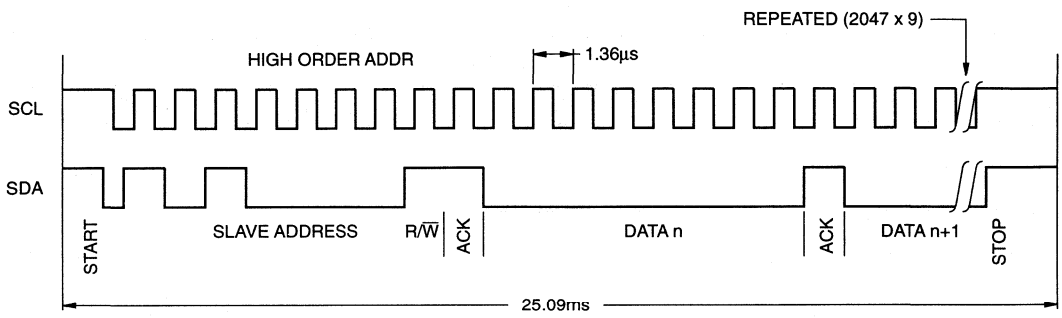
Figure 25. X24645 Burn-In Timing



Notes: (1) 89.13ms to read entire array
(2) Select inputs: S0–S2 are set HIGH
(3) Voltage levels:
Vin HIGH = 5V
Vout LOW = 0.4V max.
(4) V_{CC} = 5.5V

3906 ILL F29.1

Figure 26. X24164 Burn-In Timing



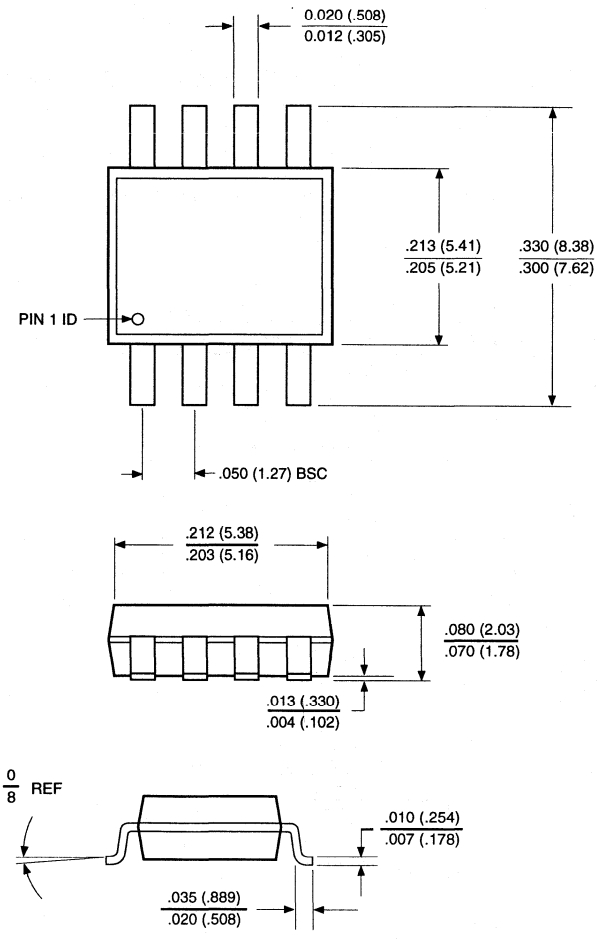
Notes: (1) 25.09ms to read entire array
(2) Select inputs: S0–S2 are set HIGH
(3) Voltage levels:
Vin HIGH = 5V
Vout LOW = 0.4V Max.
(4) V_{CC} = 5.5V

3906 ILL F30.1

Xicor®

3807-2.3 12/4/95 T12/C0/D0 NS

8-LEAD PLASTIC, 0.200" WIDE SMALL OUTLINE GULLWING PACKAGE TYPE "A" (EIAJ SOIC)

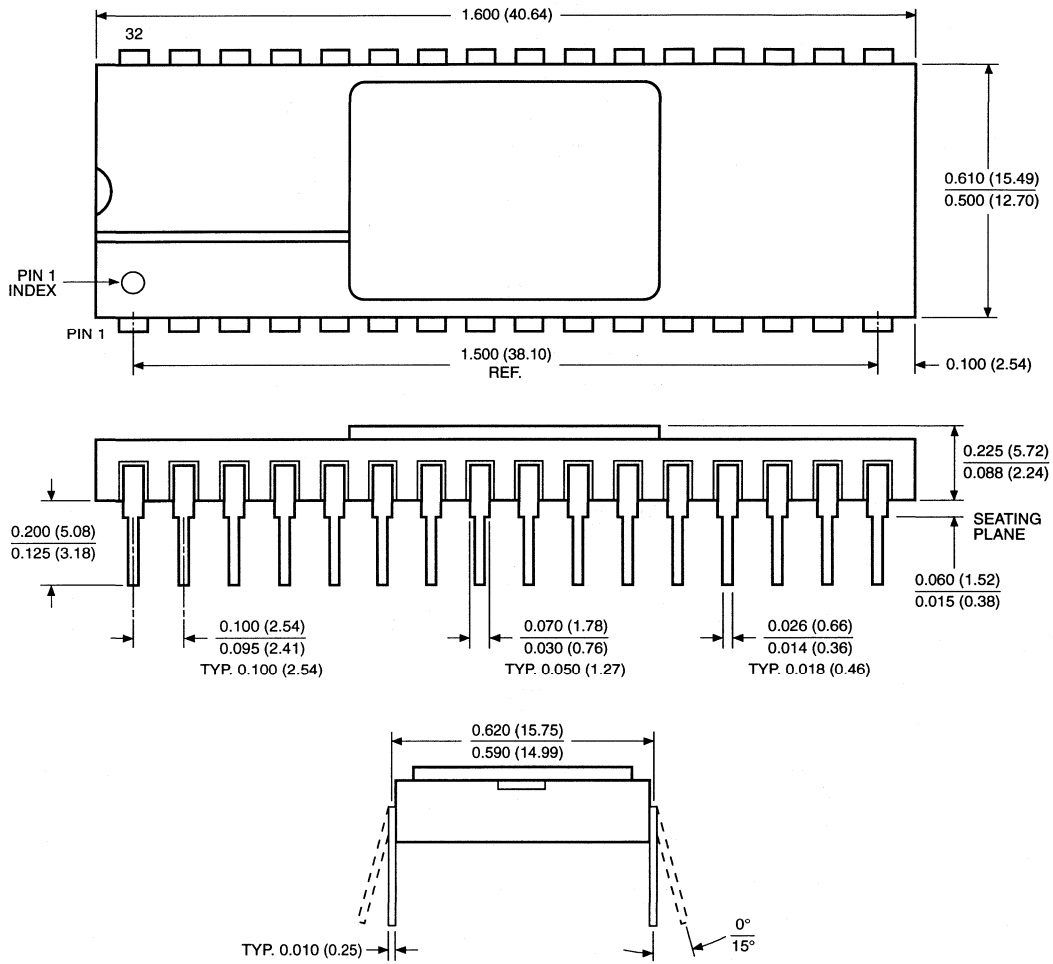


NOTE:
1. **ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)**
2. **PACKAGE DIMENSIONS EXCLUDE MOLDING FLASH**

3926 ILL F33.1

12

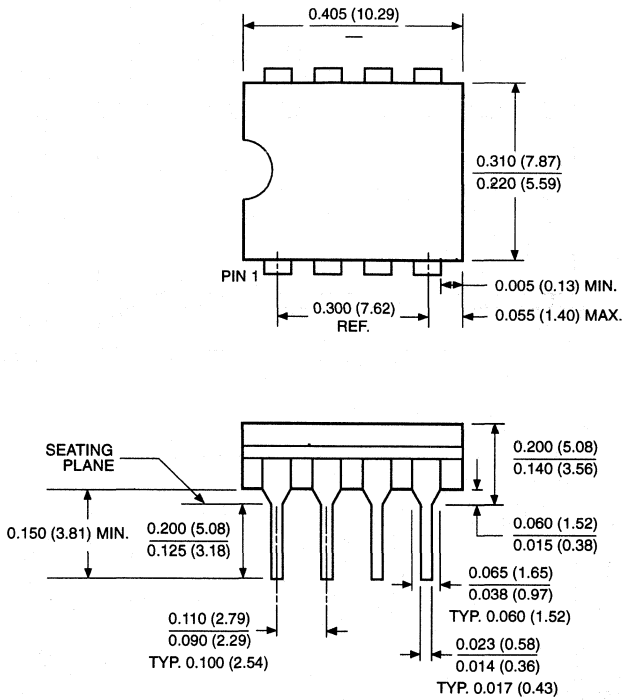
32-LEAD SIDE BRAZE PACKAGE TYPE C



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

3926 FHD F11

8-LEAD HERMETIC DUAL IN-LINE PACKAGE TYPE D



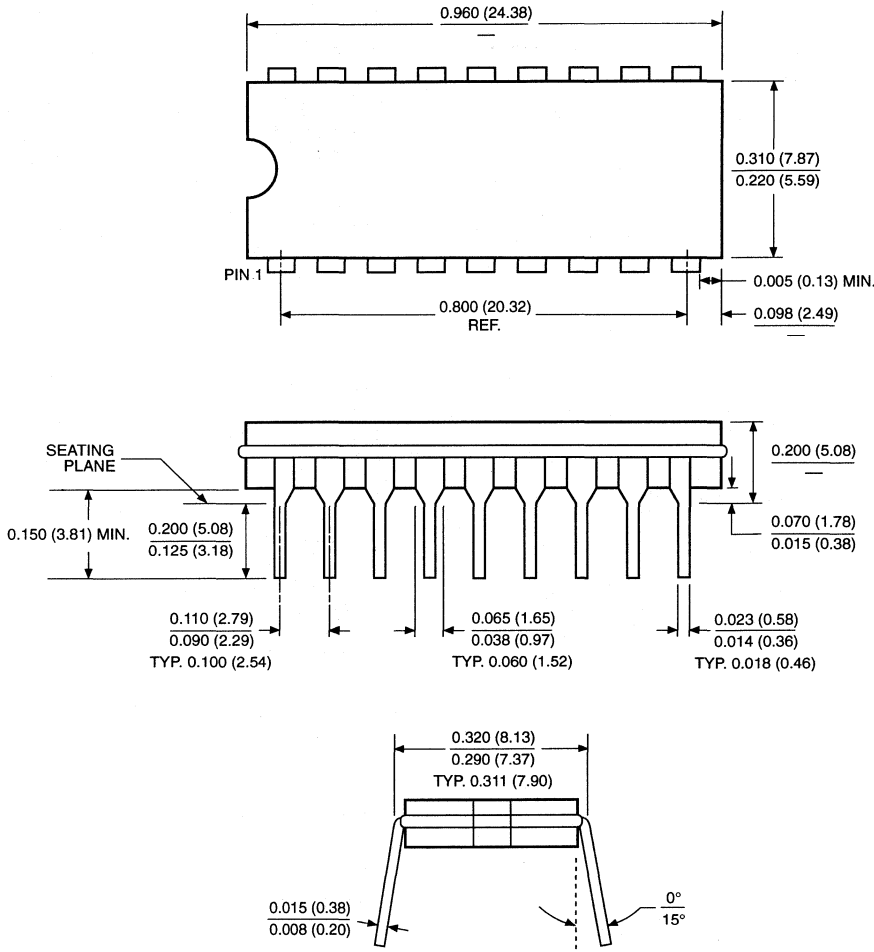
NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

3926 FHD F05

12

Packaging Information

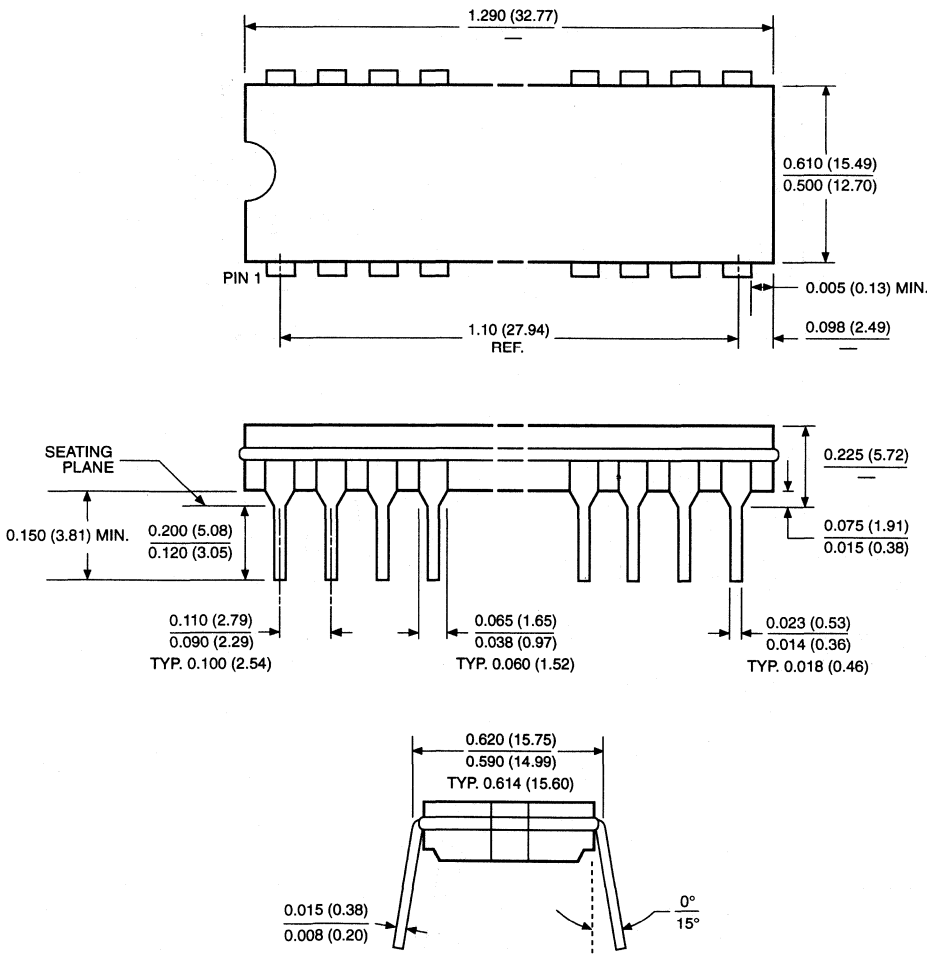
18-LEAD HERMETIC DUAL IN-LINE PACKAGE TYPE D



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

3926 FHD F06

24-LEAD HERMETIC DUAL IN-LINE PACKAGE TYPE D

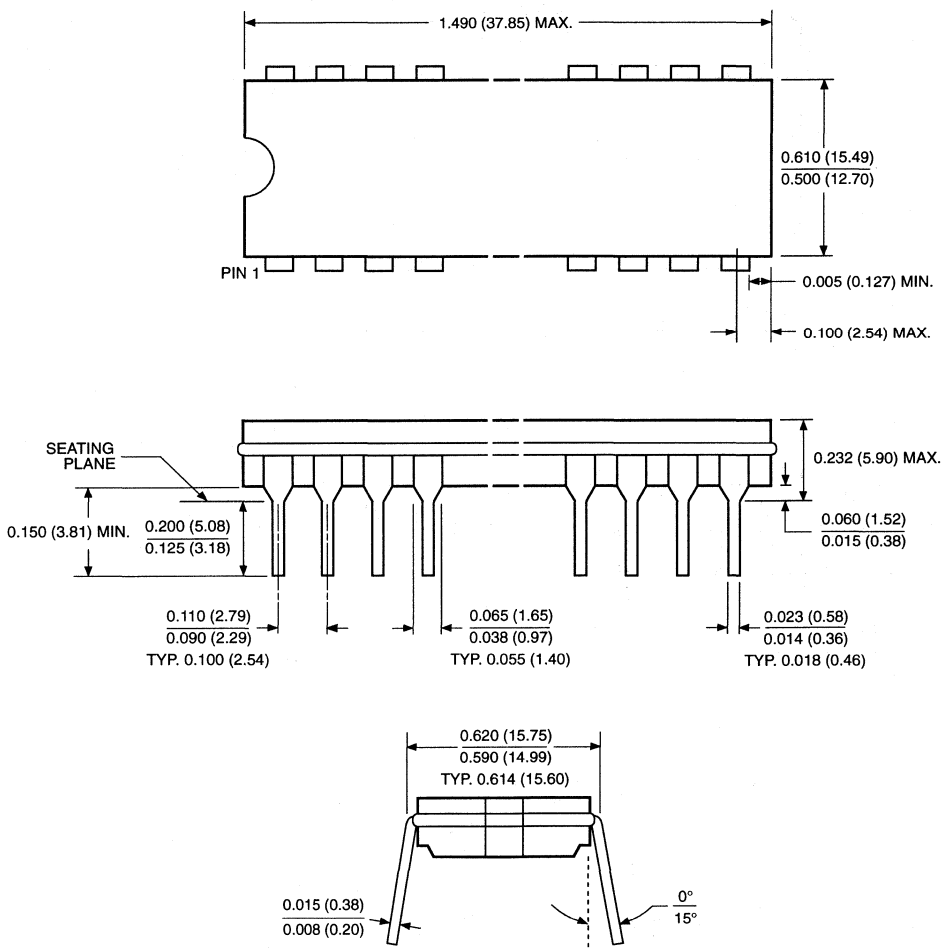


NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

3926 FHD F07

12

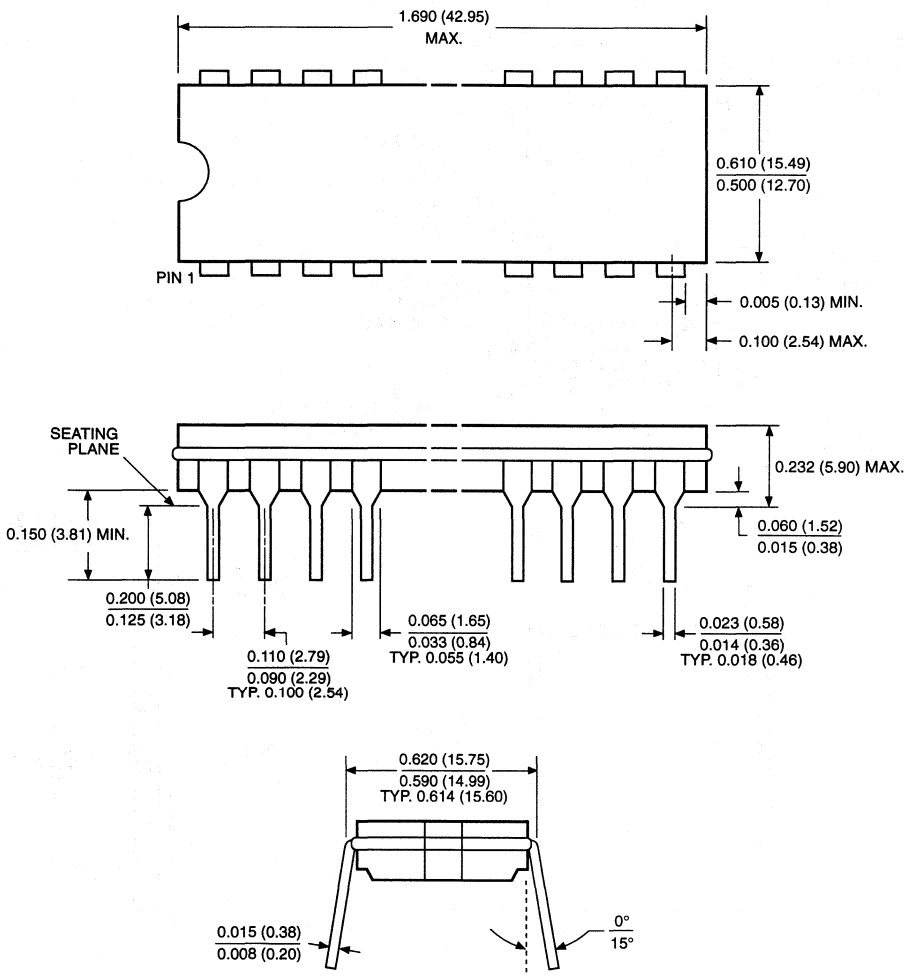
28-LEAD HERMETIC DUAL IN-LINE PACKAGE TYPE D



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

3926 FHD F08

32-LEAD HERMETIC DUAL IN-LINE PACKAGE TYPE D

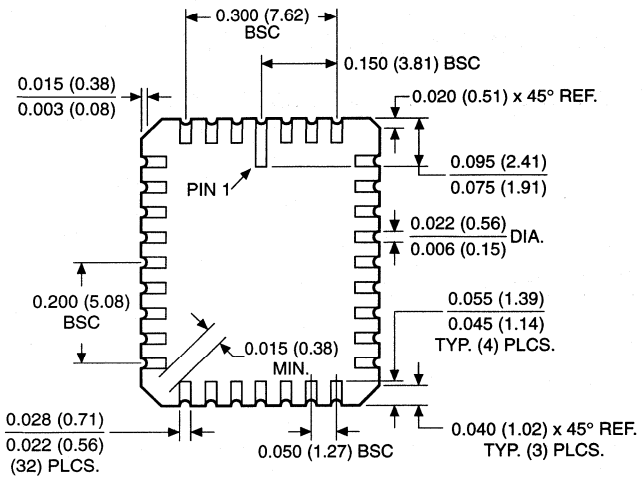


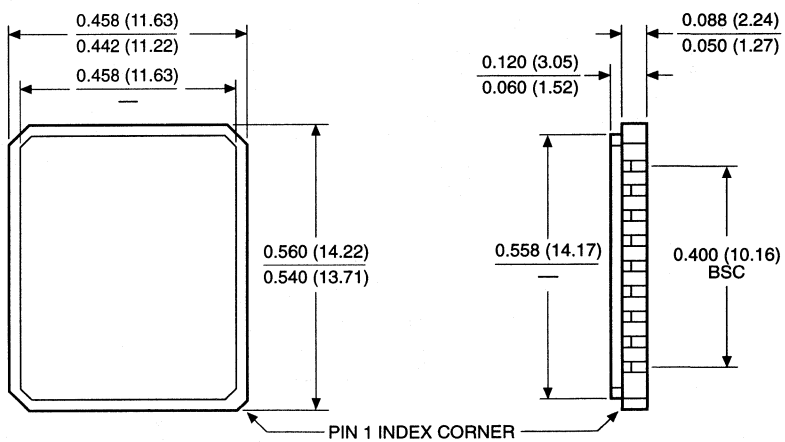
NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

3926 FHD F09

12

32-PAD CERAMIC LEADLESS CHIP CARRIER PACKAGE TYPE E

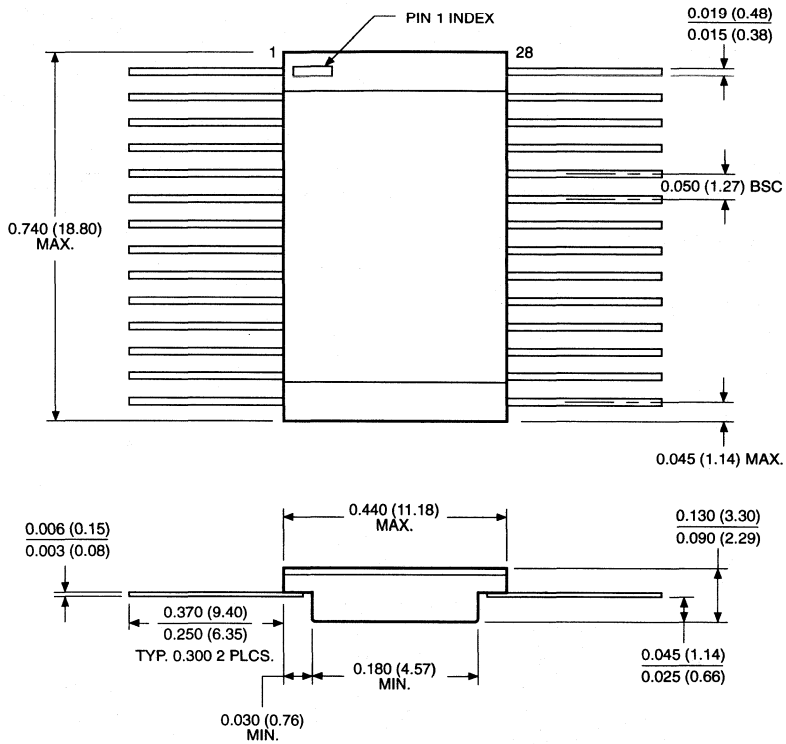




NOTE:
1. **ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)**
2. **TOLERANCE: ±1% NLT ±0.005 (0.127)**

3926 FHD F14

28-LEAD CERAMIC FLAT PACK TYPE F

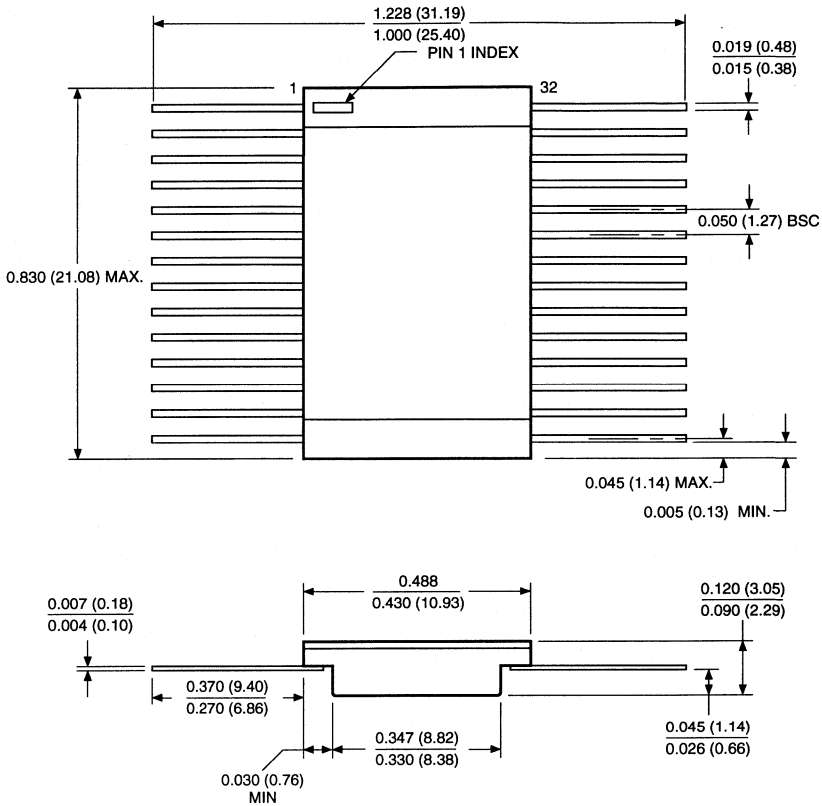


NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

3926 FHD F16

12

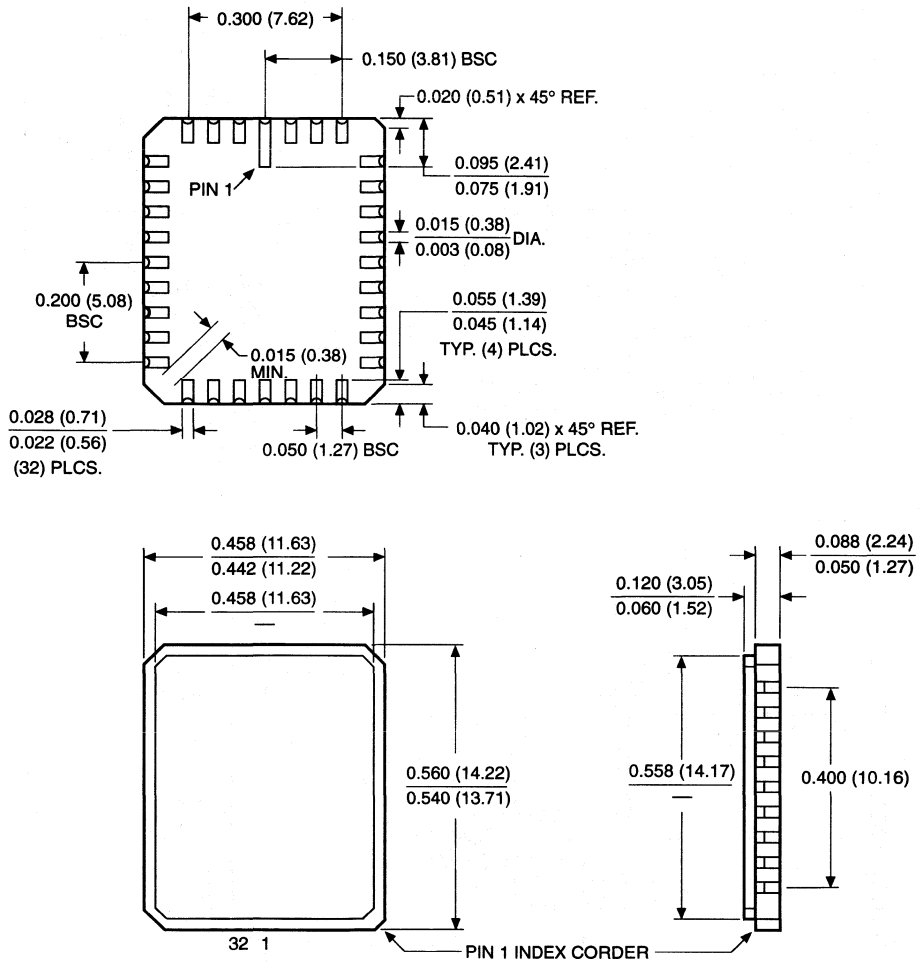
32-LEAD CERAMIC FLAT PACK TYPE F



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

3926 FHD F20

32-PAD CERAMIC LEADLESS CHIP CARRIER (GLASS FRIT SEAL) PACKAGE TYPE G



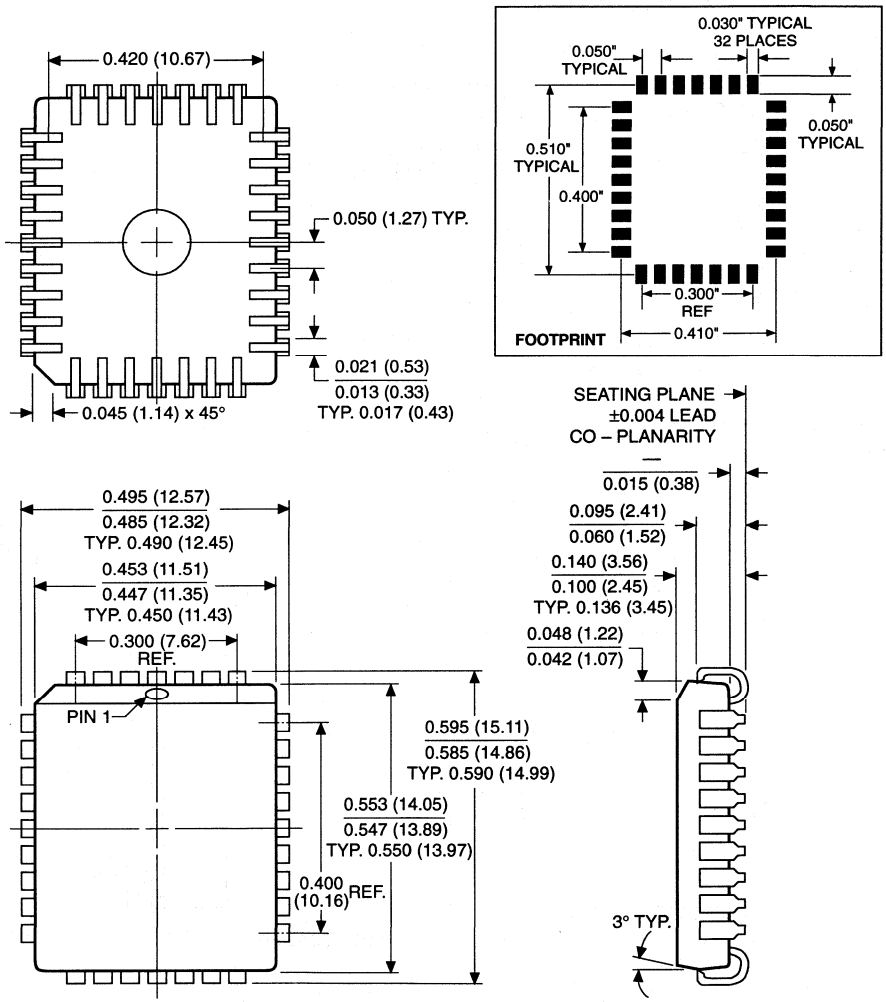
NOTE:

1. **ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)**
2. **TOLERANCE: ±1% NLT ±0.005 (0.127)**
3. **FOR EXTENDED STORAGE TEMPERATURE ENVIRONMENTS**

3926 FHD F19

12

32-LEAD PLASTIC LEADED CHIP CARRIER PACKAGE TYPE J

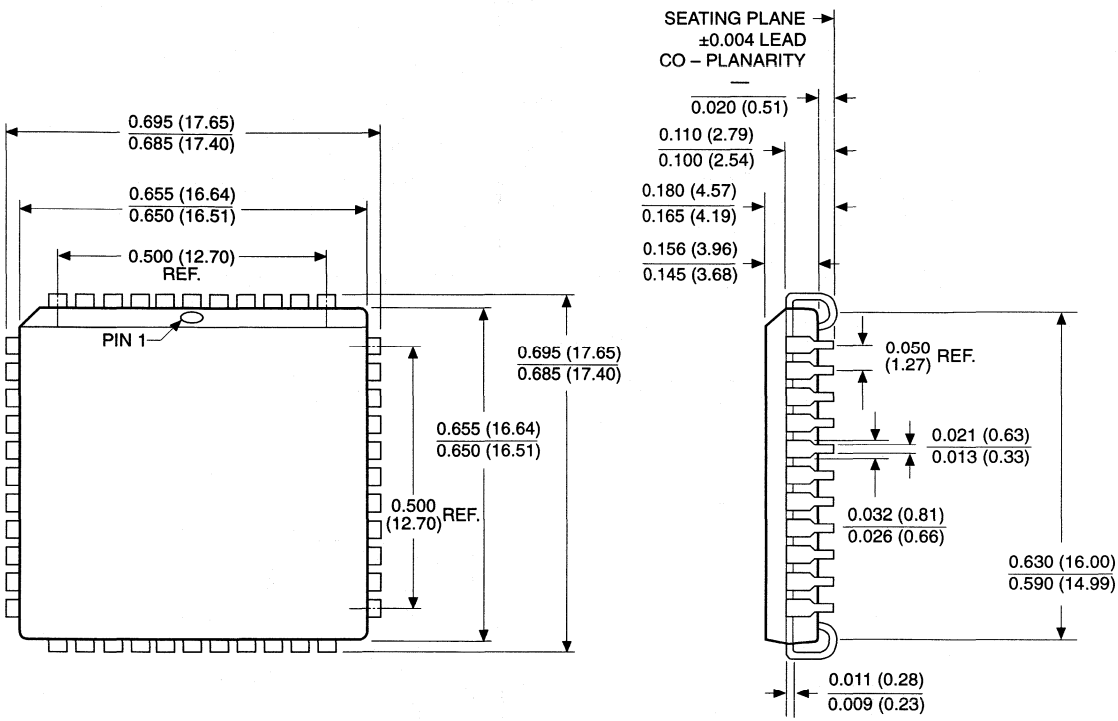


NOTES:

1. **ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)**
2. **DIMENSIONS WITH NO TOLERANCE FOR REFERENCE ONLY**

3926 FHD F13

44-PIN PLASTIC LEADED CHIP CARRIER PACKAGE

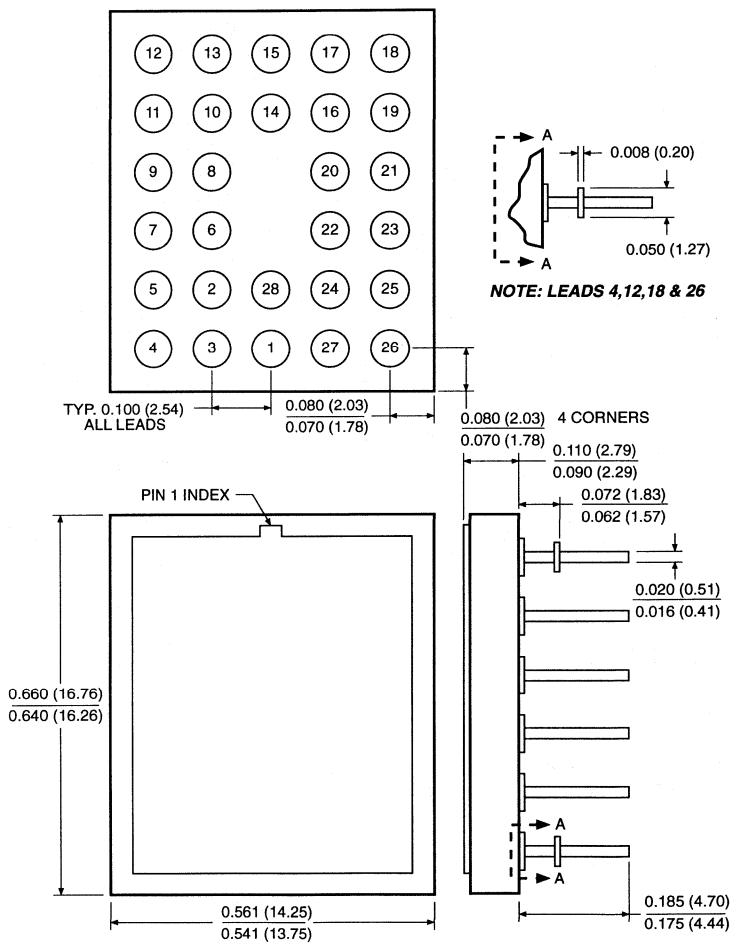


NOTES:
1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
2. DIMENSIONS WITH NO TOLERANCE FOR REFERENCE ONLY

3926 ILL F29.0

12

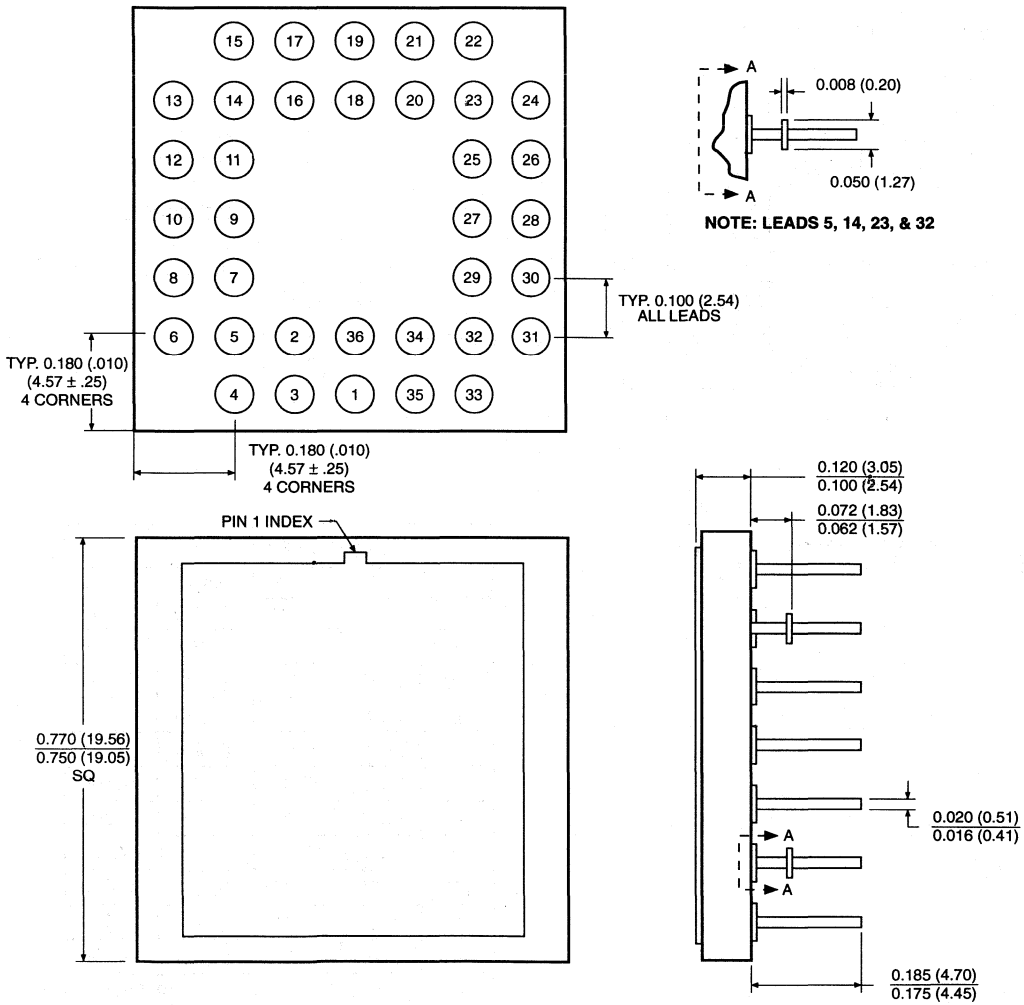
28-LEAD CERAMIC PIN GRID ARRAY PACKAGE TYPE K



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

3926 FHD F15

36-LEAD CERAMIC PIN GRID ARRAY PACKAGE TYPE K

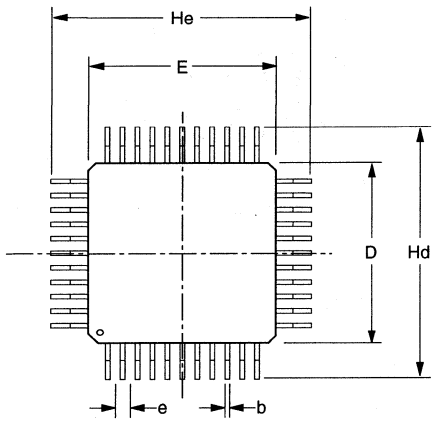


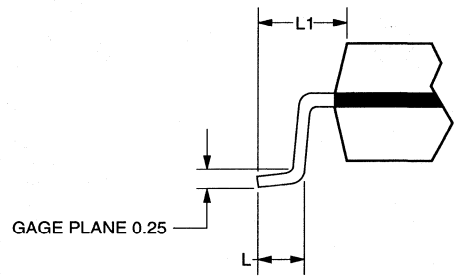
NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

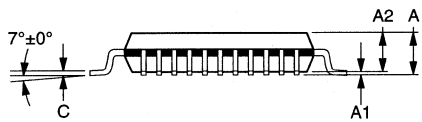
3926 FHD F21

12

44-LEAD THIN QUAD FLAT PACK (TQFP) PACKAGE TYPE L





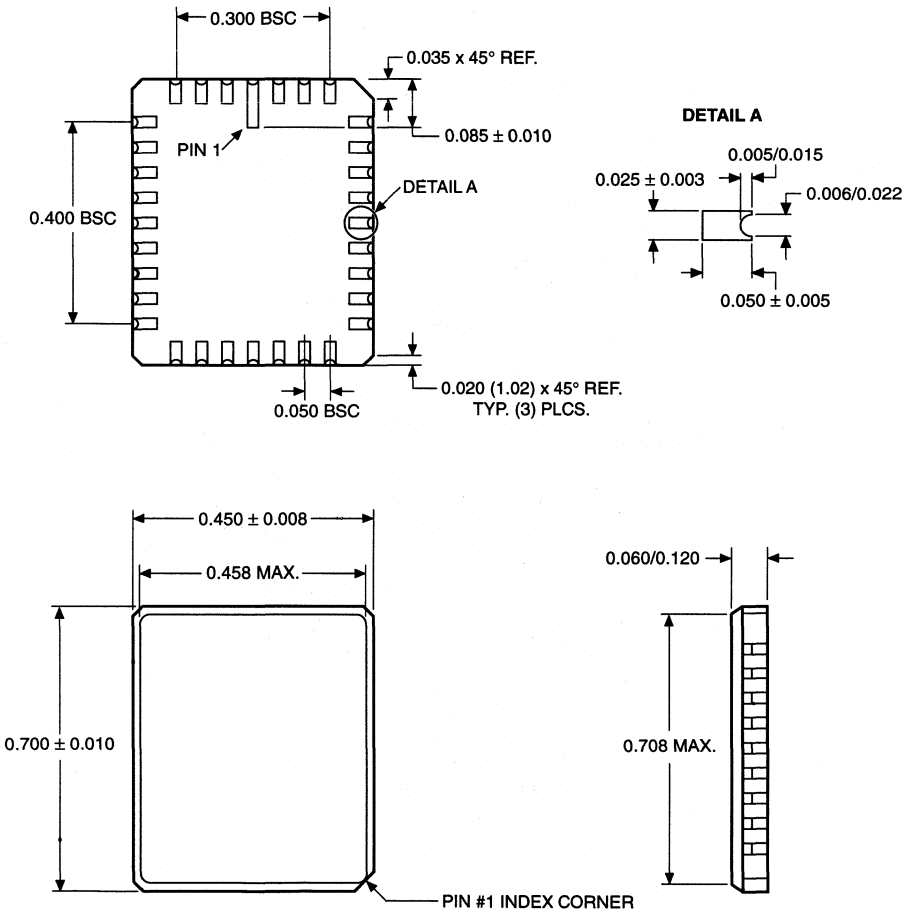


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.00	1.20	0.039	0.047
A_1	0.05	0.15	0.002	0.006
A_2	0.95	1.05	0.037	0.041
b	0.22	0.38	0.009	0.015
c	0.090	0.200	0.004	0.008
D	9.90	10.10	0.390	0.398
E	9.90	10.10	0.390	0.398
e	0.80 TYP		0.031 TYP	
Hd	11.90	12.10	0.468	0.476
He	11.90	12.10	0.468	0.476
L	0.45	0.75	0.018	0.030
L_1	1.00 TYP		0.039 TYP	
0	0	7	0	7

NOTES:
1. GAGE PLANE DIMENSION ON PAGE 1 IS IN MM.
2. LEAD COPLANARITY SHALL BE 0.10MM [0.004] MAXIMUM.

3926 ILL F36

32-PAD STRETCHED CERAMIC LEADLESS CHIP CARRIER PACKAGE TYPE N

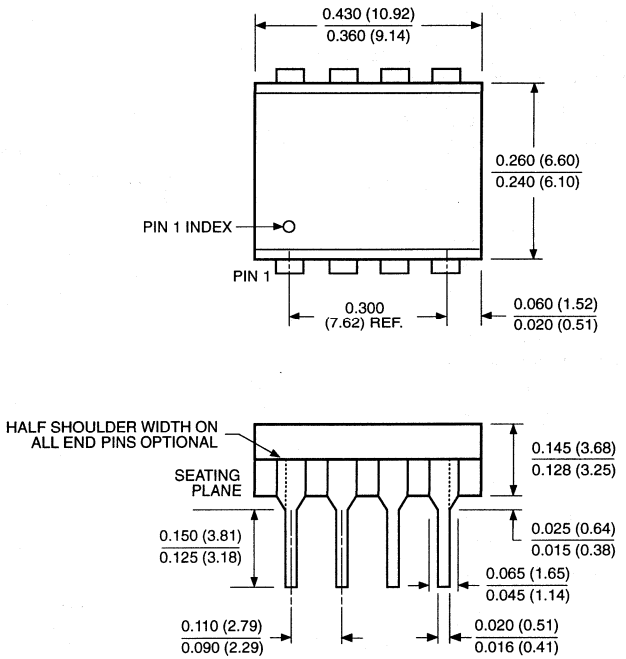


NOTE:
1. **ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)**
2. **TOLERANCE: ±1% NLT ±0.005 (0.127)**

3926 FHD F35

12

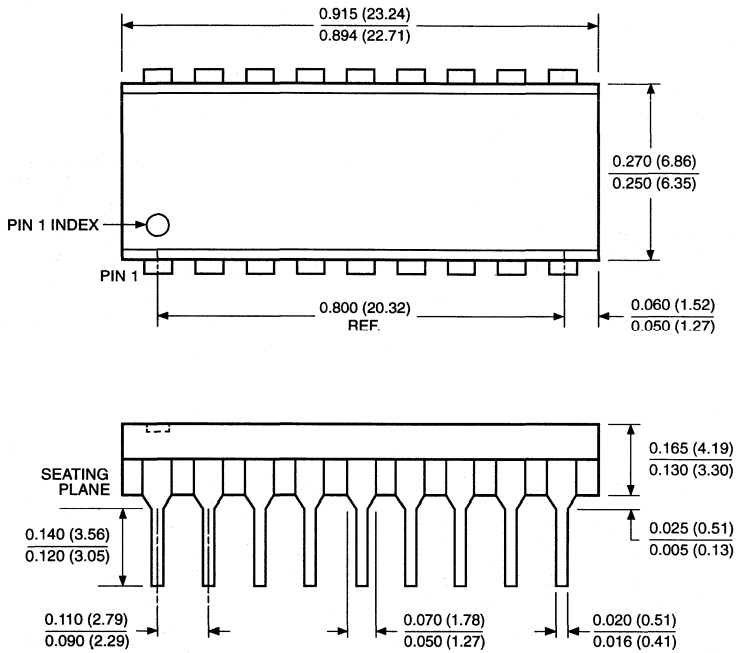
8-LEAD PLASTIC DUAL IN-LINE PACKAGE TYPE P



NOTE:
1. **ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)**
2. **PACKAGE DIMENSIONS EXCLUDE MOLDING FLASH**

3926 FHD F01

18-LEAD PLASTIC DUAL IN-LINE PACKAGE TYPE P

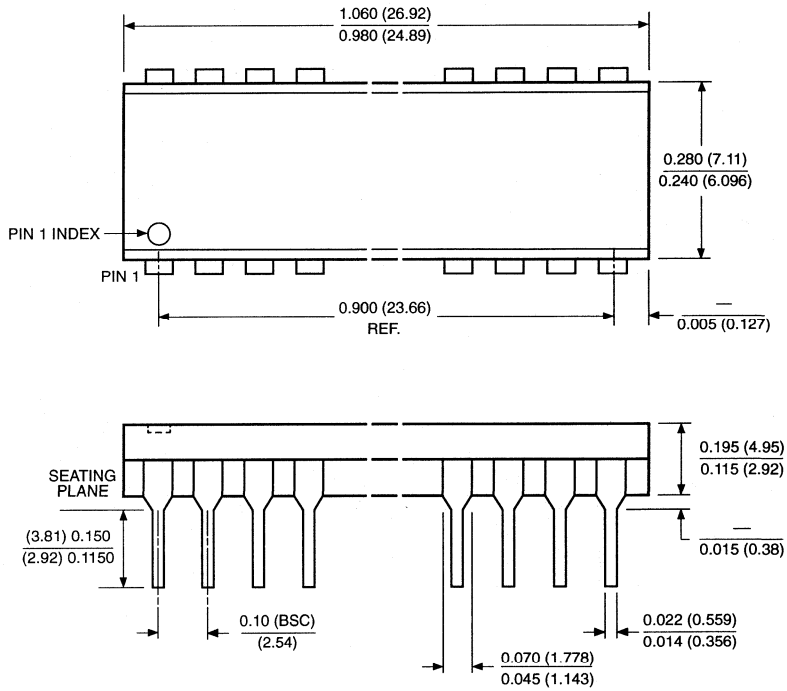


NOTE:
1. **ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)**
2. **PACKAGE DIMENSIONS EXCLUDE MOLDING FLASH**

3926 FHD F02

12

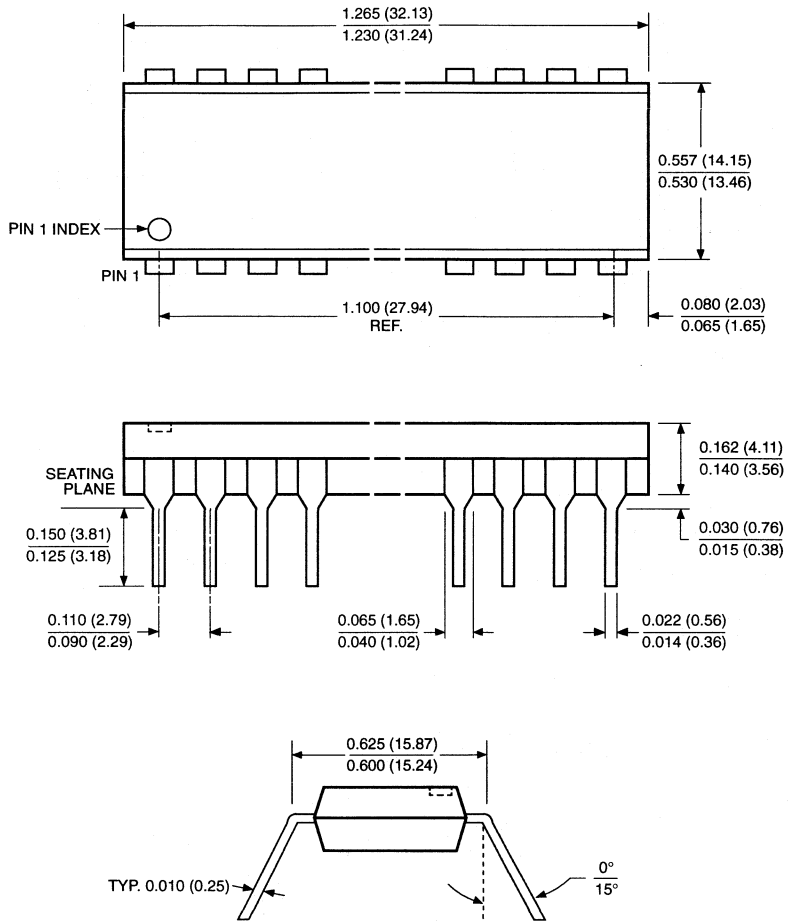
20-LEAD PLASTIC DUAL IN-LINE PACKAGE TYPE P



NOTE:
1. **ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)**
2. **PACKAGE DIMENSIONS EXCLUDE MOLDING FLASH**

3926 FHD F18.1

24-LEAD PLASTIC DUAL IN-LINE PACKAGE TYPE P

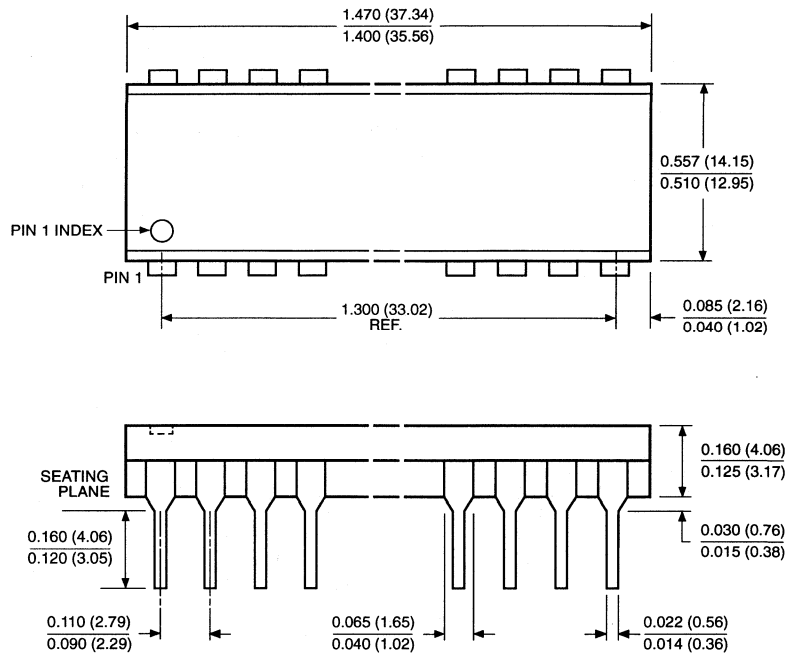


NOTE:
1. **ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)**
2. **PACKAGE DIMENSIONS EXCLUDE MOLDING FLASH**

3926 FHD F03

12

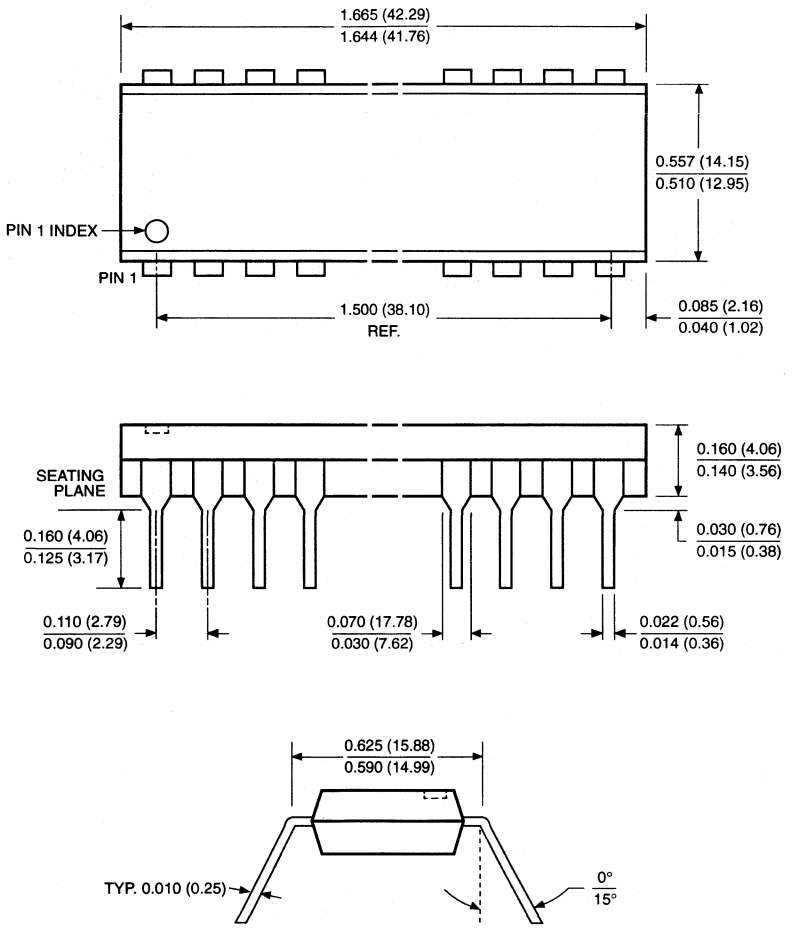
28-LEAD PLASTIC DUAL IN-LINE PACKAGE TYPE P



NOTE:
1. **ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)**
2. **PACKAGE DIMENSIONS EXCLUDE MOLDING FLASH**

3926 FHD F04

32-LEAD PLASTIC DUAL IN-LINE PACKAGE TYPE P

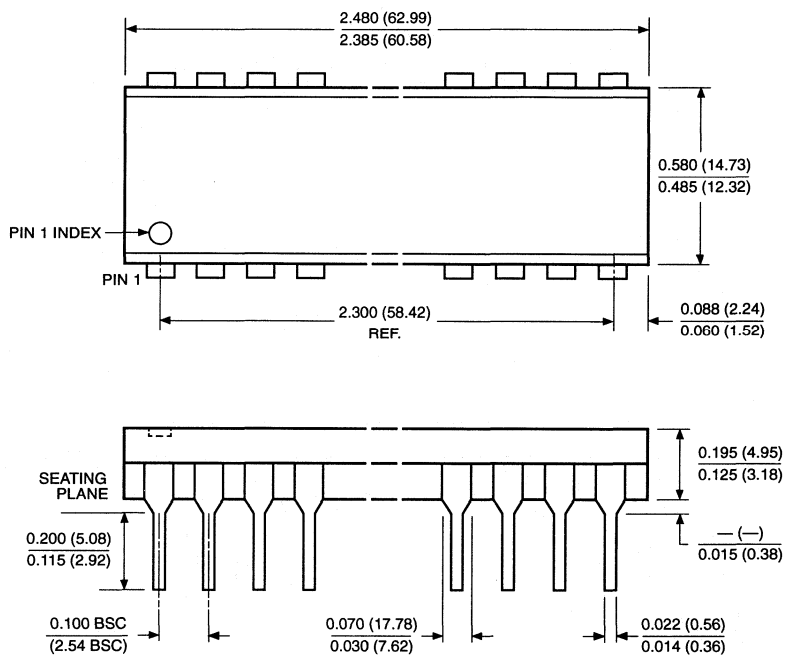


NOTE:
1. **ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)**
2. **PACKAGE DIMENSIONS EXCLUDE MOLDING FLASH**

3926 FHD F25

12

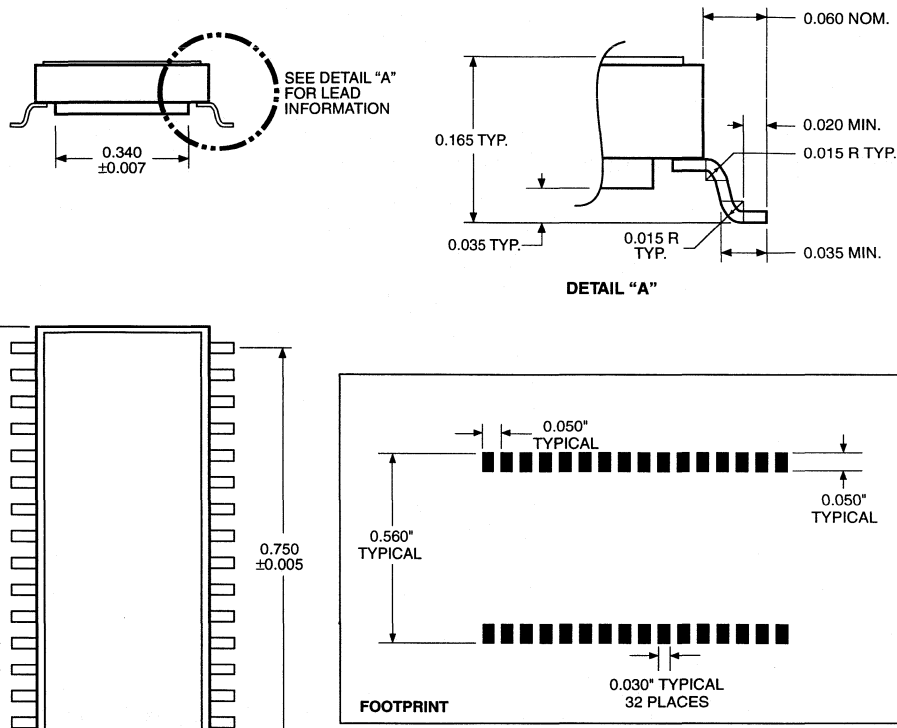
48-LEAD PLASTIC PACKAGE TYPE P



NOTE:
1. **ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)**
2. **PACKAGE DIMENSIONS EXCLUDE MOLDING FLASH**

3926 FHD F43

32-LEAD CERAMIC SMALL OUTLINE GULL WING PACKAGE TYPE R

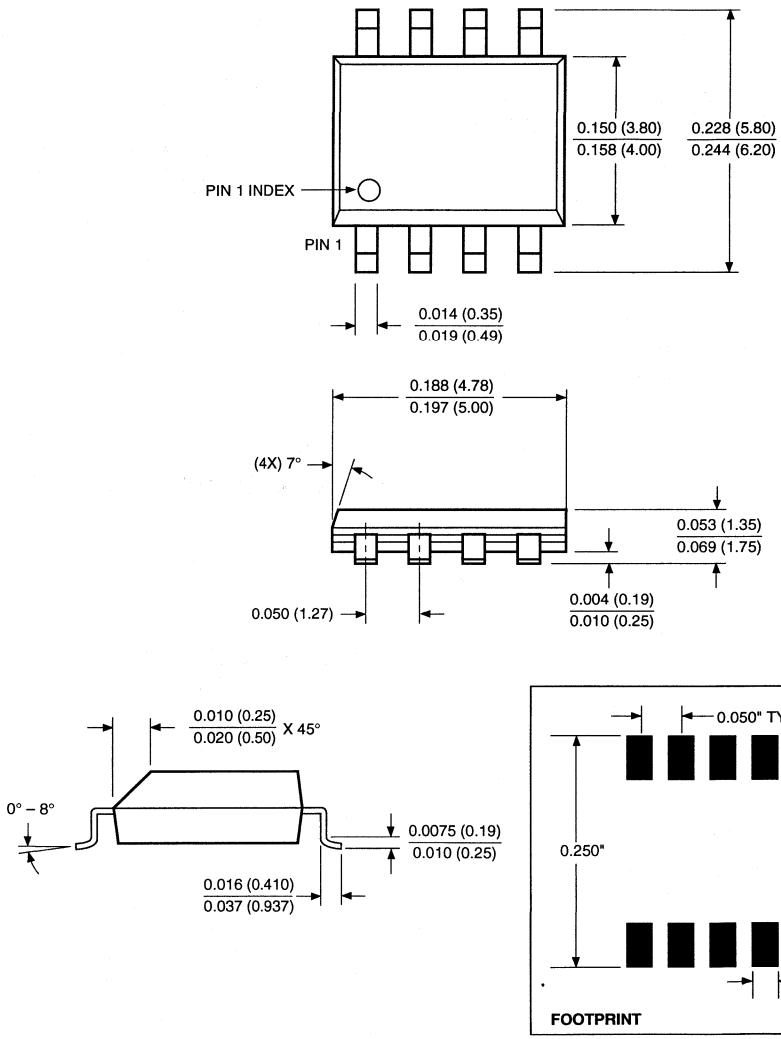


NOTES:
1. ALL DIMENSIONS IN INCHES
2. FORMED LEAD SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN 0.004 INCHES

3926 FHD F27

12

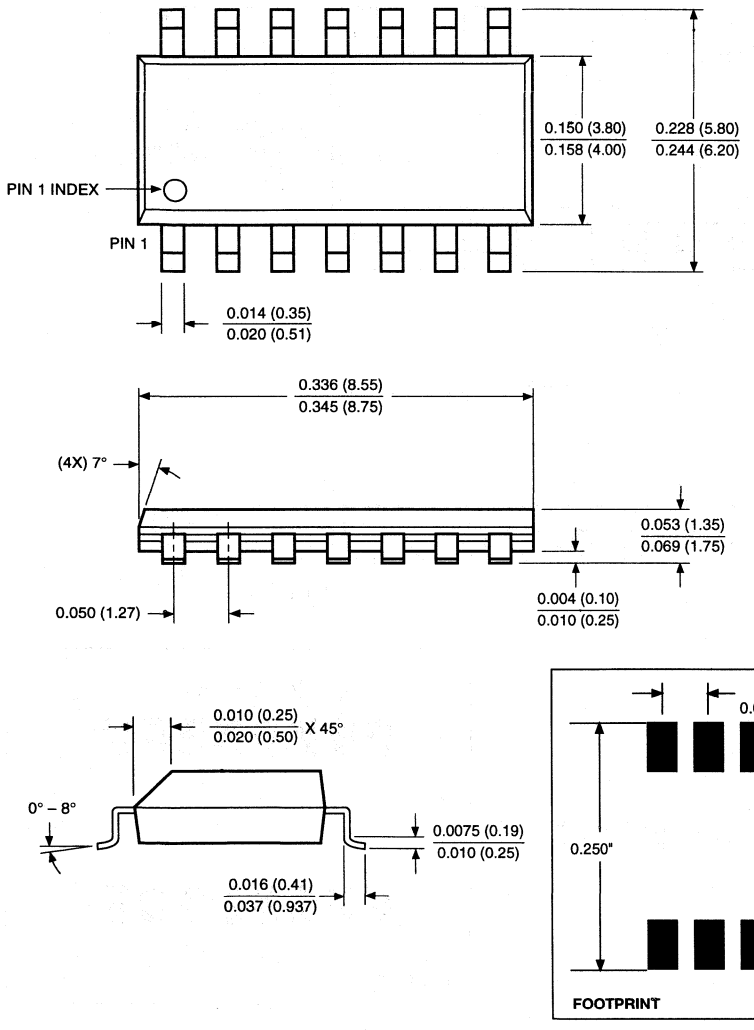
8-LEAD PLASTIC SMALL OUTLINE GULL WING PACKAGE TYPE S



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

3926 FHD F22.1

14-LEAD PLASTIC SMALL OUTLINE GULL WING PACKAGE TYPE S

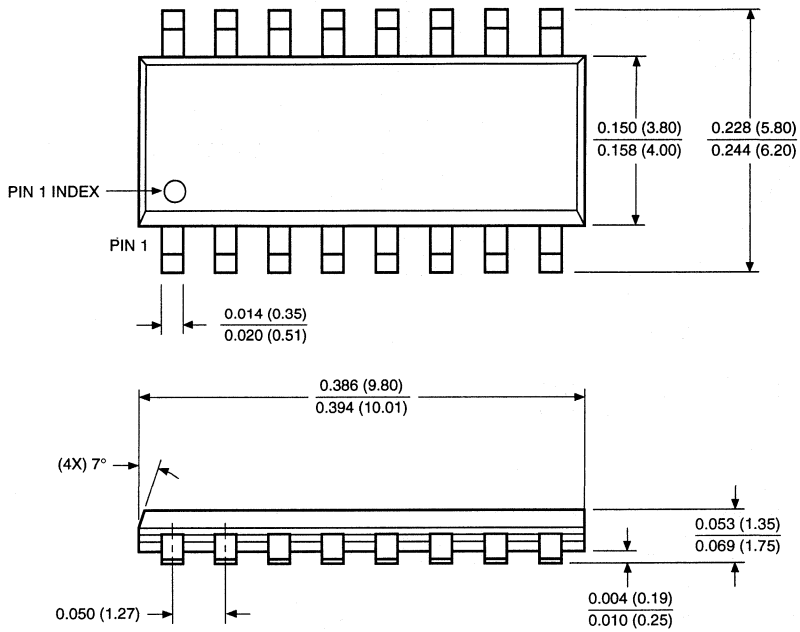


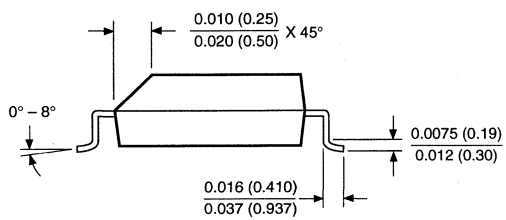
NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

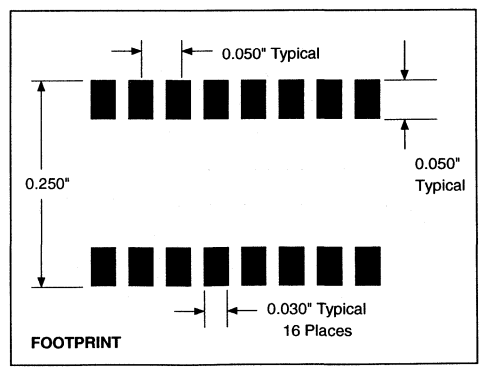
3926 FHD F10.1

12

16-LEAD PLASTIC SMALL OUTLINE GULL WING PACKAGE TYPE S



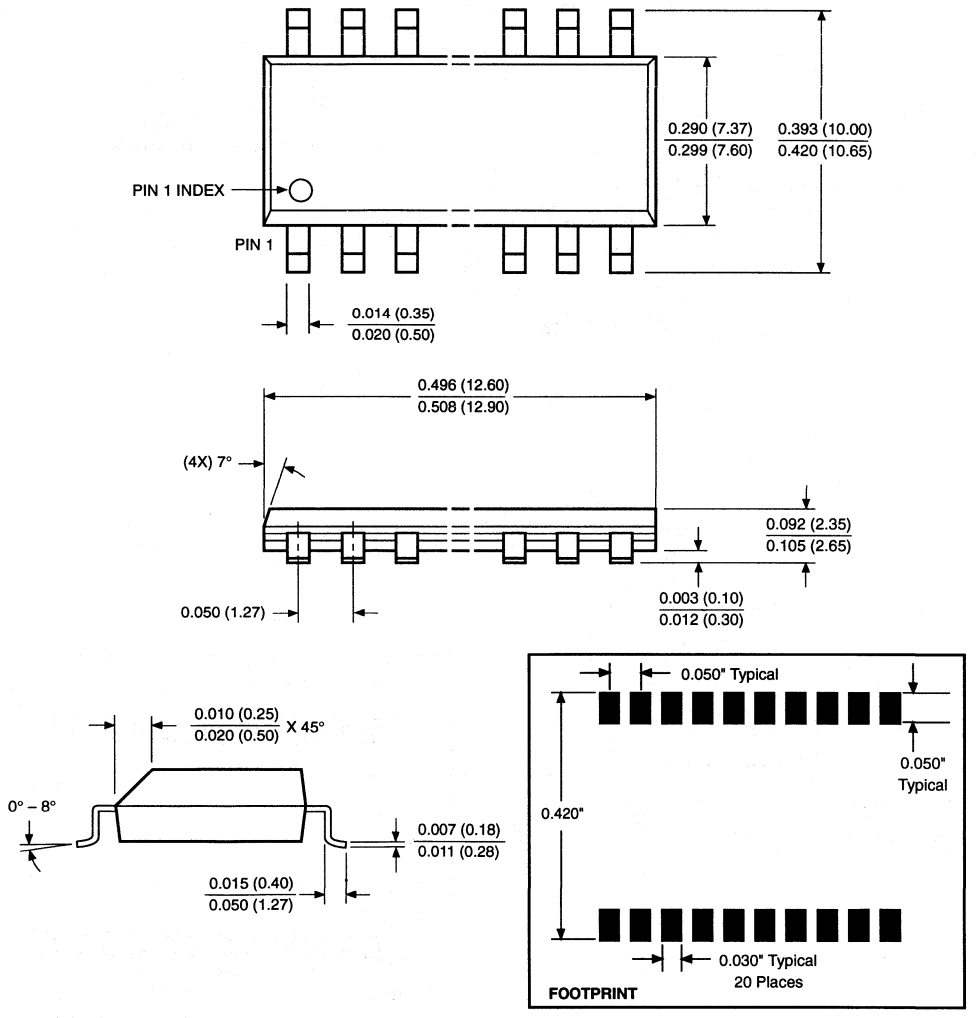




NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

3926 FHD F26

20-LEAD PLASTIC SMALL OUTLINE GULL WING PACKAGE TYPE S

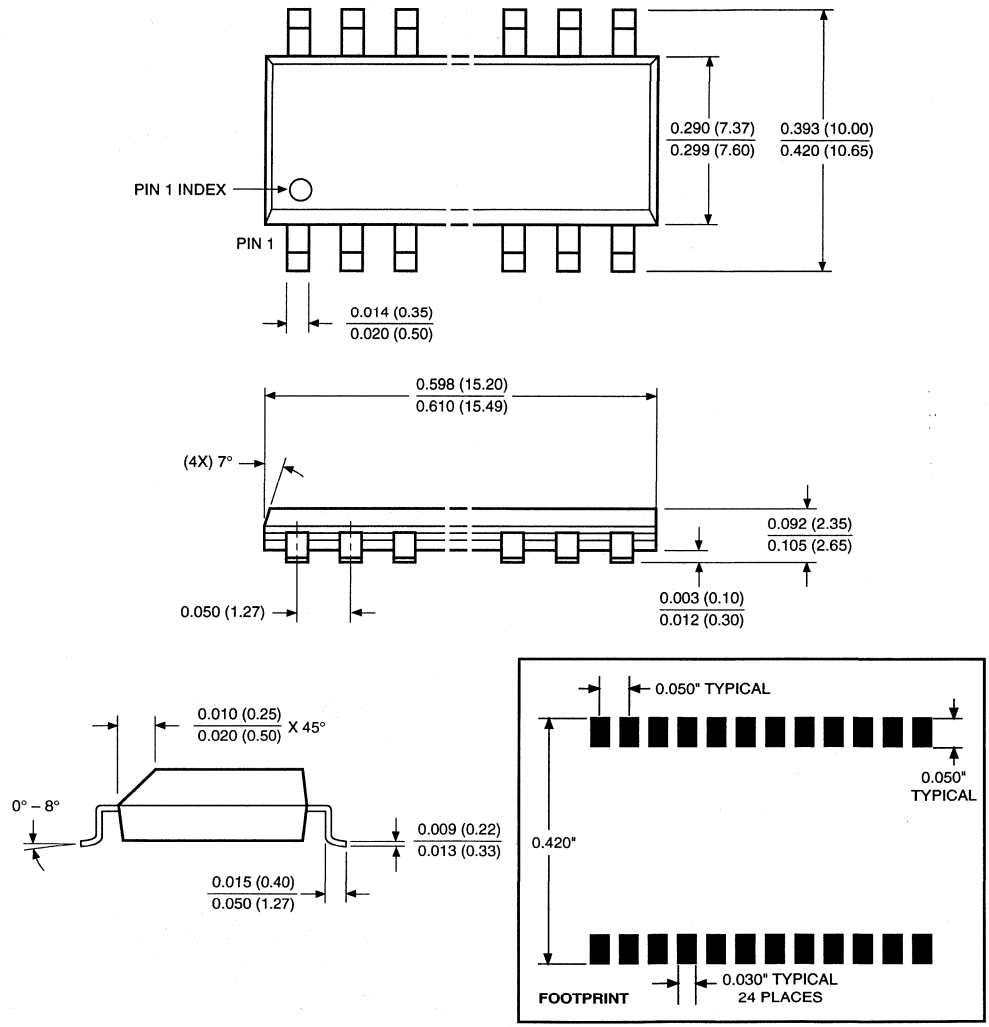


NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

3926 FHD F23

12

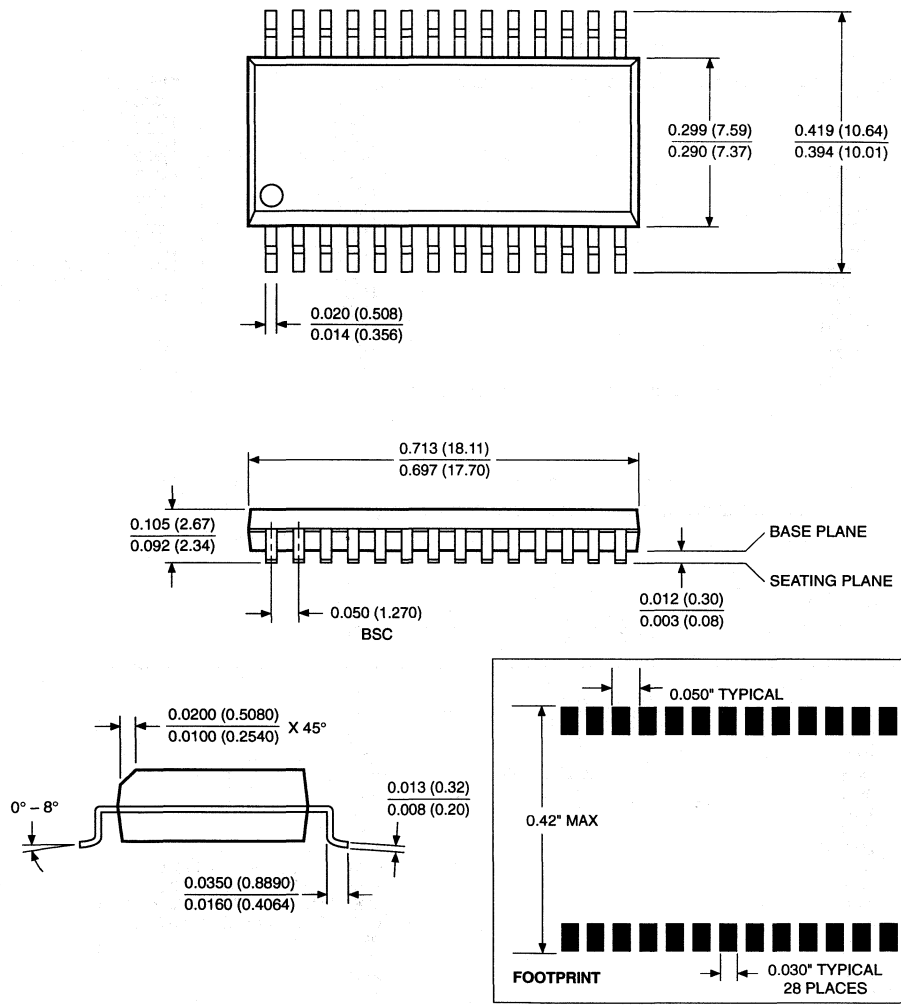
24-LEAD PLASTIC SMALL OUTLINE GULL WING PACKAGE TYPE S



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

3926 FHD F24

28-LEAD PLASTIC SMALL OUTLINE GULL WING PACKAGE TYPE S

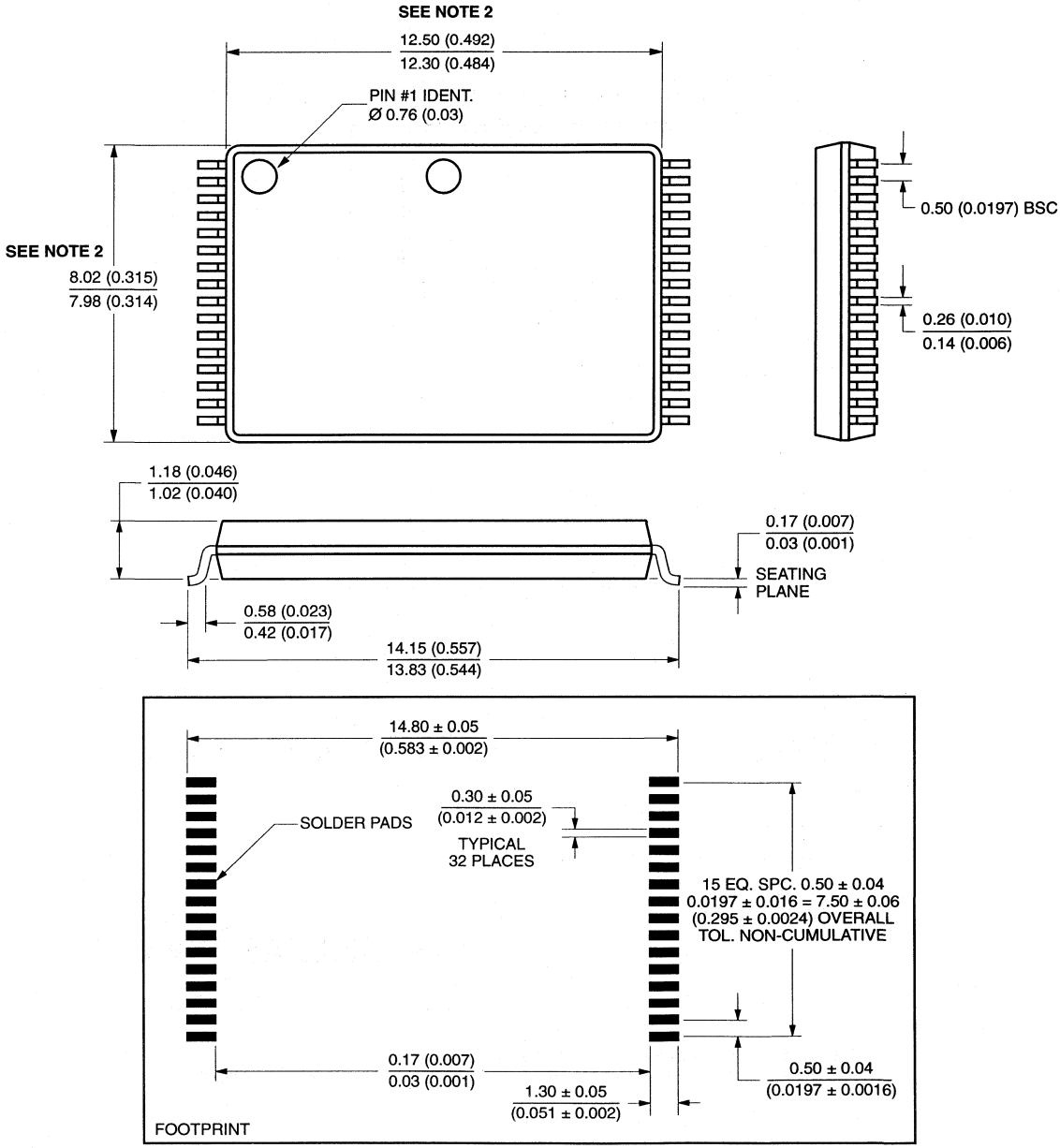


NOTES:
1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
2. FORMED LEAD SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN 0.004 INCHES

3926 FHD F17

12

32-LEAD THIN SMALL OUTLINE PACKAGE (TSOP) TYPE T

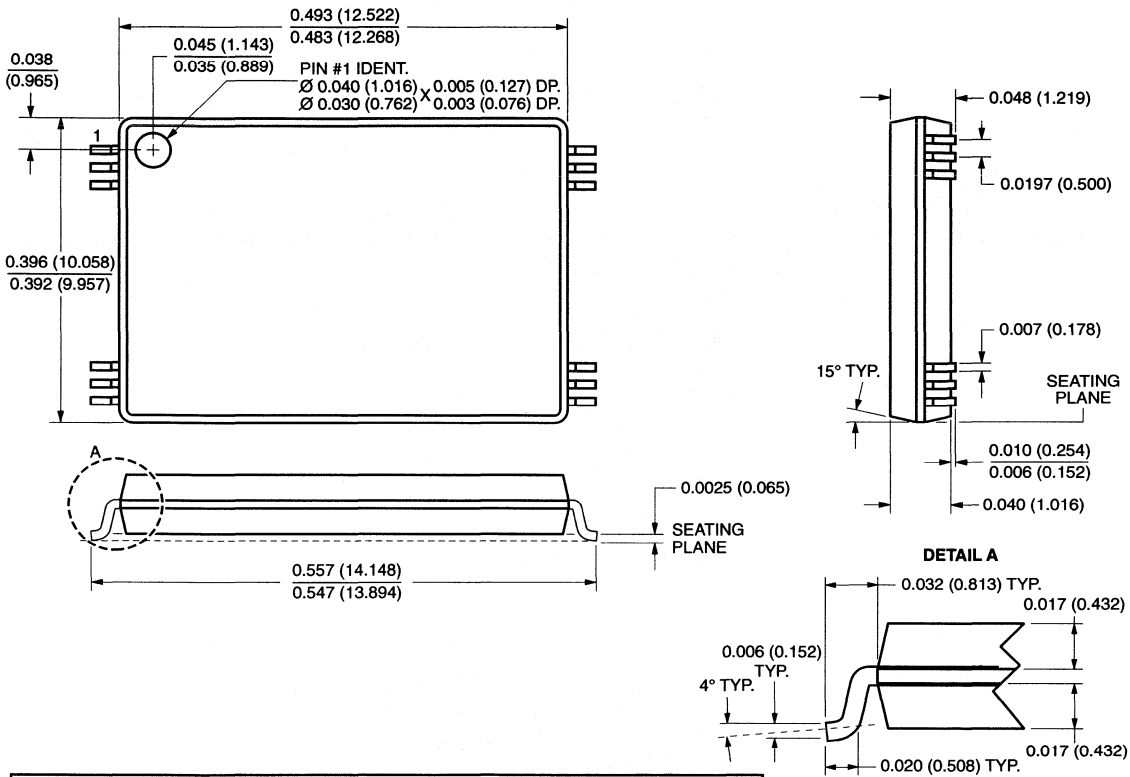


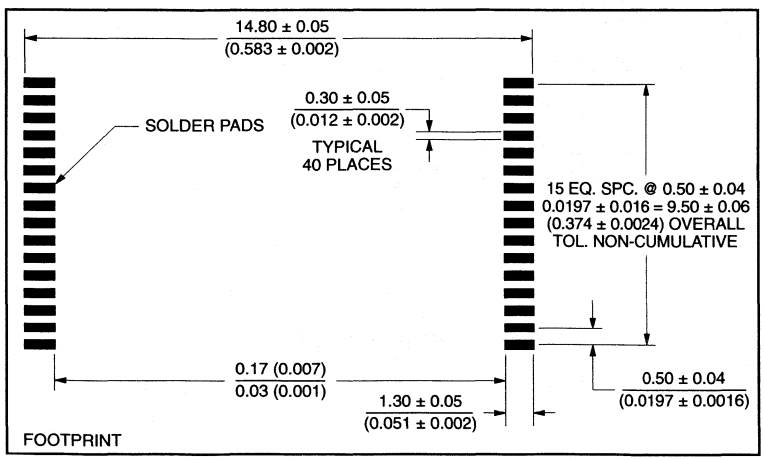
NOTE:

1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES IN PARENTHESES).

3926 ILL F38.1

40-LEAD THIN SMALL OUTLINE PACKAGE (TSOP) TYPE T



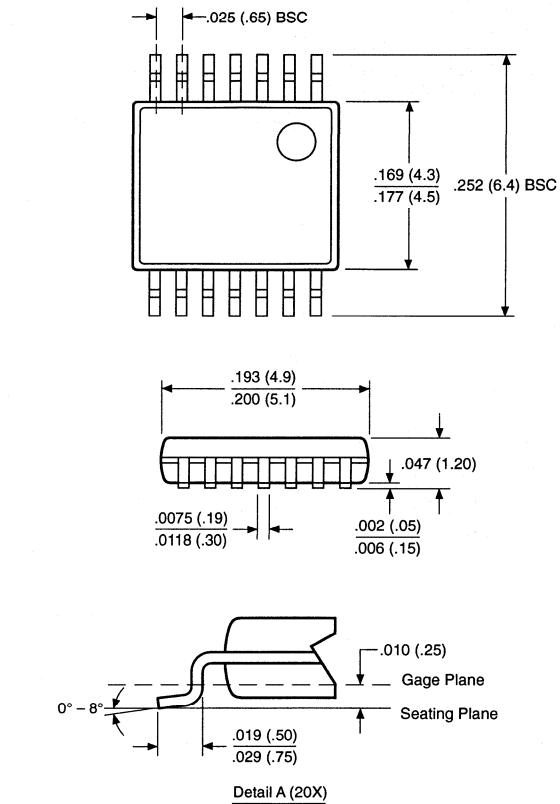


NOTE:
1. ALL DIMENSIONS ARE SHOWN IN INCHES (IN PARENTHESES IN MILLIMETERS).

3926 ILL F39.1

12

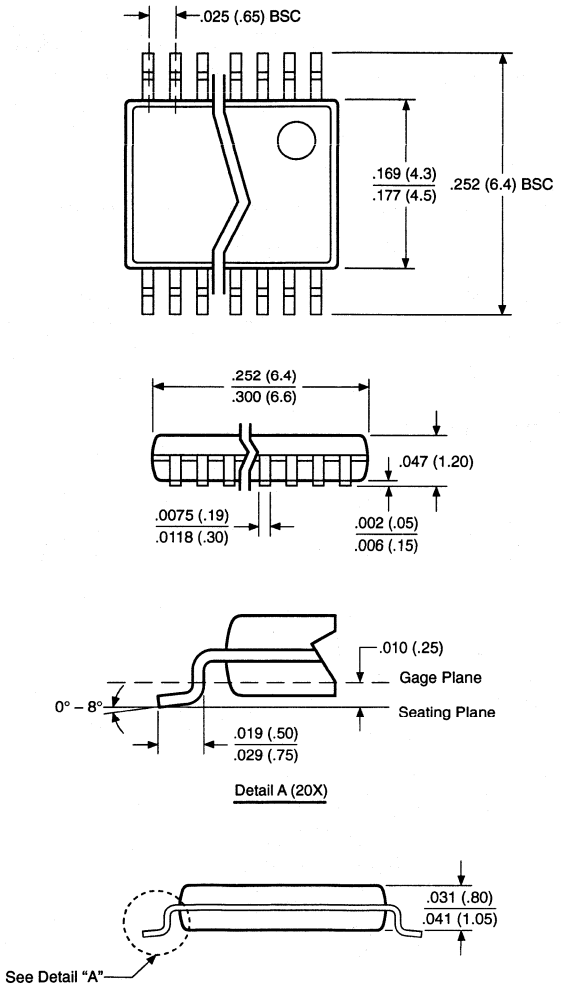
14-LEAD PLASTIC, TSSOP PACKAGE TYPE V



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

3926 FHD F32

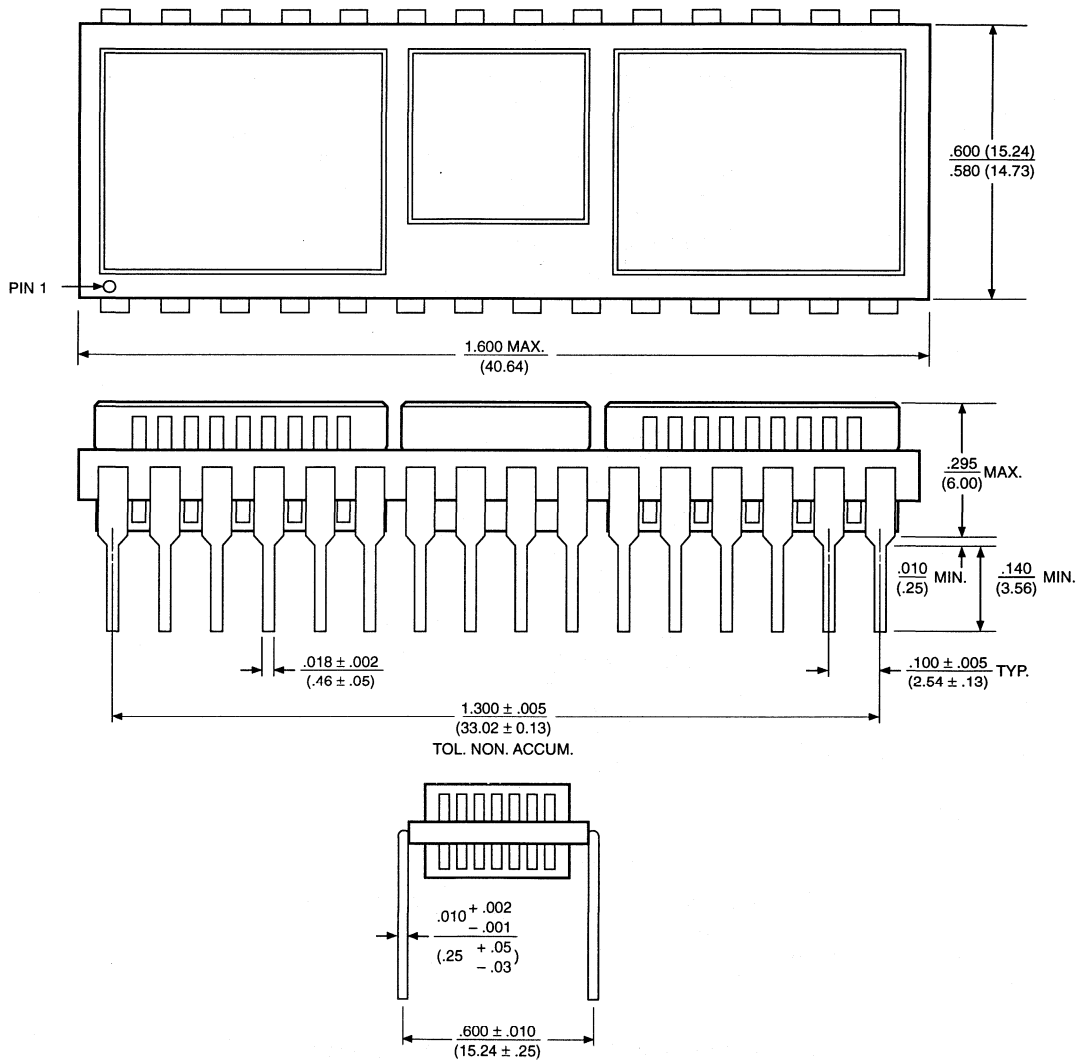
20-LEAD PLASTIC, TSSOP PACKAGE TYPE V



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

3926 FHD F45

28-PIN DUAL-IN-LINE PACKAGE CERAMIC LEADLESS CHIP CARRIERS ON CERAMIC SIDEBRAZED CERAMIC SUBSTRATE

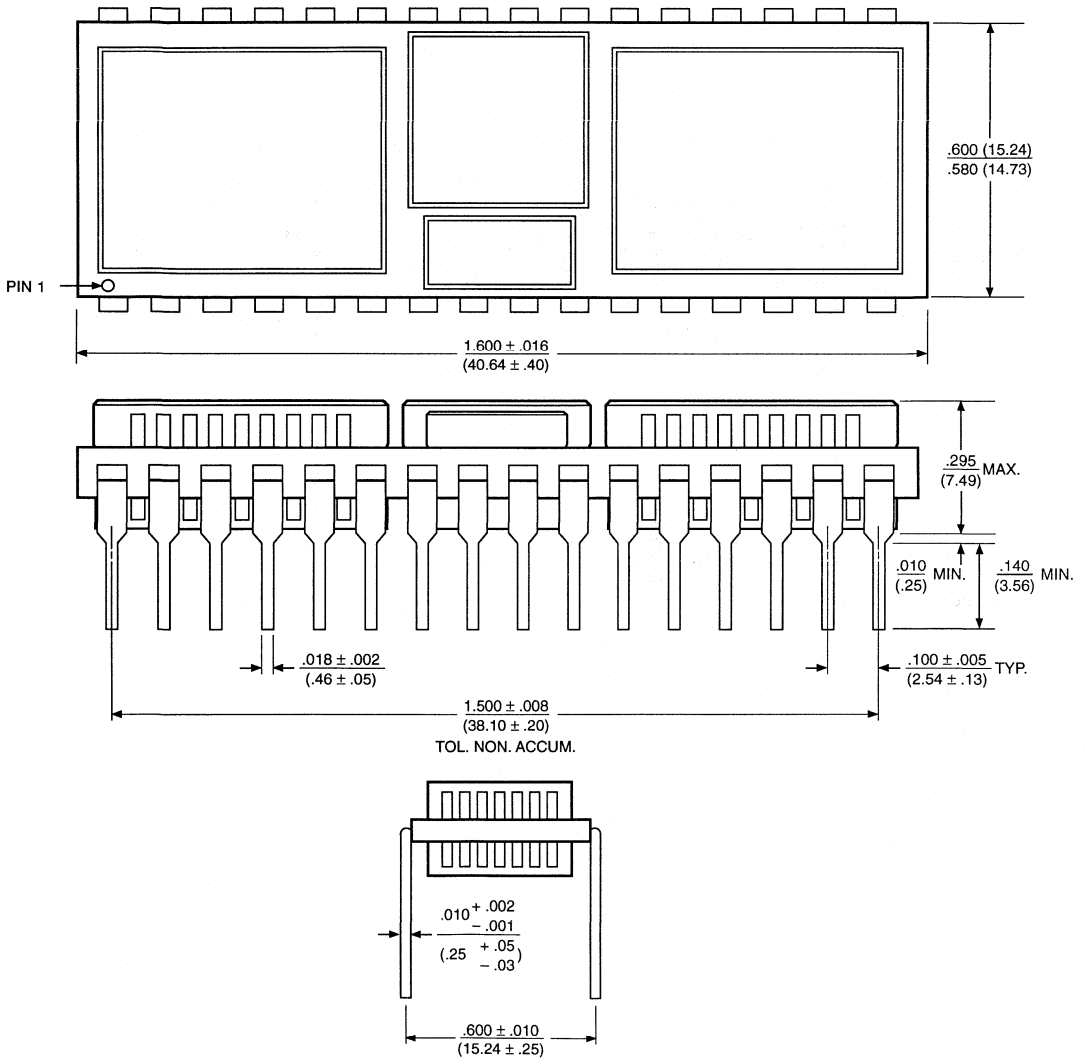


NOTES:

1. **ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)**
2. **DIMENSIONS WITH NO TOLERANCE FOR REFERENCE ONLY**

3926 FHD F40

32-PIN DUAL-IN-LINE PACKAGE
CERAMIC LEADLESS CHIP CARRIERS
ON SIDE BRAZED CERAMIC SUBSTRATE

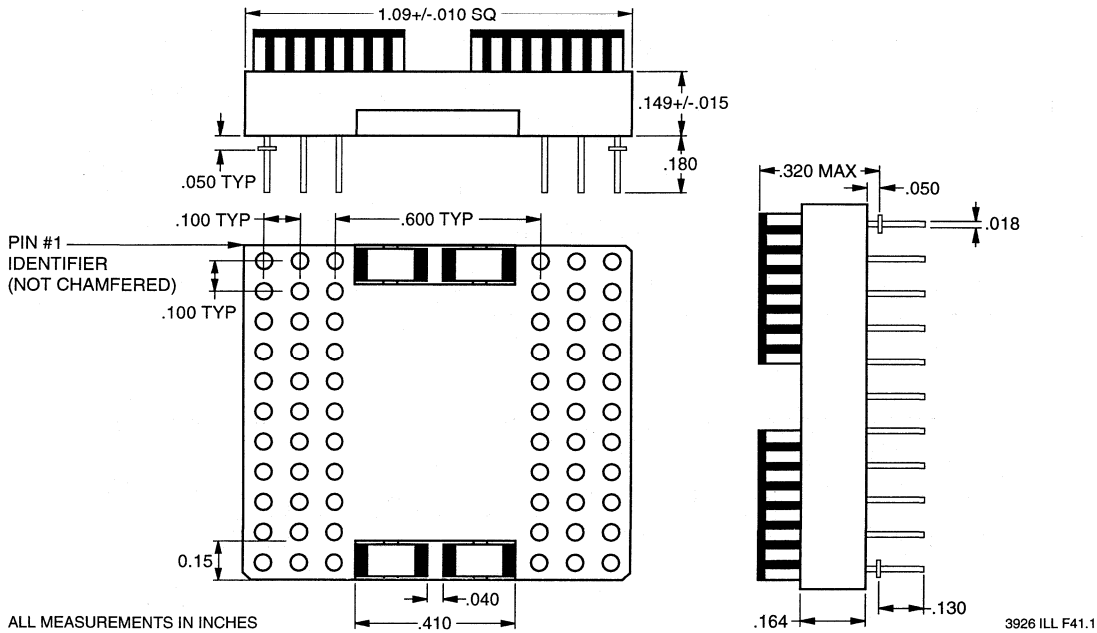


NOTES:
1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
2. DIMENSIONS WITH NO TOLERANCE FOR REFERENCE ONLY

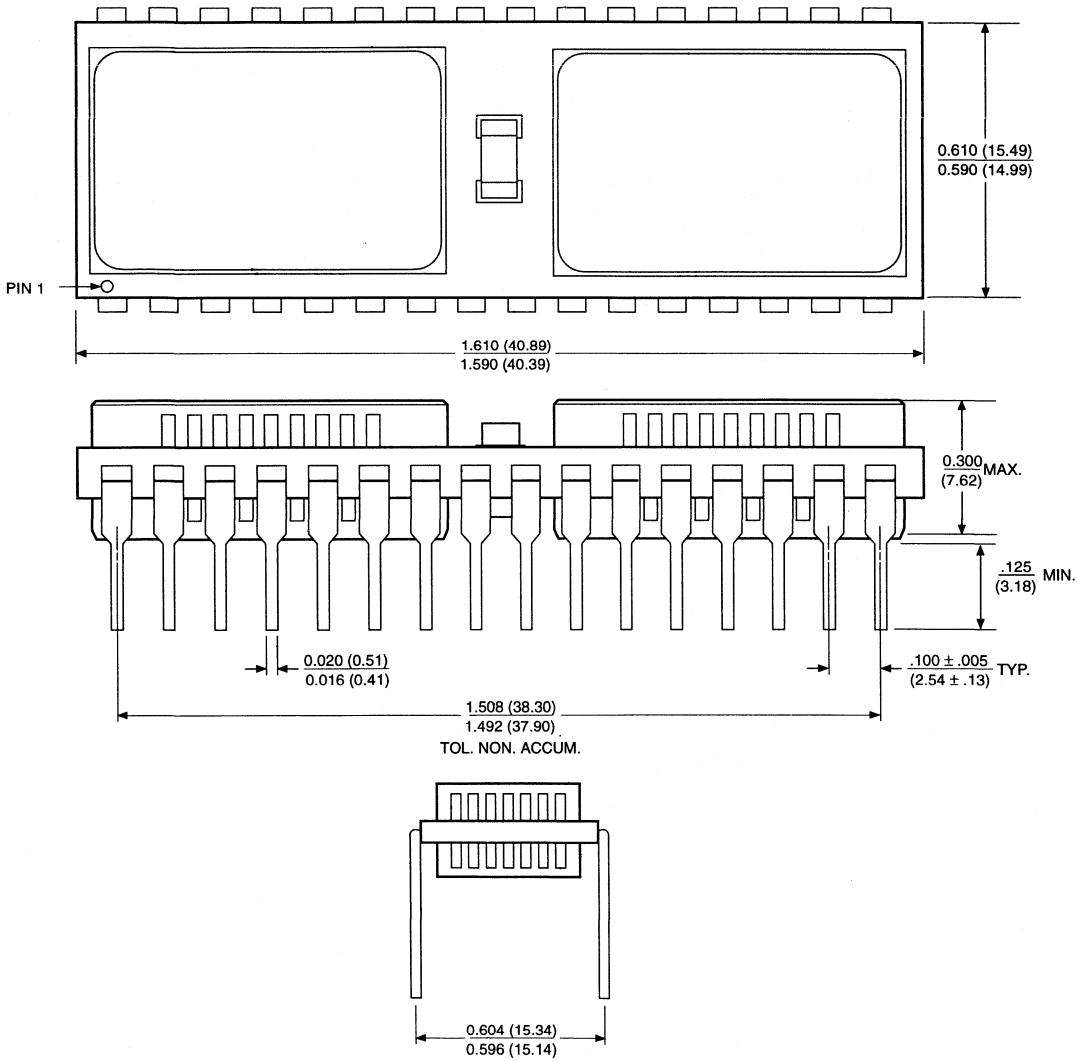
3926 FHD F12

12

66 PIN CERAMIC PUMA MODULE



32-PIN DUAL-IN-LINE MODULE USING STRETCHED CERAMIC LEADLESS CHIP CARRIERS ON SIDE BRAZED CERAMIC SUBSTRATE



NOTES:

1. **ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)**
2. **DIMENSIONS WITH NO TOLERANCE FOR REFERENCE ONLY**

3926 ILL F47

12

NOTES